

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SATCO PRODUCTS, INC.,
Petitioner,

v.

SEOUL VIOSYS CO., LTD.,

IPR2020-00655
Patent 9,627,435 B2

Before ERICA A. FRANKLIN, JEFFREY W. ABRAHAM, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

FRANKLIN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Satco Products, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 2, 6, and 7 of U.S. Patent No. 9,627,435 B2 (Ex. 1001, “the ’435 patent”). Paper 2 (“Petition” or “Pet.”). Seoul Viosys Co., Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2020). For the reasons provided below, we exercise our discretion under 35 U.S.C. § 314 to deny institution of an *inter partes* review.

A. *Real Parties-in-Interest*

Petitioner identifies Satco Products, Inc. as the real party-in-interest. Pet. 1. Patent Owner identifies Seoul Viosys Co., Ltd. as the real party-in-interest. Paper 3, 1.

B. *Related Proceedings*

Petitioner and Patent Owner provide notice of a district court litigation involving the ’435 patent: *Seoul Semiconductor Co., Ltd. v. Satco Products, Inc.*, No. 2:19-cv-04951 (EDNY). Pet. 1; Paper 3, 1. Patent Owner also notes that the ’435 patent is among other patents asserted in *Seoul Semiconductor Co. Ltd. et al. v. Service Lighting and Electrical Supplies, Inc. d/b/a 1000bulbs.com*, No. 2-18-cv-00386 (NDTX) and *Semiconductor Co. Ltd. et al. v. Archipelago Lighting, Inc.*, No. 5:17-cv-01890 (CDCA) Paper 3, 1–2.

C. *The ’435 Patent*

The ’435 patent relates to a “nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.” Ex. 1001, 1:27–32.

The Specification explains that a “light emitting device” refers to “an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers.” *Id.* at 1:34–37. One of the indexes indicating the performance of light emitting devices is the extraction efficiency. *Id.* at 2:9–13. “The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device.” In other words, the Specification explains that “the light emitting device becomes bright as the extraction efficiency becomes high.” *Id.* at 2:17–18. Importantly, the extraction efficiency of the light emitting device is influenced by the shape and surface pattern of a chip, the structure of a chip, and the packaging type. *Id.* at 2:17–19. According to the Specification, careful attention, therefore, should be paid to those factors when designing a light emitting device.

The Specification describes a problem with prior art light emitting devices as follows,

Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

Id. at 2:65–3:13. To solve that problem, the present invention provides “a light emitting device wherein light produced from a side surface of a semiconductor layer, which is not perpendicular to but included at a predetermined slop[e] from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device.” *Id.* at 3:42–46. The Specification explains that the result device exhibits “more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency.” *Id.* at 3:47–49.

Figure 32 of the '435 patent is set forth below.

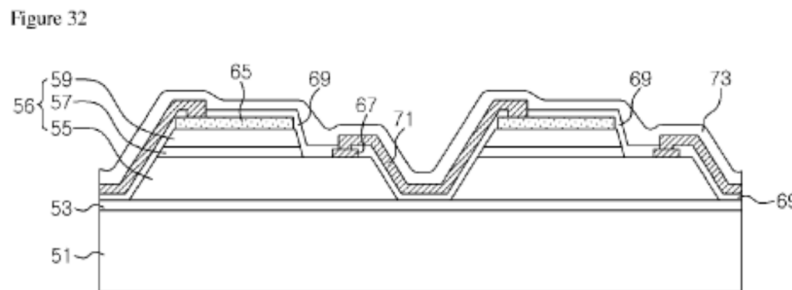


Figure 32 is a sectional view illustrating a light emitting diode (“LED”) for AC operation according to an embodiment of the invention. *Id.* at 17:1–3. A plurality of light emitting cells 56 are disposed on substrate 51. A buffer layer 53 may be disposed between light emitting cells 56 and substrate 51. *Id.* at 17:31–32. The light emitting cells 56 include lower semiconductor layer 55 and upper semiconductor layer 59. *Id.* at 17:9–11. The upper and lower semiconductor layers may be N-type and P-type, respectively. *Id.* at 17:13–16. Active layer 57 is disposed between the upper and lower semiconductor layers. *Id.* at 17:12–13.

The Specification explains,

Side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51 and get narrowed toward upside. The inclination of the side surfaces

improves emission efficiency of a light produced in the active layers 57, and helps conformal deposition of the other layers which will be formed on the light emitting cells 56.

Id. at 17:39–45. The entire surface of the light emitting cells 56 is covered by insulation layer 69.

D. Illustrative Claim

Petitioner challenges independent claim 1 and dependent claims 2, 6, and 7 of the '435 patent. Independent claim 1, set forth below, is illustrative.

1. A light-emitting device, comprising:
 - a substrate;
 - a first light emitting cell disposed on the substrate and a second light emitting cell disposed on the substrate, wherein the first and second light emitting cells comprise:
 - a first semiconductor layer and a second semiconductor layer;
 - an active layer disposed between the first and the second semiconductors layers; and
 - a first inclined surface;
 - a first conductive material disposed on the second semiconductor layer of the second light emitting cell;
 - a first insulation layer that overlaps the first conductive material and the first and second light emitting cells;
 - a second conductive material that overlaps the first insulation layer and electrically connects the first light emitting cell and the second light emitting cell; and
 - a second insulation layer that overlaps the second conductive material,
 - wherein both the first insulation layer and the second insulation layer comprise a light transmitting material; and
 - wherein the first inclined surface is continuous and has a slope of approximately 20° to approximately 80° from a horizontal plane of the substrate.

Ex. 1001, 21:2–27.

E. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1, 2, 6, and 7 would have been unpatentable on the following grounds.

Claims Challenged	35 U.S.C. §	Reference(s)
1, 2, 6, 7	103(a) ¹	Yang ² , Schubert, ³ Aanegola ⁴
1, 2, 6, 7	103(a)	Yang, Van Zant, ⁵ Hawrylo, ⁶ Yukimoto ⁷
1, 7	102	Salam ⁸
2, 6	103(a)	Salam

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the ’435 patent issued has an effective filing date prior to March 16, 2013, the pre-AIA version of § 103 applies.

² Yang et al., US 2005/01790472 A1, published Aug. 18, 2005 (“Yang,” Ex. 1004).

³ Schubert, *Light-Emitting Diodes*, 1st ed. New York: Cambridge University Press 2003 (“Schubert,” Ex. 1007).

⁴ Aanegola et al., US 2005/0239227 A1, published Oct. 27, 2005 (“Aanegola,” Ex. 1008).

⁵ Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, 4th ed. Ch. 12, “Deposition,” New York: McGraw Hill 2000 (“Van Zant,” Ex. 1013).

⁶ Hawrylo et al., US 4,095,011, issued June 13, 1978 (“Hawrylo,” Ex. 1014).

⁷ Yukimoto, US 2003/0010989, published Jan. 16, 2003 (“Yukimoto,” Ex. 1020).

⁸ Salam, US 6,346,771 B1, issued Feb. 12, 2002 (“Salam,” Ex. 1005).

We refer to the two grounds based on combinations including Yang as the “Yang grounds,” and the two grounds based upon Salam as the “Salam Grounds.”

Petitioner also relies on the Declaration of P. Morgan Pattison, Ph.D. (Ex. 1003). Patent Owner relies on the Declaration of Daniel Feezell, Ph.D. (Ex. 2001).

II. ANALYSIS

A. *Person of Ordinary Skill in the Art*

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

Petitioner asserts that a person of ordinary skill in the art at the time of the invention would have had

A Ph.D. in chemical engineering, materials engineering, or electrical engineering (with a focus on semiconductor materials), or similar advanced post-graduate education in this area, as well as at least 2 years of experience relating to LED design and fabrication. (See, e.g., Ex-1003-Pattison at ¶¶21-25; Ex-1001 at 1:26-32 (describing the “Field of the Invention”).) A person with less education but more relevant practical experience, depending on the nature of that experience and degree of exposure to LED fabrication and design (including the involved materials, chemistry, and physics), could also qualify as a POSITA in the field of the ’435 patent. (Ex-1003-Pattison at ¶¶26-27.)

Pet. 10. Patent Owner neither addresses Petitioner’s description of the level of ordinary skill in the art, nor provides its own description in the Preliminary Response.

At this stage of the proceeding, we adopt Petitioner’s definition as we find it is consistent with the level of skill in the art at the time of the invention as reflected by the prior art and the ’435 patent. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. Claim Construction

The Board applies the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2020). Under that standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317.

Petitioner asserts that the claim terms in the challenged claims should receive their plain and ordinary meanings and that no express constructions of the terms is needed. Pet. 10–11. Patent Owner agrees that no claim terms require construction. Prelim. Resp. 8–9.

At this stage of the proceeding, we agree with the parties that express construction of claim terms is unnecessary for purposes of rendering this Decision. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

C. The Yang Grounds

Petitioner asserts that claims 1, 2, 6, and 7 are rendered obvious by Yang in view of Schubert and/or Aanegola. Pet. 27–66. Petitioner asserts also that claims 1, 2, 6, and 7 are rendered obvious by Yang in view of Van Zant, and in further view of Hawrylo and/or Yukimoto. *Id.* at 66–73. Patent Owner challenges both contentions. Prelim. Resp. 11–63.

I. Yang

Yang relates to an integrated light-emitting device including multiple p-n diodes integrated monolithically on a single insulating substrate.

Ex. 1004 ¶ 7. In one embodiment of the light-emitting device, at least one sidewall of the light-emitting diode is beveled. *Id.* ¶ 14. Beveling at least one sidewall of the light-emitting device enhances light extraction. *Id.* ¶ 17. The p-n diodes may have at least one beveled sidewall to enhance light extraction out of the light-emitting diodes. *Id.* ¶¶ 15, 17.

Yang’s Figure 1 is set forth below.

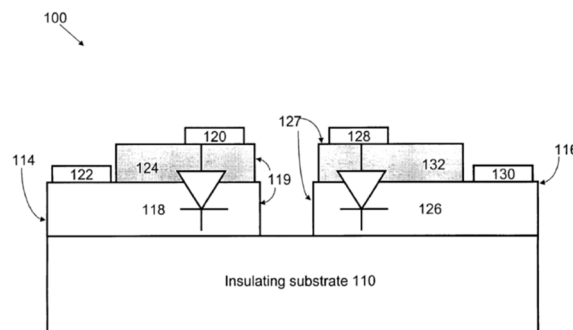


FIG. 1

Yang's Figure 1 shows a schematic cross-section of an integrated light-emitting device that includes two p-n diodes on the same substrate isolated from each other. *Id.* ¶ 18. The integrated device includes two p-n diodes 114, 116 over insulating substrate 110. *Id.* ¶ 38. P-n diode 114 includes semiconductor layers 118 and 124, together forming p-n diode structure 119, and electrodes 120 and 122. *Id.* P-n diode 116 includes semiconductor layers 126 and 132, together forming p-n diode structure 127, and electrodes 128 and 130. *Id.* The semiconductor layers 118, 124, 126, and 132 are monolithically grown over insulating substrate 110. *Id.*

Yang's Figure 2 is set forth below.

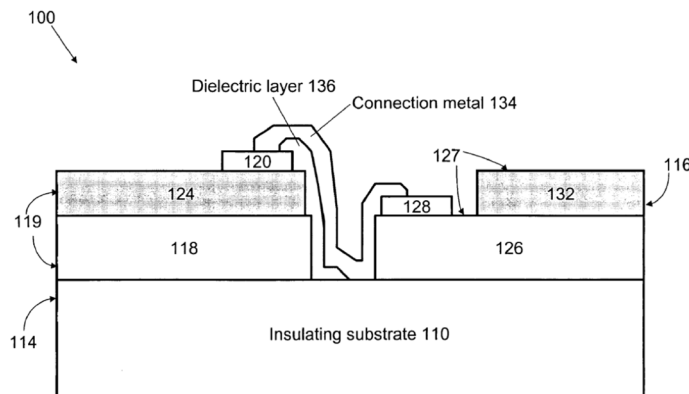
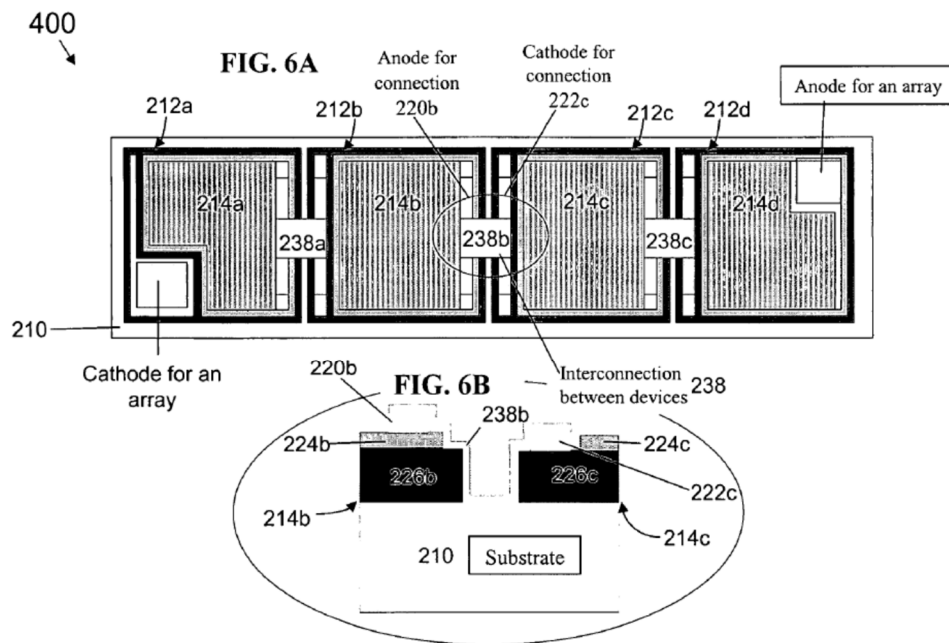


FIG. 2

Yang's Figure 2 shows a schematic cross-section of an integrated light-emitting device that includes two p-n diodes with electrodes from each diode connected after device isolation. *Id.* ¶ 19. As in Figure 1, Figure 2 depicts the device 100 including two p-n diodes 114, 116, over insulating substrate 110. *Id.* ¶¶ 38, 40. As shown in Figure 1, Figure 2 depicts P-n diode 114 includes semiconductor layers 118 and 124, together forming p-n diode structure 119, and electrodes 120 and 122. *Id.* ¶ 38. P-n diode 116 includes semiconductor layers 126 and 132, together forming p-n diode structure 127, and electrodes 128 and 130. *Id.* The semiconductor layers 118, 124, 126, and 132 are monolithically grown over insulating substrate 110. *Id.*

Electrode 120 (anode) of p-n diode 114 is connected to electrode 128 (cathode) of p-n diode 116 via connection metal 134. *Id.* ¶ 40. Insulating layer 136 is deposited between the p-n junction structures p-n diode 114 and connection metal 134 to avoid shorting p-n diode 114 with connection metal 134. *Id.*

Yang's Figures 6a and 6b are set forth below.



FIGS. 6A-6B

Figure 6a of Yang is a schematic top view of an integrated light-emitting device of the invention with an array of four light-emitting diodes monolithically integrated in series over a common substrate. *Id.* ¶ 23.

Figure 6b of Yang depicts an enlarged cross-section of the circled area in Figure 6a, and shows the interconnection between two adjacent diodes. *Id.*

¶ 24. Light-emitting diodes 214b and 214c are interconnected through electrodes 220b and 222c of opposite polarities. *Id.* ¶ 52. Semiconductor layers 224b and 224c and 226b and 226c form p-n diode structures for light-emitting diodes 214b and 214c. *Id.*

Yang's Figure 8 is set forth below.

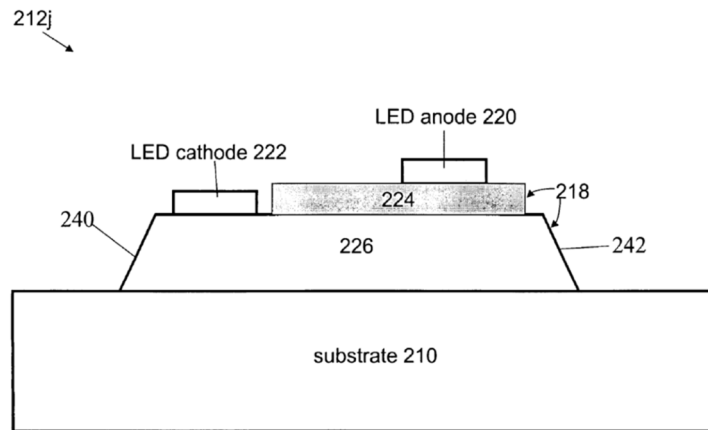


FIG. 8

Figure 8 of Yang is a schematic cross-section of a light-emitting device of the invention with beveled sidewalls 240 and 242 of semiconductor layer 226. *Id.* ¶¶ 28, 63. P-n diode structure 218, including p-type semiconductor layer 224 and a stack of p- and n-type semiconductor layers 226, is formed on a substrate. *Id.* ¶ 63. “Preferably, the side wall is beveled to have a slope of about between 10 and about 50 degrees, more preferably about 30 degrees, with respect to a line normal to a major plane of the substrate.” *Id.*

2. Analysis

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) if in the record, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18

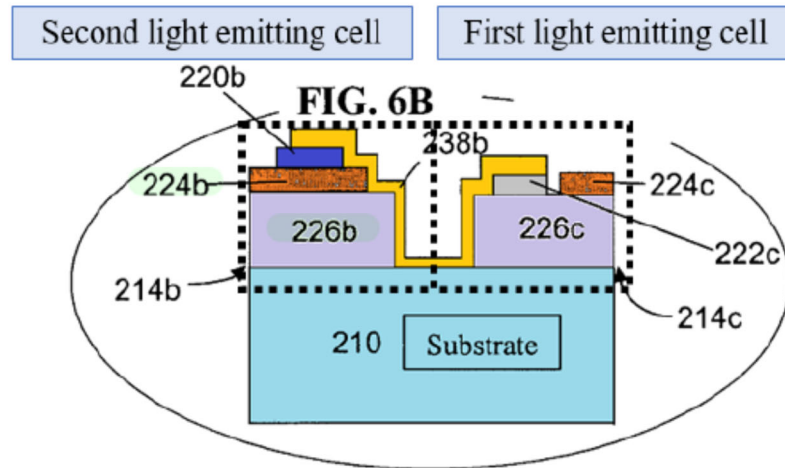
(1966). Consideration of the *Graham* factors “helps inform the ultimate obviousness determination.” *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc).

For each of the Yang grounds, Petitioner asserts that Yang expressly discloses every limitation of the challenged claims except for the limitations requiring “a second insulation layer that overlaps the second conductive material” and reciting that “the second insulation layer comprise[s] a light transmitting material.” Pet. 27, 70. Petitioner asserts that those limitations are conventional aspects of an LED package that were known in the art, as evidenced by Schubert and/or Aanegola (ground 1) and Van Zant, Hawrylo, and Yukimoto (ground 2). *Id.*

In the following discussion, we focus on Petitioner’s assertion in each of the Yang grounds that Yang teaches “the first and second light emitting cells comprise:” (a) “a first semiconductor layer” and “a second semiconductor layer,” (b) “an active layer disposed between the first and the second semiconductors layers,” and (c) “a first inclined surface,” wherein “the first inclined surface is continuous and has a slope of approximately 20° to approximately 80° from a horizontal plane of the substrate,” as recited by independent claim 1. Pet. 32–61, 70; Ex. 1001, 21:6–12, 25–27.

We begin by referring to Petitioner’s annotated version of Yang’s Figure 6b, along with Petitioner’s table identifying the first and second semiconductor layers in the figure. Petitioner’s annotated version of Yang’s Figure 6b and Petitioner’s table are set forth below.

Figure	“first semiconductor layer”	“second semiconductor layer”
6B, first cell (214c)	n-type layer 226b (light purple)	p-type layer 224b (orange)
6B, second cell (214b)	n-type layer 226c (light purple)	p-type layer 224c (orange)

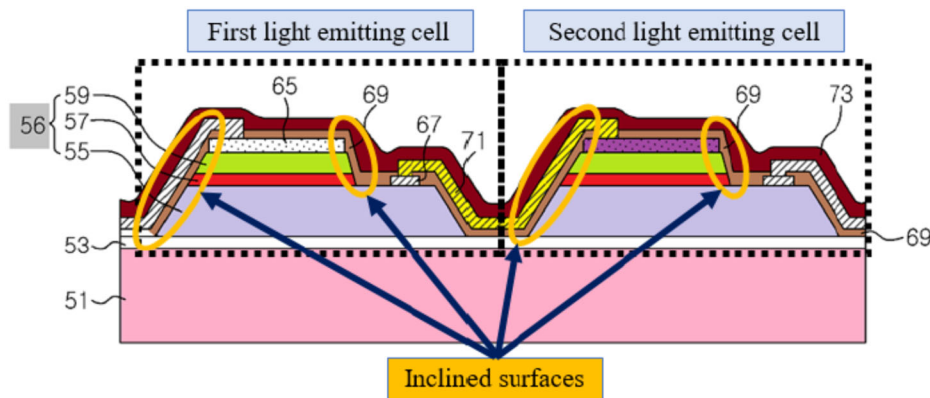


Petitioner’s annotated version of Yang’s Figure 6b includes dashed boxes and two headings to identify what it alleges to be Yang’s first and second light emitting cells. Pet. 36, 38. The annotated version of Yang’s Figure 6b also depicts the “substrate” (210) with a blue color, the “first semiconductor layer” (226b, 226c) of each light emitting cell with a light purple color, the “second semi-conductor layer” (224b, 224c) of each light emitting cell with an orange color, the “first conductive material” (220b) disposed on the second semiconductor layer (224b) of the second light emitting cell (214b) with a dark purple color, and a “second conductive material” (238b) with a gold color. *Id.* at 35, 38, 44–46, 52.

Petitioner notes that Yang’s Figure 6b does not depict an active layer. *Id.* at 39. Petitioner has not added a depiction of the active layer in its annotated version of Yang’s Figure 6b. Petitioner asserts, however, that Yang discloses the limitation “an active layer disposed between the first and the second semiconductors layers,” as recited by claim 1, by teaching, in reference to Figure 1, that “[i]n a preferred embodiment, semiconductor

layers 118 and [126] include an active layer” Pet. 39 (quoting Ex. 1004 ¶ 38 (brackets are Petitioner’s)).⁹ Petitioner asserts also that Yang explains that “an active region can be sandwiched between the n-type and p-type gallium nitride-based semiconductor layers.” *Id.* at 40 (quoting Ex. 1004 ¶ 68).

For the “first inclined surface,” Petitioner initially refers to its annotated version of Figure 32 of the ’435 patent, set forth below. Pet. 41.



Petitioner’s annotated version of Figure 32 of the ’435 patent adds dashed boxes and headers to indicate the first and second light emitting cells, and adds a different color to each component of the light emitting device, wherein the “substrate” (50) is pink, the “first semiconductor layer” (55) is light purple, the “active layer” (57) is red, and the “second semiconductor layer” (59) is green. *See* Pet. 37, 41. The Petitioner’s annotated version of

⁹ When quoting Yang, Petitioner replaces reference numeral 125 with reference numeral 126, correcting what appears to be a mistake in Yang. Reference numeral 125 does not appear in Yang Figure 1, and elsewhere in paragraph 38, Yang identifies the n-type semiconductor layer using reference numeral 126. Ex. 1004 ¶ 38 (“In FIG. 1, semiconductor layers 118 and 126 represent n-type semiconductor layers.”). We note that the same mistake appears a second time in Yang paragraph 38. *Id.* (“Alternatively, semiconductor layers 118 and 124 [*sic*, 126] can be a stack of p-type and n-type semiconductor layers”).

Figure 32 of the '435 also adds a gold circle around what Petitioner considers to be the inclined surfaces of the light emitting cells. *Id.* at 41.

Of those identified inclined surfaces, Petitioner asserts that the “first inclined surface” of the light emitting cells corresponds to the “longer inclined surface on the left side of each respective light emitting cell shown in Figure 32” of the '435 patent. *Id.* Notably, the longer inclined surface on the left side of each light emitting cell includes the surface of the first and second semiconductor layers, and the active layer disposed therebetween. *Id.* Similarly, for the limitation reciting that “the first inclined surface is continuous and has a slope of approximately 20° to approximately 80° from a horizontal plane of the substrate,” Petitioner identifies the left side of each inclined surface as having such a continuous surface. *Id.* at 60.

Petitioner asserts that Yang discloses these same inclined surfaces by teaching that the light-emitting diode can have at least one sidewall that is beveled. *Id.* at 42 (citing Ex. 1004 ¶ 61). Petitioner also relies on Yang's Figure 8 as showing the use of beveled sidewalls 240 and 242 on the stack of semiconductor layers 226, wherein, “[p]referably, the side wall is beveled to have a slope of about 10 and about 50 degrees, more preferably about 30 degrees, with respect to a line normal to the major plane of the substrate.” *Id.* at 42–43 (citing Ex. 1004 ¶ 63) (emphasis omitted). Petitioner asserts also that it would have been obvious to use beveled sidewalls with the embodiments of Yang illustrated in Figures 6a-6b per Yang's express suggestion to do so. *Id.* at 43. Further, Petitioner asserts it would have been obvious to make such sidewalls continuous, as shown in Yang's Figure 8. *Id.* at 61.

Patent Owner argues, among other things, that Petitioner has failed to demonstrate that Yang teaches “a first inclined surface” that is “continuous

and has a slope of approximately 20° to approximately 80° from a horizontal plane of the substrate,” as required by claim 1. Prelim. Resp. 36. Patent Owner agrees with Petitioner that the ’435 patent depicts the first inclined surface that is continuous as the longer inclined surface on the left side of the light-emitting cell in Figure 32, comprising the first and second semiconductor layers 55, 59 with the active layer 57 therebetween. *Id.* at 36–40, *see* Pet. 41. Patent Owner contends, however, that Petitioner has not supported its assertion that Yang similarly discloses an inclined surface that is continuous. Prelim. Resp. 37. Patent Owner recognizes that Yang’s Figure 8 discloses an inclined surface in the light emitting cells, but asserts that it does not disclose an inclined surface that is continuous. *Id.* Patent Owner observes that only the sidewall of semiconductor layer 226 is beveled and that such incline does not continue to include the sidewall of semiconductor layer 224, or that of an active layer (not shown in Figure 8). *Id.* at 38. Patent Owner asserts that “[t]he presence of the vertical sidewall in the semiconductor layer 224 creates a step or transition from the beveled sidewall of the semiconductor layer 226. It does not continue.” *Id.* Patent Owner asserts that Petitioner’s declarant, Dr. Pattison, does not provide any further explanation or analysis of how Yang discloses an inclined wall that is continuous by stating that “[a]s shown above, the inclined surface is continuous, as show in FIG. 8, and preferably has a slope of 30°.”). *Id.* at 40 (quoting Ex. 1003, 60).

Based upon our consideration of the arguments and evidence, we agree with Patent Owner that Petitioner has not shown sufficiently for institution that Yang teaches or suggests that its light emitting cells comprise an inclined surface that is continuous, as required by independent claim 1. As set forth above, Petitioner demonstrates with its annotated version of

Figure 32 of the '435 patent that for an inclined surface to be continuous, the inclined surface must extend along a surface of the first and second semiconductor layers, with the active layer disposed therebetween. *See* Pet. 41, 60. Referring to Yang's Figure 6b, and what Petitioner labels as the first and second light emitting cells, Petitioner identifies semiconductor layer 226b/c as the recited "first semiconductor layer" and semiconductor layer 224b/c as the recited "second semiconductor layer." Pet. 38. Petitioner relies on Yang's teachings that an active layer may be sandwiched between the semiconductor layers. *Id.* at 39–40. For example, Petitioner refers to Yang's teaching, in reference to Figure 1, that "semiconductor layers 118 and [126] include an active layer" Pet. 39 (quoting Ex. 1004 ¶ 38) (emphasis omitted). Petitioner also relies on Yang's teaching that "an active region can be sandwiched between the n-type and p-type gallium nitride-based semiconductor layers." *Id.* at 40 (quoting Ex. 1004 ¶ 68).

We note that Yang teaches that semiconductor layers 118 and 126 in Figure 1 may represent n-type semiconductor layers, or alternatively, each may be a "stack of p-type and n-type semiconductor layers where the top layer of the stack is an n-type semiconductor layer." Ex. 1004 ¶ 38. Similarly, Yang teaches, in reference to Figure 8, that p-n diode structure 218 includes p-type semiconductor layer 224 and a stack of p- and n-type semiconductor layers 226. *Id.* ¶ 63. Thus, Yang's teachings relating to the placement of an active layer allow that active layer to be placed either within the "stack" of p- and n-type semiconductor layers, or above those layers that may be stacked.

Therefore, referring to Yang's Figure 6b, the active layer may be disposed within stacked semiconductor layers depicted as 226b, or the active layer may be placed between semiconductor layers 226b and 224b. The

same is true for Figure 8. In Yang's Figure 8, the active layer may be disposed within stacked semiconductor layers depicted as 226, or the active layer may be between semiconductor layers 226 and 224. The challenged claims limit the location of the active layer by requiring it to be "disposed between the first and the second semiconductor layers." Petitioner has identified what it considers to be the first semiconductor and second semiconductor layers in Yang's Figure 6b: the "first semiconductor layer" is 226b/c, and the "second semiconductor layer" is 224b/c. Pet. 38. In Yang's Figure 8, Petitioner contends first semiconductor layer corresponds with structure 226, and the second semiconductor layer corresponds with structure 224. To meet the claim limitation for the active layer, the active layer must be disposed between those first and second semiconductor layers, i.e., between structures 226b/c and 224b/c, and not within structure 226b/c for Figure 6b. The same is true with respect to Figure 8. In other words, to read on claim 1, the active layer must be disposed between structures 226 and 224, and not within structure 226.

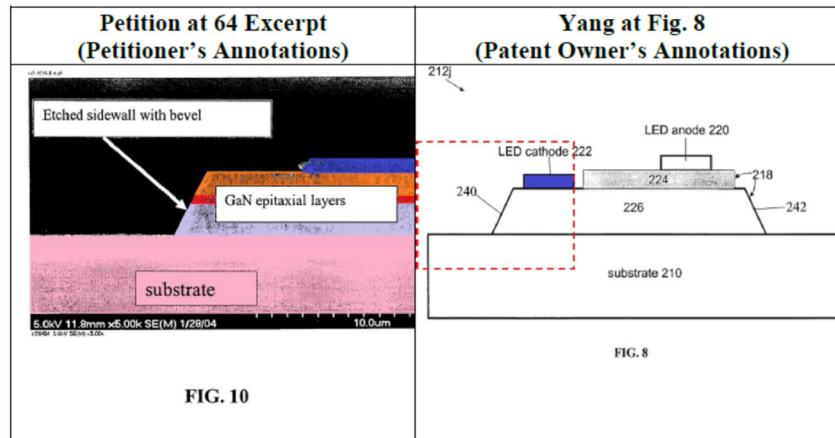
Based on that required positioning of the active layer, in view of Petitioner's identified first and second semiconductor layers, we agree with Patent Owner that Petitioner has not shown that Yang's Figure 8 depicts an inclined surface that is continuous, as required by claim 1. Instead, Figure 8 shows only an inclined surface on what Petitioner considers to be the first semiconductor layer. As discussed above, it is Petitioner's own position that for an inclined surface to be continuous as claimed, the incline must continue along the first semiconductor layer, the active layer, and the second

semiconductor layer. We do not see, nor has Petitioner shown, that Yang discloses that feature.

Insofar as Petitioner asserts, in the alternative, that it would be obvious to make the sidewalls in Yang's Figures 6a-6b to have beveled sidewalls that are continuous, Petitioner has failed to set forth its obviousness rationale sufficiently for institution. Pet. 61. In particular, Petitioner does not explain sufficiently how and why a person of ordinary skill in the art would have modified Yang's Figures 6a-6b embodiment to have continuous sidewalls. What is missing from the Petition is, for example, the identification of some teaching or suggestion in the prior art or some knowledge in the art that it would have been obvious to modify Yang's structure to extend the inclined surface on the first semiconductor layer upward along the surface of the upper active layer and further along the surface of the second semiconductor layer, and to do so such that the resulting incline is continuous and has a slope within the recited degree range. Instead, Petitioner relies on an unsupported assertion that Yang depicts a continuous sidewall in Figure 8. Pet. 61. Indeed, Petitioner's obviousness contention as to the required "continuous" feature of the first inclined surface is presented in one sentence: "It would further be obvious to make such sidewalls continuous, as shown in FIG. 8, and preferably with a slope of 30." *Id.* (citing Ex. 1004 ¶ 63, and Figs. 10–11).

To the extent that Petitioner relies upon Yang's Figure 10 in that citation, we note that Yang explains that Figure 10 is a cross-sectional scanning electron microscope image of the light-emitting device in Figure 8. Ex. 1004 ¶¶ 74, 80. Petitioner, nevertheless, relies on a modified version of Yang's Figure 10 (regarding dependent claim 7) wherein Petitioner indicates that the inclined sidewall depicted comprises two semiconductor layers with

an active layer disposed in between them. Pet. 64. Patent Owner provides an annotated version of Yang's Figure 8 and places it side-by-side with Petitioner's modified version of Figure 10, as set forth below.



Patent Owner's side-by-side figures depict Petitioner's modified version of Yang's Figure 10 on the left and Patent Owner's annotated version of Yang's Figure 8 on the right. Prelim. Resp. 42. Petitioner modifies Yang's Figure 10 by adding light purple, red, and orange colored sublayers to the beveled layer labeled "GaN epitaxial layers," where no such sublayers are shown in the original figure. Patent Owner asserts that Petitioner relies on numerous incorrect assumptions and interpretations of Yang's teachings. *Id.* at 40. We agree. As can be appreciated from the side-by-side annotated versions of Yang's figures, Figure 10 depicts semiconductor layer 226 as the etched sidewall with bevel. Below the semiconductor layer is the substrate and above the semiconductor layer is the LED cathode, as similarly depicted in Yang's Figure 8. Yang's Figure 10 does not include the portion of Yang's Figure 8 depicting semiconductor layer 224, which Petitioner has relied upon as the second semiconductor layer. Nor does Yang's Figure 10 depict an active layer, much less an active layer disposed between semiconductor layers 224 and 226. Thus,

Petitioner's reliance on Yang's Figure 10 as showing a continuous inclined surface is unsupported and misplaced.

Further, as Patent Owner asserts, the testimony of Petitioner's declarant, Dr. Pattison, also fails to support either an express teaching or an obviousness rationale regarding the continuous first inclined surface limitation, as he merely states “[a]s shown above, the inclined surface is continuous, as shown in FIG. 8, and preferably has a slope of 30°.” Prelim. Resp. 39–40; Ex. 1003, 60.

Petitioner does not rely on any of the other cited art, in either Yang ground, to address the continuous inclined surface limitation. Because Petitioner has failed to show that Yang teaches or suggests a light emitting device comprising a first inclined surface that is continuous, as required by independent claim 1, we determine that Petitioner has not shown a reasonable likelihood of prevailing on its assertion that independent claim 1 would have been rendered obvious by the combined teachings of Yang, Schubert and/or Aanegola, or the combined teachings of Yang, Van Zant, and Hawrylo and/or Yukimoto. For at least the same reasons, we also determine that Petitioner has not shown a reasonable likelihood of prevailing on its assertion that dependent claims 2, 6, and 7 would have been rendered obvious by either of those combined teachings.

D. The Salam Grounds

Petitioner asserts that claims 1 and 7 are anticipated by Salam. Pet. 73–94. Petitioner asserts also that claims 2 and 6 are rendered obvious by Salam. *Id.* at 94–96. Patent Owner challenges both contentions. Prelim. Resp. 63–94.

1. Salam

Salam relates to single-chip LED lamps that are up to 250 times more powerful than a conventional single-chip LED lamp. Ex. 1005, 1:5–8.

Salam Figure 3 is set forth below.

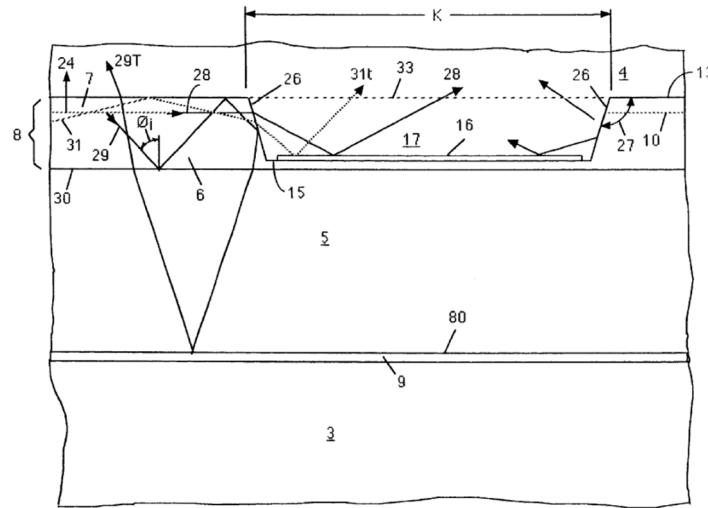


FIG. 3

Salam Figure 3 is a sectional view of a portion of an LED chip according to an embodiment of the invention. *Id.* at 2:50. Figure 3 depicts an LED chip mounted on metal support 3. *Id.* at 3:15. The chip comprises transparent base 5 over which is formed layer 6 of n-type semiconductor material. *Id.* at 3:20–21. A layer of p-type semiconductor material 7 is formed over n-layer 6. *Id.* at 3:21–22. Semiconductor layer 8 comprises semiconductor layers 6 and 7. *Id.* at 3:24–25. The chip includes active region 10. *Id.* at 3:32–35.

Salam Figure 10 is set forth below.

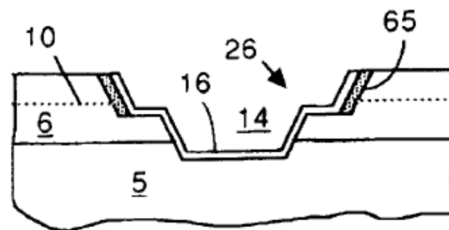


FIG. 10

Salam Figure 10 illustrates an arrangement for a trench that can be used in any of the embodiments of the invention. *Id.* at 9:42–43. “As shown, trench 14 cuts into substrate 5, and includes translucent dielectric 65 over the p-layer portion of stepped sidewall 26.” *Id.* at 9:43–45. Salam teaches that “in various arrangements discussed herein trench 14 may have a side-wall profile that includes one or more steps.” *Id.* at 8:22–24.

2. Analysis

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Schering Corp. v. Geneva Pharms*, 339 F.3d 1373, 1379 (Fed. Cir. 2003) (quoting *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987)).

For its anticipation challenge of independent claim 1 and dependent claim 7, Petitioner provides annotated versions of Salam’s Figures 3 and 5 along with a table identifying how those figures allegedly disclose each limitation of the challenged claims. Pet. 46–47. Petitioner’s annotated versions of Salam’s Figures 3 and 5 and Petitioner’s table are set forth below.

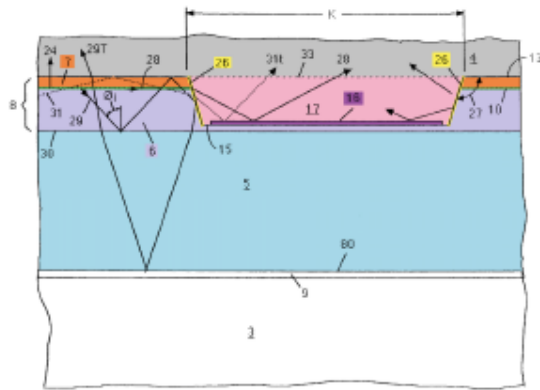


FIG. 3

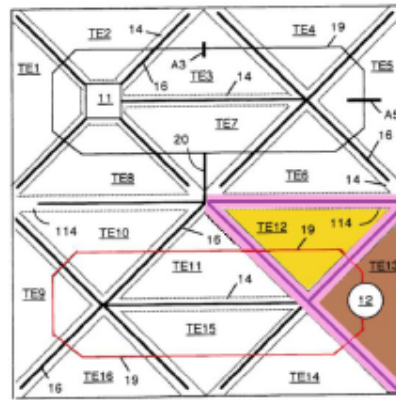
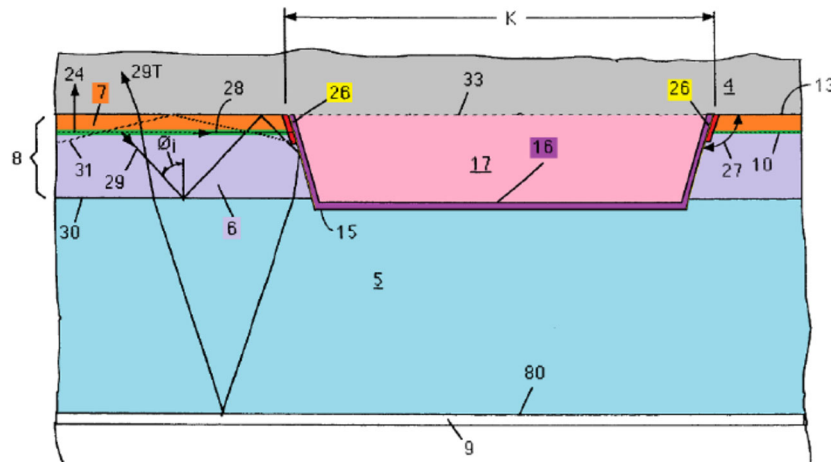


FIG. 5

Limitation	Salam-771
[1-PRE] A light emitting device	FIGS. 3, 5 relate to light emitting devices
[1a] substrate	Substrate 5 (blue)
[1b] 1st and 2nd cells	Two light emitting elements TE12 & TE13
[1c-i] 1st semiconductor layer	p-type layer 7 (orange in FIG. 3)
[1c-ii] 2nd semiconductor layer	n-type layer 6 (light purple in FIG. 3)
[1c-iii] active layer	Active region 10 (green in FIG. 3)
[1c-iv] and [1i] 1st inclined surface, 20°-80°	Side faces 26 (yellow in FIG. 3)
[1d] 1st conductive layer	Gold conductor 16 (dark purple)
[1e] 1st insulation layer	Transparent dielectric 17 (pink)
[1f] 2nd conductive layer	Conductor 19 (red)
[1g] 2nd insulation layer	Transparent dielectric material 4 (gray)
[1h] light-transmitting insulation layers	See 1e and 1g
[2] transparent electrode	See 1d
[6] ITO, nickel, or gold transparent electrode	See 1d
[7a-7c] 2nd inclined surface of 20°-80°	See 1c-iv and 1i

Petitioner's annotated versions of Salam's Figures 3 and 5 include color coding for certain elements listed in the table. Petitioner explains that the table shows the correspondence between the claim limitations and Salam with reference to the annotated versions of Figures 3 and 5. *Id.* at 73.

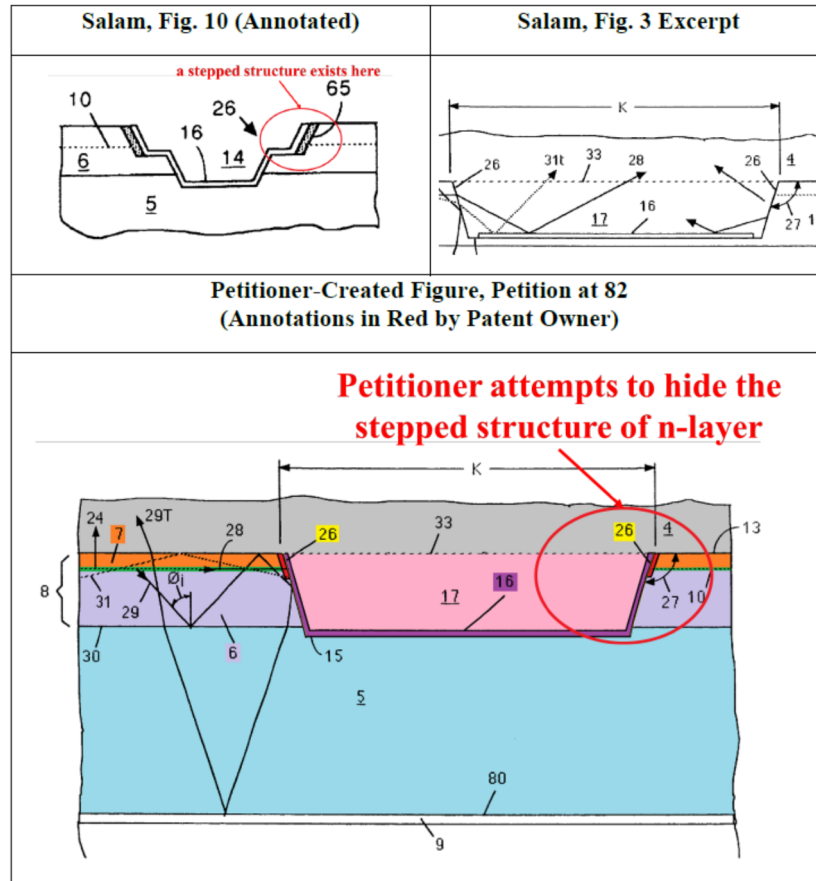
In its discussion of the claim limitations, Petitioner relies on another annotated version of Salam’s Figure 3 that it refers to as an “alternative embodiment” of Figure 3. Pet. 84. We refer to this figure as Petitioner’s alternative version of Salam’s Figure 3, set forth below.



Petitioner’s alternative version of Salam’s Figure 3 has been created by Petitioner to reflect features from Salam’s Figures 3 and 10. In this version, trench 17 is modified to cut into substrate 5. Pet. 79–80. According to Petitioner, Salam teaches that modification by disclosing that “FIG. 10 shows another arrangement for trench 14 that can be used in any of the chips described herein. As shown, trench 14 cuts into substrate 5, and includes translucent dielectric 65 over the p-layer portion of stepped side wall 26.” *Id.* (quoting Ex. 1005, 9:42–47) (emphasis omitted). Petitioner’s alternative version of Salam’s Figure 3 also modifies the trench 14 in an attempt to remove the steps from the inner side-wall profile. Petitioner draws support for that modification from Salam’s teaching that “in various arrangements discussed herein, trench 14 may have a side-wall profile that includes one or more steps.” *Id.* at 80 (quoting Ex. 1005, 8:17–24) (emphasis omitted). According to Petitioner, because Salam teaches that the side-wall profile “may” include one or more steps, those steps in Figure 3 may be removed.

Id. at 80–81. Based on those modifications, Petitioner asserts that Salam discloses a first inclined surface that is continuous. *Id.* at 84–85, 91–92.

Patent Owner challenges Petitioner’s anticipation ground because, among other reasons, Petitioner relies on its own redrawn version of Salam’s figures that are not supported by Salam’s disclosure to show anticipation. Prelim. Resp. 73. In particular, Patent Owner asserts that in redrawing Salam’s Figure 3, Petitioner attempts to hide the stepped structure of the n-layer. *Id.* at 73–74. According to Patent Owner, Petitioner’s alternative version of Salam’s Figure 3 (which combines features of Figure 10) still includes a stepped structure on the first semiconductor (n-type layer) 6. Petitioner’s annotated figures indicate this layer with a light purple color. *See* Pet. 73. Patent Owner reproduces Petitioner’s alternative version of Salam’s Figure 3 and adds annotations to show the stepped structure of the n-layer. Patent Owner’s annotation of Petitioner’s alternative version of Salam’s Figure 3 is set forth below.



Patent Owner shows in its annotated version of Salam’s Figure 10 where the stepped structure exists. As shown in Figure 10, that stepped structure runs along the surface of n-layer 6, i.e., the first semiconductor layer. Prelim. Resp. 74. Similarly, Patent Owner’s annotations of Petitioner’s alternative version of Salam’s Figure 3 show that the stepped structure on the surface of n-layer 6 remains. *Id.* at 74, 79. According to Patent Owner, Petitioner has, therefore, not shown even in its alternative version of Salam’s Figure 3 that Salam discloses a first inclined surface that is continuous.

Based upon our review of the arguments and evidence, we agree with Patent Owner that Petitioner has not identified a disclosure in Salam wherein the light emitting device comprises a first inclined surface that is continuous.

Even if Petitioner had explained how a person of ordinary skill in the art would have at once envisaged the chip depicted in Petitioner's alternative version of Salam's Figure 3, Petitioner has not shown that such alternative version of the chip includes a first inclined surface that is continuous.

Indeed, Petitioner's alternative version does not even show that what it refers to as the first semiconductor layer having a first inclined surface that is continuous. As seen in Petitioner's alternative version of Salam's Figure 3, the first semiconductor layer 6 (colored light purple) has a step at side wall 26 (colored red). Pet. 82; Prelim. Resp. 74; *see also* Ex. 1005, 9:46–47 (“Track 16 makes electrical contact with n-layer 6 at side wall 26.”).

Because Petitioner has failed to show that Salam discloses a light emitting device comprising a first inclined surface that is continuous, as required by independent claim 1, we determine that Petitioner has not shown a reasonable likelihood of prevailing on its assertion that independent claim 1 is anticipated by Salam. For at least the same reasons, we also determine that Petitioner has not shown a reasonable likelihood of prevailing on its assertion that dependent claim 7 is anticipated by Salam.

For its obviousness challenge of dependent claims 2 and 6, Petitioner again relies on Salam as disclosing the elements of claim 1, including the first inclined surface that is continuous, as set forth in its anticipation challenge. Pet. 94–96. Accordingly, we determine that Petitioner has not shown a reasonable likelihood of prevailing in its challenge of claims 2 and 6 for at least the same reasons discussed regarding the challenge of the claim 1 from which claims 2 and 6 depend.

III. CONCLUSION

For the foregoing reasons, we deny the Petition and decline to institute the requested *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that that Petitioner's request for an *inter partes* review of 1, 2, 6, and 7 of the '435 patent is *denied*.

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