

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC,
Patent Owner.

IPR2020-01020¹
Patent RE42,035 E

Before KARL D. EASTHOM, BARBARA A. BENOIT, and
SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00391 and has been joined as a party to this proceeding.

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 (the “challenged claims”) of U.S. Patent No. RE42,035 E (Ex. 1001, the “’035 patent”). Petitioner filed a Declaration of Dr. Stanley Shanfield (Ex. 1002) with its Petition. Arbor Global Strategies LLC (“Patent Owner”), filed a Preliminary Response (Paper 7, “Prelim. Resp.”). The parties also filed authorized preliminary briefing. Papers 8–11.

After the Institution Decision (Paper 11, “Inst. Dec.”), Patent Owner filed a Patent Owner Response (Paper 16, “PO Resp.”) and a Declaration of Dr. Krishnendu Chakrabarty (Ex. 2015); Petitioner filed a Reply (Paper 19) and a Reply Declaration of Dr. Stanley Shanfield (Ex. 1030); and Patent Owner filed a Sur-reply (Paper 24, “Sur-reply”). Thereafter, the parties presented oral arguments via a video hearing (September 14, 2021), and the Board entered a transcript into the record. Paper 29 (“Tr.”).

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies itself, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. Pet. 82. Taiwan Semiconductor Manufacturing Co. Ltd. identifies itself and TSMC North America as real parties-in-interest. *See* IPR2021-00391, Paper 2, 79. Patent Owner identifies itself. Paper 5, 1.

B. Related Proceedings

The parties identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd. et al.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) (“District Court” or “District Court”) as a related infringement action involving the ’035 and two related patents, U.S. Patent No. 7,282,951 B1 and U.S. Patent No. 6,781,226 B2, which contain the same specification as the ’035 patent. *See* Pet. 82; Paper 5.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in the two related patents, respectively IPR2020-01021 and IPR2020-01022.

C. The ’035 patent

The ’035 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the ’035 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” *Id.*

Figure 4 follows:

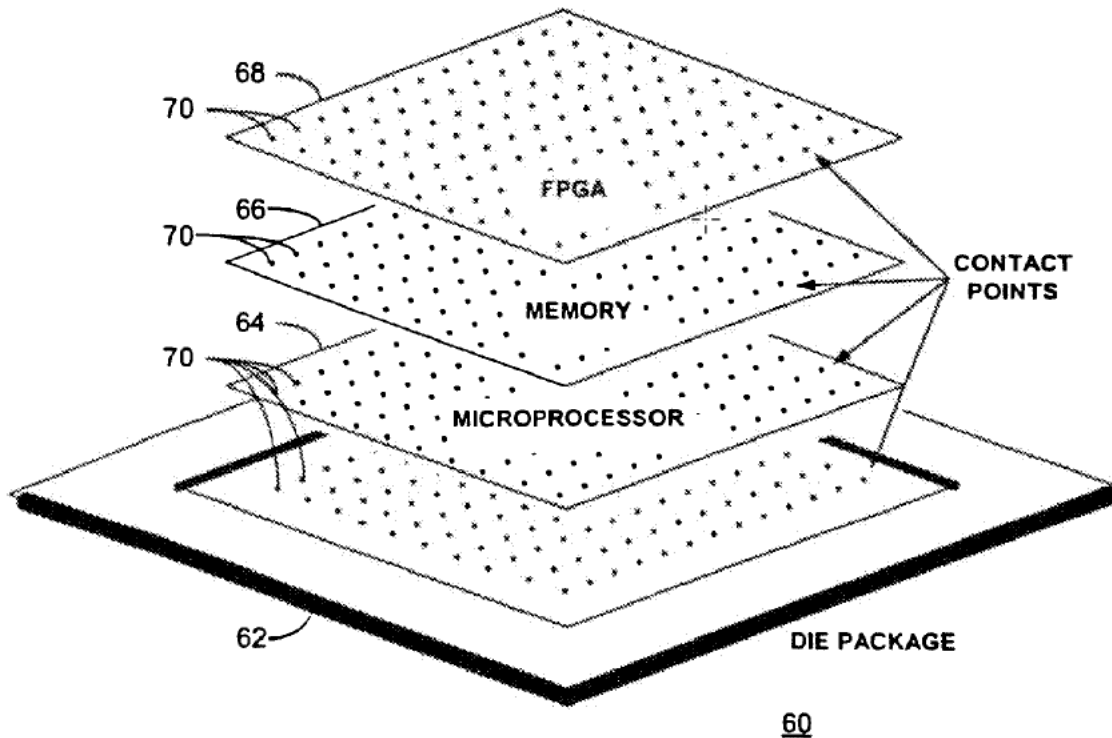


Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using metal and “contact points, or holes, 70.” Ex. 1001, 4:6–20.

The '035 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” *See* Ex. 1001, 1:17–32.

Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See id.* A “reconfigurable processor” provides a known benefit of flexibly providing the specific functional units required by an application after manufacture. *See id.*

D. Illustrative Claims 1 and 10

The Petition challenges independent claims 1, 9, 17, and 25, and claims 3, 4, 8, 9, 11, 13–16, 19–22, 26, 28, and 29, which ultimately dependent from one of the independent claims. Claim 1 illustrates the challenged claims at issue:

1. A processor module comprising:

[1.1] at least a first integrated circuit die element including a programmable array;

[1.2] at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and

[1.3] wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

Ex. 1001, 6:11–22 (information added by Board to conform to Petitioner’s nomenclature); *see* Pet. 17–19 (addressing claim 1).

E. The Asserted Grounds

Petitioner challenges claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 patent on the following grounds (Pet. 3):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 5, 7	102 ²	Alexander ³
9, 13, 15	103	APA, Alexander
1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29	103	Koyanagi, ⁴ Alexander
1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29	103	Bertin, ⁵ Cooke ⁶

II. ANALYSIS

Petitioner challenges claims 1, 5, and 7 for anticipation and claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 for obviousness. Patent Owner disagrees.

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103. For purposes of institution, the '035 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA versions of § 102 and § 103 apply. The parties describe December 5, 2001 as the earliest effective filing date at issue here. PO Resp. 4–5; Pet. 9.

³ M.J. Alexander et al., “Three-dimensional Field-programmable Gate Arrays,” Proceedings of Eighth International Application Specific Integrated Circuits Conference, September 18–22, 1995. Ex. 1006.

⁴ M. Koyanagi et al., “Future System-on-silicon LSI Chips,” IEEE Micro, Vol. 18, Issue 4, July/August 1998. Ex. 1007.

⁵ Bertin, US 6,222,276 B1, issued Apr. 24, 2001. Ex. 1009.

⁶ Cooke, US 5,970,254, issued Oct. 19, 1999. Ex. 1008.

A. *Legal Standards*

“Section 103(a) forbids issuance of a patent when ‘the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.’” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.⁷ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

“In order to render a claimed invention obvious, the prior art as a whole must enable one skilled in the art to make and use the apparatus or method.” *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1289, 1297 (Fed. Cir. 2010), *vacated on other grounds*, 374 F. App’x 35 (2010), *reinstated in part*, 649 F.3d 1276, 1296 (2013) (en banc) (reinstating obviousness portion of *Therasense*); *see also In re Kumar*, 418 F.3d 1361, 1368 (Fed. Cir. 2005) (similar holding in the context of examination). However, any “suggestion that [the prior art references] are non-enabled is

⁷ The Petition states that secondary considerations do not exist. Pet. 79. On this record, Patent Owner does not assert secondary indicia of nonobviousness.

misplaced, since even ‘[a] non-enabling reference may qualify as prior art for the purpose of determining obviousness,’ *Symbol Tech., Inc. v. Opticon, Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991), and even ‘an inoperative device . . . is prior art for all that it teaches,’ *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989).” *ABT Sys., LLC v. Emerson Elec. Co.*, 797 F.3d 1350, 1360 n.2 (Fed. Cir. 2015)). Moreover, prior art references carry a presumption of enablement. *See In re Antor Media*, 689 F.3d 1282, 1287–1288 (Fed. Cir. 2012); *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003); *Apple Inc. v. Corephotonics, Ltd.*, No. 2020-1438, 2021 WL 2577597, at *4 (Fed. Cir. June 23, 2021) (nonprecedential) (holding that in the context of AIA trial proceedings, “regardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art” and that “[i]t was error for the Board to suggest otherwise”).

B. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Shanfield, Petitioner contends that [a] person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have been a person having a Master’s degree in Electrical Engineering, Computer Engineering, or Physics with three to five years of industry experience in integrated circuit design, layout, packaging or fabrication. Ex. 1002 ¶¶ 55–58. A greater level of experience in the relevant field may compensate for less education, and vice versa.

Pet. 9.

Patent Owner contends that “a person of ordinary skill in the art . . . would have had a Bachelor’s degree in Electrical Engineering or a related and either (1) two or more years of industry experience; and/or (2) an

advanced degree in Electrical Engineering or related field.” PO Resp. 4–5 (citing Ex. 2015 ¶ 33).

We adopt Petitioner’s proposed level of ordinary skill in the art as we did in the Institution Decision, which comports with the teachings of the ’035 patent and the asserted prior art. *See* Inst. Dec. 19. Patent Owner’s proposed level is slightly lower than Petitioner’s but it overlaps with Petitioner’s proposed level. Even if we adopted Patent Owner’s proposed level, the outcome would remain the same.

C. Claim Construction

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2019). Under the same standard applied by district courts, claim terms acquire their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Based on the current record, no terms require explicit construction. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the

controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Anticipation, Alexander, Claim 1, 5, and 7

1. Alexander

Alexander describes “stacking together a number of 2D FPGA bare dies” to form a 3D FPGA. Ex. 1006, 1. Alexander explains that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” *Id.*

Petitioner annotates Alexander’s Figure 2 as follows:

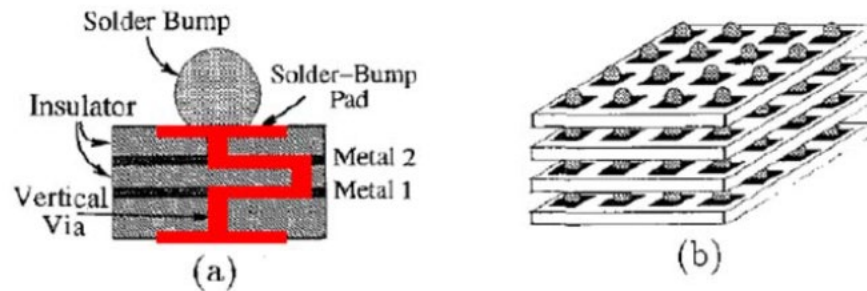


Figure 2(a) shows vertical metal connections (red) traversing a chip with a solder pad and bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1006, 253.

Alexander explains that stacking bare dies to form a 3D FPGA results in a chip with a “significantly smaller physical space,” lower “power consumption,” and greater “resource utilization” and “versatility” as compared to conventional layouts. *Id.*

2. Anticipation Analysis, Claims 1, 5, and 7

Claim 1 follows:

1. A processor module comprising:

[1.1] at least a first integrated circuit die element including a programmable array;

[1.2] at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and

[1.3] wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

Petitioner reads the claim limitations on the following annotated Figures 2a and 2b in Alexander (supported by other disclosures therein) (Pet. 18–19):

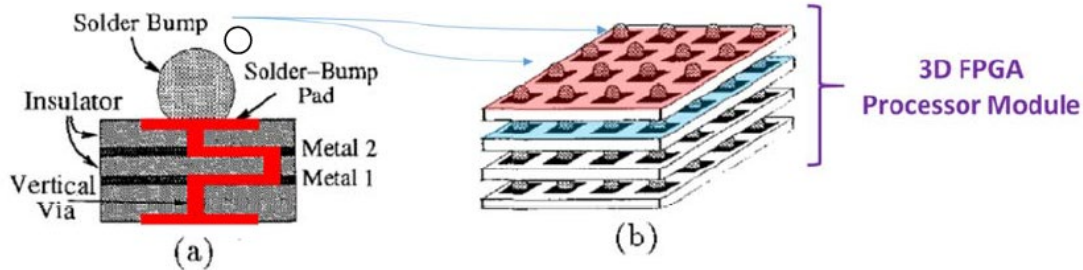
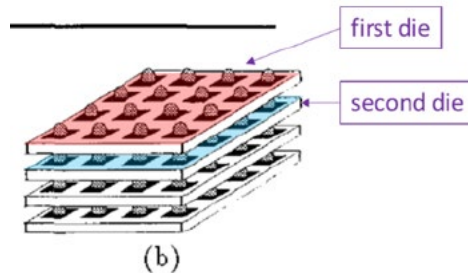


Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.



Petitioner’s annotated version of Alexander’s Figure 2b above shows the claimed first and second dies, with at least the first die and second die each including the claimed “programmable array” (a “2D FPGA die”), and with the claimed “contact points” represented by the red vertical vias in Alexander’s Figure 2a and also connected to the solder bumps in Figure 2b. See Pet. 17–19.

Quoting from Alexander and citing Dr. Shanfield, Petitioner explains as follows:

First, as shown in Alexander Figure 2(b), the adjacent first (red) and second (blue) dies are electrically coupled by a number of contact points (terminated at solder bumps) distributed throughout the surfaces of the dies. Ex. 1006, 1 (“The 3D FPGA is [] built by stacking multiple dies using solder bumps to implement the **vertical interconnections** between layers (Figure 2(b)).”). **Second**, as shown in Alexander Figure 2(a), the contact points include “vertical via[s]” (red) that traverse said die elements through a thickness thereof. Ex. 1006, 1 (“Aside from solder bumps to establish the vertical interconnections, each individual die in our 3D paradigm has vias [red] passing through the die itself, enabling electrical interconnections between the two sides of the die.”); Ex. 1002 ¶ 81.

Pet. 19 (quoting Ex. 1006, 1) (emphasis by Petitioner).

Patent Owner argues that “Alexander does not disclose ‘at least a second integrated circuit die element stacked with and electrically coupled to said programmable array,’ as recited in Claim 1 because Alexander’s proposed 3D FPGA is limited to ‘at least a first integrated circuit die element **including a programmable array.**’” PO Resp. 10 (quoting claim 1) (emphasis by Patent Owner). According to Patent Owner, “Alexander does not disclose ‘at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element.’” *Id.* at 11 (citing Ex. 2015 ¶ 48). Patent Owner reasons that “Alexander discloses modifying the known 2D FPGA architecture to form a single 3D FPGA where each logic block has six immediate neighbors instead of the typical four.” *Id.* (citing Ex. 1010, 1). According further to Patent Owner, “because Alexander fails to disclose stacking any integrated die elements with the 3D FPGA, Alexander does not

disclose ‘at least a second integrated circuit die element stacked with and electrically coupled to the programmable array.’” *Id.* at 12. In its Sur-reply, Patent Owner argues that “even if the claims could be read broadly enough for the term ‘first integrated circuit die element including a programmable array’ to encompass an array spread over more than a ‘first integrated circuit,’ Alexander does not disclose any *other* (i.e. second) “integrated circuit die element stacked with and electrically coupled to said programmable array.” Sur-reply 12.

These arguments do not undermine Petitioner’s showing. To the extent Patent Owner’s Sur-reply raises the issue, claim 1 does not recite “any other” integrated circuit that requires the first and second integrated circuits to be different types of circuits. As summarized above, including Petitioner’s annotated versions of Alexander’s figures, Petitioner relies on separate 2D FPGA on each die stack—“a first integrated die element” and a “second integrated die element” in that stack—not the complete 3D stack as “a first integrated die element.” Claim 1 recites “*at least* a first integrated circuit die element including a programmable array” and it recites “at least a second integrated circuit die element.” Therefore, claim 1 reads on one die element that includes one of Alexander’s 2D FPGAs and a second die element that includes another of Alexander’s 2D FPGAs, as Petitioner’s annotated Figure 2b above portrays.

Stated differently and as Petitioner persuasively argues, claim 1 encompasses Alexander’s different 2D FPGA layers that connect together into a 3D FPGA, forming the claimed “processor module.” *See* Reply 4–5 (“Alexander’s 3D FPGA is formed by stacking multiple ‘2D FPGA bare dies,’ and each 2D FPGA bare die can properly be mapped to either the

claimed first or second die element, as is annotated in Figure 2(b) above, because each includes a ‘programmable array’ as required by claim 1.”).

The ’035 patent supports this interpretation of a “processor module,” as recited in the preamble of claim 1, as including two 2D FPGA dies. For example, it states that “a particular embodiment” of “a *processor module* with reconfigurable capability may be constructed by *stacking one or more* thinned microprocessor, memory and/or *field programmable gate array* (*‘FPGA’*) *die elements* and interconnecting the same utilizing contacts that traverse the thickness of the die.” Ex. 1001, code (57) (emphasis added). As the Petition shows, Alexander discloses “one or more . . . field programmable gate array (*‘FPGA’*) die elements . . . interconnect[ed with each other] . . . utilizing contacts that traverse the thickness of the die.” *See id.*; Pet. 19. The specification also contemplates 3D stacks with “two or more FPGA die”: “[I]nter-cell connections currently limited to two dimensions of a single die may be routed up and down the stack in three dimensions.” *Id.* at 5:14–16.

Patent Owner also argues that Alexander is non-enabling (1) because of thermal issues with the designs Alexander describes and (2) “[b]ecause the public was not in possession of Tru-Sci Technologies’ wafer-thinning technology for more than one year prior to the claimed invention’s filing date.” PO Resp. 14, 16.

Initially, Alexander, a prior art reference, carries a presumption of enablement. *Antor Media*, 689 F.3d at 1287–1288; *Amgen*, 314 F.3d at 1355. Patent Owner argues that the presumption does not apply because “for a non-patent publication, such as Alexander, to be presumptively enabling, it must have been “cited by an examiner . . . barring any showing

to the contrary by a patent applicant or patentee.” PO Resp. 13 (quoting *Antor Media*, 689 F.3d at 1288. Patent Owner also argues that “[w]hile it is true that a ‘[e]nablement of an anticipatory reference may be demonstrated by a later reference,’ the Federal Circuit has made clear that the later reference ‘must show that the claimed subject matter was in possession of the public more than one year prior to the applicant’s filing date.’” *Id.* at 16 (quoting *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1379 (Fed. Cir. 2001)).⁸

Petitioner argues that Patent Owner “misrepresents the law.” As Petitioner argues, ‘[a] prior art printed publication does not need to have been ‘cited by an examiner’ to be presumed enabling.” Reply 5. In *Corephotonics*, 2021 WL 2577597, at *4 (nonprecedential), in the context of AIA trial proceedings, the court held that “regardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art” and that “[i]t was error for the Board to suggest otherwise.”

The 1995 publication date of Alexander antedates the ’035 patent’s effective filing date of December 5, 2001 by more than six years. *See* Ex. 1006, 1 (“0-7803-2702-1/95 \$ 4.00 © IEEE-1995”); PO Resp. 4 (specifying “December 5, 2001” as “the earliest effective filing date of the ’035 Patent”); Inst Dec. 20–25 (finding the publication date of Alexander is

⁸ The “more than one year prior to the applicant’s filing date” requirement arises from “anticipation under 35 U.S.C. § 102(b).” *See Bristol-Myers Squibb*, 246 F.3d at 1379.

December 5, 2001).⁹ As Petitioner shows, even if wafer thinning is relevant to the claimed invention somehow, Tru-Si Technologies described its wafer-thinning process in 1999, more than one year prior to the effective filing date of the '035 patent. Reply 8 (citing Ex. 2008, 1–2). As Petitioner also shows, Koyanagi published in 1998 and describes wafer thinning. Reply 8 (citing Ex. 1007, 19; Ex. 1030 ¶¶ 42–44); Pet. 39.

Moreover, as Petitioner also argues, claims 1, 5, and 7 do not recite wafer thinning. *See* Reply 8; Pet. 39. Claim 8 depends from claim 1 and recites “wherein said die elements are thinned to a point at which said contact points traverse said thickness of said die elements.” *See* Reply 8; Pet. 39. Claim 8 further indicates that claims 1, 5, and 7 do require wafer thinning.

In other words, contrary to Patent Owner’s arguments, Alexander need not enable “wafer-thinning technology,” because challenged claims 1, 5, and 7 at issue here do not require that technology. Even so, the '035 patent admits the “wafer-thinning technology” was known and “developed by Tru-Sci Technologies” prior to the invention. *See* Ex. 1001, 2:20–30; Prelim. Resp. 18–19 (citing Ex. 1001, 2:20–30; Ex. 2008); *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1379 (Fed. Cir. 2001) (“Enablement of an anticipatory reference may be demonstrated by a later reference”). Accordingly, an artisan of ordinary skill reading Alexander

⁹ Patent Owner does not challenge this preliminary finding in its Response. After a full review of the record, we incorporate and adopt this finding as supported by a preponderance of the evidence.

would have considered Alexander enabled for such known technology at the time of the invention.¹⁰

Patent Owner also contends that Alexander recognizes “[a] number of important issues remain to be addressed . . . including heat dissipation, thermal stress, and physical design considerations.” PO Resp. 14 (quoting Ex. 1006, 4). Patent Owner also contends that Alexander “declared that the industry must find ways of ‘reducing power consumption in 3D FPGA architectures’ in order to mitigate the thermal issues, which remained a major concern that hindered 3D design and development.” *Id.* (quoting Ex. 1006, 4). According to Patent Owner because of these thermal issues, “a skilled artisan could not make the claimed invention based on Alexander without undue experimentation.” *Id.*

Contrary to this characterization, Alexander states that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” Ex. 1006, 1. Patent Owner contends this is not “sufficient” because Alexander does not employ the same disclosed wafer-thinning process by Tru-Si-Technologies that the patent describes. PO Resp. 15 (citing Ex. 1001, 2:16–

¹⁰ In its sur-reply in IPR2020-01021 challenging claims in a related patent, Patent Owner states that “[t]he inventors of the ’951 Patent, however, readily admit that they did not invent TSVs [through-silicon vias] or stacking of die elements.” IPR2021-01021, Paper 24, 3 (citing U.S. Patent No. 7,282,951 (the “951 patent”), 2:29–40 as “discussing Tru-Si Technologies”). The named inventors of the ’951 patent and the ’035 patent are the same, John M. Huppenthal and D. James Guzy, and both patents rely on the same effective filing date of December 5, 2001 through the same patent, U.S. Patent No. 6,627,985. *Compare* IPR2021-01021, Ex. 1001, codes (63, 75) (the ’951 patent), *with* Ex. 1001, codes (64, 75) (the ’035 patent).

30). However, as noted above, the claims at issue here do not require that wafer-thinning process and even if they do, the process was well-known years before the effective date of the invention. *See also supra* note 10 (admitting that the named inventors did not invent stacking and TSVs (through-semiconductor vias) and citing Tru-Si Technologies). Other record references, such as Bertin and Koyanagi, discussed below, show enablement of vias extending through dies at the time of the invention. As Petitioner also argues, “Koyanagi, published before the Tru-Si paper in 1998, also undisputedly teaches the fabrication of 3D ICs that involves wafer thinning, as detailed in the Petition with regard to claim 8.” Reply 8 (citing Pet. 39; Ex. 1007, 19; Ex. 1030 ¶¶ 42–44).

According further to Petitioner, “Dr. Chakrabarty admits that technologies to fabricate stacked dies using TSVs were available and known before the claimed 2001 priority date of the ’035 patent.” Reply 9 (citing Ex. 1035, 310:15–311:14). Dr. Chakrabarty’s cited testimony supports Petitioner: “Koyanagi’s work was ’98, ’99. He’s generally credited as being the first to convincingly show 3D stacking with these vias. And then there was the Tru-Si work around the same time.” Ex. 1035, 311:10–14.

Although Alexander describes “important issues” that need to be addressed, Alexander also states that “[t]he manufacturing yield of such parts may be kept at reasonable levels using effective fabrication and testing methodology.” Ex. 1006, 4. As Petitioner points out, Alexander solves heat problems by eliminating input and output buffers where “large portion of the total power is expended” so that “3D stacking of FPGAs ‘tends to significantly reduce the power consumption.’” Reply 6 (quoting Ex. 1006, 4).

As Petitioner also shows, Alexander specifically describes “[a] number of thermal-reduction techniques” (Ex. 1006, 3) as including “‘thermal bumps in pillars’ as heat removing pipes, and the use of thermal gels.” Reply 6–7 (quoting Ex. 1006, 3; citing Ex. 1003 ¶¶ 37–39).

Patent Owner also argues that “Alexander proposed a 3D FPGA,” but “the authors admitted that it could not fabricate its proposed design.” PO Resp. 26. But as Petitioner argues, whether Alexander’s authors actually manufactured the disclosed die stack is not determinative, especially here where Alexander lists multiple well-known solutions to any thermal problems. *See* Reply 8 (citing *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (stating that “no ‘actual creation or reduction to practice’ is required” for a prior art reference to anticipate claims (quoting *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1380–81 (Fed. Cir. 2003))).

Based on the foregoing discussion, Petitioner persuasively shows that Alexander anticipates claim 1. Petitioner also presents a persuasive showing supported by the record with respect to dependent claims 5 and 7. Pet. 20–21. Patent Owner does not address dependent claims 5 and 7 separately from claim 1. *See* PO Resp. 10–16. Accordingly, based on the record, including arguments and cited evidence in Patent Owner’s Response and Sur-reply, Petitioner shows by a preponderance of evidence that Alexander anticipates claims 1, 5, and 7.

E. Obviousness, Alexander and Admitted Prior Art, Claims 9, 13, and 15

Claim 9 recites the following:

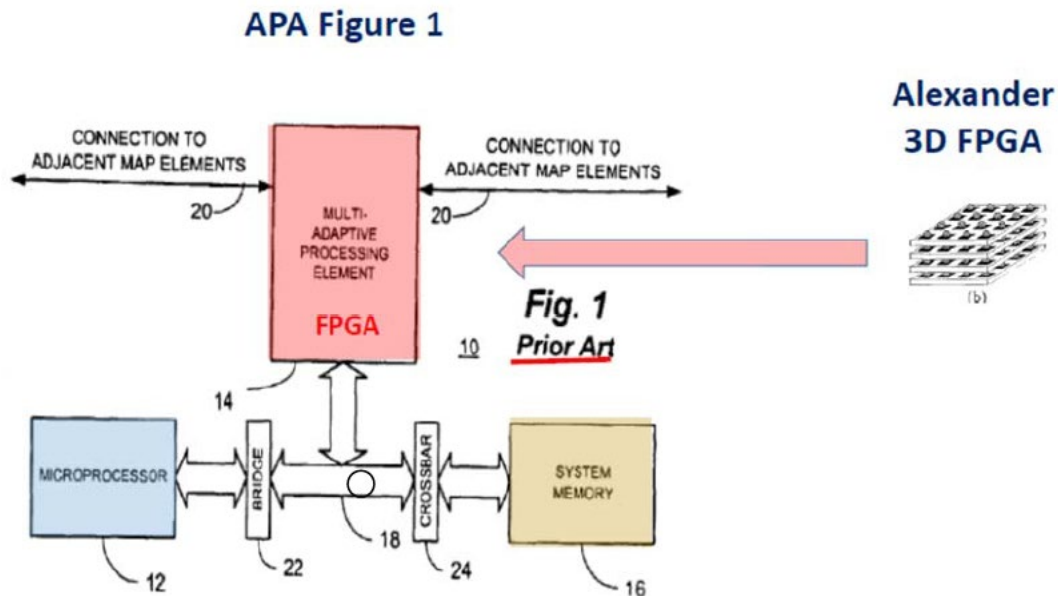
9. A reconfigurable computer system comprising:
a processor;
a memory;

at least one processor module including at least a first integrated circuit die element having a programmable array and at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element; and

wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

Petitioner reads the last two clauses of claim 9 onto Alexander's 3D processor module. *See* Pet. 21–22. Petitioner contends that with the exception of the specific structure of the claimed processor module as outlined in the last two clauses above (which represent the bulk of claim 9), the other claimed components of the “reconfigurable computer system” (i.e., memory, processor, and programmable array) generally were well known as the '035 patent admits. *See id.* at 10–11, 21–22 (citing Ex. 1001, 3:38–58, Fig. 1); Pet. Prelim. Reply 7.

Petitioner reproduces the following annotated version of admitted prior art Figure 1 of the '035 patent along with Alexander's FPGA at Figure 2b to illustrate the proposed ground (Pet. 21):



Petitioner's annotated "APA figure 1" above depicts a known reconfigurable computer system as admitted in '035 patent supplemented by Alexander's 3D FPGA in place of the known FPGA. *See* Pet. 21 (arguing that "the 'prior art reconfigurable computer system' depicted in APA Figure 1 incorporates 'one or more multi-adaptive processing (MAPTM) elements 14,' each of which 'may comprise an FPGA'" (quoting Ex. 1001, 3:39–58)). As Petitioner argues, the '035 patent admits that Figure 1 "is a simplified functional block diagram of a portion of a prior art reconfigurable computer system [that] incorporates [] one or more microprocessors 12 [blue], one or more multi-adaptive processing [] elements 14 [red] and an associated system memory 16 [tan]." Pet. 22–23 (quoting Ex. 1001, 3:38–43 and referring to annotated "APA Figure 1").

Relying on testimony by Dr. Shanfield and based on teachings in Alexander, Petitioner contends that “[a] POSITA therefore would have been motivated to use Alexander’s 3D FPGA in the APA’s reconfigurable computer system to save space and increase processing speed.” Pet. 22 (citing Ex. 1006, 1; Ex. 1002 ¶ 87). Petitioner explains that Alexander states that its “3D FPGA has a high number of very short vertical interconnections, which ‘alleviates the performance degradation inherent in conventional die packaging and printed-circuit board techniques.’” Pet. 22 (quoting Ex. 1006, 1). Petitioner also explains that “[i]ntegrating different components into a 3D stacked module achieves the well-known benefits of ‘miniaturization, lower power consumption, and large-scale integration.’” Pet. 27 (citing Ex. 1010, 1712–13; Ex. 1002 ¶ 104).

Patent Owner argues that “neither the APA nor *Alexander* disclose *how* to combine a programmable array, a microprocessor, and a memory die into a 3D IC.” PO Resp. 18. As Petitioner argues, however, the Petition does not combine these three claim elements into a 3D IC. Reply 10. Rather, claim 9 “requires (1) a processor, (2) a memory, and (3) a processor module having at least two stacked die elements, one of which includes a programmable array.” *Id.* In other words, “[t]he microprocessor (blue) and system memory (tan) of APA Figure 1 are conventional components and not stacked dies, and they are mapped respectively to the claimed processor and memory of claim 9.” *Id.* at 11 (citing Pet. 23; Ex. 1030 ¶¶ 45–47).

Petitioner’s showing is persuasive. The ’035 patent shows that prior art computer systems using FPGAs, microprocessors, and memory, using hybrid or discrete components, generally were known. *See* Ex. 1001, 3:12–15, 37–57. In addition to referring to Figure 1 as prior art (which employs

hybrid or discrete components), the '035 patent admits in a related context that “three *known* limiting factors [including data access to and from cache memory] in “hybrid system[s]” that use “discrete microprocessors and FPGAs will only become significant as microprocessor speeds continue to increase.” *See* Ex. 1001, 2:1–3 (emphasis added), Fig. 1. This admitted prior knowledge of limiting factors in the prior art APA system and the attempt to improve upon the APA system by improving upon microprocessor speeds implies that the system, including known microprocessors and FPGAs, generally was well known. *See* Ex. 1001, 1:16–18 (“In addition to *current commodity* IC microprocessors, another type of processing element is *commonly referred* to as a reconfigurable or adaptive, processor.”) (emphasis added).

In relying on the APA Figure 1, Petitioner quotes the '035 patent to show that “FPGA-based reconfigurable processor systems were well known in the art.” *See* Pet. 10 (“Conventionally, the ability for a reconfigurable processor to alter its hardware [] is typically accomplished through the use of some form of field programmable gate array (‘FPGA’)”) (quoting Ex. 1001, 1:28–33). Similarly, the '035 patent admits that the microprocessors “to execute an application” were well-known system components of a “conventional ‘load/store’ paradigm,” with the “reconfigurable processor” providing benefits over that paradigm. *See id.* at 1:18–27. In context, prior art Figure 1 simply represents a well-known “reconfigurable computer system 10” that includes an FPGA coupled to a

well-known processor and memory in a conventional manner. *See id.* at 3:38–57.¹¹

Relying on Figure 5 of the '035 patent, Patent Owner also argues that “Petitioner overlooks that the '035 Patent describes a wide configuration data port that through buffer cells allows the parallel updating of logic cells in the FPGA.” PO Resp. 23 (citing Ex. 1001, 4:42–62). Patent Owner also argues that the “'035 Patent greatly improved upon FPGA reconfiguration time, which conventionally took ‘millions of processor clock cycles to complete the reconfiguration.’” *Id.* (citing Ex. 1001, 1:42–56). Patent Owner argues that this “[t]his improvement was an important aspect of the '035 Patent’s claimed SDH (stacked die hybrid) processor, and, further confirms the challenges that the inventors of the '035 Patent faced when innovating in this space, and illustrates that Petitioner trivializes these challenges to make its obviousness argument.” *Id.* at 24 (citing Ex. 2015

¹¹As indicated in the Institution Decision, which we adopt and incorporate by reference as supported by the full record, Petitioner’s use of the admitted prior art comports with the “Treatment of Statements of the Applicant in the Challenged Patent in *Inter Partes* Reviews Under § 311” (“Memorandum”) (Ex. 2009), *available* at https://www.uspto.gov/sites/default/files/documents/signed_aapa_guidance_memo.pdf. *See* Inst. Dec. 31–33. Patent Owner’s Response does not contest Petitioner’s showing as not complying with the Memorandum. In short, Petitioner employs the admitted prior art as “[s]tatements made in the specification of the patent that is being challenged in an IPR . . . as evidence of . . . general knowledge,” in combination with Alexander as “one or more prior art patents or printed publications,” employing the admitted prior art “to . . . supply missing claim limitations that were generally known in the art prior to the invention” and “demonstrate the knowledge of the ordinarily-skilled artisan at the time of the invention.” *See* Memorandum at 9; Inst. Dec. 31–33.

¶ 61). Patent Owner also argues that “neither the APA nor Alexander disclose how to combine a programmable array, a microprocessor, and a memory die into a 3D IC, which would take undue experimentation.” *Id.* at 18. Patent Owner contends that Dr. Shanfield’s deposition testimony acknowledges that “combining different types of chips using TSVs into a 3D IC” “cannot be casually thrown together.” *Id.* at 19 (arguing Petitioner “slaps the APA and Alexander’s proposed 3D FPGA together without worrying about what connects to what”).

Contrary to these arguments, claim 9 does not recite or require a “stacked die hybrid,” “buffer cells,” any improvements in FPGA reconfiguration times, or a “3D IC.” Claim 9 recites a “reconfigurable computer system” in the preamble, but it does not even recite how the “memory” and “processor” functionally or structurally relate to the “first and second integrated circuit die elements” of the “processor module.”

As indicated above, Alexander carries a presumption of enablement as a prior art reference. *See Antor Media*, 689 F.3d at 1288; *Amgen*, 314 F.3d at 1355. Alexander employs multi-chip module fabrication techniques “to establish electrical contacts between the interconnect substrate and pads on individual dies.” Ex. 1006, 4. As to obviousness, Petitioner relies on known systems that include a microprocessor, FPGA, and memory. Pet. 22–23 (citing “APA Figure 1”). Petitioner persuasively shows that an artisan of ordinary skill readily could have connected the known FPGA module in a processor and memory system as a substitute for a prior art FPGA, with the system performing as predicted, as evidenced by the block diagram wiring connections in admitted prior art Figure 1 of the ’035 patent, in order to save

space and increase processing speed with a reasonable expectation of success. *See* Pet. 10–11, 21–25 (citing Ex. 1002 ¶¶ 85–93).

Patent Owner also alleges thermal issues in Alexander render the claimed combination “inoperable.” PO Resp. 25–28. Again, however, Patent Owner relies on a module or stack of a “3D FPGA with other power hungry components, such as logic dies including microprocessors” to support its arguments. *Id.* at 27. This argument mischaracterizes the breadth of claims 9, 13, and 15, which do not require a stack that includes a 3D FPGA stack with a microprocessor and memory in that stack, as Petitioner shows and as outlined above.

Based on the foregoing discussion, Petitioner shows persuasively that the combined teachings of Alexander and the APA would have rendered claim 9 obvious. Petitioner also persuasively shows that claims 13 and 15, which depend from claim 9, would have been obvious as adding features that “Alexander also discloses.” Pet. 25. Patent Owner does not address dependent claims 13 and 15 separately from independent claim 9. *See* PO Resp. 17–28. Accordingly, based on the record, including arguments and cited evidence in Patent Owner’s Response and Sur-reply, Petitioner shows by a preponderance of evidence that the combined teachings of Alexander and the APA would have rendered claims 9, 13, and 15 obvious.

F. Obviousness, Koyanagi and Alexander, Claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29

Petitioner contends the subject matter of claims 1, 3, 5–9, 13–17, 19–22, 25, 26, 28, and 29 would have been obvious over the combination of Koyanagi and Alexander. Pet. 17–46. Patent Owner disputes Petitioner’s contentions. PO Resp. 28–36.

1. *Koyanagi*

Koyanagi describes a “three-dimensional integration technology” (“3D”) that involves vertically stacking and interconnecting chips using “a high density of vertical interconnections” (Ex. 1007, 17) to “connect[] each layer (*id.* at 18).

Koyanagi explains that its 3D-integration technology “enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips.” Ex. 1007, 17–18 (“More than 10^5 interconnections per chip form in a vertical direction in these 3D . . . chips.”) Koyanagi’s system “dramatically increase[s] wiring connectivity while reducing the number of long interconnections.” *Id.* at 17.

Koyanagi’s Figure 1a follows:

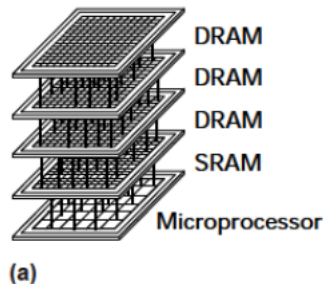


Figure 1a illustrates a stack of chips including dynamic random access memory (DRAM) chips and a synchronous random access memory (SRAM) chip “stacked on a microprocessor” chip. *See* Ex. 1007, 17. Koyanagi describes “form[ing] as many vertical interconnections as possible” to “remove the generated heat” and form “electrical wirings.” *Id.* According to one embodiment in Koyanagi, “2D image signals move simultaneously in a vertical direction and are processed in parallel.” *Id.* at 18. Koyanagi also describes a variety of uses: “Typical examples of these new system LSIs

include a merged logic memory (MLM) LSI chip as shown in Figure 1 . . . , and a 3D shared memory for parallel processor systems.” *Id.* at 17.

2. *Obviousness Analysis, Koyanagi and Alexander, Claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28 and 29*

Claim 1’s preamble recites “[a] processor module comprising.”

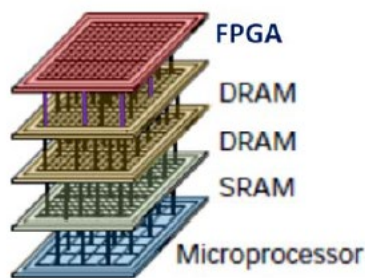
Petitioner relies on the combined teachings of Koyanagi and Alexander, with Koyanagi disclosing all elements of the processor module except for a “programmable array.” *See* Pet. 30–36. Petitioner provides reasons to combine Koyanagi and Alexander as discussed further below. *See id.* at 25–30.

Claim 1 recites limitation 1.1, “at least a first integrated circuit die element including a programmable array,” and limitation 1.2, “at least a second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element.”

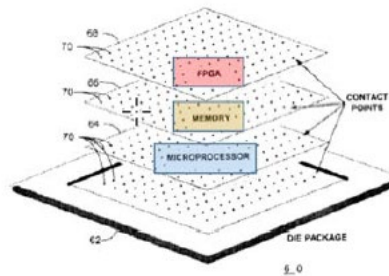
Petitioner contends that it would have been obvious to employ Alexander’s FPGA as an integrated circuit layer in Koyanagi’s stack of integrated circuit layers (dies). *See* Pet. 17–32. Petitioner provides reasons supported by the record to employ FPGAs in Koyanagi’s stack: “Alexander explains that FPGAs are particularly useful because of their flexibility and re-usability; they can be flexibly reconfigured to ‘implement arbitrary logic’ and thus ‘provide designers with a faster and more economical design cycle.’” *Id.* at 26 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 102).

Petitioner provides the following modified version of Koyanagi’s Figure 1 in a side-by-side comparison of the ’035 patent’s Figure 4:

Koyanagi Figure 1M



'951 Patent Figure 4



Koyanagi's Figure 1a on the left, labeled Figure 1M and annotated by Petitioner, shows a stack of dies with Alexander's FPGA die replacing one of Koyanagi's DRAMs. The '035 patent's Figure 4 on the right as annotated by Petitioner shows a similar configuration. *See* Pet. 31. In addition to the rationale noted above, Petitioner explains that “[a] POSITA would have been motivated to combine the teachings of Koyanagi with those of Alexander in order to create a 3D reconfigurable processor module with improved performance and area-efficiency.” *Id.* at 25 (citing Ex. 1002 ¶ 97).

To further support this rationale, Petitioner explains that “Koyanagi Figure 1(a) . . . illustrates a 3D stacked module that integrates a microprocessor die, an SRAM die and multiple DRAM dies.” Pet. 25–26 (citing Ex. 1007, 17–18). Petitioner explains that “Koyanagi Figure 2 . . . depicts another 3D module formed by stacking other types of dies not shown in the Figure 1(a) chip, including a processor array and output circuit die.” *Id.* at 26 (citing Ex. 1007, 17–18). Petitioner also shows that “Koyanagi discloses a universal 3D-integration scheme that is agnostic to the type and functionality of the stacked dies” (Pet. 26), quoting Koyanagi as follows: “We propose *various kinds* of new system on-silicon LSI chips (system LSIs) based on this new 3D-integration technology.” *Id.* (emphasis by Petitioner) (quoting Ex. 1007, 17; citing Ex. 1002 ¶ 101).

As indicated above, Petitioner contends that Alexander “explains that FPGAs are particularly useful because of their flexibility and re-usability; they can be flexibly reconfigured to ‘implement arbitrary logic’ and thus ‘provide designers with a faster and more economical design cycle.’” Pet. 26 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 102). Citing several examples from the prior art, the testimony of Dr. Shanfield, and admissions in the ’035 patent, Petitioner explains that “FPGAs are also commonly used with a microprocessor and memories to form a reconfigurable processor system.” *Id.* at 26–27 (citing Ex. 1002 ¶ 103; Ex. 1008, code (57) (“A reconfigurable processor chip has a mixture of reconfigurable arithmetic cells and logic cells for higher effective utilization than a standard FPGA. The reconfigurable process includes a standard microprocessor”); Ex. 1020, Fig. 1B; Pet. § VI.A).¹²

Based on the above and other evidence, Petitioner explains why a person of ordinary skill in the art would have been motivated to combine the teachings of Alexander and Koyanagi to form a die stack with an FPGA die, including increased data speed, lower power, miniaturization, and other benefits:

A POSITA would have been motivated to apply Koyanagi’s universal 3D integration teachings to vertically stack the components of an FPGA-based reconfigurable computer system. Integrating different components into a 3D stacked

¹² Section VI.A of the Petition quotes the ’035 patent as follows: “Conventionally, the ability for a reconfigurable processor to alter its hardware [] is typically accomplished through the use of some form of field programmable gate array (‘FPGA’)” Pet. 10 (quoting Ex. 1001, 1:28–33). The Petition also relies partly on prior art Figure 1 in the ’035 patent, which shows FPGA 14, microprocessor 12, and system memory 16, all connected together on a bus. *See id.*

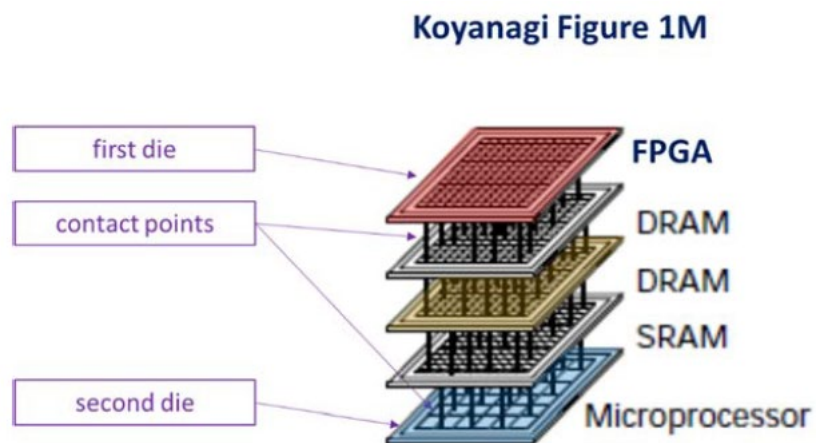
module achieves the well-known benefits of “miniaturization, lower power consumption, and large-scale integration.” Ex. 1010, 1712–13; Ex. 1002 ¶ 104. This is particularly important because FPGAs are relatively large devices. Ex. 1001, 1:41–46. In addition, Koyanagi’s 3D integration solves a well-known problem, which is that prior art FPGA-based systems experienced significant speed degradation due to the long circuit board wirings that interconnect the components of such a system. Ex. 1006, 1 (the flexibility provided by FPGAs “is achieved at the cost of substantial performance penalty, due primarily to interconnect delay”); Ex. 1002 ¶ 105. By contrast, Koyanagi’s 3D integration scheme makes use of “a huge number” (e.g., 100,000) of very short through-silicon contacts (“buried interconnections”) to interconnect the stacked dies. Ex. 1007, 17, 19; Ex. 1002 ¶ 106. This high density vertical interconnection scheme—which uses through-silicon contacts that are orders of magnitude more abundant and orders of magnitude shorter than circuit board wirings—“dramatically increase[s] wiring connectivity while reducing the number of long interconnections” and significantly improves system speed. [Ex. 1007,] 17.

Pet. 27–28.

Petitioner explains that both references “depict the use of through-silicon contacts . . . that traverse a die to connect to solder bumps” and “both illustrate vertical stacking of integrated circuit dies and depict solder bumps that are distributed throughout the surface of the dies.” *Id.* at 28–29 (annotating Ex. 1006, Figs. 2a, 2b; Ex. 1007, Figs. 1A, 5; quoting Ex. 1006, 1 (“One method to build a 3D FPGA entails stacking together a number of 2D FPGA bare dies [and] vertically interconnect adjacent FPGA layers. . . . Aside from solder bumps to establish the vertical interconnections, each individual die in our 3D paradigm has vias passing through the die itself”)); Ex. 1007, 17 (“By vertically stacking and gluing several LSI wafers together, we have created a new 3D-integration technology [in which] we

formed as many vertical interconnections as possible in our LSIs.”), 19 (describing “buried interconnections” that pass through the circuit dies to connect to microbumps on the surface of the dies)).

Claim 1 also recites limitation 1.3, “wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.” In addition to the showing outlined above, Petitioner’s annotated version of Koyanagi’s Figure 1 depicts the contact points relied upon by Petitioner:



Koyanagi’s Figure 1 above as annotated by Petitioner (“Figure 1M”) shows the number of contact points as set forth in limitation [1.3] “distributed throughout the surfaces of said die elements” and “travers[ing] said die elements through a thickness thereof.” Pet. 33–34. To further support this showing, Petitioner quotes Koyanagi: “More than 10^5 interconnections per chip form in a vertical direction in these 3D LSI chips [to] dramatically increase wiring connectivity” *Id.* at 33 (quoting Ex. 1017, 17).

Petitioner relies on similar teachings in Alexander, including Alexander’s teaching that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” Pet. 34–35 (quoting Ex. 1006, 1; citing Ex. 1002 ¶¶ 118–119); *see supra* Section III.D.1 (Alexander’s Figs. 2a, 2b showing vertical vias and solder bumps). Petitioner provides similar motivation to combine Alexander and Koyanagi as summarized above in connection with limitations 1.1 and 1.2. *See* Pet. 25–30 (§ 7C.1: “**Reasons to Combine Koyanagi and Alexander**”).

Patent Owner asserts that it would not have been obvious to combine Koyanagi and Alexander because of “significant technical challenges [such] that a POSITA would not have been motivated to attempt this combination.” PO Resp. 24. For example, Patent Owner contends that “a POSITA would understand that figuring out *how* to combine an FPGA, memory, and microprocessor into a 3D integrated circuit would require undue experimentation and could not be simply slapped together, as Petitioner’s expert recognized and admitted.” *Id.* at 29 (citing Ex. 2014, 81:21–82:19). To support this “slapped together” and “undue experimentation” argument, Patent Owner quotes Petitioner’s expert as stating that “*you don’t just slap it together without worrying about what connects to what.*” *Id.* (emphasis by Patent Owner) (quoting Ex. 2014, 81:21–82:19). To further support its argument that it would not have been “obvious to try stacking Alexander’s FPGAs on Koyanagi’s 3D multichip module,” Patent Owner asserts that “Petitioner’s alleged combination of Koyanagi’s 3D integration of memory chip layers with Alexander’s FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined

device inoperable.” *Id.* at 36 (citing Ex. 1035 ¶ 78). Patent Owner presents a number of arguments that track the arguments outlined above and relate to asserted technical challenges based on heat dissipation and an alleged failure by Petitioner to show “what connects to what” (*id.* at 19). *See* PO Resp. 18–36.

Dr. Shanfield’s deposition testimony relied upon by Patent Owner does not support Patent Owner’s argument about “undue experimentation” with respect to how to combine the teachings of Koyanagi and Alexander to arrive at the claimed processor module. In the passage containing the quoted testimony that Patent Owner relies upon, Dr. Shanfield testifies as follows:

You have obviously got to have a circuit in mind that you're wanting to create a system-level circuit, a module-level circuit; and so you're going to need to consider which connections you want a TSV connecting to something below.

So you don't just slap it together without worrying about what connects to what.

On the other hand, the putting together of the -- in Bertin, he describes the putting together of these chips and how that can be done in detail. And that piece of it is -- I guess you could characterize that as something that comes with the process and in itself isn't something you think specifically about every one of 50,000 connections. They're all done by the process that he gives an example of.

Ex. 2014, 82:4–19.¹³

Dr. Shanfield’s testimony indicates that artisans of ordinary skill readily would have been able to connect different die circuits together “obviously” with “a circuit in mind . . . to create a system-level circuit, [or] a module-level circuit . . . consider[ing] which [TSV] connections [she]

¹³ Bertin (Ex. 1009) is employed in the ground discussed below. *See infra* § II.G.

want[s].” *See id.* As Petitioner similarly argues, “[n]othing in Dr. Shanfield’s testimony, however, suggests that Petitioner ‘slap[ped] together’ Koyanagi and Alexander.” Reply 14; Ex. 1030 ¶ 79 (testifying that Patent Owner quotes his testimony “out of context” and that “at the system or circuit design level, each TSV is an interconnection between specific circuits”).

As Petitioner also persuasively argues, the Petition “provide[s] a detailed explanation of *how* Koyanagi and Alexander would have been combined to disclose each limitation of the Challenged Claims and *why* a POSITA would have been motivated to combine them—to create a 3D reconfigurable processor module with improved performance and area-efficiency.” Reply 15 (citing Pet. 25). Claim 1 recites “said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements.” Petitioner’s annotated Figure 1M and its other contentions show how to electrically couple circuits of the dies together using through-vias with as much detail as challenged claim 1 requires. *See, e.g., supra* Figure 1M. Petitioner also provides sufficient detail with respect to all of the challenged claims at issue in this section (i.e., claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28 and 29). *See* Pet. 25–55.

In addition, the ’035 patent provides the same level of detail with respect to stacking chips using conductive vias as Koyanagi, Alexander, and the combined teachings of the references as set forth by the Petition. *See* Pet. 31 (*comparing* “Koyanagi Figure 1M,” *with* “’035 Patent Figure 4”); Ex. 1001, Fig 4 (illustrating a die package comprising an FPGA die, memory die, and processor die, with generic “CONTACT POINTS” on each die).

The '035 patent does not portray or particularly describe connections between microprocessor die 64 and the other dies (memory die 66 and FPGA die 68) other than to show generic contacts in Figure 4. This lack of description suggests an artisan of ordinary skill readily knew how to connect FPGA and memory to a microprocessor.

Patent Owner contends that the “inventive SDH processor arranges die-area contacts, such as through-silicon vias (‘TSVs’), into a wide configuration data port that not only increases the number and decreases the length of available connections between the SDH [stacked-die hybrid] dies, but also reprograms the programmable array within a single clock cycle.” PO Resp. 1–2. But the wide configuration data port as described with respect to Figure 5 does not pertain to the microprocessor die or to any claim limitation.¹⁴ Also, even if somehow the challenged claims require a wide

¹⁴ Figure 5 of the '035 patent illustrates a wide configuration data port “functional block diagram” embodiment described as applicable to the more generic Figure 4 embodiment, which (without Figure 5) is “a representative embodiment of the present invention.” *See* Ex. 1001, 4:6–11, 5:29–34. Figure 5’s block diagram implements a “total reconfigur[ation] in one clock cycle by updating all of the configuration cells in parallel.” Ex. 1001, 3:29–32. But Figure 5 only generally indicates connections between memory die 66 buffer cells 88 and FPGA die 68 logic cells 84. Figure 5 does not show any connections to processor die 64. *See* Ex. 1001, Fig. 5, 4:42–61; Ex. 1035, 157:3–17, 158:10–12 (agreeing that “memory die 66” is “to the left of the very wide configuration data port 82 in Figure 5, although not shown” and the “connections” shown in Figure 5 “are formed by the TSVs that are between the memory die [not shown in Figure 5] and the FPGA die” “to the right of Figure 5”). Also, as Petitioner argues, the challenged claims do not require reconfiguration in one clock cycle. Reply 16. Rather, claim 1 requires a “programmable array” without specifying how to program the array. Claim 15 recites that the “programmable array [be] reconfigurable as a processing element,” but also does not require reconfiguration in one clock cycle. The '035 patent also describes “an added benefit” relevant to Figure

data port, that the “very wide configuration data port” 84 in Figure 5 is merely a box without any description in the ’035 patent specification further evidences that the inventors of the ’035 patent considered its structure and function to be well-known. *See* Ex. 1035, 163:14–17 (testifying that “[c]onfiguration data port” . . . is a well-known term” and agreeing that “that’s just a data port used for configuration, basically”).

As Petitioner explains, the “fundamental 3D interconnection technology—which is agnostic to the dies it connects . . . already existed, as amply disclosed in Koyanagi, and provides the motivation to combine with Alexander.” Reply 13. In other words, as the Petition shows, Alexander teaches that reconfiguration of FPGAs was well known, and the record shows that it also was well known and admitted in the prior art that FPGAs were employed with microprocessors and memory. *See* Pet. 26–27 (citing Ex. 1006, 1; Ex. 1002 ¶¶ 102–103; Ex. 1008; Ex. 1020, Fig. 1B); *see also* Pet. 22–23 (discussing “APA Figure 1”); Pet. 3–4 (discussing FPGA reconfiguration as well-known).

Petitioner shows that rerouting well-known electrical coupling between FPGAs, memory, and processors using the stacking techniques and through-vias of Koyanagi and Alexander would have been obvious. *See, e.g.*, Pet. 26 (“FPGAs are also commonly used with a microprocessor and memories to form a reconfigurable processor system.” (citing Ex. 1008, code (57); Ex. 1002 ¶ 103; Ex. 1020, Fig. 1B)), 31 (noting that “Figure 4 of the

4 “[i]n addition to . . . benefits” of reconfiguration in one clock cycle relevant to Figure 5: “Because the various die 64, 66 and 68 (FIG. 4) have very short electrical paths between them. The signal levels can be reduced while at the same time the interconnect clock speeds can be increased.” *Id.* at 4:64–66.

'035 Patent . . . is the only illustration of a stacked processor module in the '035 Patent” and relying on “Koyanagi Figure 1M” to illustrate vertical coupling as similar to Figure 4 of the '035 patent); Reply 18 (arguing that “the ['035] patent simply asserts that stacking dies reduces power consumption, which was a well-known fact in the art.” (citing Ex. 1001, 4:62–67; Ex. 1002 ¶ 41; Ex. 1010, 1712–13)); Pet. 4 (arguing “that stacking dies to form 3D modules were well-known prior to the alleged invention of the '035 patent” and citing known advantages of such modules, including “high packing density,” “high speed,” “parallel signal processing,” and “integration of many functions on a single chip”) (quoting Ex. 1010, 1704; citing Ex. 1002 ¶ 41).¹⁵

As Petitioner also argues, Patent Owner neither disputes that “Alexander teaches stacking FPGA dies” nor that “Koyanagi teaches stacking different types of bare dies using TSVs to form 3D multi-chip modules.” Reply 14 (citing Resp. 5–6; Ex. 1035, 55:17–20; 310:15–311:14; 314:2–5). At the cited deposition pages, Petitioner quotes Dr. Chakrabarty as admitting that “Koyanagi teaches ‘3D integration of different types of dies using TSV technology’ (*id.* (quoting Ex. 1035, 55:17–20)), and that “Koyanagi has been recognized [as one of] the earliest papers that demonstrated the reliability of 3D stacking through silicon vias” (*id.* (quoting Ex. 1035, 55:17–20)).

¹⁵ The cited pages of Akasaka (Ex. 1010) further supports Petitioner’s showing based on re-routing of known prior art circuitry by stating that “[t]he first step in 3-D system design . . . begin[s] with the integration of conventional functions already realized in 2-D devices,” which results in “miniaturization, low power consumption, and large-scale integration.” Ex. 1010, 1712–13.

Petitioner explains that Dr. Chakrabarty also “admits that a ‘logic chip’ as disclosed in Koyanagi (Ex. 1007, 17) may be an FPGA.” Reply 15 (citing Ex. 1035, 129:2–7 (admitting that logic includes an FPGA), 86:20–87:10 (“logic chip” includes an FPGA), 220:20–24 (same); Ex. 1030 ¶¶ 17–18). Petitioner further contends that “Koyanagi explains that the use of TSVs allows forming a very large number (in the order of 100,000) of short vertical interconnects, which ‘dramatically increase[s] wiring connectivity while reducing the number of long interconnections.’” *Id.* at 14–15 (quoting Ex. 1007, 17; citing Pet. 27–28; Ex. 1035, 254:18–21 (admitting that Koyanagi teaches “hundreds of thousands of TSVs”), 247:3–9 (same); Ex. 1030 ¶¶ 17–18)). As noted above, in addition to saving area, reducing power consumption, and generally improving performance by stacking dies with TSVs (*id.* at 30), Petitioner explains that the “high density vertical interconnection scheme—which uses through-silicon contacts that are orders of magnitude more abundant *and* orders of magnitude shorter than circuit board wirings—‘dramatically increase[s] wiring connectivity while reducing the number of long interconnections’ and significantly improves system speed.” Pet. 27–28 (quoting Ex. 1007, 17).

In other words, as Petitioner persuasively shows, the prior art of record, including Koyanagi, provides reasons for stacking different types of integrated circuit dies together, including logic chips, with conductive vias to electrically couple the integrated circuits on the different layers of the dies. The record shows that logic chips include FPGAs, thereby suggesting that Koyanagi in combination with Alexander how to form the processor module of claim 1 with a reasonable expectation of success and without undue experimentation.

Patent Owner argues that “Petitioner’s facile attempt to assert that *Koyanagi* discloses a ‘logic chip’ that ***could*** be a programmable array (*see* Reply at 14–15) fails as a disclosure of a genus is not a disclosure of a species.” Sur-reply 3. This argument mischaracterizes Petitioner’s showing as one of anticipation and does not address Petitioner’s obvious showing based on the combined teachings of *Koyanagi* and *Alexander*. Pet. 25–36.

Patent Owner also asserts that “***buffer*** cells in the memory of the wide configuration data port ‘enables the FPGA . . . to be totally reconfigured in one clock cycle.’” PO Resp. 24. Therefore, according to Patent Owner, “Petitioner has not demonstrated that any of these details were known in the art or would have been obvious to a POSITA at the time of the invention.” *Id.* However, as Petitioner persuasively argues and as noted above, “an improved/shortened reconfiguration time is not claimed in any challenged claim of the ’035 patent.” Reply 16; *see also supra* note 14 (discussing buffer cells of Figure 5).

In Patent Owner’s Sur-reply, Patent Owner argues that *Koyanagi* relies on CAD tools, and that Dr. Shanfield relies on this disclosure for “***providing*** evidence of a reasonable expectation of success,” but “Dr. Shanfield cannot and does not establish that the use of CAD tools when attempting to combine *Koyanagi* and *Alexander* would result in the claimed invention.” Sur-reply 4 (citing Ex. 2017, 20:3–6, 23:22–25:7; Ex. 1007, 17). Based on these assertions, Patent Owner contends that “Dr. Shanfield does not demonstrate that any CAD tools would have resulted in ‘a memory array functional to accelerate external memory references to the processing element’ as opposed to any other possible interconnection scheme.” *Id.* at 4.

Contrary to these Sur-reply arguments, none of the challenged claims recite “a memory array functional to accelerate external memory references to the processing element.” And in any case, Dr. Shanfield’s testimony, Koyanagi, and Alexander all show that artisans of ordinary skill would have been able to use routine tools available at the time of the invention, such as CAD tools, and motivated to use them as an aid to establish the desired connections between circuits. *See* Ex. 1007, 17 (“A powerful CAD tool proves indispensable for 3D LSI design, specifically for 3D wiring routing because combining 2D multilevel metallization with vertical interconnections forms this complicated 3D wiring.”); Ex. 2017, 20:3–6 (agreeing that it is “a fair understanding that an engineer, when designing 3D architecture, would use some sort of CAD tool in designing the circuitry”), 24:6–21 (testifying that “CAD tools are always used for routing in the design and manufacture of integrated circuits,” and “the engineering connected with CAD has been resolved in [Alexander’s] description for his particular approach, and he’s just simply explaining to the person skilled in the art reading this that this is how he did it, and this is what worked well for him” (discussing “Section 6 of Alexander”)). In Section 6, Alexander describes the CAD-based “framework” as “enable[ing] the use of a wide variety of graph-search algorithms to construct routing solutions, and works quite well in practice.” Ex. 1006, 4 (citing several documents for “3D FPGA routing”). In other words, the record shows that an artisan of ordinary skill would have readily been able and motivated to use routine tools to route connections vertically in stacked chips. Moreover, the ’035 patent does not mention using CAD tools, indicating either that such tools

were not needed for the invention or that they were so well-known that mentioning them was not important for purposes of describing the invention.

Patent Owner also argues that “[b]ecause of the power consumption by FPGAs, and other logic dies, and the resulting thermal issues, a POSITA would not have found it obvious to stack logic a programmable array [sic], such as an FPGA, with other die, let alone . . . microprocessor chips on top of one another.” PO Resp. 34 (citing Ex. 2015 ¶ 76). As Petitioner argues, however, Patent Owner presents “no evidence that an FPGA consumes any more power than other logic chips, such as microprocessors, to support PO’s allegation that there are unique power consumption and thermal issues that ‘plagued’ FPGAs.” Reply 16 (citing Ex. 1035, 116:11–117:5). As noted above, Dr. Chakrabarty admits that Koyanagi discloses a logic chip and an FPGA is a logic chip. Reply 15 (citing Ex. 1007, 17; Ex. 1035, 129:2–7, 86:20–87:10, 220:20–24; Ex. 1030 ¶¶ 17–18). Patent Owner appears to agree that FPGAs and other logic chips consume the same (or similar) amount(s) of power. *See* PO Resp. 34 (“Because of the power consumption by FPGAs, *and other logic dies*, and the resulting thermal issues” (emphasis added)); Reply 16 (citing Ex. 1035, 116:11–117:5 (Dr. Chakrabarty testifying that he did not analyze or cite articles comparing power consumption of microprocessors, programmable arrays, and FPGAs)).

The thrust of Patent Owner’s arguments about thermal issues rests on the undisputed principle that increasing power consumption increases heat generation. *See* PO Resp. 34; Reply 16–17. For example, Patent Owner explains that “serious thermal issues” arise because “the power consumption by logic dies, such as FPGAs and microprocessors, increase the operating

temperatures.” PO Resp. 36. However, as Petitioner argues and as Dr. Chakrabarty confirms, using many short vertical conductive vias versus long conductive runs “reduces power consumption and improves heat removal.” See Reply 17. For example, as Petitioner points out, Dr. Chakrabarty acknowledges that

[w]hat Koyanagi says *is actually obvious* to anybody who is skilled in the art. *Anybody who is skilled in the art would know that via is conductive. It is a conductor for both electricity and for heat. And therefore, if you have lots of vias, you’re going to take out the heat.*

Ex. 1035, 256:9–15 (emphasis added); see Reply 17 (quoting Ex. 1035, 256:6–15). Therefore, as Petitioner persuasively argues, “[r]ather than thermal issues deterring a POSITA from combining Koyanagi and Alexander, Koyanagi’s solution to heat dissipation provides further motivation to combine them with an expectation that the combination would be successful.” Reply 17–18 (citing Ex. 1030 ¶ 53).

Furthermore, as Petitioner also argues, not only do Koyanagi and Alexander individually or collectively solve heat problems in stacked dies with a “high density vertical interconnection scheme” using high numbers of conductive vias with “orders of magnitude shorter than circuit board wirings,” the combined system “significantly improves system speed” by decreasing the interconnect delay. See Pet. 27–28 (citing Ex. 1002 ¶¶ 105–106; Ex. 1007, 17, 19; Ex. 1006, 1). This resulting speed increase provides further motivation for the combination as proposed by Petitioner.

Patent Owner also argues that “FPGAs, and other logic dies, perform computational operations that result in extensive switching activities that consume a significant amount of dynamic power.” PO Resp. 34 (citing Ex. 2015 ¶ 75). To support this argument, Patent Owner states that “*Alexander*[]

notes that a large portion of the power consumption is due to driving I/O buffers.” PO Resp. 34 (citing Ex. 1006, 4). Patent Owner adds that the “FPGA use of I/O pins impact[s] the total power requirements since ‘considerations like I/O standards used and data rates expected determine how fast the I/Os toggle and how fast the logic must be clocked.’” *Id.* (quoting Ex. 2012, 1; citing Ex. 2015 ¶ 75).

This line of argument fails because as noted above, Koyanagi discloses stacking “other logic dies” (e.g., a microprocessor) with memory, as Dr. Chakrabarty concedes. *See* Reply 15 (citing Ex. 1007, 17; Ex. 1035, 129:2–7, 86:20–87:10 220:20–24; Ex. 1030, ¶¶ 17–18). Also, as Petitioner persuasively argues, “Alexander teaches stacking FPGA dies” (i.e., stacking several logic dies). *Id.* at 14. No dispute exists over the fact that using a sufficient number of TSVs solves any heat problems in stacked dies that include one or more logic dies. *See* Reply 17 (arguing that Koyanagi “solv[es] any heat problem by forming ‘as many vertical interconnections as possible’ because they ‘remove the generated heat’” and that “Dr. Chakrabarty admitted this”) (quoting Ex. 1007, 17; citing Ex. 1035, 290:4–7, 256:6–15, 291:16–292:13)). In addition to Koyanagi’s solution, Petitioner persuasively notes that “Alexander points out that 3D integration ‘using MCM technology’ advantageously eliminates input and output buffers where ‘a large portion of the total power is expended,’ and thus 3D stacking of FPGAs ‘tends to significantly reduce power consumption.’” Reply 18 (quoting Ex. 1006, 4).¹⁶ In other words, contrary to Patent Owner’s arguments, part of Alexander’s chip stacking solution involves using heat

¹⁶ An “MCM” is a “multi-chip module.” Ex. 1004, 1.

conducting vias with the option of eliminating I/O buffers and any heat generating switching associated therewith. *See* Ex. 1006, 4 (“[W]hen chips are interconnected using MCM technology, such I/O buffers are often unnecessary, which tends to significantly reduce the power consumption.”). Also, the challenged claims here do not require I/O buffers (or clocking, driving, or switching thereof).

Based on the foregoing discussion, Petitioner persuasively shows that the combination of Koyanagi and Alexander would have rendered claim 1 obvious. Relying partly on its showing with respect to claim 1, Petitioner provides a similar and persuasive showing for independent claims 9, 17, and 25, which largely track the limitations recited in claim 1. *See* Pet. 31–35, 40–44, 47–49, 50–55.

For example, independent claim 25 also recites the limitation “whereby said processor and said programmable array are operational to share data therebetween.” Similar to its showing with respect to independent claim 1, the Petition relies on “Koyanagi Figure 1M” that shows Alexander’s FPGA die in Koyanagi’s die stack electrically coupled with DRAM memory and a microprocessor. Pet. 53. The Petition persuasively relies on its motivation with respect to claim 1 and also provides evidence that “FPGAs are commonly configured as hardware accelerators to offload computationally-intensive operations from microprocessors; thus they share data with the microprocessors, for example through shared memory.” *Id.* (citing Ex. 1002 ¶ 152; Ex. 1008, 4:32–60 (describing various ways a processor and FPGA of a reconfigurable chip share data, including via registers that are “read or written by either the processor or the FPGA logic”); Ex. 1017, 5:59–67. Patent Owner does not

address claim 25 individually. Based on the record, Petitioner persuasively shows that the combination of Koyanagi and Alexander would have rendered claim 25 obvious.

Claims 8 depends from claim 1 and recites “wherein said die elements are thinned to a point at which said contact points traverse said thickness of said die elements.” Dependent claims 16 and 22, which depend from claims 9 and 17 respectively, recite materially the same limitation. Pet. 47, 50 (relying on the showing for claim 8). Petitioner refers to its showing with respect to claim 1 and further relies on Koyanagi’s teaching that the “[f]ormation of buried interconnections, metal microbumps, *wafer thinning*, . . . are key technologies for achieving 3D LSI.” Pet. 39 (emphasis by Petitioner) (quoting Ex. 1007, 19). Petitioner also relies on Koyanagi’s teaching that “each die is thinned ‘from [its original] thickness of 270 μm to [a thickness of] 70 μm ,’ after which ‘silicon trench[es] (at a depth of 70 μm -deep)’ are created in the thinned die and then ‘filled with low resistive polysilicon or CVD tungsten to form the buried interconnection[s] [red].” *Id.* (quoting Ex. 1007, 19–20). Patent Owner does not address claims 8, 16, and 22 individually. Based on the record, Petitioner persuasively shows that the combination of Koyanagi and Alexander would have rendered claims 8, 16, and 22 obvious.

Dependent claims 3, 5–7, 11, 13–15, 19–21, 26, 28 and 29 recite limitations including “a microprocessor,” “at least a third integrated circuit die element stacked with and electrically coupled to at least one of said first or second integrated circuit die elements,” “a memory,” “wherein said programmable array is reconfigurable as a processing element,” “said die elements are thinned,” “whereby said processor and said programmable

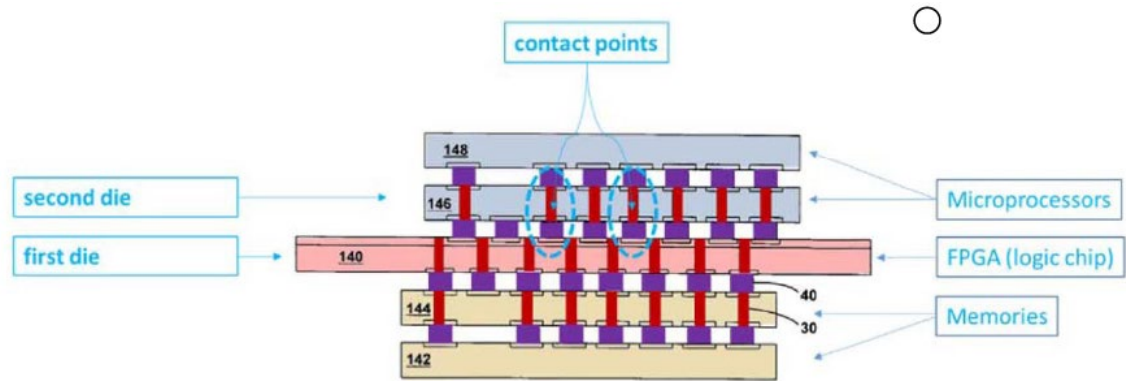
array are operational to share data,” “wherein said memory is operational to at least temporarily store . . . data,” and a “memory array.” The Petition shows that Koyanagi discloses these limitations or the recitations of these well-known circuit elements amount to combining “familiar elements according to known methods . . . [to] yield predictable results.” *See KSR*, 550 U.S. at 416; Pet. 36–40, 44–47, 49–50, 54. Patent Owner does not address these dependent claims separately from claim 1. *See* PO Resp. 28–36.

Accordingly, based on the record and as summarized above, including arguments and cited evidence in Patent Owner’s Response and Sur-reply, Petitioner establishes by a preponderance of evidence that claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 would have been obvious.

G. Obviousness, Bertin and Cooke, Claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29

Petitioner contends that claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 would have been obvious over the combination of Bertin and Cooke. *See* Pet. 55–79. Similar to Koyanagi, Bertin teaches stacking different types of chips, including logic chips, microprocessors, and controllers to minimize latency and maximize bandwidth and heat dissipation, using through-chip conductors. *See* Pet. 15–16 (summarizing Bertin), 55–62 (citing Ex. 1009, 1:20–27, 2:61–65, 4:57–60, 6:49–51, 7:16–34, Figs. 18, 22; Ex. 1002 ¶¶ 166–172).

Petitioner’s “Annotated Figure 22A,” which represents how Petitioner combines relevant teachings of Bertin and Cooke (Pet. 61), follows:



Bertin in view of Cooke
Figure 22A

Annotated Figure 22A above represents how Petitioner employs Cooke's FPGA in place of logic chip 140 in Bertin's stack of chips, which includes Bertin's first (140) and second (146) chips, memory chips (144, 142), microprocessor chips (146, 148), logic chip (140), and contact portions (red) extending through the various chips, including the claimed first and second integrated circuit dies (chips). *See* Pet. 61; Ex. 1009, 7:16–34, Fig. 22.

In other words, Bertin does not disclose an FPGA but discloses “logic chip” or “microprocessor” 140 in the middle or bottom of a “stack of chips” connected together with “high speed chip-to-chip connections through the silicon,” as portrayed in Figures 21 and 22. Ex. 1009, 7:16–42 (“FIGS. 21 and 22 illustrate the ability to stack similar chips while providing high speed chip-to-chip connections through the silicon.”). Petitioner relies on Bertin's teaching of generally “stack[ing] similar chips” (*id.*) and Cooke's description of FPGAs, microprocessors, and memory planes in a similar stack of circuits. *See* Pet. 48 (citing Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1002 ¶¶ 162–163). Petitioner contends that it would have been obvious to use Cooke's FPGAs in Bertin's 3D stacks to improve

performance, area-efficiency, packing densities, and speed by avoiding interconnect delays. *See* Pet. 56–58 (citing Ex. 1001, 1:36–2:9; Ex. 1006, 1; Ex. 1009, 2:61–65; Ex. 1002 ¶¶ 160–163). Petitioner also reads the limitations of challenged claims 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 on the combined teachings of Bertin and Cooke, providing a detailed showing, supported by the references and expert testimony. *See id.* at 62–79.

Patent Owner challenges Petitioner’s showing. PO Resp. 37–44. Patent Owner advances similar arguments to those addressed above with respect to the combined teachings of Koyanagi and Alexander. For example, Patent Owner argues that “[a] POSITA would understand that figuring out *how* to combine an FPGA, memory, and microprocessor into a 3D integrated circuit would require undue experimentation.” PO Resp. 38. To support this “undue experimentation”/“how to combine” argument (*see id.*), Patent Owner relies on the same testimony by Dr. Shanfield addressed above (§ II.F.2) that “you don’t just slap [chips] together without worrying about what connects to what.” PO Resp. 39 (quoting Ex. 2014, 81:21–82:19). Contrary to this argument, however, Dr. Shanfield’s testimony does not support Patent Owner for reasons similar to those explained above—i.e., Petitioner and Dr. Shanfield do not propose simply “slap[ping] together” the combined teachings of Bertin and Cooke without considering how to electrically couple the FPGA and “integrated circuit” as claimed and disclosed in the prior art. *See* Pet. 55–62; Ex. 1030 ¶¶ 72–73; Ex. 1002 ¶¶ 158–165. In other words, Petitioner provides a detailed mapping showing how to combine the references with factual underpinnings and rationale supported by the record, as summarized above. *See* Pet. 55–62; Ex. 1030

¶¶ 72–73; Ex. 1002 ¶¶ 158–165.

The record shows that experimentation would not have been undue in Petitioner’s reading of the broad challenged claims onto the specific teachings of the combined references. Patent Owner argues that “Petitioner simply suggests—without any sufficient explanation as to how the references would be combined—that Bertin’s through chip connectors would somehow be combined with Cooke’s FPGA to achieve the claimed invention.” PO Resp. 39–40. Contrary to this argument, as similarly explained above in connection with Koyanagi and Alexander, claim 1 does not require, and the ’035 patent does not describe, any more level of granularity regarding the “through chip connectors” in “the claimed invention” than Petitioner provides as summarized above, including by virtue of “Annotated Figure 22A.” Also, as the thrust of Dr. Shanfield’s testimony and the record shows, an artisan of ordinary skill readily would have been able to couple FPGA, memory, and microprocessor circuits together using vias. *See* Ex. 2014, 81:21–82:19 (testifying that “[y]ou have obviously got to have a circuit in mind that you’re wanting to create a system-level circuit, a module-level circuit; and so you’re going to need to consider which connections you want a TSV connecting to something below”); Ex. 1030 ¶ 79 (testifying that “at the system or circuit design level, each TSV is an interconnection between specific circuits”).

Similar to block diagram forms for connecting circuits together as shown in Cooke, Bertin, and the ’035 patent’s Figure 4, the long prior art connections similarly represented in block diagram form in prior art Figure 1 of the ’035 patent all imply that an artisan of ordinary skill in the art readily would have been able to couple the claimed circuits together based on

teachings in Bertin and Cooke without undue experimentation in the relatively predictable integrated circuits arts according to the breadth of the claims. *See* Pet. 55–62 (relying on the combined teachings of Bertin and Cooke); Ex. 1001, Fig. 1, Fig. 4; Pet. 10–11 (discussing admitted prior art Figure 1 of the '035 patent as showing a “simplified functional block diagram of a portion of a *prior art* reconfigurable computer system 10” (quoting Ex. 1001, 3:38–51)); Ex. 1008, code (57) (describing coupling between reconfigurable FPGA, microprocessor, and memory), Fig. 2 (showing “MEMORY PLANES” stacked over an “FPGA PLANE,” Fig 8A (showing a “CONFIGURATION VERTICAL STACK”); Ex. 1009, Fig. 21 (showing chip stack similar to Figure 4 of the '035 patent), Fig. 22 (similar). Similar to the admitted prior art known FPGA, microprocessor and memory circuits, Petitioner persuasively relies on Cooke’s teachings of connecting FPGAs to microprocessors and memory. *See* Pet. 56–57 (citing Ex. 1002 ¶ 162; Ex. 1008, 2:3–11, 3:3–13, 2:40–55, Figs. 1, 2, 8A).

Patent Owner also argues that “while Cooke suggests connecting vertically stacked memory to a 2D chip comprising a microprocessor and FPGA, Cooke does not disclose either stacking the vertical memory stack above the FPGA or using die-area interconnects in such an arrangement.” PO Resp. 41 (citing Ex. 2014, 74:17–75:6 (contending that Dr. Shanfield “admit[s] that FIG. 2 [of Cooke] is merely a schematic relationship that does not show how the elements are physically configured”)). Patent Owner also argues that the claims require “cache memory.” *Id.* at 40.

This line of argument does not relate to a claim limitation in a clear fashion. None of the challenged claims require a “cache memory” or “stacking the vertical memory stack *above* the FPGA or using die-area

interconnects *in such an arrangement*.” See PO Resp. 41 (emphasis added). Moreover, this argument supports Petitioner by showing further that connecting an FPGA to a microprocessor in a memory stack was well-known. In other words, Patent Owner admits that “Cooke suggests connecting vertically stacked memory to a 2D chip comprising a microprocessor and FPGA.” PO Resp. 41 (emphasis omitted). To the extent Patent Owner’s argument points to Cooke’s microprocessor and FPGA as existing on the same plane, this argument attacks Cooke individually rather than addressing the asserted combination. Also, the challenged claims do not preclude stacking Cooke’s FPGA and microprocessor plane as a die within Bertin’s microprocessor and memory stack, and it does not preclude connecting multiple processors together. See Pet. 57–58 (addressing claim 1, employing “Annotated Figure 22A”).

Patent Owner’s Sur-reply tracks similar arguments in its Response. For example, Patent Owner argues that “*Cooke*’s memory planes are located on a single chip along with the processor and reconfigurable FPGA, not on a stacked memory die.” Sur-reply 8. Patent Owner also argues that in Cooke, “many different types of interfaces are used to interface between the embedded processor and the reconfigurable portions of the single chip.” *Id.* (citing Ex. 1006, 1:67–2:11). Patent Owner contends this “background” shows that Petitioner “does not adequately explain how or why the references would have been combined to arrive at the claimed invention.” See *id.* at 9. But this background further shows that artisans of ordinary skill readily knew how to electrically couple the well-known FPGA, microprocessor, and memory circuits together. Also, the challenged claims do not preclude other forms of connections in addition to vias.

Petitioner also notes that “in the parallel [D]istrict [C]ourt litigation, Dr. Chakrabarty opined that all the components of Cooke’s reconfigurable system are stacked dies.” Reply 23 (citing Ex. 1034, 139:4–141:3; *see also* Ex. 1035, 190:10–17, 191:10–17; Ex. 1030 ¶ 75). The record supports Petitioner. For example, Petitioner quotes Dr. Chakrabarty at paragraph 89 of his District Court expert report, which states as follows: “Cooke is directed to a re-configurable processor chip having interconnections around the periphery of the stack die elements.” Ex. 1034, 139:17–19. Dr. Chakrabarty also describes Cooke’s Figure 2 and states “here is the FPGA plane and memory planes and we are trying to configure the FPGA from the memory planes and *we need a vertical connectivity.*” *Id.* at 140:16–19 (emphasis added). A vertical connectivity suggests a stack of circuits. *See* Ex. 1030 ¶ 75 (noting that Dr. Chakrabarty testified that “it seems to be the case” that his “view [] in the Eastern District of Texas case [is] that Cooke teaches a stacked die reconfigurable system but that the interface for configuring is on the periphery of the dies”) (quoting Ex. 1035, 191:10–17; citing Ex. 1035, 190:12–21; Ex. 1034, 139:4–141:3). Therefore, even if Cooke discloses a single die with memory, an FPGA, and a microprocessor using “different types of interfaces with the embedded processor,” Cooke at least discloses stacks of circuits connected together, including memory planes, a microprocessor and an FGPA plane, thereby suggesting the coupling of an FPGA in Bertin’s stack. *See* Ex. 1008, 2:16–18, 6:47–48, Fig. 2 (showing “MEMORY PLANES” stacked over an “FPGA PLANE,” Fig 8A (showing a “CONFIGURATION VERTICAL STACK”).

As further motivation, Petitioner explains that “Bertin’s 3D integration solved well-known problems of prior art FPGA-based computer

systems, such as significant speed degradation due to long circuit-board wirings, and long reconfiguration times due to memory bus bandwidth constraint.” *See* Reply 23 (citing Pet., 16, 55–56). Also, “Bertin’s 3D integration scheme made use of a large number of very short TSVs to interconnect stacked dies, significantly improving system speed and reconfiguration time.” *Id.* at 23. In other words, connecting the FPGA using the TSVs instead of Cooke’s peripheral connections would have been obvious in view of Bertin to improve speed and increase bandwidth as Petitioner shows. Dr. Chakrabarty’s testimony supports Petitioner’s showing. *See, e.g.*, Ex. 1034, 140:16–19 (describing Cooke’s Figure 2 and stating “here is the FPGA plane and memory planes and we are trying to configure the FPGA from the memory planes and *we need a vertical connectivity*” (emphasis added)). In another instance, Dr. Chakrabarty testifies that an artisan of ordinary skill would not have been motivated to use Cooke’s circuitry “in just one corner” and further shows that acceleration occurs by use of many vias:

The problem is not only about -- not only that your vertical -- you cannot have many vertical vias in just one corner.

The problem also is the impact on timing because *you will get almost no acceleration because your signal would have to be routed first on the horizontal layer and then it will have to be sent along the vertical layer, the periphery, to the next layer, and then it has to be routed once again on the other tier horizontally.*

So there is really no motivation. So anybody who understands this technology or is trying to get the advantage of this will not be motivated to implement it like this.

Ex. 1035, 195:9–22 (emphasis added). This testimony further supports Petitioner’s showing of the obviousness of coupling Cooke’s FPGA circuitry in Bertin’s stack using vias throughout the dies to electrically couple the

FPGA, memory, and microprocessor circuits on different dies to facilitate greater speed between those circuits.

Patent Owner also argues that “a POSITA would not have found the ’035 Patent’s claimed invention—stacking a *thinned* microprocessor die element, a memory die element, and a FPGA . . . obvious to try with a reasonable expectation of success because of the known thermal issues, which a POSITA would *not* have ignored.” PO Resp. 43–44 (first emphasis added). Contrary to this argument, none of the challenged claims, except claim 8, require “a thinned microprocessor die element,” as addressed further below.

Moreover, Patent Owner correctly points out that a person of ordinary skill “would *not* have ignored” “known thermal issues.” *Id.* This argument supports Petitioner’s showing, because it implies that an artisan of ordinary skill would have addressed known thermal issues and “would have expected the combination of Bertin and Cooke to be successful.” Reply 25 (citing Ex. 1002 ¶16). The record shows that such an artisan would have had a reasonable expectation of success based on known teachings as solving heat problems as admitted by Dr. Chakrabarty. *See id.* at 25–26 (citing Ex. 1035, 247:10–15 (agreeing that “Bertin pays a lot of attention to the thermal issues” and Bertin uses TSVs “as heat pipes”)); Ex. 1035, 247:1–248:17 (similar testimony).

As indicated above, claim 8 recites “[t]he processor module of claim 1 wherein said die elements are thinned to a point at which said contact points traverse said thickness of said die elements.” Petitioner contends that “[a] POSITA would have understood that the process of forming through-chip conductors [in Bertin] requires the die elements to be sufficiently thin.” Pet.

66 (citing Ex. 1002 ¶ 180; Ex. 1007). The “are thinned” language in the processor module of claim 8 is a product-by-process step and does not require a disclosure of a process step of thinning, provided the die structure of Bertin is thin enough such that “said contact points traverse said thickness of said die elements.” The record shows that Bertin’s contacts “traverse said thickness of said die elements.” *See* Pet. 65–66 (reproducing Figures 21 And 22 of Bertin); citing Ex. 1002 ¶¶ 179–180); Ex. 1006, Fig. 21, Fig. 22; PO Resp. 43–44.

Dependent claims 16 and 22 recite materially the same limitation and depend from claims 9 and 71, respectively. *See* Pet. 70–71, 74 (relying on the showing for claim 8). Accordingly, Petitioner shows persuasively that claims 8, 16, and 22 would have been obvious over the combined teachings of Bertin and Cooke.

Further regarding the known thermal issues, Patent Owner relies on its arguments with respect to Koyanagi and Alexander, and contends that “a POSITA would understand that Petitioner’s alleged combination of Bertin with Cooke’s FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined device inoperable.” PO Resp. 44. According to Patent Owner, “the power consumption by logic dies, such as FPGAs and microprocessors, increase the operating temperatures.” *Id.*

This line of argument ignores that Patent Owner agrees that Bertin teaches a “broad invocation of logic chips” (PO Resp. 42), and also agrees that “*Cooke* suggests connecting vertically stacked *memory* to a 2D chip comprising a microprocessor and FPGA” (*id.* at 41). For the reasons discussed above, these patents carry a presumption of enablement. *See*

Antor Media, 689 F.3d at 1287–1288; *Amgen*, 314 F.3d at 1355. Regarding operability, Petitioner cites Dr. Chakrabarty’s admission that “Bertin pays a lot of attention to the thermal issues” and Bertin uses TSVs “as heat pipes.” *See* Reply 25 (citing Ex. 1035, 247:10–15, 246:14–247:2). Accordingly, Petitioner persuasively shows that the combined teachings of Bertin and Cooke “include the heat dissipation features of Bertin such that a POSITA would have expected the combination of Bertin and Cooke to be successful.” *Id.* (citing Ex. 1002 ¶ 165).

Patent Owner also argues that Petitioner’s assertion that “*Bertin*’s ‘logic chip’ *could* be a programmable array fails,” because “disclosure of a genus is not a disclosure of a species.” Sur-reply 9. This argument mischaracterizes Petitioner’s showing as one of anticipation and does not address Petitioner’s obvious showing based on the combined teachings of Bertin and Cooke. *See* Pet. 55–69.

Based on the foregoing discussion, Petitioner persuasively shows that the combination of Bertin and Cooke would have rendered claim 1 obvious. Relying partly on its showing with respect to claim 1, Petitioner provides a similar and persuasive showing for independent claims 9, 17, and 25, which largely track the limitations recited in claim 1, and a persuasive showing supported by the record with respect to dependent claims 3, 5–9, 11, 13–17, 19–22, 25, 26, 28 and 29. *See id.* at 62–79. The Petition shows that Bertin discloses these recitations or they involve well-known circuit elements and amount to combining “familiar elements according to known methods . . . [to] yield predictable results.” *See KSR*, 550 U.S. at 416; Pet. 62–79; *supra* § II.F.D (summarizing the added claim limitations).

Patent Owner does not address independent claims 9, 17, and 25 or dependent claims 3, 5–9, 11, 13–16, 19–22, 25, 26, 28 and 29 separately from claim 1, other than as discussed above in connection with claims 8, 16, and 22. *See* PO Resp. 37–44.

Accordingly, based on the record and as summarized above, including arguments and cited evidence in Patent Owner’s Response and Sur-reply, Petitioner establishes by a preponderance of evidence that the combination of Bertin and Cooke would have rendered obvious claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29. *See* Pet. 55–79.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.¹⁷ In summary:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent -able
1, 5, 7	102	Alexander	1, 5, 7	

¹⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent -able
9, 13, 15	103(a)	APA, Alexander	9, 13, 15	
1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29	103(a)	Koyanagi, Alexander	1, 3, 5–9, 11, 13–17, 19– 22, 25, 26, 28, 29	
1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29	103(a)	Bertin, Cooke	1, 3, 5–9, 11, 13–17, 19– 22, 25, 26, 28, 29	
Overall Outcome			1, 3, 5–9, 11, 13–17, 19– 22, 25, 26, 28, 29	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2

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