

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., and
TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC,
Patent Owner.

IPR2020-01021¹
Patent 7,282,951 B2

Before KARL D. EASTHOM, BARBARA A. BENOIT, and
SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00394 and has been joined as a party to this proceeding.

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1, 4, 5, 8, 10, and 13–15 (the “challenged claims”) of U.S. Patent No. 7,282,951 B2 (Ex. 1001, “the ’951 patent”). Pet. 1. Petitioner filed a Declaration of Dr. Stanley Shanfield (Ex. 1002) with its Petition. Arbor Global Strategies LLC (“Patent Owner”), filed a Preliminary Response (Paper 7).

After the Institution Decision (Paper 11, “Inst. Dec.”), Patent Owner filed a Patent Owner Response (Paper 16, “PO Resp.”) and a Declaration of Dr. Krishnendu Chakrabarty (Ex. 2015); Petitioner filed a Reply (Paper 19) and a Reply Declaration of Dr. Stanley Shanfield (Ex. 1030); and Patent Owner filed a Sur-reply (Paper 24, “Sur-reply”). Thereafter, the parties presented oral arguments via a video hearing (September 14, 2021), and the Board entered a transcript into the record. Paper 29 (“Tr.”).

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies itself, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. Pet. 74. Taiwan Semiconductor Manufacturing Co. Ltd. identifies itself and TSMC North America as real parties-in-interest. *See* IPR2021-00394, Paper 2, 71. Patent Owner identifies itself. Paper 5, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd. et al.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed

October 11, 2019) (“District Court”) as a related infringement action involving the ’951 and two related patents, U.S. Patent No. RE42,035 E and U.S. Patent No. 6,781,226 B2, which contain the same specification as the ’035 patent. *See* Pet. 74; Paper 5.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in the two related patents, respectively IPR2020-01020 and IPR2020-01022. Taiwan Semiconductor Manufacturing Co. Ltd. filed petitions in IPR2021-00391 and IPR2021-00393, and the Board joined it as a party to IPR2020-01020 and IPR2020-01022, respectively.

C. The ’951 patent

The ’951 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the ’951 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” *Id.*

Figure 4 follows:

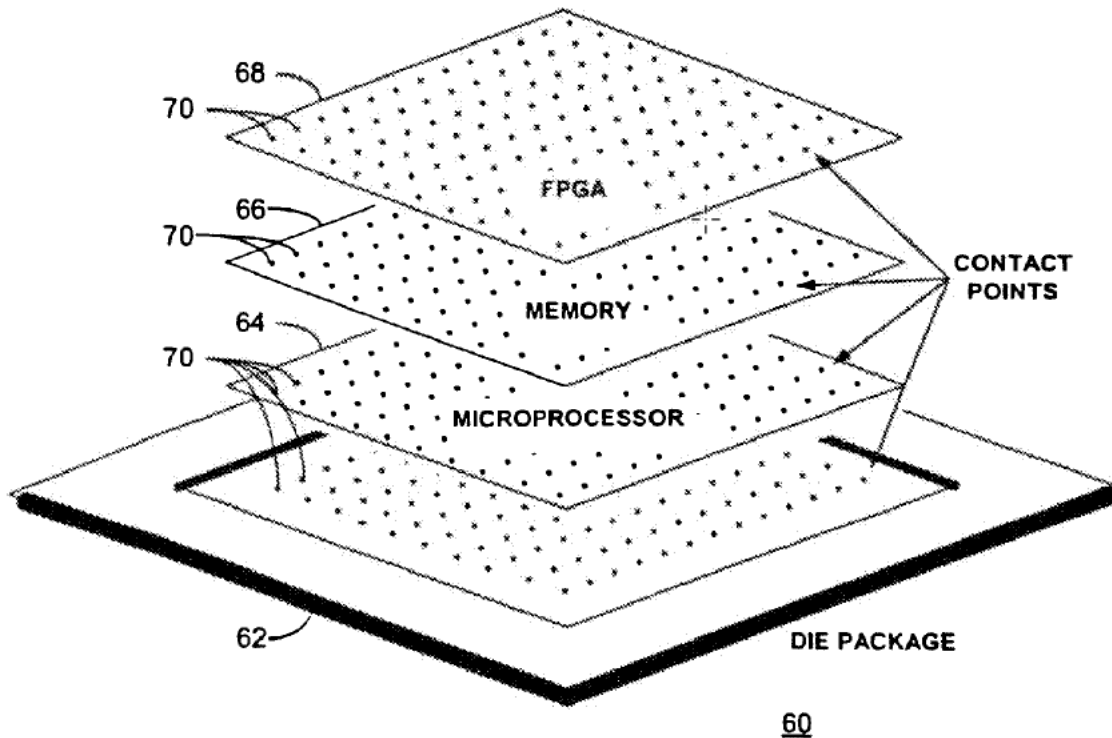


Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using metal and “contact points, or holes, 70.” Ex. 1001, 4:6–20.

The '951 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” *See* Ex. 1001, 1:26–41. Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See id.* A “reconfigurable processor” provides a known benefit of flexibly providing the specific functional units required by an application after manufacture. *See id.*

D. Illustrative Claims 1 and 10

The Petition challenges independent claims 1, 5, and 10, and claims 4, 8, and 13–15, dependent respectively therefrom. Claims 1 and 10 illustrate the challenged claims at issue.

1. A processor module comprising:

[1.1] at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and

[1.2] at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element

[1.3] wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and

[1.4] wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.

Ex. 1001, 7:58–8:4 (information added by Board to conform to Petitioner’s nomenclature); *see* Pet. 23–30 (addressing claim 1).

10. A processor module comprising:

at least a first integrated circuit functional element including a programmable array;

at least a second integrated circuit functional element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit functional element; and

at least a third integrated circuit functional element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit functional elements respectively wherein said memory is functional to accelerate external memory references to said programmable array.

Ex. 1001, 7:58–8:4, 8:42–55.

E. The Asserted Grounds

Petitioner challenges claims of the '951 patent as follows (Pet. 2):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 4, 5, 8, 10, 13–15	103 ²	Koyanagi, ³ Alexander ⁴
1, 4, 5, 8, 10, 13–15	103	Bertin, ⁵ Cooke ⁶

II. ANALYSIS

Petitioner challenges claims 1, 4, 5, 8, 10, 13–15 as obvious. Patent Owner disagrees.

A. Legal Standards

“Section 103(a) forbids issuance of a patent when ‘the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of institution, the '951 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies. The parties describe December 5, 2001 as the earliest effective filing date at issue here. PO Resp. 5; Pet. 4.

³ M. Koyanagi et al., “Future System-on-silicon LSI Chips,” IEEE Micro, Vol. 18, Issue 4, July/August 1998. Ex. 1007.

⁴ M.J. Alexander et al., “Three-dimensional Field-programmable Gate Arrays,” Proceedings of Eighth International Application Specific Integrated Circuits Conference, September 18–22, 1995. Ex. 1006.

⁵ Bertin, US 6,222,276 B1, issued Apr. 24, 2001. Ex. 1009.

⁶ Cooke, US 5,970,254, issued Oct. 19, 1999. Ex. 1008.

invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.⁷ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Shanfield, Petitioner contends that [a] person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have been a person having a Master’s degree in Electrical Engineering, Computer Engineering, or Physics with three to five years of industry experience in integrated circuit design, layout, packaging or fabrication. Ex. 1002 ¶¶ 55–58. A greater level of experience in the relevant field may compensate for less education, and vice versa.

Pet. 10.

Patent Owner contends that “a person of ordinary skill in the art . . . would have had a Bachelor’s degree in Electrical Engineering or a related

⁷ The Petition states that “Patent Owner vaguely asserted the presence of secondary considerations in the District Court case, but has not provided any evidence sufficient to establish a nexus between the alleged evidence and the Challenged Claims.” Pet. 70. On this record, Patent Owner does not assert secondary indicia of nonobviousness.

and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.” PO Resp. 4 (citing Ex. 2015 ¶ 33).

We adopt Petitioner’s proposed level of ordinary skill in the art as we did in the Institution Decision, which comports with the teachings of the ’951 patent and the asserted prior art. *See* Inst. Dec. 18–19. Patent Owner’s proposed level is slightly lower but it overlaps with Petitioner’s proposed level. Even if we adopted Patent Owner’s proposed level, the outcome would not change.

C. Claim Construction

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2019). Under the same standard applied by district courts, claim terms acquire their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Claims 1, 5, and 10 respectively recite “a memory array functional to accelerate external memory external memory references to the processing element,” “said memory array is functional to accelerate external memory

references to the processing element,” and “wherein said memory is functional to accelerate external memory references to said programmable array” as recited respectively in claims 1, 5, and 10. In other words, the challenged claims all require the materially same “functional to accelerate” limitation.

In the Institution Decision, we preliminarily determined that the construction of this “functional to accelerate” limitation is “a number of vertical contacts that traverse the memory die in the *internal* periphery of the die and provide contacts on the surface of the memory die.” Inst. Dec. 24 (emphasis added). To add context to that construction, we also preliminarily stated that “the ‘functional to accelerate’ limitations require a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) *within the periphery* of the die to allow multiple short paths for data transfer between the memory and processor.” *Id.* at 25 (emphasis added).

Patent Owner here argues that “the term ‘internal periphery’ is not described in the specification, and will not add clarity to the meaning of the term.” PO Resp. 8 (citing Ex. 2015 ¶ 39).⁸ Patent Owner also argues that

⁸ In a related institution decision also involving challenges to claims 1, 5, and 10 of the ’951 patent, Patent Owner similarly argues that “[t]he requirement of an ‘internal periphery’ . . . excludes embodiments such as the embodiment shown in figure 5 of the ’951 Patent, which shows contacts distributed throughout a die, not just in the ‘internal periphery’ of the die.” *Id.* at 21. IPR2020-01568, Paper 7 (preliminary response), 20–21 (emphasis added). In response, the Board determined that the accelerate limitation means “a number of vertical contacts that traverse the memory die within the periphery of the die and provide contacts on the surface of the memory die.” *See* IPR2020-01568, Paper 12 (institution decision), 26.

“the Board’s preliminary construction only adds ambiguity to the meaning of this term because it requires “a number of vertical contacts that . . . provide contacts *on the surface* of the memory die,” and further, claim 1 already recites that ““a second integrated circuit functional element’ has ‘a number of contact points distributed throughout *the surfaces* of said functional element.”” *See id.* at 9 (emphasis added). Therefore, Patent Owner offers the following “suggest[ion]”: “To the extent that the Board finds it necessary to mention contacts in the context of the claimed ‘memory array,’ Patent Owner suggests that the Board use the term ‘*a number of vertical contacts distributed throughout the surface of and traversing the memory die.*’” PO Resp. 8 (emphasis added). For reasons discussed further below and in the Institution Decision, the record, including the specification, supports Patent Owner’s suggestion, and we determine that Patent Owner’s claim construction suggestion is materially the same as the preliminary claim construction set forth in the Institution Decision. *See, e.g.,* Ex. 1001, 2:41–44 (“[S]ince these differing die do not require wire bonding to interconnect, *it is now also possible to place interconnect pads throughout the total area of the various die rather than just around their periphery.*”) (emphasis added); Inst. Dec. 24–25.

In addition to Patent Owner’s suggestion above, Patent Owner also argues that “the term ‘a memory array functional to accelerate external memory references to the processing element’ means ‘a memory array that allows the parallel loading of data *through buffer cells.*’” PO Resp. 6 (emphasis added). Patent Owner asserts that “[i]n its preliminary response, Patent Owner advocated that this term should be accorded its plain and

ordinary meaning.” PO Resp. 5. It is not clear if Patent Owner maintains (i.e., in its Response) that the phrase carries its plain and ordinary meaning.⁹

In any event, the record does not support Patent Owner’s proposed requirement for “buffer cells” under the plain and ordinary meaning of the “functional to accelerate” clause or under lexicography principles, prosecution history or otherwise, for the reasons advanced by Petitioner and as addressed below. In line with Patent Owner’s suggestion and as we similarly determined in the Institution Decision, the “functional to accelerate” limitations require “a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory and processor.” *See* Ex. 1001, Fig. 4 (showing numerous contact points); Inst. Dec. 25 (materially similar construction); PO Resp. 8 (Patent Owner’s suggestion). We adopt and incorporate the claim construction findings in the Institution Decision, much of which we repeat here for completeness. *See* Inst. Dec. 19–25.

Petitioner argues that “[t]he Board correctly construed” the “functional to accelerate” clause in the Institution Decision. Reply 11. According to Petitioner, Patent Owner’s new “attempt to read buffer cells into the claims, based on an embodiment in the specification in which buffer

⁹ In the related *inter partes* case, Patent Owner does maintain in its response there that it “construes all terms in ‘accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.’” IPR2020-01568, Paper 18 (response), 9 (quoting C.F.R. § 42.100(b)). In its preliminary response in that case, Patent Owner states that the District Court also construed the claims according to their plain meaning. IPR2020-01568, Paper 7 (preliminary response), 19.

cells are in fact not used for the claimed acceleration, should be rejected.” *Id.* at 7 (citing *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358F.3d 898, 908 (Fed. Cir. 2004) (“The fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives.”)). Petitioner also argues that Patent Owner consistently argued “the plain and ordinary meaning” of “the ‘accelerate’ claim term” prior to institution “both to the Board and the district court . . . and never mentioned ‘buffer cells’.” *Id.* (citing Ex. 1036 (district court claim construction order), 49). The record supports Petitioner’s argument that Patent Owner shifted its claim construction position relative to its position in the District Court to specifically include buffer cells here. *See* Ex. 1036, 49 (construing the “functional to accelerate” clause according to its “[p]lain and ordinary meaning”); Inst. Dec. 19–25 (addressing the parties’ arguments).¹⁰

Petitioner also persuasively argues that “Dr. Shanfield testifie[s] that ‘the specification attributes the claimed acceleration to the stacking of an FPGA die and a memory die,’ where they are interconnected ‘using contact points distributed through the dies.’” Reply 8 (quoting Ex. 1002 ¶ 90; citing Ex. 1001, 2:33–46, 2:65–3:2). In the District Court proceeding, as Petitioner points out, Patent Owner argued that “the short” interconnects “allow[] for accelerated external memory references.” *Id.* at 6 (quoting Ex. 1028 (Patent Owner’s claim district court construction brief arguing that the claims are definite), 29). That is, Patent Owner argued as follows in the District Court proceeding:

¹⁰ Patent Owner is under no obligation in an *inter partes* review to provide any claim construction (either prior to or after the Institution Decision).

The specification teaches in several sections that ***the short interconnects to the memory die allows for accelerated external memory references***, providing additional context for a POSITA to interpret the claims. . . . For example, the '951 Patent states that in reference to Figures 4 and 5 that acceleration to external memory is performed because ***“the FPGA module may employ stacking techniques to combine it with a memory die for accelerating external memory references as well as to expand its on chip block memory.”***

Ex. 1028, 29 (citing or quoting the '951 Patent, Figs. 4, 5, 2:56–3:2); Reply 6 (emphasis added by Petitioner) (quoting Ex. 1028, 29). The parties appear to agree that the numerous “short interconnects” (conductive vias) in Figure 4 enable parallel processing or loading (even though Patent Owner did not argue explicitly in the District Court that the claims require parallel loading (Ex. 1028, 26–29)).¹¹ See Pet. 4 (arguing that the advantages of die stacking using vias extending through the dies were well-known, and include ‘high speed’ and ‘parallel signal processing’”), 15 (discussing Ex. 1009, 7:16–34 (stacking with through-hole contacts minimizes latency and maximizes bandwidth)); PO Resp. 3 (“The '951 Patent explains how electrical

¹¹ Patent Owner also argued in the District Court that “[f]or example, . . . the specification also discloses . . . a memory array and a *buffer cell which can be part of the memory die with short interconnects*, thus improving the speed of and access to memory in comparison to the prior art.” Ex. 1028, 29. This argument of an example of buffer cells that “can be” used to improve speed is not an argument that the claims *require* buffer cells, especially where Patent Owner relies mainly on the “short interconnects” (vias) to improve speed.

connections, such as TSVs [through-silicon vias], are used to load configuration data in a parallel fashion”¹²

“[I]n . . . agreement with” Patent Owner’s District Court arguments (*see* Reply 6), as we preliminarily determined in the Institution Decision, the ’951 patent specification supports Petitioner in several places by consistently tying data acceleration to stacking techniques that include vias extending through the stacked dies. *See* Ex. 1001, 2:65–3:2 (“[T]he FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references as well as to expand its on chip block memory.”), 2:31–60 (describing how “metal contacts can traverse the thickness of the wafer” to create “a single very compact structure” and ultimately “accelerat[e] the sharing of data between the microprocessor and FPGA”), 2:63–65 (“Further disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of accelerating external FPGA reconfiguration”); *see* Pet. 30 (citing Ex. 1001, 2:65–3:2; Ex. 1007, 17, 19; Ex. 1002 ¶ 93). These passages do not rely on buffer cells for data acceleration.

As also preliminarily determined in the Institution Decision, the Petition “shows that the advantages of die stacking using vias extending through the dies were well-known, and include ‘high speed’ and ‘parallel signal processing.’” Inst. Dec. 22 (quoting Ex. 1010, 1704; citing Ex. 1002 ¶ 39; Pet. 4); *see also* Pet. 4 (quoting Ex. 1010, 1704; citing Ex. 1002 ¶ 39). As the record shows, this data speed increase (data acceleration relative to

¹² Petitioner’s challenges include a showing of short via connections throughout all the dies in the stack of the prior art dies for enabling parallel signal processing. *See infra* §§ II.D, II.E.

the prior art) arises from relatively shorter signal paths using conductive vias extending through dies as opposed to using longer prior art contact runs toward the periphery to ultimately connect dies at the edges thereof. *See* Pet. 15 (discussing Ex. 1009, 7:16–34 (stacking with through-hole contacts minimizes latency and maximizes bandwidth)); Ex. 1006, 1 (“interconnect delay” occurs in prior art non-stacked FGPAs); Ex. 1010, 1704 (“High-speed performance is associated with shorter interconnection delay time and parallel processing. . .”).

The abstract of the ’951 patent further supports this interpretation. It specifically ties “stacking . . . die elements and interconnecting the same utilizing contacts that traverse the thickness of the die” to create a “processor module” with the claimed “acceleration”: “The processor module disclosed *allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA* element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” Ex. 1001, code (57) (emphasis added). The abstract, which specifically describes data “acceleration” based on “stacking” and “contacts that traverse the thickness of the die” does not even mention buffer cells. *Id.* Even though the abstract refers to data acceleration “between *the microprocessor and the FPGA* element,” and the challenged claims recite “a memory array functional to accelerate external memory external memory references to the processing element,” the same principle of using short via connections through the dies to accelerate data transfers applies.

Supporting this interpretation, as noted above and in the Institution Decision, the ’951 patent states that “the FPGA module may employ stacking techniques to combine it with a memory die for the purpose of

*accelerating external memory references.” Id. at 2:66–3:2 (emphasis added); see also Ex. 1001, 5:20–23 (“[S]tacking die 64, 66 and 68 with through-silicon contacts . . . serves . . . [the] traditional role of *fast access memory*. However, in this new assembly [memory] *is accessible by both the microprocessor 64 and the FPGA 68 with equal speed.*”).* The recitation in claim 1, “memory array functional to accelerate external memory references to the processing element,” and similar recitations in the remaining challenged claims, directly track the specification’s language describing this embodiment for “*accelerating external memory references*” *id. at 2:66–3:2*) contrary to Patent Owner’s arguments otherwise. *See* Sur-reply 3 (arguing that “Petitioner cannot point to a single distinct embodiment in the ’951 Patent that does not use buffer cells to accelerate memory references to the processing element”). And this “accelerating” language is in juxtaposition to other language in the same passage stating that “[f]urther disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of *accelerating external FPGA reconfiguration.*” *Id. at 2:63–65.* These juxtaposed passages illustrate the difference between “*accelerating external FPGA reconfiguration*” (*id.*) which the challenged claims do not recite, and “*accelerating external memory references*” (*id. at 2:66–3:2*), which the challenged claims do recite.

Figure 4 of the '951 patent, which follows, also supports this interpretation:

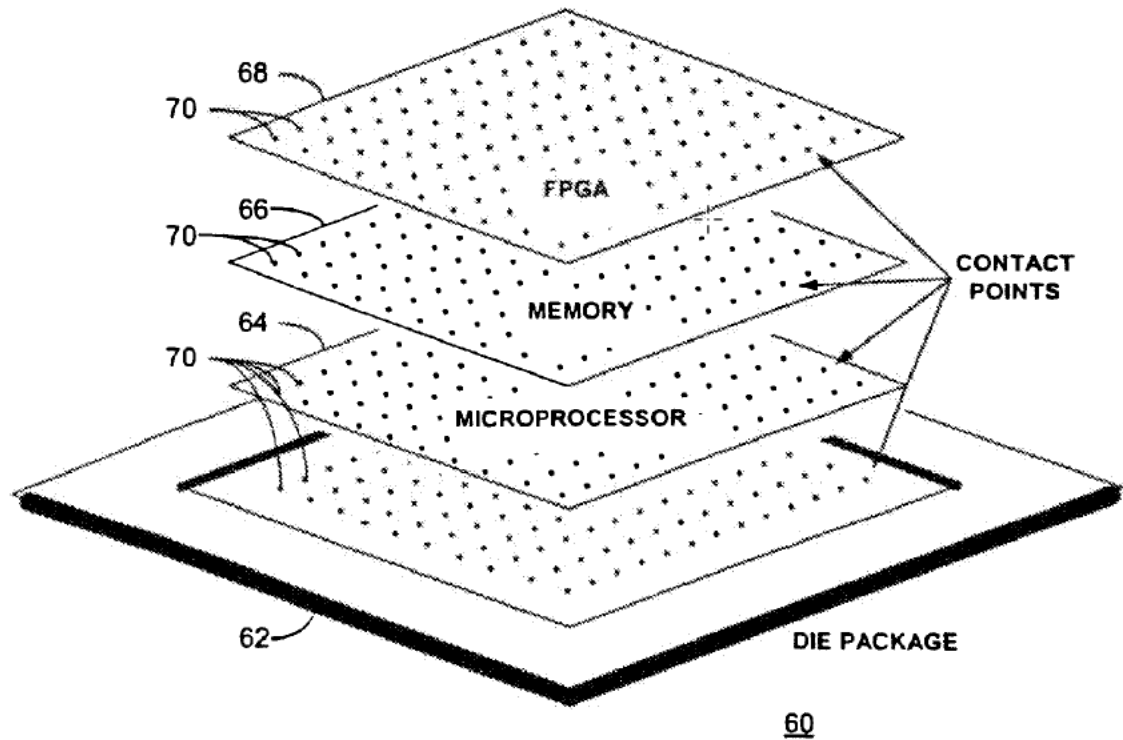


Fig. 4

As depicted above, Figure 4 shows a number of contact points (which represent vias) throughout the periphery of the FPGA die, memory die, and microprocessor die. As indicated above, these vias or “contacts . . . traverse the thickness of the die.” Ex. 1001, code (57). Similar to the abstract, Figure 4 does not specifically depict (and the related disclosure does not describe) buffer cells. *Id.* at 4:9–44; *compare id.*, with *id.* at 4:54–55 (describing buffer cells are preferably on memory die 66 in the context of Figure 5, which applies as an embodiment of Figure 4).

Nevertheless, Patent Owner relies on Figure 5 of the '951 patent to support its contention that the “functional to accelerate” clause requires

“buffer cells,” i.e., “a memory array that allows the parallel loading of data through *buffer cells*.” See PO Response 6–7 (emphasis added). Patent Owner’s annotated version of Figure 5 follows (*id.* at 7):

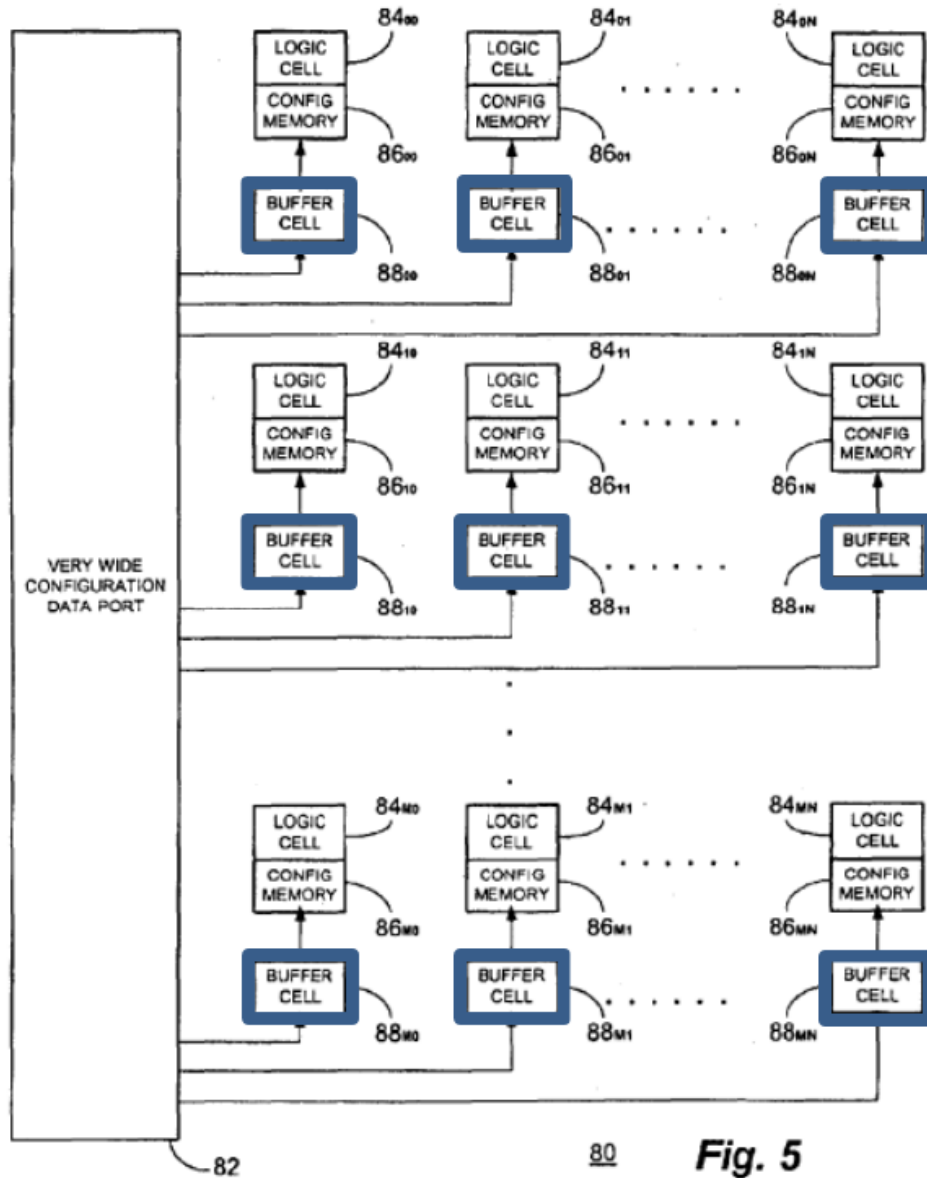


Figure 5, as annotated by Patent Owner above, shows (blue) “BUFFER CELL[S]” 88 connected to “CONFIG MEMORY” cells 86, in turn connected to “LOGIC CELLS” 84, at the output of a “VERY WIDE CONFIGURATION DATA PORT.” The ’951 patent states that “FIG. 5 is a

corresponding functional block diagram of the configuration cells of the reconfigurable processor module of FIG. 4 wherein the FPGA may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel.” Ex. 1001, 4:9–13.

This description of “wherein the FPGA may be totally reconfigured” signifies that Figure 5 represents one embodiment of the generic disclosure of what the Figure 4 embodiment “may” include. In other words, the generic embodiment of Figure 4, like the challenged claims, does not *require* “wherein the FPGA may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel.” *See id.* Rather, “FIG. 4 is a simplified, exploded isometric view of a reconfigurable processor module *in accordance with the present invention comprising a hybrid device incorporating a number of stacked integrated circuit die elements.*” *Id.* at 4:5–8 (emphasis added). And even if the claims somehow require the capability of reconfiguring the FPGA in one clock cycle using parallel via connections, the specification does not show that any challenged claims require buffer cells for that purpose, as Petitioner persuasively shows.

In reference to Figure 5, Patent Owner contends that buffer cells 88 allow for acceleration of “memory references” because the “memory array . . . *doesn’t need to wait for the FPGA to cease operating*”:

The specification discloses that *the buffer cells 88 (which are associated with the wide configuration data port) can be loaded in parallel with configuration data while the FPGA is in operation.* [Ex. 1001,] 5:29–39. *As a result of the parallel loading of data into the buffer cells while the FPGA and its logic cells are in operation,* the memory array can accelerate memory references to the configuration memory 86 of the FPGA (*because it doesn’t need to wait for the FPGA to cease operating*), as compared to a configuration that did not include the disclosed

buffer cells. *Id.* at 5:42–44 (“FPGA 68 [can] be totally reconfigured in one clock cycle with all of its configuration logic cells 84 updated in parallel.”).

PO Resp. 8 (citing Ex. 2015 ¶ 38) (emphasis added). Patent Owner’s arguments show that “configuration” or “reconfiguration” through parallel loading can occur without buffer cells—i.e., reconfiguration in one clock cycle or otherwise can occur *when the FPGA is not operating*.¹³ *See id.*

In its Sur-reply, Patent Owner stresses that “a **memory array** is responsible for the claimed acceleration of data references.” Sur-reply 2. Patent Owner argues that “that the claims require a ‘memory array,’ not ‘a number of vertical contacts.” *Id.* at 1. But Patent Owner’s other arguments contradict this last argument, because Patent Owner otherwise agrees and argues that the claimed acceleration requires a number of vertical contacts, specifically TSVs: “[T]he ’951 Patent discloses and *claims* an entirely new arrangement of *TSVs* (i.e., the wide configuration data port) that that provides parallel connections between a memory die and a programmable array through buffer cells *and configuration memory*.” Sur-reply 3–4 (emphasis removed and added). Under Patent Owner’s theory, the claim construction should also include TSVs (in a wide configuration data port) and configuration memory as part of the memory array if the memory array also includes the buffer cells. But Patent Owner does not argue, and the record does not show, that TSVs or configuration memory (on the right in Figure 5) are part of the *memory array*. *See* Ex. 1001, Fig. 5; Ex. 1035,

¹³ The challenged claims each recite a “programmable array,” which includes, but does not require, an FPGA. Nothing in the challenged claims requires reconfiguring multiple times, reconfiguring in one clock cycle, or reconfiguring through buffer cells, to satisfy the “programmable” limitation.

157:3–17, 158:10–12 (agreeing that “memory die 66” is “to the left of the very wide configuration data port 82 in Figure 5, although not shown” and the “connections” shown in Figure 5 “are formed by the TSVs that are between the memory die [not shown in Figure 5] and the FPGA die” “to the right of Figure 5”).

For example, Patent Owner also argues that the specification discloses that “the buffer cells 88 are preferably a portion of the *memory die 66*.” Sur-reply 2 (emphasis added by Board) (quoting Ex. 1001, 5:38–39). But this specification sentence does not describe buffer cells in the *memory array*—i.e., memory die 66 is simply a type of substrate for a memory array, buffer cells, and other memory circuitry. See Ex. 1001, Fig. 4, Fig. 5, 5:38–39. Patent Owner’s inclusion of buffer cells in its claim construction, where the disclosed buffer cells are also not part of a memory array, undermines Patent Owner’s argument that Petitioner’s claim construction is incorrect because it includes vias. Patent Owner’s arguments otherwise acknowledge that the claimed acceleration requires numerous vias, as noted above and as explained further below. Patent Owner’s suggestion, and other arguments and evidence, support the finding that it is the numerous vias extending through dies like the memory die, to a memory array, which enables the “memory array *functional* to accelerate external memory external memory references to the processing element.” See Ex. 1001, Fig. 4.

Dr. Chakrabarty, Patent Owner’s expert, agrees that the “*large number of connections*, which are obtained through the TSVs, *accelerate the data transfer between the memory and the FPGA*.” Ex. 1035, 270:7–11. As Petitioner also persuasively shows, “Dr. Chakrabarty admit[s] that it is the vertical contacts of the memory die that perform the claimed acceleration,”

and “he admit[s] that the buffer cells in Figure 5 of the ’951 patent do *not* serve to perform the claimed acceleration, but *to allow the wide configuration data port and the FPGA to operate independently of each other.*” Reply 9 (emphasis added) (citing Ex. 1035, 160:11–161:13 (agreeing that buffer cells allow new configuration data to be sent over the configuration data port *while the FPGA is operating under its previous configuration*), 164:22–165:12 (agreeing that buffer cells support an *asynchronous* configuration update and that another “way of” “updat[ing] the configuration” without buffer cells is waiting until the “FPGA is idle”); Ex. 1030 ¶ 28)); *see also* Ex. 1030 ¶¶ 17–21, 28–29 (persuasively testifying that buffer cells support *asynchronous* reconfiguration and the claimed acceleration does not require buffer cells).

Therefore, as Petitioner persuasively argues, “the description of Figure 5 confirms that the purpose of the buffer cells is not to perform the claimed ‘acceleration,’ but to allow asynchronous updating of the logic cells.” Reply 11 (citing Ex. 1001, 5:34–41 (describing that “buffer cells 88” “can be loaded while the FPGA 68 comprising the logic cells 84 are in operation”)). As Petitioner also persuasively argues, “[w]ith or without the buffer cells, the large number of TSVs that form the wide configuration data port accelerate data transfer from the memory to the FPGA, as Dr. Chakrabarty admits.” *Id.* (citing Ex. 1035, 155:7–22 (agreeing that Figure 4’s configuration data port includes TSVs connecting the memory die to the FPGA die), 157:23–158:3 (agreeing that “the reason it’s a very wide configuration data port [in Figure 5] is because it has a lot of connections through these TSVs between the memory die and FPGA die”), 269:24–270:11 (agreeing that the “large number of connections” obtained through

the TSVs “accelerate the data transfer between the memory and the FPGA” in Figure 5).¹⁴

In addition, the relied-upon upon passage by Patent Owner pertaining to Figure 5 and buffer cells describes a single clock cycle reconfiguration benefit (which the challenged claims do not require) instead of a more generic data acceleration that includes external memory references. *See* Ex. 1001, 5:29–50. And the specification refers to this reconfiguration benefit as described at column 5 as “[i]n *addition*” to “an *added* benefit of overall reduced power requirements and *increased operating bandwidth*. *Because*

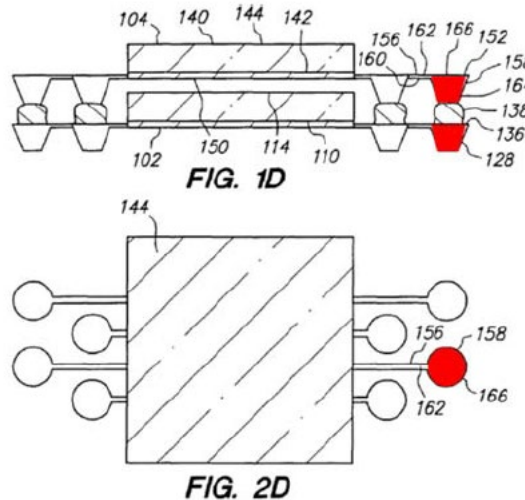
¹⁴ In other words, the record shows that a wide (or very wide) configuration data port (*see* Fig. 5) is essentially a known interface that enables a large number of vias to connect the dies for parallel data transfers. *See* PO Resp. 3–4 (urging parallel data transfer in its claim construction); Reply 11; Ex. 1035, 155:7–22 (agreeing that a configuration data port includes many TSVs), 157:23–158:3 (agreeing that configuration data port is wide because “it has a lot of connections through these TSVs”), 163:8–163:21 (agreeing that a “configuration data port” is “just a data port used for configuration” and “data port is just an interface to send data from one place to another”), 269:24–270:11 (agreeing that the “large number of connections” (TSVs) “accelerate the data transfer between the memory and the FPGA” in Figure 5). In comparison to the wide configuration data port of Figure 5, the ’951 patent refers to Prior Art Figure 3 in describing loading cells “in a byte serial fashion,” “through a *relatively* narrow, for example, 8 bit port that results in the long reconfiguration times.” Ex. 1001, 4:54–60 (emphasis added), Fig. 3. In other words, a byte in Figure 3 represents, “for example,” 8 bits, and Prior Art Figure 3 represents loading 8 bits (of a byte) in parallel and then loading each such byte serially to successive logic cells during a reconfiguration. *See id.*; *see also* Ex. 1035, 270:6–274:18 (discussing the number of bits in a wide configuration data port versus a narrow port as depending on the context, including “how much parallelism you want” (*id.* at 272:14–15), generally agreeing that a “large number of connections, which are obtained through the TSVs, accelerate the data transfer” (*id.* at 270:6–11)).

the various die 64, 66 and 68 (FIG. 4) have very short electrical paths between them, the signal levels can be reduced while at the same time the interconnect clock speeds can be increased.” *Id.* at 5:51–56 (emphasis added). As found above, the parties generally agree that the specification describes data acceleration in terms of numerous short via connections to enable parallel data transfers—further enabling increased bandwidth (depending on the clock rate). *See supra* note 13; *infra* note 15. The specification also describes a stack of functional circuits, including a microprocessor, FPGA, and memory, as claimed, without any mention of Figure 5’s buffer reconfiguration scheme. *See, e.g.,* Ex. 1001, code (57) (describing “significant acceleration in the sharing of data” due to “stacking” and “contacts that traverse the thickness of the die”), 7:26–29 (describing Figure 11 as depicting “a module . . . wherein three functional elements are fabricated on a single base wafer, including functional elements 100, 106, and 112”).

Finally, as noted in the Institution Decision, prosecution history plays an important role in understanding the claims and supports the claim construction. Under *Phillips*, “[l]ike the specification, *the prosecution history provides evidence of how the PTO and the inventor understood the patent.*” *Phillips*, 415 F.3d at 1317 (emphases added). Here, the prosecution history provides some understanding of “wherein said memory array is functional to accelerate external memory references to said processing element.” The Examiner indicated allowance of dependent claim 35 (if written in independent form) over Lin (U.S. Patent No. 6,451,626), finding Lin does not teach or suggest this

“accelerate” limitation. *See* Ex. 1004, 68, 73–74; Pet. 8–9 (discussing prosecution history).

Addressing the prosecution history, Petitioner provides the following figures from Lin:



Petitioner’s annotations of Lin’s Figures 1D and 2D show that Lin discloses contacts on the sides of dies, instead of a number contact vias extending throughout the periphery and thickness of the dies. *See* Pet. 9 (citing Ex. 1019, Figs. 1D, 2D; Ex. 1004, 73). Accordingly, in light of Lin’s teachings and the specification, the prosecution history further supports the understanding that the “functional to accelerate” limitations require a large number of short contacts extending throughout the thickness of the wafers in a vertical direction (i.e., vias) throughout the die to allow multiple short paths for data transfer between the memory and processor. *Compare*, Ex. 1001, Fig. 4 (showing numerous contact points) *and* Ex. 1001, 2:41–44 (“[S]ince these differing die do not require wire bonding to interconnect, *it is now also possible to place interconnect pads throughout the total area of the various die rather than just around*

their periphery.”) (emphasis added), *with* Ex. 1019, Fig. 1D, 2D (showing peripheral contact points).

Accordingly, for the reasons above, the construction of the “functional to accelerate” limitations is “a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory and processor.”

Based on the current record, no other terms require explicit construction. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness, Koyanagi and Alexander, Claims 1, 4, 5, 8, 10, and 13–15

Petitioner contends that claims 1, 4, 5, 8, 10, and 13–15 would have been obvious over the combination of Koyanagi and Alexander. Pet. 17–46. Patent Owner disputes Petitioner’s contentions. PO Resp. 16–30.

1. Koyanagi

Koyanagi describes a “three-dimensional integration technology” (“3D”) that involves vertically stacking and interconnecting chips using “a high density of vertical interconnections” (Ex. 1007, 17) to “connect[] each layer” (*id.* at 18).

Koyanagi explains that its 3D-integration technology “enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips.” *Id.* at 17–18 (“More than 10^5 interconnections per chip form in a vertical direction in these 3D . . . chips.”). Koyanagi’s system “dramatically

increase[s] wiring connectivity while reducing the number of long interconnections.” *Id.* at 17.

Koyanagi’s Figure 1a follows:

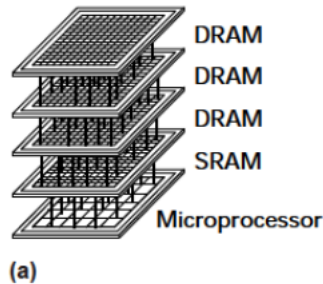


Figure 1a illustrates a stack of chips including dynamic random access memory (DRAM) chips and a synchronous random access memory (SRAM) chip “stacked on a microprocessor” chip. *See* Ex. 1007, 17. Koyanagi describes “form[ing] as many vertical interconnections as possible” to “remove the generated heat” and form “electrical wirings.” *Id.* According to one embodiment in Koyanagi, “2D image signals move simultaneously in a vertical direction and are processed in parallel within each LSI [large-scale integration] layer. As a result, using 3D-image-processing LSIs leads to a dramatic processing speed improvement of more than three orders of magnitude.” *Id.* Koyanagi also describes a variety of uses: “Typical examples of these new system LSIs include a merged logic memory (MLM) LSI chip as shown in Figure 1 . . . , and a 3D shared memory for parallel processor systems.” *Id.* at 17.

In addition to enhancing speed, “[v]ertical interconnections can remove the generated heat since, in addition to their function as electrical wirings, they can act as heat pipes. In fact, some vertical interconnections act solely as generated heat removers.” *Id.*

2. *Alexander*

Alexander describes “stacking together a number of 2D FPGA bare dies” to form a 3D FPGA. Ex. 1006, 1. Alexander explains that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” *Id.*

Petitioner annotates Alexander’s Figure 2 as follows:

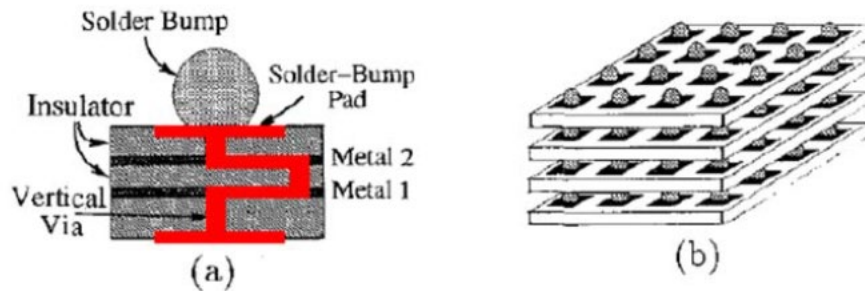


Figure 2(a) shows vertical metal connections (red) traversing a chip with a solder pad and bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1006, 253.

Alexander explains that stacking bare dies to form a 3D FPGA results in a chip with a “significantly smaller physical space,” lower “power consumption,” and greater “resource utilization” and “versatility” as compared to conventional layouts. *Id.*

3. *Obviousness Analysis, Koyanagi and Alexander, Claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28 and 29*

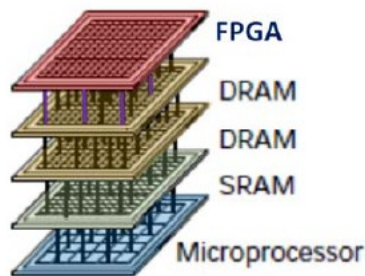
Claim 1’s preamble recites “[a] processor module comprising.” Petitioner relies on the combined teachings of Koyanagi and Alexander, with Koyanagi disclosing all elements of the processor module except a “programmable array.” See Pet. 23–24. Petitioner provides reasons to combine Koyanagi and Alexander as discussed further below. See *id.* at 17–23.

Claim 1 recites limitation 1.1, “at least a first integrated circuit functional element including a programmable array that is programmable as a processing element.” *See* Pet. 24. Petitioner contends that it would have been obvious to employ Alexander’s FPGA as an integrated circuit layers in Koyanagi’s stack. *See* Pet. 17–25. Quoting Alexander, Petitioner contends that “[f]ield programmable gate arrays (FPGAs) are **(re)programmable** chips that can implement **arbitrary logic**.” *Id.* at 24 (quoting Ex. 1006, 1 (emphasis by Petitioner); citing Ex. 1002 ¶ 84; Ex. 1013, 6 (“The FPGA can be visualized as programmable logic blocks embedded in programmable interconnect []. Unlike ASICs, the logic and interconnect resources are uncommitted, and can be configured to implement different logic functions and connectivity.”)).¹⁵

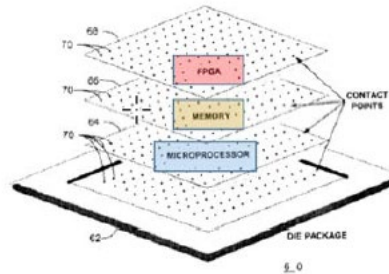
Petitioner provides the following modified version of Koyanagi’s Figure 1 in a side-by-side comparison of the ’035 patent’s Figure 4:

¹⁵ ASICs are application specific integrated circuits. Ex. 1013, 5. Exhibit 1013 is a textbook by Varghese et al., Low-Energy FPGAs—Architecture and Design (2001). Varghese shows the knowledge and the level of ordinary skill in the art at or near the time of the invention in 2001. As noted above, the parties describe December 5, 2001 as the earliest effective filing date at issue here. *Supra* note 2 (citing PO Resp. 5; Pet. 4). Even if we do not consider Varghese (due to its 2001 publication date) as evidencing the knowledge and level of ordinary skill in the art around the time of the invention, Petitioner’s showing is persuasive without it.

Koyanagi Figure 1M



'951 Patent Figure 4



Koyanagi's annotated Figure 1 (labeled 1M by Petitioner) on the left shows a stack of dies, including Alexander's FPGA die, which essentially replaces one of Koyanagi's DRAM dies (*see supra* § II.F.1)), and the '951 patent's Figure 4 on the right shows a similar configuration. *See* Pet. 24.

Petitioner provides evidence that "FPGAs . . . can be flexibly configured and reconfigured to 'implement arbitrary logic' and thus 'provide designers with a faster and more economical design cycle.'" Pet. 18 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 76). Petitioner provides other reasons why a person of ordinary skill in the art ("POSITA") would have been motivated to employ Alexander's FPGA in a Koyanagi's die stack:

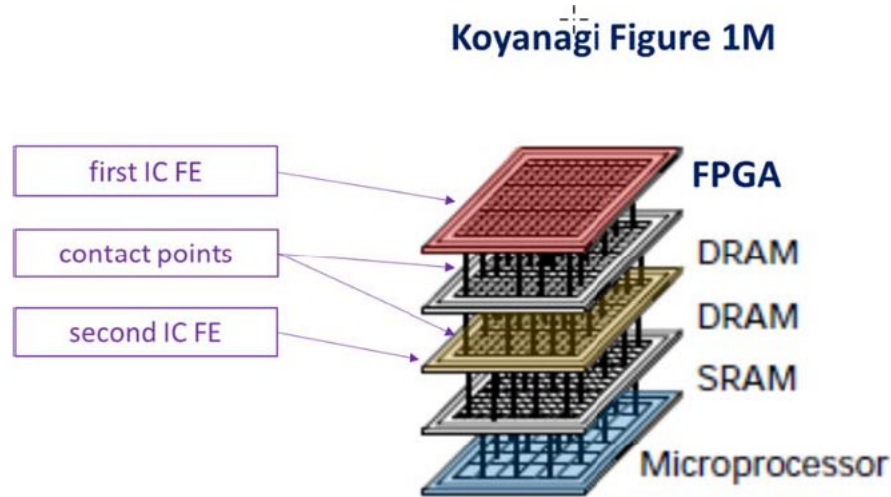
A POSITA would have been motivated to apply Koyanagi's broadly applicable 3D integration scheme to stack Alexander's FPGA bare die over the memory and microprocessor die of Koyanagi Figure 1(a) to form a compact 3D reconfigurable module to *save area, reduce power consumption, and improve performance*. [Ex. 1002 ¶ 82]. A POSITA would have found it obvious to try such stacking and would have had a reasonable expectation of success doing so because both Alexander and Koyanagi teach the same 3D integration scheme whereby bare dies are stacked and interconnected using distributed through-silicon contacts, and because Koyanagi provides broadly applicable, detailed teachings with regard to stacking different types of dies. *Id.*; Ex. 1002 ¶ 82.

Pet. 22–23 (emphasis added).

Petitioner provides citations to Koyanagi and Alexander to support the showing that they include “common teachings” involving “the *same* 3D-integration scheme.” *See* Pet. 20, 17–23 (citing Ex. 1007, 17, 19, Figs. 1, 5; Ex. 1006, 1; Ex. 1002 ¶¶ 79–82). Petitioner provides evidence that known “speed and power dissipation” and other advantages of stacking dies existed prior to the invention. *Id.* at 19 (noting advantages of a 3D stacking system including “miniaturization, low power consumption, and large-scale integration,” and “speed and power dissipation of a total chip”) (quoting Ex. 1010, 1712–13)); *see also* Ex. 1002 ¶ 82 (“A POSITA would have been motivated to apply Koyanagi’s broadly applicable 3D integration scheme to stack Alexander’s FPGA bare die over the memory and microprocessor die of Koyanagi Figure 1(a) to form a compact 3D reconfigurable module to save area, reduce power consumption, and improve performance.”).

Claim 1 recites limitation 1.2, “at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element,” and limitation 1.3, “wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements.”

Petitioner's annotated version of Koyanagi Figure 1 depicts stacked functional elements electrically coupled by distributed contact points:



Petitioner's Figure 1M is an annotated version of Koyanagi's Figure 1 and shows "the top FPGA die ('first IC FE' [integrated circuit functional element]) and the memory die ('second IC FE') . . . electrically coupled by a large number of contact points distributed throughout the surfaces of the functional elements." Pet. 26. To support this showing, Petitioner quotes Koyanagi: "More than 10^5 [100,000] interconnections per chip form in a vertical direction in these 3D LSI chips or 3D MCMs. Consequently, we can dramatically increase wiring connectivity while reducing the number of long interconnections"). *Id.* at 26–27 (quoting Ex. 1007, 17; citing Ex. 1002 ¶ 87).

Petitioner relies on similar teachings in Alexander, including that Alexander "describe[s] 'a matrix of $100 \times 100 = 10,000$ solder bumps' formed over the surface of each die." Pet. 27 (quoting Ex. 1006, 1; citing Ex. 1002 ¶ 88; reproducing Ex. 1006, Figs. 2a, 2bs); *see supra* § II.D.2 (Alexander's Figs. 2a, 2b showing vertical vias and solder bumps). Petitioner provides similar motivation to combine Alexander and Koyanagi

as summarized above in connection with element [1.1]. *See* Pet. 17–23 (§ 7A.1: “**Reasons to Combine Koyanagi and Alexander**”).

Finally, claim 1 recites limitation 1.4, “wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.” Petitioner relies on the combined teachings of Koyanagi and Alexander to address this claim limitation. According to Petitioner, the ’951 patent “specification attributes the claimed acceleration to the stacking of an FPGA die and a memory die, whereby a wide configuration data port interconnects the stacked memory die and the FPGA using contact points distributed throughout the dies.” Pet. 28 (quoting Ex. 1001, 2:65–3:2 (“[T]he FPGA module may employ stacking techniques to combine it with a memory die for the purpose of accelerating external memory references as well as to expand its on chip block memory”); citing Ex. 1001, 2:33–46). Petitioner contends that the combination of Koyanagi and Alexander “renders the claimed acceleration obvious because this prior art combination discloses the same way to accelerate external memory references as is described in the ’951 Patent specification.” *Id.* (citing Ex. 1002 ¶ 90).

Petitioner also cites a number of known benefits that an increased number of vertical contacts provides, including “obtain[ing] more connections between the die[s]” to mitigate bus bottlenecks common in conventional 2D layout, and to increase speed by providing more abundant and shorter circuit board wirings. *See* Pet. 30 (citing Ex. 1001, 2:65–3:2; Ex. 1007, 17, 19; Ex. 1002 ¶ 93). In addition, Petitioner quotes Koyanagi’s bandwidth /speed gains and contends that “[t]he large number of contact points distributed throughout the dies form vertical interconnections that

‘enable large data bandwidth in vertical data transfer’ and thus ‘accelerate’ external memory references to the FPGA processing element in the exact same way discussed in the ’951 Patent specification.” *Id.* at 29–30 (first quote quoting Ex. 1007, 17 (“More than 10^5 [100,000] interconnections per chip form in a vertical direction. . . . Vertical interconnections enable large data bandwidth in vertical data transfer.”); citing Ex. 1001, 2:41–46 (disclosing placing contacts “throughout the total area of the various die rather than just around their periphery” to obtain “many more connections between the die”), 2:65–3:2 (similar); Ex. 1002 ¶ 92)).

Dr. Shanfield credibly testifies that Koyanagi’s stacked die module, which supplies a “large data bandwidth in vertical data transfer,” mimics the ’951 patent’s wide configuration data port. *See* Ex. 1002 ¶¶ 90–93.¹⁶ A large data bandwidth functionally represents a relatively large parallel

¹⁶ A large data bandwidth based on the numerous vias is another way of describing a relatively large parallel transfer of data using the vias distributed throughout the dies to provide the claimed data acceleration. *See* Ex. 1002 ¶¶ 90–93 (citing Ex. 1007, 17 (“Vertical interconnections enable large data bandwidth in vertical data transfer.”); Ex. 1007, 17 (“2D image signals move simultaneously in a vertical direction and are processed in parallel within each LSI [large-scale integration] layer. As a result, using 3D-image-processing LSIs leads to a dramatic processing speed improvement of more than three orders of magnitude.”); Pet. 4 (showing that “expected advantages of 3D stacks of chips are ‘high packing density,’ ‘high speed,’ ‘parallel signal processing,’ and ‘integration of many functions on a single chip’” (quoting Ex. 1010, 1704). Dr. Chakrabarty similarly testifies that a large “number of connections . . . obtained through TSVs[] accelerate the data transfer,” “acceleration is essentially how much bandwidth you’re getting” and “bandwidth is a product of the bit width and the transfer rate.” Ex. 1035, 270:7–11, 274:6–10. He also agrees that, assuming the same clock transfer rate in the systems of Figures 3 and 5, the “wide configuration data port as in Figure 5 accelerates external memory references compared to what’s in Figure 3.” *Id.* at 274:11–17.

transfer of data using numerous vias distributed throughout the dies to provide the claimed data acceleration. *See supra* notes 14, 16; Ex. 1002 ¶¶ 90–93; Ex. 1007, 17 (quoted above); Pet. 4 (showing that “expected advantages of 3D stacks of chips are ‘high packing density,’ ‘high speed,’ ‘parallel signal processing,’ and ‘integration of many functions on a single chip’” (quoting Ex. 1010, 1704)).

Patent Owner relies on its claim construction of “a memory array functional to accelerate external memory references to the processing element” as “a memory array that allows the parallel loading of data through *buffer cells*.” PO Resp. 14 (citing Ex. 2015 ¶¶ 50–52). Based on this proposed claim construction, Patent Owner asserts that the combination of Koyanagi and Alexander “does not teach or suggest a memory array functional to accelerate external memory references to the processing element” as recited in claims 1, 5, and 10. *See id.* As Petitioner contends, however, this argument fails because the challenged claims do not require buffer cells to support the accelerate function in the challenged claims. *See* Reply 11–12; *supra* § II.C (Claim Construction). As explained above, and contrary to Patent Owner’s argument, the ’951 patent does not describe the buffer cells as “necessary for the memory array to accelerate memory references to the processing element.” *See id.* at 16 (citing Ex. 2015 ¶ 52); *supra* § II.C (Claim Construction).

As Petitioner argues, the combined Koyanagi and Alexander system mimics the ’951 patent’s disclosure by employing stacked dies with a “large number of contact points distributed throughout the surfaces of the dies.” Pet. 29; *see also supra* notes 14, 16. Petitioner also provides evidence that an artisan of ordinary skill would have known of several advantages in

stacking 3D chips with multiple vias including “high packing density,” “high speed,” “parallel signal processing,” and “integration of many functions on a single chip.” *Id.* at 4 (citing Ex. 1010, 1704; Ex. 1002 ¶ 39). Petitioner points to Koyanagi’s “key benefit” as “enab[ling] large data bandwidth in vertical data transfers” (Ex. 1007, 17) to mitigate bus bottlenecks, further showing that multiple vias provide for parallel signal processing and increased processing speed in stacked dies as found above. *See* Pet. 30 (citing Ex. 1007, 17, 19); *supra* § II.C (Claim Construction); *supra* notes 14, 16. In other words, Petitioner shows how the combined teachings of Koyanagi and Alexander teach or suggest to an artisan of ordinary skill the accelerate clause in the challenged claims by providing a large number of short parallel via connections, thereby functionally enabling large data bandwidths and parallel processing, as was well-known at the time of the invention. *See* Pet. 4, 17–23, 28–29; Ex. 1007, 17–18; *supra* notes 14, 16; Reply 15–17; *In re Graves*, 69, F.3d 1147, 1152 (Fed. Cir. 1995) (holding that “Rockwell . . . anticipates claim 4, even if it does not specifically disclose simultaneous monitoring of the output points, if simultaneous or parallel monitoring is within the knowledge of a skilled artisan”).

Patent Owner also contends that “[a] POSITA would not have been motivated to combine *Koyanagi* with *Alexander* because neither *Koyanagi* nor *Alexander* disclose how to combine a programmable array, a microprocessor, and a memory die into a 3D IC, which would take undue experimentation to perform without using the ’951 Patent as a roadmap.” PO Resp. 18. According to Patent Owner, “[a] POSITA would understand that figuring out *how* to combine an FPGA, microprocessor, and memory into a 3D integrated circuit that accelerates memory references to the FPGA

would require undue experimentation.” *Id.* at 19. Patent Owner also contends that “Petitioner fails to demonstrate not only why a POSITA would have ignored . . . known thermal issues, but also how the POSITA would modify Koyanagi’s 3D multichip module with Alexander’s FPGAs considering the well-established 3D FPGA thermal issues.” *Id.* at 26–27. Further addressing “how,” Patent Owner contends that “the ’951 Patent describes that the configuration of the *buffer cells* in the memory array that accelerate the speed at which data travels to the programmable array.” *Id.* at 24 (emphasis added). According further to Patent Owner, “the ’951 Patent greatly improved upon FPGA reconfiguration time, which conventionally took ‘millions of processor clock cycles to complete the reconfiguration.’” *Id.* (quoting Ex. 1001, 1:52–57). And “[t]his improvement . . . illustrates that Petitioner trivializes these challenges to make its fallacious obviousness argument.” *Id.*

These claim construction arguments that rely on “buffer cells” fail for the reasons noted above, the challenged claims do not require buffer cells. *See supra* § II.C (Claim Construction). As summarized above, the ’951 patent describes in its abstract and other places, including in reference to Figure 4, providing accelerated data transfers and reconfiguration without buffer cells by using numerous short vias to connect circuits in the stacked dies. *See id.* As outlined above, Petitioner provides ample motivation supported by the record as to “how and why” an artisan of ordinary skill would have combined the stacked die features of Koyanagi with the similar features of Alexander, to include the well-known FGPA, and it shows how the vertical interconnections employed in both references track the disclosed invention to obtain the claimed acceleration. *See, e.g.,* Pet. 29 (annotating

Koyanagi's Figure 1). Wiring similar well-known circuits with short conductive vias instead of long conventional conductors would have been obvious and well-within the ordinary skill of an artisan, motivated by many reasons (for example, speed/bandwidth gains, compactness, power consumption, FPGA design flexibility) as the Petition shows and as Koyanagi and Alexander suggest as discussed above. *See, e.g.*, Ex. 1006, Abstract (describing a "fabrication technology" and "expected manufacturing yield"), 1 (describing "10,000 solder bumps" "to establish the vertical interconnections" and "enabling electrical interconnections between the two sides of the die," by "adapting multi-chip module (MCM) fabrication technology"); Ex. 1007, 17 (similarly describing MCM technology and using 10,000 (10^5) "interconnections per chip" to make 3D MCMs "fabricated using our new integration technology"), Fig. 6 (showing "Fabrication sequence of 3D LSI").

Petitioner persuasively shows, and Patent Owner agrees, that "Alexander teaches stacking FPGA dies" and "Koyanagi teaches stacking different types of bare dies using TSVs to form 3D multi-chip modules." *See* Reply 15 (citing PO Resp. 9–11 (describing the teachings of Koyanagi and Alexander); Ex. 1035, 55:17–20; 310:15–311:14; 314:2–5)); PO Resp. 25 ("Alexander proposed stacking several portions of a 2D FPGA to form a single 3D FPGA.") At the cited deposition pages, Petitioner quotes Dr. Chakrabarty as admitting that "Koyanagi teaches '3D integration of different types of dies using TSV technology' (*id.* (quoting Ex. 1035, 55:17–20)), and that "Koyanagi has been recognized [as one of] the earliest papers that demonstrated the reliability of 3D stacking through silicon vias" (*id.* (quoting Ex. 1035, 55:17–20)). Patent Owner's argument that "Alexander

only teaches a single 3D FPGA” simply glosses over Alexander’s teaching of “stacking together a number of 2D FPGA bare dies” to form the 3D FPGA. *See* PO Resp. 20 (quoting Ex. 1006, 1). In other words, Alexander does not restrict stacking a 2D FPGA die to other 2D FPGA dies, even if it teaches stacking such dies and connecting each array together to form a 3D FPGA. Moreover, the challenged claims do preclude multiple layers of 2D FPGAs (i.e., a 3D FPGA) in the stack.

To support its “undue experimentation” argument, Patent Owner contends that Petitioner “slaps *Koyanagi* and *Alexander* together” and quotes Dr. Shanfield as testifying that “*you don’t just slap [circuits or modules] together without worrying about what connects to what.*” PO Resp. 20 (emphasis by Patent Owner) (quoting Ex. 2014, 81:21–82:19). Patent Owner also argues that “*how* to combine an FPGA, microprocessor, and memory into a 3D integrated circuit that accelerates memory references to the FPGA would require undue experimentation.” *See* PO Resp. 19. Patent Owner also asserts that “Petitioner’s alleged combination of *Koyanagi*’s 3D integration of memory chip layers with *Alexander*’s FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined device inoperable.” *Id.* at 30 (citing Ex. 2015 ¶ 71). Patent Owner presents a number of arguments that track the arguments outlined above and relate to asserted technical challenges based on heat dissipation and (as addressed above) an alleged failure by Petitioner to show “how to combine a programmable array, a microprocessor, and a memory die into a 3D IC” (*id.* at 18). *See* PO Resp. 14–30.

“In order to render a claimed invention obvious, the prior art as a whole must enable one skilled in the art to make and use the apparatus or method.” *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1289, 1297 (Fed. Cir. 2010), *vacated on other grounds*, 374 F. App’x 35 (2010), *reinstated in part*, 649 F.3d 1276, 1296 (2013) (en banc) (reinstating obviousness portion of *Therasense*); *see also In re Kumar*, 418 F.3d 1361, 1368 (Fed. Cir. 2005) (similar holding in the context of examination). However, any “suggestion that [Koyanagi] and [Alexander] are non-enabled is misplaced, since even ‘[a] non-enabling reference may qualify as prior art for the purpose of determining obviousness,’ *Symbol Tech., Inc. v. Opticon, Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991), and even ‘an inoperative device . . . is prior art for all that it teaches,’ *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989).” *ABT Sys., LLC v. Emerson Elec. Co.*, 797 F.3d 1350, 1360 n.2 (Fed. Cir. 2015)). Moreover, Koyanagi and Alexander, as prior art references, carry a presumption of enablement. *See In re Antor Media*, 689 F.3d 1282, 1287–1288 (Fed. Cir. 2012); *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003); *Apple Inc. v. Corephotonics, Ltd.*, No. 2020-1438, 2021 WL 2577597, at *4 (Fed. Cir. June 23, 2021) (nonprecedential) (holding that in the context of AIA trial proceedings, “regardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art” and that “[i]t was error for the Board to suggest otherwise”).¹⁷

¹⁷ Petitioner carries the ultimate burden of showing obviousness. *Corephotonics*, No. 2020-1438, 2021 WL 2577597, at *4 states that “the patentee/applicant has the burden to prove non-enablement for . . . prior art” in an anticipation context. *Corephotonics* suggests but does not specify the

Moreover, Dr. Shanfield's deposition testimony relied upon by Patent Owner does not support Patent Owner's argument that combining the teachings of Koyanagi and Alexander to arrive at the claimed processor module requires "undue experimentation." In the passage that includes the quoted testimony that Patent Owner relies upon, Dr. Shanfield testifies as follows (about another reference of record, Bertin (Ex. 1009)):

You have obviously got to have a circuit in mind that you're wanting to create a system-level circuit, a module-level circuit; and so you're going to need to consider which connections you want a TSV connecting to something below.

So you don't just slap it together without worrying about what connects to what.

On the other hand, the putting together of the -- in Bertin, he describes the putting together of these chips and how that can be done in detail. And that piece of it is -- I guess you could characterize that as something that comes with the process and in itself isn't something you think specifically about every one of 50,000 connections. They're all done by the process that he gives an example of.

Ex. 2014, 82:4–19.

Dr. Shanfield's deposition testimony does not indicate that Petitioner "slaps *Koyanagi* and *Alexander* together without worrying about what connects to what. . . . to arrive at the claimed '3D integrated circuit' or that arriving at the claimed invention would have required "undue experimentation." *See* PO Resp. 19–20. Rather, Dr. Shanfield's deposition testimony indicates that an artisan of ordinary skill readily would have been

contours of the enablement burden in an obviousness context in an AIA proceeding. In any event, regardless of which party carries the burden on enablement, Petitioner shows that there is no undue experimentation in arriving at the claim invention, as summarized below.

able to connect different die circuits together “obviously” with “a circuit in mind . . . to create a system-level circuit, [or] a module-level circuit . . . consider[ing] which [TSV] connections [she] want[s].” *See id.* As Petitioner argues, “[n]othing in Dr. Shanfield’s testimony, however, suggests that Petitioner ‘slap[ped] together’ Koyanagi and Alexander.” Reply 14; *see* Ex. 1030 ¶ 84 (testifying that Patent Owner quotes his (Dr. Shanfield’s) deposition testimony “out of context,” and “at the system or circuit design level, each TSV is designed as an interconnection between specific circuits” and “a TSV that is part of a configuration data port of an FPGA interconnects memory and FPGA circuits located respectively in a memory die and an FPGA die”).

As Petitioner also argues and as summarized above, the Petition “provide[s] a detailed explanation of *how* Koyanagi and Alexander would have been combined to disclose each limitation of the Challenged Claims and *why* a POSITA would have been motivated to combine them—‘to create a 3D reconfigurable processor module with improved performance and area-efficiency.’” Reply 16 (quoting Pet. 17). By way of example, Petitioner’s annotated Figure 1M, which represents combined teachings of Koyanagi and Alexander, shows how to connect the dies together using conductive vias as challenged claim 1 requires. Petitioner also provides persuasive detail with respect to the remaining challenged claims at issue in this section (i.e., claims 4, 5, 8, 10, 13–15). *See* Pet. 31–46. By teaching similar stacking techniques for similar circuits including the use of conductive vias with logic dies including FPGAs, memory, and microprocessors, Koyanagi and Alexander collectively evidence a reasonable expectation of success without undue experimentation in arriving at the claimed invention. *See Otsuka*

Pharm. Co., v. Sandoz, Inc., 678 F.3d 1280, 1296 (Fed. Cir. 2012) (“The inventor’s own path itself never leads to a conclusion of obviousness; that is hindsight. What matters is the path that the person of ordinary skill in the art would have followed, as evidenced by the pertinent prior art.”). In other words, Petitioner shows that the claimed invention involves a routine combination of familiar elements to yield predictable results, namely combining Alexander’s known 2D-FPGA die with Koyanagi’s similar die stack, or simply substituting Alexander’s known 2D-FPGA die in place of a similar DRAM memory die in the die stack of Koyanagi, with the coupled circuits functioning with processing speed gains and other benefits as expected. *See* Pet. 27–29; Reply 14 (citing *KSR*, 550 U.S. at 416 (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”))).

In its Sur-reply, Patent Owner argues that “Koyanagi does not explain how its TSVs would work with a 3D FPGA architecture, which includes configuration memory, configuration logic cells, and programmable switch blocks.” Sur-reply 8. This argument is not commensurate in scope with the broadly challenged claims, which do not require “configuration memory, configuration logic cells, and programmable switch blocks.” To the extent the claimed programmable array implies logic cells, Alexander discloses a “logic block” with “six immediate neighbors . . . as opposed to four in the 2D case.” Ex. 1006, 1, Fig. 1a (depicting logic cells of the array of a 2D FPGA connected in parallel to those of another 2D FPGA and “enabl[ing] each channel segment to connect to some subset of the channel segments incident on the other five faces of the 3D switch block”); *see* Pet. 12–13, 18–

19 (relying on Alexander’s FPGAs and providing reasons for employing same including flexibility).

The ’951 patent does not provide any more specific detail with respect to stacking processor, memory, and FPGA dies to obtain the claimed acceleration using conductive vias than Koyanagi, Alexander, or the combined teachings of the references as set forth by the Petition. *Compare* Ex. 1001, Fig 4 (illustrating a die package comprising an FPGA die, memory die, and processor die, with generic “CONTACT POINTS” on each die), *with* Ex. 1006, Fig. 2 (similar); Ex. 1007, Fig. 1a (similar), *and supra* Fig. 1M (similar). Figure 5 of the ’951 patent does not portray any specific via connections between the *three* circuit dies in Figure 4 and the well-known wide data port and simply provides a “functional block diagram” without describing any electrical connections to microprocessor 64.¹⁸ *See* Ex. 1035, 157:3–17, 158:10–12 (agreeing that “memory die 66” is “to the left of the very wide configuration data port 82 in Figure 5, although not shown” and the “connections” shown in Figure 5 “are formed by the TSVs that are between the memory die [not shown in Figure 5] and the FPGA die” “to the right of Figure 5”), 163:14–17 (testifying that “[c]onfiguration data port . . . is a well-known term” and agreeing that “that’s just a data port used for configuration, basically”). That the “very wide configuration data port” 84 in Figure 5 is merely a box without any description in the ’951 patent

¹⁸ Figure 5 purports to illustrate “functional block diagram” that includes a wide configuration data port and applies to an embodiment of Figure 4 for implementing a “total reconfigur[ation] in one clock cycle by updating all of the configuration cells in parallel.” *See* Ex. 1001, 5:29–32, Fig. 5. But the challenged claims do not require the one clock cycle reconfiguration feature as discussed above. *See supra* § II.C (Claim Construction).

specification signifies that the inventors of the '951 patent considered its structure and function to be well-known.

As Petitioner argues, “Figure 1M illustrates how a POSITA would have understood Koyanagi and Alexander would be combined” Reply 17. Similarly, regarding thermal considerations, Petitioner persuasively argues that “the '951 patent is devoid of discussion of thermal considerations,” and it “simply asserts that stacking dies reduces power consumption, which was a well-known fact in the art.” *Id.* at 18 (citing Ex. 1001, 5:51–53; Ex. 1002 ¶ 78; Ex. 1010, 1712–13)).¹⁹

The lack of specific circuit connection detail in the '951 patent, Koyanagi, and Alexander reveals that an artisan of ordinary skill would have required minimal experimentation, direction, and guidance to obtain the broadly claimed invention in the relatively predictable art of stacked integrated circuit dies to obtain an operable “processor module” as claimed with a reasonable expectation of success. Also, as the Petition asserts, the '951 patent shows, by way of block diagram of admitted prior art Figure 1, that artisans of ordinary skill readily knew how to electrically connect a microprocessor, system memory, and an FPGA together. *See* Pet. 5 (“[T]he patent admits that it was well-known in the art to combine FPGAs (red), microprocessors (blue), and memory (tan) to form a reconfigurable processor system, as is depicted in Figure 1 (‘APA Figure 1’) of the '951 Patent below.”), 6 (annotating prior art Fig. 1 of the '951 patent). Similarly,

¹⁹ The cited pages of Akasaka (Ex. 1010) support Petitioner by stating that “[t]he first step in 3-D system design . . . begin[s] with the integration of conventional functions already realized in 2-D devices,” which results in “miniaturization, *low power consumption*, and large-scale integration.” Ex. 1010, 1712–13 (emphasis added).

Alexander indicates, by describing its 3D “(re)programmable” FPGAs (Ex. 1006, 253), that an artisan of ordinary skill would have known how to connect well-known circuit dies together using conductive vias for parallel processing as Koyanagi also teaches, instead of using long runs implied by APA Figure 1 of the ’951 patent. *See supra*

§§ II.D.1, II.D.2, note 19 (Akasaka teaching that “[t]he first step in 3-D system design . . . begin[s] with the integration of conventional functions already realized in 2-D devices”); Pet. 19–20 (showing how the “high density vertical interconnection scheme” in Alexander and Koyanagi teaches eliminating long circuit runs in the prior art).

Petitioner explains that Dr. Chakrabarty “admits that a ‘logic chip’ as disclosed in Koyanagi (Ex. 1007, 17) may be an FPGA.” Reply 15 (citing Ex. 1035, 129:2–7 (admitting that logic includes an FPGA), 86:20–87:10 (same), 220:20–24 (same); Ex. 1030 ¶¶ 35–36).²⁰ Petitioner further contends that “Koyanagi explains that the use of TSVs allows forming a very large number (in the order of 100,000) of short vertical interconnects, which ‘dramatically increase[s] wiring connectivity while reducing the number of long interconnections.’” *Id.* (quoting Ex. 1007, 17; citing Pet. 13; Ex. 1035, 254:18–21 (admitting that Koyanagi teaches “hundreds of thousands of TSVs”), 247:3–9 (same); Ex. 1030 ¶¶ 35–36). As noted above,

²⁰ Koyanagi refers to a 3D MLM (merged logic memory) LSI (large scale integration) die stack with respect to Figure 1a, which portrays microprocessor (logic) dies stacked with DRAM (memory) dies. Ex. 1007, 17–18, Fig. 1a. In other words, logic as disclosed in Koyanagi includes a microprocessor, and Dr. Chakrabarty and Dr. Shanfield agree that a logic chip generally signifies logic chips such as microprocessors, ASICs, and FPGAs, as a limited class of processing chips known to one of ordinary skill in the art. *See* Ex. 1030 ¶ 36 (citing Ex. 1035, 129:2–7).

in addition to saving area, reducing power consumption, and generally improving performance by stacking dies with TSVs, Petitioner explains that the

high density vertical interconnection scheme—which uses through-silicon contacts that are orders of magnitude more abundant *and* orders of magnitude shorter than circuit board wirings in conventional 2D layout—“dramatically increase[s] wiring connectivity while reducing the number of long interconnections” and significantly improves system speed; in particular, it provides fast memory access and thus serves to “accelerate” external memory references.

Pet. 19–20 (first quotation quoting Ex. 1007, 17; citing *id.* at 19; Ex. 1002 ¶ 93).

In other words, as Petitioner persuasively shows, the prior art of record, including Koyanagi and Alexander, provides well-known benefits and reasons for stacking different types of chips together using conductive vias, including logic chips that include FPGAs, thereby suggesting in combination with Alexander how to form an operable processor module as claim 1 recites with a reasonable expectation of success and without undue experimentation. *See* Pet. 4, 17–23; Reply 11–20.

In Patent Owner’s Sur-reply, Patent Owner argues that Koyanagi relies on CAD tools, and that Dr. Shanfield relies on this disclosure for “*providing* evidence of a reasonable expectation of success,” but “Dr. Shanfield cannot and does not establish that the use of CAD tools when attempting to combine Koyanagi and Alexander would result in the claimed invention.” Sur-reply 8 (citing Ex. 2017, 20:3–6, 24:22–25:7; Ex. 1007, 17). Based on these assertions, Patent Owner contends that “Dr. Shanfield does not demonstrate that any CAD tools would have resulted in ‘a memory array functional to accelerate external memory references to the processing

element’ as opposed to any other possible interconnection scheme.” *Id.* Patent Owner’s Sur-reply arguments, Dr. Shanfield’s testimony, Koyanagi, and Alexander, all show that artisans of ordinary skill would have been able to use routine tools available at the time of the invention, such as CAD tools, and motivated to use them as an aid to establish the desired connections between circuits. *See* Ex. 1007, 17 (“A powerful CAD tool proves indispensable for 3D LSI design, specifically for 3D wiring routing because combining 2D multilevel metallization with vertical interconnections forms this complicated 3D wiring.”); Ex. 2017, 20:3–6 (agreeing that it is “a fair understanding that an engineer, when designing 3D architecture, would use some sort of CAD tool in designing the circuitry”), 24:6–21 (testifying that “CAD tools are always used for routing in the design and manufacture of integrated circuits,” and “the engineering connected with CAD has been resolved in [Alexander’s] description for his particular approach, and he’s just simply explaining to the person skilled in the art reading this that this is how he did it, and this is what worked well for him” (discussing “Section 6 of Alexander”)). In Section 6, Alexander describes the CAD-based “framework” as “enabl[ing] the use of a wide variety of graph-search algorithms to construct routing solutions, and works quite well in practice.” Ex. 1006, 4 (citing several documents for “3D FPGA routing”). In other words, the record shows that an artisan of ordinary skill would have readily been able and motivated to use routine tools to route connections vertically in stacked chips. Moreover, the ’951 patent does not mention using CAD tools, indicating either that such tools were not needed for the invention or that they were so well-known that mentioning them was not important for purposes of describing the invention.

Patent Owner also argues that “[b]ecause of the power consumption by FPGAs, and other logic dies, and the resulting thermal issues, a POSITA would not have found it obvious to stack a programmable array, such as an FPGA, with other die[s], let alone a microprocessor.” PO Resp. 28 (citing Ex. 2015 ¶ 69). As noted above, Dr. Chakrabarty admits that Koyanagi discloses a logic chip and an FPGA is a logic chip. Reply 15 (citing Ex. 1007, 17; Ex. 1035, 129:2–7, 86:20–87:10, 220:20–24; Ex. 1030 ¶¶ 35–36). Patent Owner argues that FPGAs and other logic chips, such as microprocessors, consume the same (or similar) amount(s) of power. *See* PO Resp. 34 (“Because of the power consumption by FPGAs, *and other logic dies*, and the resulting thermal issues” (emphasis added)); Ex. 1035, 116:11–117:5 (Dr. Chakrabarty testifying that he did not analyze or cite articles comparing power consumption of microprocessors, programmable arrays, and FPGAs).

Contrary to Patent Owner’s arguments, as Petitioner shows, Alexander, a presumptively enabled prior art reference, discloses stacking multiple 2D FPGAs (logic chips) together with solutions to any thermal issues, contradicting Patent Owner’s arguments that multiple logic chips present an inoperable device or insurmountable thermal problems or otherwise would have been unobvious. *See* Pet. 19–22 & n. 6 (discussing power and heat considerations, showing a reasonable expectation of success in stacking different dies, and also noting that Koyanagi stacks different types of dies together) (citing Ex. 1006, 1; Ex. 1007, 17; Ex. 1002 ¶¶ 79–81); Reply 19 (arguing that “Alexander also lists conventional thermal-reduction techniques that are also applicable to 3D FPGAs, such as the use of ‘thermal bumps and pillars’ (illustrated below in Figure 2(b)) as

heat removing pipes—similar to the express teachings of both Koyanagi and Bertin”) (citing Ex. 1006, 3; 1007, 17; Ex. 1009, 2:61–65; Ex. 1030 ¶ 60).

The thrust of Patent Owner’s thermal challenge arguments rests on the well-known principle that increasing power consumption increases heat generation. *See* PO Resp. 27–28; Reply 16–17 (“**Koyanagi** explicitly teaches that using TSVs in 3D ICs reduces power consumption and improves heat removal (because TSVs also serve as heat pipes)”); Ex. 1006, 3 (“As the power-to-area/volume increases, *so does the operating temperature unless heat can be effectively dissipated*) (emphasis added). For example, Patent Owner explains that FPGAs consume substantially more dynamic power than DRAMs resulting in significantly higher temperatures and corresponding heat dissipation problems. PO Resp. 28.

However, as Petitioner argues and as Dr. Chakrabarty confirms, using many short vertical conductive vias (e.g., TSVs) versus long conductive runs “reduces power consumption and improves heat removal (because TSVs also serve as heat pipes).” Reply 17 (citing Ex. 1007, 17). In other words, Dr. Chakrabarty acknowledges that

[w]hat Koyanagi says *is actually obvious* to anybody who is skilled in the art. *Anybody who is skilled in the art would know that via is conductive. It is a conductor for both electricity and for heat. And therefore, if you have lots of vias, you’re going to take out the heat.*

Ex. 1035, 256:9–15 (emphasis added); *see* Reply 17 (partially quoting Ex. 1035, 256:9–15). Therefore, as Petitioner persuasively argues, rather than ignoring thermal issues or deterring a person of skill in the art from combining Koyanagi and Alexander, “a POSITA would have been motivated to find a solution to the alleged thermal issues, and would have

recognized that a large number of 3D interconnections between dies contribute to such a solution.” *See* Reply 21 (citing Ex. 1030 ¶ 53).

Patent Owner also argues that “the power consumption needs of FPGAs, as well as other logic dies, as opposed to memory, were far greater as they are driven by dynamic power that is based upon the specific use of each resource and is a function of the signals toggling and capacitive loads charging and discharging.” PO Resp. 27–28 (citing Ex. 2012, 1; Ex. 2013, 4; Ex. 2015 ¶ 68). To support this argument, Patent Owner states that “*Alexander*[] notes that a large portion of the power consumption is due to driving I/O buffers.” *Id.* at 28 (citing Ex. 1006, 4). Patent Owner adds that the FPGA “use of I/O pins impact[s] the total power requirements since ‘considerations like I/O standards used and data rates expected determine how fast the I/Os toggle and how fast the logic must be clocked.’” *Id.* (quoting Ex. 2012, 1; citing Ex. 1035 ¶ 68). Patent Owner also asserts that “while *Alexander* proposed a 3D FPGA, the authors admitted that it could not fabricate its proposed design.” *Id.* at 25 (citing Ex. 1006, 4). Advancing similar arguments, Patent Owner concludes that “Petitioner’s contention that it would be obvious to try stacking *Alexander*’s FPGAs on *Koyanagi*’s 3D multichip module crumbles under the weight of contradictory evidence.” *Id.* at 30.

This line of argument fails because *Koyanagi* and *Alexander* individually and collectively teach ready solutions to any heat challenges in stacking “different types of bare dies using TSVs to form 3D multi-chip modules” and “*Alexander* teaches stacking FPGA dies.” *See* Reply 15, 19 (referencing *Alexander*’s conventional thermal-reduction techniques including “thermal bumps and pillars” as similar to *Koyanagi*’s heat pipe

and/or via teachings (quoting Ex. 1006, 3; citing Ex. 1007, 17)). No reasonable dispute exists on this record over the fact that using a sufficient number of conductive vias solves any heat problems in stacked dies that include one or more logic dies. *See id.* at 17 (arguing that Koyanagi “solv[es] any heat problem by forming ‘as many vertical interconnections as possible’ because they ‘remove the generated heat’” and that “Dr. Chakrabarty admitted this”) (quoting Ex. 1007, 17; citing Ex. 1035, 290:4–7) (agreeing that “Koyanagi teaches using a lot of these TSVs” “[a]s a way to removing heat”)). In addition to Koyanagi’s solution for addressing thermal issues, Petitioner persuasively notes that “Alexander points out that 3D integration ‘using MCM technology’ advantageously eliminates input and output buffers where ‘a large portion of the total power is expended,’ and thus 3D stacking of FPGAs ‘tends to significantly reduce power consumption.’” Reply 19 (quoting Ex. 1006, 4).²¹

Given that, similar to Koyanagi, Alexander specifically describes “[a] number of thermal-reduction techniques” as including “thermal bumps in pillars” (Ex. 1006, 3), whether Alexander’s authors actually manufactured the disclosed die stack is not determinative. *See* Reply 19 (citing *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (stating that “no ‘actual creation or reduction to practice’ is required” for a prior art reference to anticipate claims (quoting *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1380–81 (Fed. Cir. 2003))). Also, as noted above, Alexander is presumed to be enabled for what it teaches, *see Antor Media*, 689 F.3d at 1287–1288, *Amgen Inc.*, 314 F.3d at 1355; *Corephotonics*, 2021 WL

²¹ An “MCM” is a “multi-chip module.” Ex. 1006, 1.

2577597, at *4, namely a die stack of interconnected 2D FPGAs with through-vias that reduce “interconnect delay” and provide “shorter signal propagation delay,” wherein the disclosed “3D FPGAs have good implications with respect to power consumption.” Ex. 1006, 1.

Therefore, contrary to Patent Owner’s arguments, part of Alexander’s chip stacking solution involves using known thermal reduction techniques (e.g., such as conductive vias as Koyanagi describes and/or thermal bumps and pillars as Alexander describes) with the added option of eliminating I/O buffers and any heat generating switching associated therewith. *See* Ex. 1006, 4 (“[W]hen chips are interconnected using MCM technology, such I/O buffers are often unnecessary, which tends to significantly reduce the power consumption.”). Finally, the challenged claims here do not require I/O buffers (or clocking, driving, or switching thereof).

Furthermore, as Petitioner also argues, not only does Koyanagi and Alexander’s method individually or collectively solve heat problems using “a huge number” of short vias in stacked dies, this “high density vertical interconnection scheme” with vias “orders of magnitude shorter than circuit board wirings in conventional 2D layout” “significantly improves system speed” by decreasing the interconnect delay to accelerate external memory references. Pet. 30 (citing Ex. 1002 ¶¶ 92–93; Ex. 1007, 17, 19). This resulting speed increase provides further motivation for the combination as proposed by Petitioner.

Based on the foregoing discussion and a review of the record, including Patent Owner’s evidence and arguments as presented in the Response and Sur-reply as summarized above, Petitioner persuasively shows that the combination of Koyanagi and Alexander would have rendered claim

1 obvious. Relying partly on its showing with respect to claim 1, Petitioner provides a similar and persuasive showing for independent claims 5 and 10, which largely track the limitations recited in claim 1. *See* Pet. 31–44.

Claim 4 depends from claim 1 and recites an “electrically coupled “third integrated circuit.” Claim 8 depends from claim 5 and recites a similar limitation. Claim 13 depends from claim 10 and recites that the “memory” comprises a “memory array.” Claim 14 depends from claim 10 and recites that the “programmable array” is “reconfigurable.” Claim 15 depends from claim 10 and recites that the three “integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements.” The Petition shows that Koyanagi discloses these well-known circuit elements or that the recitations thereof amount to combining “familiar elements according to known methods . . . [to] yield predictable results.” *See KSR*, 550 U.S. at 416; Pet. 31, 36–37, 45–46. In summary, the Petition presents a persuasive showing supported by the record with respect to dependent claims 4, 8, 13, 14, and 15. *See id.* at 31, 36–37, 45–46. Patent Owner does not address claims 4, 5, 8, 10, 13, 14, and 15 separately from claim 1. *See* PO Resp. 14–30.

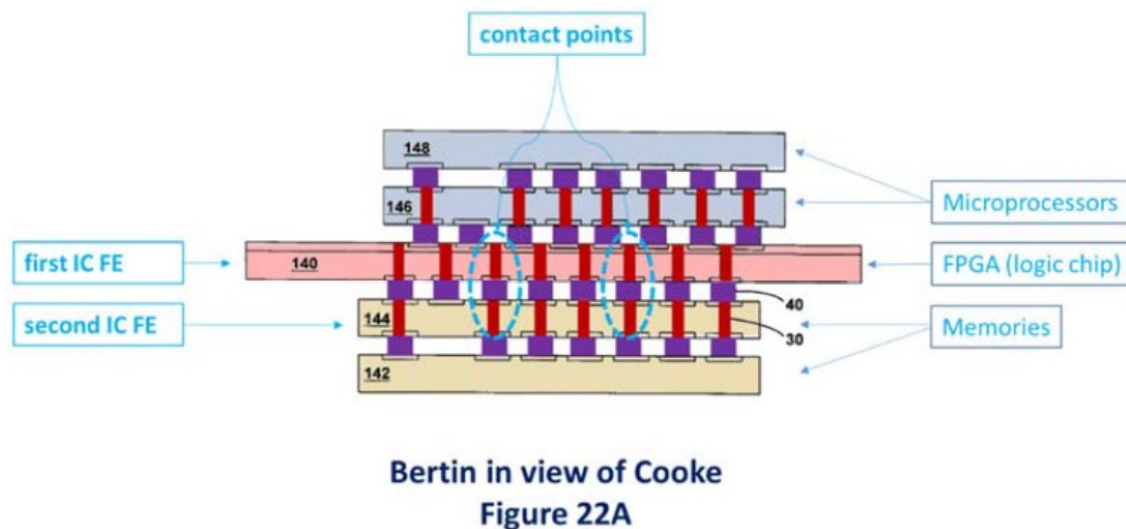
Accordingly, based on the record and as summarized above, Petitioner establishes by a preponderance of evidence that claims 1, 4, 5, 8, 10, and 13–15 would have been obvious.

E. Obviousness, Bertin and Cooke, Claims 1, 4, 5, 8, 10, and 13–15

Petitioner contends claims 1, 4, 5, 8, 10, and 13–15 would have been obvious over the combination of Bertin and Cooke. *See* Pet. 46–61. Similar to Koyanagi, Bertin teaches stacking different types of chips, including logic

chips, microprocessors, and controllers to minimize latency and maximize bandwidth and heat dissipation, using through-chip conductors (vias). *See id.* at 47 (citing Ex. 1009, 1:20–27, 6:49–51, 7:16–34; Ex. 1002 ¶¶ 118–120).

Petitioner’s “Annotated Figure 22A,” which represents how Petitioner combines relevant teachings of Bertin and Cooke (Pet. 53), follows:



Annotated Figure 22A above represents the combined teachings of Bertin and Cooke, showing Cooke’s FPGA in place of logic chip 140 in Bertin’s stacked system, which includes Bertin’s first (140) and second (146) dies, memory dies (144, 142), microprocessor dies (146, 148), and logic die (140), and contact portions (red) extending through the various dies, including the claimed first and second die. *See* Pet. 50–52 (citing Ex. 1009, 7:16–34 (describing stacking a logic chip with other chips in Figure 22), Fig. 22; Ex. 1002 ¶¶ 127–128; Ex. 1008, 2:58–60 (describing “DP-FPGA” that include arithmetic logic units or ALUs), Figure 1 (depicting DP-FPGA blocks), 1:48–64 (describing “reconfigurable computing” by loading a “specific hardware logic function” into an FPGA at one point and replacing it later).

In other words, Bertin does not disclose an FPGA but discloses logic chip or processor 140 in the middle or bottom of a “stack of chips” such as the chip stacks of Figures 21 and 22, respectively. Ex. 1009, 7:16–42. Petitioner relies on Bertin’s chip stacks in general and Cooke’s description of FPGAs, microprocessors, and memory planes in a similar chip or die stack. See Pet. 46–52 (citing Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1009, 6:49–51; Ex. 1002 ¶¶ 118–120). Petitioner contends that it would have been obvious to use Cooke’s FPGAs in Bertin’s 3D stacks to minimize latency, maximize bandwidth, and improve packing densities, heat efficiency, heat dissipation, and speed by avoiding interconnect delays. *Id.* at 46–50 (citing Ex. 1006, 1; Ex. 1009, 1:20–57, 2:61–65, 7:16–34; Ex. 1002 ¶¶ 119–120). Petitioner also reads the claim limitations of the remaining challenged claims on to the combined teachings of Bertin and Cooke, providing a detailed showing, supported by the references and expert testimony. See *id.* at 58–71.

Patent Owner challenges Petitioner’s showing. PO Resp. 30–44. Patent Owner advances similar arguments to those addressed above with respect to the combined teachings of Koyanagi and Alexander. For example, Patent Owner argues that “[a] POSITA would understand that figuring out **how** to combine an FPGA, memory, and microprocessor into a 3D integrated circuit would require undue experimentation.” *Id.* at 35. To support this “undue experimentation”/“how to” argument, Patent Owner relies on the same testimony by Dr. Shanfield addressed above that “you don’t just slap [circuits] together without worrying about what connects to what.” *Id.* at 36 (quoting Ex. 2014, 81:21–82:19). Contrary to this argument, however, Dr. Shanfield’s testimony does not support Patent

Owner for reasons similar to those explained above—i.e., Petitioner and Dr. Shanfield do not propose simply “slap[ping] together” the combined teachings. Rather, Petitioner provides a detailed mapping showing how to combine the references with factual underpinnings and rationale supported by the record, as summarized above and as exemplified by Annotated Figure 22A. *See* Pet. 46–52 (citing Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1009, 6:49–51; Ex. 1002 ¶¶ 118–120).

Patent Owner also does not describe what experimentation would have been undue in Petitioner’s reading of claim 1 onto this detailed mapping. Rather, Patent Owner argues that “Petitioner simply suggests—without any explanation as to how—that *Bertin*’s through chip connectors would somehow achieve *Cooke*’s aspirational goal of instantaneous reconfiguration of FPGAs in a processor chip.” PO Resp. 37. Contrary to this argument, Petitioner explains how *Cooke*’s system reconfigures FPGAs. *See* Pet. 48, 52. Petitioner points out that “*Cooke* discloses a tightly integrated FPGA, microprocessors and a ‘vertical stack’ of memory planes.” *Id.* at 48 (citing Ex. 1008, 2:3–11, 2:40–55, Figs. 2, 8A; Ex. 1002 ¶ 121). The depicted stacks show an interface bus. The fact that *Cooke* generally describes how to reconfigure an FPGA at this level of detail (similar to the ’951 patent’s description, *see* Ex. 1001, Figs. 3–5, 5:29–50) suggests that an artisan of ordinary skill readily would have recognized how to reconfigure an FPGA in similar die stacks, such as that of *Bertin*, to arrive at an operable device with a reasonable expectation of success and without undue experimentation.

Patent Owner also argues that “Petitioner uses the ’951 Patent to glean advantages from its instrumental improvement over the art—reconfiguration

of FPGA in one clock cycle as opposed to the millions of clock cycles it took in the conventional art.” *Id.* at 37. Patent Owner stresses that it is the “**buffer cells**” that “greatly improved upon FPGA reconfiguration time,” and that “[t]his improvement was the basis for the ’951 Patent, and, further confirms the challenges that the inventors of the ’951 Patent faced when innovating in this space, and illustrates that Petitioner trivializes these challenges to make its fallacious obviousness argument.” *Id.* at 39–40. All of these arguments rely on Patent Owner’s unsupported claim construction argument that “the phrase ‘a memory array functional to accelerate external memory references to the processing element’ means ‘a memory array that allows the parallel loading of data through *buffer cells*.’” *Id.* at 30 (emphasis added) (“Petitioner’s proposed combination of *Bertin* with *Cooke* does not satisfy this limitation as the combination does not teach or suggest a memory array that uses buffer cells to accelerate memory references to a processing element.”).

Contrary to this line of argument, as set forth above with respect to the ground based on Koyanagi and Alexander and the claim construction of the “accelerate” clause, the challenged claims do not require buffers or a reconfiguration in one clock cycle. *See supra* §§ II.C (Claim Construction), II.D. And even if somehow buffers or reconfiguration are claim requirements, Petitioner persuasively shows that “the components of Cooke stacked according to Bertin’s teachings **include tristate buffers** in the FPGA of Cooke, and those tristate buffers operate for the same purpose as the buffer cells in the ’951 patent.” Reply 23 (citing Ex. 1035, 160:18–161:1 (showing that Dr. Chakrabarty testifies that buffer cells in ’951 patent “decouple[] the loading of the configuration bits through [] the wide

configuration data port [] from the operation of the logic cells under its current configuration.”).

As similarly explained above in connection with Koyanagi and Alexander, the challenged claims at issue here only require, in relevant part, generalized circuit connections, namely the general recitation of “electrically coupled” and recitation of the “functional to accelerate.” The ’951 patent does not describe with any more level of granularity than Petitioner provides in reliance on Cooke and Bertin’s teachings as summarized above, including by virtue of “Annotated Figure 22A.” Also, as the thrust of Dr. Shanfield’s deposition testimony and the record shows, an artisan of ordinary skill readily would have been able to connect the claimed circuits together using conductive vias. *See* Ex. 2014, 82:4–19; Ex. 1002

¶¶ 124 (testifying that “Bertin provides broadly applicable, detailed teachings with regard to stacking different processors, memories and logic chips such as FPGAs”), 130–136 (addressing the “electrical coupling” and “functional to accelerate” limitations in claim 1); Ex. 1030 ¶ 84 (testifying that “at the system or circuit design level, each TSV is designed as an interconnection between specific circuits” and “a TSV that is part of a configuration data port of an FPGA interconnects memory and FPGA circuits located respectively in a memory die and an FPGA die”).

Similar to block diagram forms for connecting circuits together as shown in Cooke, Bertin, and the ’951 patent, the long prior art connections similarly represented in block diagram form in admitted prior art Figure 1 of the ’951 patent, and the lack of detail with respect to Figures 4 and 5 of the ’951 patent, all shows that an artisan of ordinary skill in the art readily would have been able to connect desired circuits together to form an

operable device without undue experimentation. *Compare* Ex. 1001, Fig. 1, Fig. 4, *with* Ex. 1008, Fig. 2, Fig. 8a *and* Ex. 1009, Fig. 21, Fig. 22.

Discussing Figures 21 and 22, Bertin states that some of its “connections allow for parallel input/output connections.” Ex. 1009, 7:31.

Patent Owner also argues that “while *Cooke* suggests utilizing vertically stacked memory with a single IC die having microprocessor and FPGA functionality, *Cooke* does not disclose either stacking the vertical memory stack above the FPGA or using die-area interconnects in such an arrangement.” PO Resp. 41 (citing Ex. 2014, 74:17–75:6 (contending that Dr. Shanfield “admit[s] that FIG. 2 [of *Cooke*] is merely a schematic relationship that does not show how the elements are physically configured)); *see also* Sur-reply 12 (arguing “*Cooke*’s system is made up of a single chip”).

This line of argument minimizes the circuit stacking teachings of *Cooke* and mischaracterizes the testimony of Dr. Shanfield. Dr. Shanfield testifies that *Cooke* “portray[s] in the schematic drawing, Figure 2, *a vertical stack of memory plane*.” Ex. 2014, 74:17–75:6 (emphasis added). Claim 1 does not require “stacking the vertical memory stack *above* the FPGA or using die-area interconnects *in such an arrangement*.” *See* PO Resp. 41 (emphasis added). And Patent Owner admits that “*Cooke* suggests utilizing *vertically stacked memory* with a single IC die having microprocessor and FPGA functionality.” PO Resp. 41. To the extent Patent Owner argues *Cooke* does not disclose a die stack because *Cooke* discloses “a single chip with on-chip components” (Sur-reply 13), Patent Owner’s arguments do not address the combined teachings of the references, including Petitioner’s reliance on Bertin’s die stack benefits and *Cooke*’s FPGA benefits. *See* Pet.

15–16, 50–57. In addition, claim 1 neither precludes stacking a single logic die that includes Bertin’s “microprocessor and FPGA functionality” (*see id.*) with the separate microprocessor die and memory dies of Bertin, nor does it preclude stacking multiple processors. *See* Pet. 57 (Annotated Figure 22A).

The record also does not support Patent Owner’s argument that “Cooke never describes that the vertical memory stack is also stacked with the FPGA.” PO Resp. 42 (citing Ex. 2015 ¶ 87). Contrary to this argument, as the Petition shows, Cooke’s Figure 2 specifically portrays an “FPGA PLANE” stacked with “MEMORY PLANES.” Ex. 1007, Fig. 2; Pet. 48 (“As shown in Cooke, Figure 8a and 2 show stacked memory planes and memory planes with an ‘FPGA’ plane . . .”) (reproducing Ex. 1008, Fig. 2, Fig. 8A, 2:3–11, 3:13–18; citing Ex. 1002 ¶ 121). To support this showing, Petitioner points out that “in the parallel District Court litigation, Dr. Chakrabarty opined that all the components of Cooke’s reconfigurable system are stacked dies.” Reply 25 (citing Ex. 1034, 139:4–141:3; Ex. 1030 ¶ 79; Ex. 1035, 191:10–17, 190:12–21). At the cited portion of the transcript, Dr. Chakrabarty testifies that in Cooke’s Figure 2, “here is the FPGA plane and memory planes . . . and we need vertical connectivity.” Ex. 1034, 140:16–19. Vertical connectivity suggests a circuit stack. *See also id.* at 139:17–19 (asserting in a cross-examination question that Dr. Chakrabarty states (in a District Court expert report at paragraph 89) that “Cooke is directed to a re-configurable processor chip having interconnections around the periphery of the stack die elements”).

Patent Owner also argues that the Petition’s assertion that “supposes that *Bertin* inherently suggests 3D FPGA stacking because it describes logic chips” is “a red herring,” because “[t]here are many specific types of ICs,

including microprocessors, graphic processing units (“GPUs”), application specific integrated circuits (“ASICs”), and microcontrollers, that fall under the generic definition of a logic chip.” PO Resp. 42. This argument simply does not address the Petition’s showing and Dr. Chakrabarty’s admission as discussed above that an FPGA is a type of logic chip, so that Bertin’s FPGA is a logic chip embraced and suggested by Cooke’s logic chip given known properties and advantages of an FPGA. *See, e.g.*, Ex. 1035, 129:1–7 (agreeing that “logic is understood [to] . . . mean[] it could be an FPGA, it could be a ASIC, could be a microprocessor, could be a microcontroller”).

As to known FPGA advantages and benefits, Petitioner describes FPGA’s as providing “arbitrary logic” and “[u]nlike ASICs, the logic and interconnect resources are uncommitted, and can be configured to implement different logic functions and connectivity.” Pet. 52 (citing Ex. 1002 ¶ 128; Ex. 1006, 1; Ex. 1013, 6); *see also* Ex. 1006, 1 (“FPGAs” are “(re)programmable chips that can implement arbitrary logic” and “provide designers with a faster and more economical design cycle”). Petitioner also shows that “[r]econfigurable computing blends the benefits of software and ASIC hardware” (Pet. 3 (citing Ex. 1002 ¶ 38)), and that “[t]he ’951 Patent admits that FPGA-based reconfigurable processor systems were well-known in the art” (*id.* at 5 (citing Ex. 1001, 1:36–42 (“Conventionally, the ability for a reconfigurable processor to alter its hardware [] is typically accomplished through the use of some form of field programmable gate array (‘FPGA’) such as those produced by Altera”))).

Therefore, contrary to Patent Owner’s characterization of Petitioner’s argument as based on “inheren[cy]” (PO Resp. 42), the Petition persuasively relies on obviousness supported by factual underpinnings and rationale. It

follows that contrary to Patent Owner’s arguments, Petitioner does not assert that a “disclosure of a genus [logic chip] is . . . necessarily a disclosure” of an FPGA. *See id.* (quoting *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1285-86 (Fed. Cir. 2017); *Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 999 (Fed. Cir. 2006)) (addition by Board).

Patent Owner also argues that “a POSITA would **not** have found the ’951 Patent’s claimed invention—stacking a *thinned* microprocessor die element, a memory die element, and a FPGA . . . obvious to try with a reasonable expectation of success because of the known thermal issues, which a POSITA would **not** have ignored.” PO Resp. 43 (emphasis to “thinned” added). Contrary to this argument, none of the challenged claims, require “a thinned microprocessor die element.”

Patent Owner correctly points out that a person of ordinary skill would have possessed “an understanding of the known thermal issues as recognized by *Alexander* and other skilled artisans.” PO Resp. 43. This argument supports Petitioner’s showing that an artisan would have addressed the known thermal issues, given the teachings of the prior art of record, including those in Bertin and Cooke. *See* Pet. 46–50 (addressing motivation and known thermal issues including Bertin’s teaching of “high performance” and “heat dissipation” (quoting Ex. 1009, 2:61–65)). And the record shows that such an artisan would have had a reasonable expectation of success based on known via heat conductor solutions as admitted by Dr. Chakrabarty (as discussed above, § II.D.3), and would have been motivated to employ those via and FPGA teachings for myriad beneficial reasons, including speed gains (based on increased bandwidth and short via connections), compactness, and known benefits with the use of FPGAs. *See* Pet. 4

(arguing that “expected advantages of 3D stacks of chips are ‘high packing density,’ ‘high speed,’ ‘parallel signal processing,’ and ‘integration of many functions on a single chip’ (quoting Ex. 1010, 1704; citing Ex. 1002 ¶ 39)), 46–50 (providing evidence that reasons to combine the similar stacked logic chips of Bertin and Cooke include to maximize bandwidth, minimize latency, eliminate performance degradation, improve heat dissipation, and provide high system packing densities and high performance communication, where Bertin’s structure generically accommodates different sizes and structures (citing Ex. 1002 ¶¶ 118–124; Ex. 1009, 1:20–57, 2:61–65, 6:49–52, 7:16–34, Figs. 21–22; Ex. 1006, 1; Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Fig. 8A)).

Further regarding the known thermal issues, Patent Owner relies on its arguments with respect to Koyanagi and Alexander, and contends that “a POSITA would understand that Petitioner’s alleged combination of Bertin with Cooke’s FPGA would only exacerbate the high operating temperatures caused by logic dies and would render the combined device inoperable.” PO Resp. 44 (citing Ex. 2015 ¶ 90). According to Patent Owner, “the power consumption by logic dies, such as FPGAs and microprocessors, increase[s] the operating temperatures.” *Id.*

This line of argument ignores that Patent Owner agrees that Bertin teaches a “broad invocation of logic chips” (PO Resp. 42), and also agrees that “*Cooke* suggests connecting vertically stacked memory to a 2D chip comprising a microprocessor and FPGA” (*id.* at 41). As noted above, tribunals presume the enablement of these patents for what they disclose. *Antor Media*, 689 F.3d at 1287–1288, *Amgen Inc.*, 314 F.3d at 1355; *Corephotonics*, 2021 WL 2577597, at *4. Regarding operability, Petitioner

cites Dr. Chakrabarty's admission that "Bertin pays a lot of attention to the thermal issues" and Bertin uses many TSVs "as heat pipes." *See* Reply 25 (quoting Ex. 1035, 247:10–15, 246:14–247:2). Accordingly, Petitioner persuasively shows that

[a] POSITA would have been motivated to vertically stack the functional components of the FPGA-based reconfigurable computer system described in Cooke according to Bertin's 3D integration teachings—which [are] designed to universally "accommodate different chip sizes and structures" (Ex. 1009, 6:49–52)—to achieve "high packing densities, [as well as] high performance inter-chip and intra-chip communication *and heat dissipation*."

Pet. 48–49 (emphasis added) (quoting Ex. 1009, 2:61–65). In other words, as Petitioner shows, "Bertin itself addresses the alleged thermal challenges in stacking FPGA" (Reply 27 (citing Ex. 1030 ¶¶ 73–75)), and the record shows ample motivation, a reasonable expectation of success, no undue experimentation, and operability, in combining the teachings of Bertin and Cooke as the Petition persuasively proposes.

Based on the foregoing discussion and a review of the record, including Patent Owner's evidence and arguments as presented in the Response and Sur-reply and as summarized above, Petitioner persuasively shows that the combination of Bertin and Cooke would have rendered claim 1 obvious. Relying partly on its showing with respect to claim 1, Petitioner provides a similar and persuasive showing for independent claims 5 and 10, which largely track the limitations recited in claim 1. *See* Pet. 59–67.

Claim 4 depends from claim 1 and recites an "electrically coupled "third integrated circuit." Claim 8 depends from claim 5 and recites a similar limitation. Claim 13 depends from claim 10 and recites that the "memory" comprises a "memory array." Claim 14 depends from claim 10

and recites that the “programmable array” is “reconfigurable.” Claim 15 depends from claim 10 and recites that the three “integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements.” The Petition shows that Bertin discloses these well-known circuit elements or the recitations thereof amount to combining “familiar elements according to known methods . . . [to] yield predictable results.” *See KSR*, 550 U.S. at 416; Pet. 58, 63, 67–71. In summary, the Petition presents a persuasive showing supported by the record with respect to dependent claims 4, 8, and 13–15. *See* Pet. 58, 63, 67–71. Patent Owner does not address claims 4, 5, 8, 10, and 13–15 separately from claim 1. *See* PO Resp. 50–44.

Accordingly, based on the record and as summarized above, Petitioner establishes by a preponderance of evidence that claims that the combination of Bertin and Cooke would have rendered obvious claims 1, 4, 5, 8, 10, and 13–15. *See* Pet. 46–71.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.²² In summary:

²² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent -able
1, 4, 5, 8, 10, 13–15	103(a)	Koyanagi, Alexander	1, 4, 5, 8, 10, 13–15	
1, 4, 5, 8, 10, 13–15	103(a)	Bertin, Cooke	1, 4, 5, 8, 10, 13–15	
Overall Outcome			1, 4, 5, 8, 10, 13–15	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1, 4, 5, 8, 10, and 13–15 the '951 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2

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