

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC,
Patent Owner.

IPR2020-01022¹
Patent 6,781,226 B2

Before KARL D. EASTHOM, BARBARA A. BENOIT, and
SHARON FENICK, *Administrative Patent Judges*.

FENICK, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00393 and has been joined as a party to IPR2020-01022.

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 13, 14, 16–23, and 25–30 (the “challenged claims”) of U.S. Patent No. 6,781,226 B2 (Ex. 1001, “the ’226 patent”). Petitioner filed a declaration of Dr. Stanley Shanfield (Ex. 1002) with its Petition. Arbor Global Strategies LLC (“Patent Owner”), filed a Preliminary Response (Paper 7). After further briefing regarding discretionary denial of institution under 35 U.S.C. § 314(a), we determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims and we instituted this proceeding on December 2, 2020, as to all challenged claims and all grounds of unpatentability. Paper 12 (“Dec. on Inst.”).

After institution, Patent Owner filed a Patent Owner Response (Paper 17, “PO Resp.”) and a declaration of Dr. Krishnedu Chakrabarty in support (Ex. 2009); Petitioner filed a Reply (Paper 20, “Pet. Reply”) and a second declaration of Dr. Shanfield in support (Ex. 1030); and Patent Owner filed a Sur-reply (Paper 25, “PO Sur-reply”). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 33 (“Tr.”). After the hearing, we issued an order (Paper 30) authorizing additional briefing regarding an issue of claim construction and this additional briefing was submitted by Petitioner (Paper 31, “Pet. Supp. Br.”) and Patent Owner (Paper 32, “PO Supp. Br.”).

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies itself, Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. Pet. 65. Taiwan Semiconductor Manufacturing Co. Ltd. identifies itself and TSMC North America as real parties-in-interest. See IPR2021-00393, Paper 2, 63. Patent Owner identifies only itself as a real party-in-interest. Paper 5, 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd. et al.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) (“related litigation”) and *Arbor Global Strategies LLC v. Xilinx, Inc.*, 1:19-cv-1986 (D. Del.) as related proceedings. See Pet. 65–66; Paper 5, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in two related patents, respectively IPR2020-01020 (challenging U.S. Patent No. RE42035) and IPR2020-01021 (challenging U.S. Patent No. 7,282,951).

C. *The '226 Patent*

The '226 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '226 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the

FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” *Id.*

Figure 4 follows:

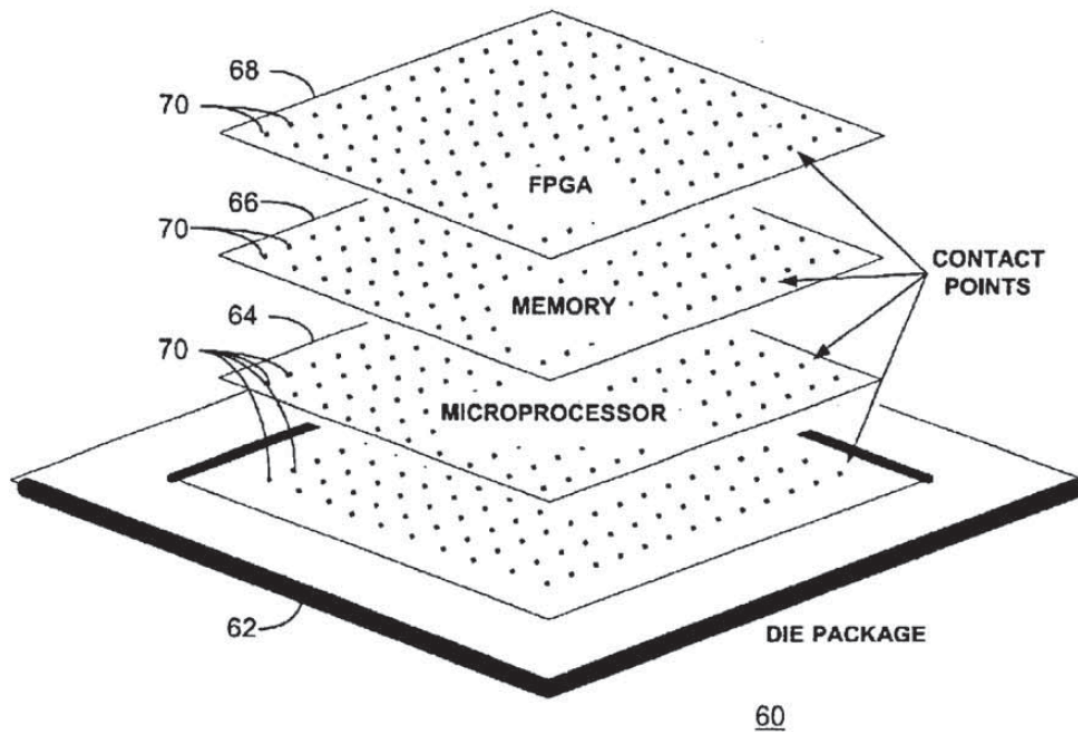


Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using contact holes 70. *Id.* at 4:9–33.

The '226 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” *See* Ex. 1001, 1:19–35. Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA), making the processor faster than one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See id.* A “reconfigurable processor”

provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See id.*

D. Illustrative Claims 13 and 22

The Petition challenges independent claims 13 and 22, and claims 14, 16–21, 23, and 25–30, which depend from one of the challenged independent claims either directly or indirectly. Claims 13 and 22, reproduced below with bracketed numbering added for reference, illustrate the challenged claims at issue:

13. A processor module comprising:

[13.1] at least a first integrated circuit die element including a programmable array;

[13.2] at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

[13.3] at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[13.4] means for reconfiguring the programmable array within one clock cycle.

Ex. 1001, 7:9–21.

22. A processor module comprising:

at least a first integrated circuit die element including a programmable array and a plurality of configuration logic cells;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[22.4] means for updating the plurality of configuration logic cells within one clock cycle.

Ex. 1001, 8:4–17.

E. The Asserted Grounds

Petitioner challenges claims 13, 14, 16–23, and 25–30 of the '226 patent on the following grounds (Pet. 2):

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
13, 14, 16–23, and 25–30	103 ²	Koyanagi ³ , Cooke ⁴
13, 14, 16–23, and 25–30	103	Bertin ⁵ , Cooke

II. ANALYSIS

Petitioner challenges claims 13, 14, 16–23, and 25–30 as obvious based on the grounds listed above. Patent Owner disagrees.

² The Leahy-Smith America Invents Act (AIA), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. The '226 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

³ M. Koyanagi et al., “Future System-on-Silicon LSI Chips,” IEEE Micro, Vol. 18, Issue 4, July/August 1998. (Ex. 1007).

⁴ Cooke, US 5,970,254, issued Oct. 19, 1999 (Ex. 1008).

⁵ Bertin, US 6,222,276 B1, issued Apr. 24, 2001 (Ex. 1009).

A. Legal Standards

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.⁶ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Shanfield, Petitioner contends that [a] person of ordinary skill in the art (“POSITA”) at the time of the ’226 Patent would have been a person having a Master’s degree in Electrical Engineering, Computer Engineering, or Physics with three to five years of industry experience in integrated circuit design, layout, packaging or fabrication. Ex. 1002 ¶¶ 45–48. A greater level of experience in the relevant field may compensate for less education, and vice versa.

Pet. 7–8.

Patent Owner asserts that

[a] person of ordinary skill in the art (“POSITA”) around December 5, 2001 (the earliest effective filing date of the ’226

⁶ No argument or evidence regarding secondary considerations has been presented in this proceeding.

Patent) would have had a Bachelor's degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 5–6 (citing Ex. 2009 ¶¶ 31–34).

As we did in the Decision on Institution, we adopt Petitioner's proposed level of ordinary skill in the art, which comports with the teachings of the '226 patent and the asserted prior art. *See* Dec. on Inst. 18–19. Patent Owner's proposed level is lower but it overlaps with Petitioner's proposed level. Even if we adopted Patent Owner's proposed level, the outcome would remain the same.

C. Claim Construction

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure.

Phillips v. AWH Corp., 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

“There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner and Patent Owner each agree that both “means for reconfiguring the programmable array within one clock cycle” (limitation

13.4 in claim 13) and “means for updating the plurality of configuration logic cells within one clock cycle” (limitation 22.4 in claim 22) are means-plus-function limitations and should be construed as per 35 U.S.C. § 112, ¶ 6. Pet. 9; PO Resp. 6–7.

Both of these limitations listed above recite “means” and further recite a function, thus creating a presumption that 35 U.S.C. § 112, ¶ 6 applies. *See* 35 U.S.C. § 112, ¶ 6 (“An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.”); *see also Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc in relevant part) (quoting *Personalized Media Commc’ns, LLC v. Int’l Trade Comm’n*, 161 F.3d 696, 703 (Fed. Cir. 1998)) (holding that “use of the word ‘means’ creates a presumption that § 112, ¶ 6 applies”). We agree with the parties that these limitations are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6.

Patent Owner additionally argues that we should construe “wide configuration data port,” which appears in challenged claims 14 and 23, and which additionally appears in each party’s proposal for the structure of the means-plus-function limitations described above. Pet. 9–12; PO Resp. 7–14. Because of this, we begin with this construction and then discuss construction of the means-plus-function terms.

1. “wide configuration data port”

While neither party proposed construction of this term in pre-institution briefing, Patent Owner did propose its construction in its

Response, and the parties each briefed the construction before the oral hearing. PO Resp. 11–14; Pet. Reply 5–11; PO Sur-reply 2–4.

Additionally, this term was one subject of our post-hearing order inviting the parties’ positions regarding the possible construction of “wide configuration data port” as “a configuration data port connecting in parallel cells on one die element to cells on another die element,” and each party submitted a post-hearing brief including a discussion of this possible construction. Paper 30; PO Supp. Br. 1–4; Pet. Supp. Br. 2–5.

a. Patent Owner’s Position

Patent Owner argues that the term “wide configuration data port” should be construed as “a configuration data port that allows the parallel updating of logic cells in a programmable array through use of buffer cells.” PO Resp. 11–14 (citing Ex. 1001, 4:50–65; Ex. 2009 ¶ 43); PO Sur-reply 2; PO Supp. Br. 1. In support of this construction, Patent Owner cites the ’226 patent’s disclosure that the wide configuration data port “is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cells 88.” Ex. 1001, 4:51–54 (quoted at PO Resp. 12). Patent Owner contends that “[t]he specification demonstrates that the buffer cells form a necessary part of the wide configuration data port and enable the port to perform its recited function of reconfiguring the programmable array within one clock cycle.” PO Resp. 12; PO Supp. Br. 1–2.

In the Sur-reply, Patent Owner also indicates that configuration memory cells should also be included in the construction of “wide configuration data port.” PO Sur-reply 2–4. Citing the same portion of the specification, Patent Owner argues that the ’226 patent describes that “the

wide configuration data port includes not only a large number of die-area contacts that interconnect stacked chips but also the buffer *and configuration memory cells (which update the logic cells)* connected in parallel via those contacts.” *Id.* at 2–3 (emphasis added). However, Patent Owner does not explain how configuration memory cells are included in, or why they are absent from, its proposed construction. Patent Owner also argues that “*it is the parallel arrangement of those connections* between the buffer cells and logic cells *(and not merely the connection themselves)* that form the wide configuration data port (and enable one clock cycle reconfiguration of the programmable array).” *Id.* at 4 (emphasis added).

With respect to the possible construction described in the order for post-hearing briefing, Patent Owner responds that a correct construction of wide configuration data port should include buffer cells. PO Supp. Br. 1–3 (arguing in the alternative that should the proposed construction be adopted, a corresponding structure for the means-plus-function claims should include a description of the use of buffer cells).

b. Petitioner’s Position

Petitioner, in its Reply, argues that the term should have its plain and ordinary meaning. Pet. Reply 6. Petitioner further asserts that one of ordinary skill in the art would have understood the term not to encompass the buffer cells, but only an interface used for communication. *Id.* at 6–8 (citing Ex. 1001, 4:7–9, 4:45–54, Figs. 3, 5; Ex. 1002 ¶¶ 50–51; Ex. 1030 ¶¶ 28–30; PO Resp. 8; Ex. 1035 (second Chakrabarty deposition), 163:8–21, 173:12–17; Ex. 1034 (first Chakrabarty deposition), 179:2–24).

Petitioner cites as an admission supporting this contention Patent Owner’s description of the ’226 patent as solving problems in the prior art

by “arrang[ing] die-area contacts, such as through-silicon vias (‘TSVs’), into a wide configuration data port that . . . reprograms the programmable array within a single clock cycle.” PO Resp. 1–2 (cited at Pet. Reply 2, 5).

Petitioner additionally cites Dr. Chakrabarty’s deposition testimony that a “configuration data port” is a well-known term for “a data port used for configuration.” Pet. Reply 6 (quoting Ex. 1035, 163:8–21). Petitioner also cites Dr. Chakrabarty’s deposition testimony in the related litigation that a wide configuration data port “is one which is wide enough to do single-cycle configuration.” *Id.* at 6 (quoting Ex. 1034, 179:4–6); *see* Ex. 1034, 178:24–185:11.

With respect to the possible construction described in the order for post-hearing briefing, Petitioner contends that rather than “connecting in parallel cells on one die element to cells on another die element,” the correct construction should describe connection in parallel “the third integrated circuit die element to logic cells of the first integrated circuit die element.” Pet. Supp. Br. 3. Petitioner argues that, in the context of the ’226 patent, this clarifies the die elements described as connected in parallel to form the wide connection data port. *Id.* (citing Ex. 1001, 4:10–20, 4:45–65, Figs. 4, 5). Regarding the use of the word “cells” in the construction, Petitioner asserts that the ’226 patent does not describe cells on a die element, with the exception of buffer cells (which are “preferably” but not always part of a memory die) and logic cells of a programmable array. *Id.* at 3–4 (citing Ex. 1001, 3:25–28, 3:33–37, 3:67–4:9, 4:45–55, 4:57–59, 5:24–28, claim 22, Figs. 3, 5).

c. Analysis and Conclusion

We determine that one of ordinary skill in the art would not understand the ordinary and customary meaning of “wide configuration data port” to include buffer cells or configuration memory cells, and construction in accordance with the prosecution history would likewise not require the inclusion of buffer cells or configuration memory cells. We also note that Patent Owner’s proposed construction (“a configuration data port that allows the parallel updating of logic cells in a programmable array through use of buffer cells”) contains some ambiguity in not making clear how buffer cells *allow* parallel updating, and we decline to provide a construction including this ambiguity.

The ’226 patent does not make extensive use of the term “wide configuration data port.” With the exception of the claims, which do not provide additional context, the references in the ’226 patent are the labelling of element 82 of Figure 5 as “very wide configuration data port” and the paragraph referencing this figure, cited extensively by both parties, in which the specification describes that:

With reference additionally now to FIG. 5, a corresponding functional block diagram of the configuration cells 80 of the reconfigurable processor module 60 of the preceding figure is shown wherein the FPGA 70 may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel. As opposed to the conventional implementation of FIG. 3, a wide configuration data port 82 is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cell 88. The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising the logic cells 84 are in operation. This then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of its configuration logic cells 84 updated in parallel. Other

methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory (“RAM”) than can be offered within the FPGA die 68 itself.

Ex. 1001, 4:45–65 (cited in whole or part at PO Resp. 8, 11–12, 31–33, 48–50; Pet. Reply 5–7, 10; PO Sur-reply 2–3, 6; Pet. Supp. Br. 1, 3–4; PO Supp. Br. 3).

Patent Owner, in focusing on this portion of the ’226 patent disclosure, does not adequately explain why buffer cells and configuration memory cells must be included in the proper construction of “wide configuration data port,” and seeks to import a functional description of the use of a wide configuration data port (“that *allows parallel updating* of logic cells in a programmable array through use of buffer cells”) into the claim construction. PO Resp. 11–14; PO Sur-reply 2–4. While the discussion in the ’226 patent describes an example of a wide configuration data port used in a specific way that aligns with Patent Owner’s proposal (Ex. 1001, 4:45–59), other examples of the use of a wide configuration data port are included (*id.* at 4:59–65), and therefore we do not agree that one of ordinary skill would understand this use to be part of the construction of the term.

We agree with Petitioner that the proper construction of the term does not require buffer cells to be specifically described. *See* Pet. Reply 6–9. Rather, we note that the specification of the ’226 patent contrasts loading of data to an FPGA in a byte serial fashion through a narrow port, which “results in [] long reconfiguration times,” with the use of a wide configuration data port, and therefore we determine that one of ordinary skill would understand the wide configuration data port, in contrast to the byte

serial “relatively narrow” port, to include parallel connections between cells in the dies. *See* Ex. 1001, 4:3–9. This additionally is consistent with certain arguments by Patent Owner, for example in the Patent Owner’s Response, which opens with a discussion of the “inventive” processor’s arrangement of die-area contacts, such as through-silicon vias, “into a wide configuration data port” and we find that description more consistent with the proper construction of this term. PO Resp. 1–2; *see also id.* at 8 (“[T]he ’226 Patent specifically identifies that the wide configuration data port reconfigures both a programmable array and/or logic cells in one clock cycle because it can communicate with many cells (which form an ‘array’) in parallel, and is therefore considered ‘wide.’”)

With respect to the construction for which we requested post-hearing briefing, “a configuration data port connecting in parallel cells on one die element to cells on another die element,” the ’226 patent describes updating the logic cells of a FPGA in one clock cycle to reconfigure the FPGA by loading associated configuration memory from buffer cells, preferably located on a different die element. Ex. 1001, 4:45–59. Additionally, the ’226 patent describes that doing this “takes advantage of the significantly increased number of connections to the cache memory die.” *Id.* at 4:59–65. This construction is supported by the Petitioner’s expert’s contention that the wide configuration data port can interconnect a memory die and an FPGA die using contact points distributed throughout the dies. *See, e.g.,* Ex. 1002 ¶¶ 50, 52; Ex. 1030 ¶¶ 28–30. This construction additionally is supported by Patent Owner’s expert’s description that “the wide configuration data port loads configuration data into buffer cells 88 in parallel” (implying that the wide configuration data port does not include the buffer cells), though

contradicted by other portions of his testimony asserting that buffer cells should be part of a wide configuration data port. *See* Ex. 2009 ¶ 36. The specification supports a construction of the wide configuration data port as a configuration data port that makes connections between die elements in parallel. Ex. 1001, 3:33–37, 4:45–65; *see also id.* at code (57) (“significant acceleration in the sharing of data between the microprocessor and the FPGA element”).

The '226 patent describes the loading of buffer cells, preferably on the memory die, while the FPGA is in operation, with the configuration logic cells then updated in parallel from the buffer cells through the significantly increased number of connections for reconfiguration in one clock cycle. Ex. 1001, 4:45–59. But none of the challenged claims requires configuring or updating while the FPGA is in operation. And the specification shows that the buffer cells are not part of the wide configuration data port. *See id.* at Fig. 5. Therefore, we determine that the specification supports a construction that the parallel connection between die elements are between cells on each die element. This parallel connection implies that cells on one die are connected in parallel to cells on another die, for example, buffer cells or configuration memory cells. *Id.* at 4:50–55, Fig. 5.

For these reasons, we construe “wide configuration data port” as “a configuration data port connecting in parallel cells on one die element to cells on another die element.”

2. Limitation 13.4 – “means for reconfiguring the programmable array within one clock cycle”

The first step in construing a means-plus-function claim element is to identify the recited function in the claim element. *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003). The

second step is to look to the specification and identify the corresponding structure for that recited function. *Id.*

Petitioner argues that the recited function for limitation [13.4] is “reconfiguring the programmable array within one clock cycle.” Pet. 9–10. Patent Owner agrees. PO Resp. 7. We also agree. *See Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999) (“[35 U.S.C. § 112, ¶ 6] does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.”)

We next review the ’226 patent to determine the corresponding structure for the identified function. Petitioner proposes in the Petition that the structure is “[a] wide configuration data port (82) interconnecting a stacked memory die (66) and FPGA die (68) using contact points (70) distributed throughout the die.” Pet. 8 (citing Ex. 1001, 4:10–65, Figs. 4, 5).

Our preliminary determination in the Decision on Institution was that the correct corresponding structure would be “a wide configuration data port interconnecting a memory and the programmable array using contact points distributed through the first integrated circuit die element and the third integrated circuit die element.” Dec. on Inst. 22–25. We asked the parties, in post-hearing briefing, to address whether the corresponding structure should be “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element.” Paper 30.

In Reply, Petitioner agrees with our preliminary determination. Pet. Reply 3–5. In its post-hearing briefing, Petitioner argues that the proper structure should be a wide configuration data port and “contact points formed throughout the areas of the first *and third* integrated circuit die elements.” Pet. Supp. Br. 1–2 (emphasis altered). Petitioner describes that

the contact points in the third die element (which, as per limitation 13.3 of claim 3, includes a memory) play a role in the claimed function. *Id.* (citing Ex. 1001, 2:34–48, 2:58–64, 4:15–20, 4:59–65; Ex. 1002 ¶¶ 51–52).

Patent Owner proposes that the structure is simply a “wide configuration data port,” according to its construction of that term, which includes buffer cells. PO Resp. 6–11; PO Sur-reply 2–9 (“[T]o the extent that the Board finds that the buffer cells are not part of the wide configuration data port, the Board nonetheless should find that they form part of the structure that performs the functions recited in the [means-plus-function] claims.”). Patent Owner argues that if we did not adopt a construction of “wide configuration data port” that describes the use of buffer cells, we should find the structure to be “a wide configuration data port, wherein buffer cells on one die element are connected in parallel to cells on another die element.” Pet. Supp. Br. 2–4; PO Sur-reply 2–9.

“While corresponding structure need not include all things necessary to enable the claimed invention to work, it must include all structure that actually performs the recited function.” *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). Conversely, structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations. *Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308–09, (Fed. Cir. 1998); *see B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997) (“[S]tructure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.”).

Given our construction of wide configuration data port, Patent Owner's argument that the corresponding structure for this limitation must require that buffer cells on one die element are connected in parallel to cells on another die element is based on the description of the use of buffer cells as used in the updating of the FPGA while it is in operation. PO Supp. Br. 3 (citing Ex. 1001, 4:50–54, Fig. 5). However, we note that this description is followed by the disclosure that “[t]he buffer cells 88 are preferably a portion of the memory die 66.” Ex. 1001, 4:50–54. It does not appear, therefore, that buffer cells are always a portion of the memory die, or are required when the FPGA is not in operation, and thus we decline to require in the corresponding structure that they be specified to be on a specific separate die element.

Rather, we find that what is disclosed as actually performing the recited function of “reconfiguring the programmable array within one clock cycle” is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.” The support for this is found in the ’266 patent’s comparison of the long reconfiguration times through a narrow port (Ex. 1001, 4:3–9) with the time to reconfigure through a wide configuration data port with a significantly increased number of connections (*id.* at 4:45–65), and the implementation of this in a module that has multiple dies “which have a number of corresponding contact points, or holes, 70 formed throughout the area of the [die] package” (*id.* at 4:9–20). The use of a wide configuration data port, as per our construction, implicates two die elements. This was reflected in our preliminary claim construction, for which the corresponding structure described “contact points distributed through the

first integrated circuit die element and the third integrated circuit die element.” Dec. on Inst. 25. As the function is “reconfiguring the programmable array within one clock cycle,” one of the die elements is the first integrated circuit die element, which includes the programmable array.

We acknowledge that, in the related litigation, the District Court for the Eastern District of Texas has construed this limitation (and limitation 22.4), in an order issued after our Decision on Institution. Ex. 1036.⁷ The District Court construed the function for this limitation identically, and the corresponding structure as “wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof.” *Id.* at 8–18. The chief distinction between this construction and the one that we adopt is the inclusion of all three die elements in the District Court claim construction, rather than only the first die element (including the programmable array) and an additional die element in ours. The parties do not reference the District Court’s claim construction in the briefing, except that Petitioner characterizes it as “a similar conclusion” to our construction in the Decision on Institution (Pet. Reply 3–5) and argues that the use of a construction specifying two dies would be “consistent with” the District Court claim construction (Pet. Supp. Br. 2). Our decision here would be the

⁷ We additionally acknowledge the construction for certain additional limitations in the challenged claims, which the parties do not address construction of, and which we do not herein construe. Ex. 1036, 18–25 (“processor module”), 25–37 (“programmable array”), 38–44 (“stacked with and electrically coupled to”), 44–49 (“contact points distributed throughout the surfaces of said die elements”). However, our Decision here would be the same were we to explicitly adopt the construction provided by the District Court for those terms.

same were we to adopt the construction provided by the District Court for the corresponding structure of the means-plus-function limitations.

Patent Owner argues, with reference to our preliminary claim construction, that a construction in which the corresponding structure is more than only a wide configuration data port would violate canons of claim construction by incorporating language from dependent claims and in creating a situation where dependent claim 14 is not narrower than the claim from which it depends. PO Resp. 9–10. Each of these arguments sounds in claim differentiation. Our reviewing court has “long held” that a claim differentiation argument cannot be relied upon “to broaden a means-plus-function limitation beyond those structures specifically disclosed in the invention.” *Saffran v. Johnson & Johnson*, 712 F.3d 549, 563 (Fed. Cir. 2013). In addition, the argument that independent claim 13 “will not be narrower than its dependent claims” (*id.* at 10) under our construction is not correct, because claims that depend from claim 13 will carry the same construction as claim 13.

For the reasons discussed above, we determine that, for means-plus-function limitation 13.4 of claim 13, the function is “reconfiguring the programmable array within one clock cycle,” and the corresponding structure is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.”

3. Limitation 22.4 – “means for updating the plurality of configuration logic cells within one clock cycle”

Petitioner and Patent Owner refer back to or recapitulate their arguments with respect to limitation 13.4 in their arguments for the function and structure of means-plus-function claim limitation 22.4. Pet. 11–12;

PO Resp. 6–11; Pet. Reply 4–11; PO Sur-reply 5–9; PO Supp. Br. 1–4; Pet. Supp. Br. 1–2. To support arguments regarding this claim term, the parties cite no additional disclosure other than that previously discussed, and we agree that the previously discussed disclosure supports the construction of claim limitation 22.4. Claim 22 differs from claim 13 in several respects, including the inclusion of a plurality of configuration logic cells in the first integrated circuit die element. Limitation 22.4 differs from limitation 13.4 in its statement of function (“updating the plurality of configuration logic cells” rather than “reconfiguring the programmable array”). The configuration logic cells referenced are included in the first integrated circuit die element, and thus here too, the corresponding structure specifies the first integrated circuit die element is included in the description of the structure. Ex. 1001, 8:4–17.

For the reasons presented above, we find that, for means-plus-function limitation 22.4 of claim 22, the function is “updating the plurality of configuration logic cells within one clock cycle,” and the corresponding structure is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.”

4. No additional constructions

No other terms require explicit construction. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness, Koyanagi and Cooke, Claims 13, 14, 16–20, 22, 23, and 25–29

Petitioner contends the subject matter of claims 13, 14, 16–20, 22, 23, and 25–29 would have been obvious over the combination of Koyanagi and Cooke. Pet. 17–40. Patent Owner disputes Petitioner’s contentions. PO Resp. 17–25 (arguments relating to limitation 13.4), 26–39 (arguments relating to the motivation to combine Koyanagi and Cooke).

1. Koyanagi

Koyanagi describes a “three-dimensional integration technology” (3D) that involves vertically stacking and interconnecting chips using “a high density of vertical interconnections” (Ex. 1007, 18) to “connect[] each layer. Ex. 1007, 17, 18.

Koyanagi explains that its 3D-integration technology “enables a huge number of metal microbumps to form on the top or bottom surfaces of the chips.” *Id.* at 17–18 (“More than 10^5 interconnections per chip form in a vertical direction in these 3D . . . chips.”). Koyanagi’s system “dramatically increase[s] wiring connectivity while reducing the number of long interconnections.” *Id.* at 17.

Koyanagi’s Figure 1a follows:

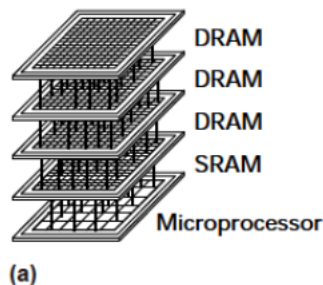


Figure 1a illustrates a stack of chips including dynamic random access memory (DRAM) chips and a synchronous random access memory (SRAM) chip “stacked on a microprocessor” chip. *See id.* at 17–18. Koyanagi

describes “form[ing] as many vertical interconnections as possible” to “remove the generated heat” and forming “electrical wirings.” *Id.* According to one embodiment in Koyanagi, “2D image signals move simultaneously in a vertical direction and are processed in parallel.” *Id.* at 18. Koyanagi also describes a variety of uses: “Typical examples of these new system LSIs include a merged logic memory (MLM) LSI chip as shown in Figure 1 . . . , and a 3D shared memory for parallel processor systems.” *Id.* at 17.

2. *Cooke*

Cooke describes “[a] reconfigurable processor chip” with “a mixture of reconfigurable arithmetic cells and logic cells for higher effective utilization than a standard FPGA.” Ex. 1008, code (57). “A configuration memory stack is provided, allowing for nearly instantaneous reconfiguration.” *Id.* In Cooke, “[e]ach FPGA has two or more memory planes which can shift into the FPGA function in a single cycle.” *Id.* at 2:45–49.

3. *Claim 13*

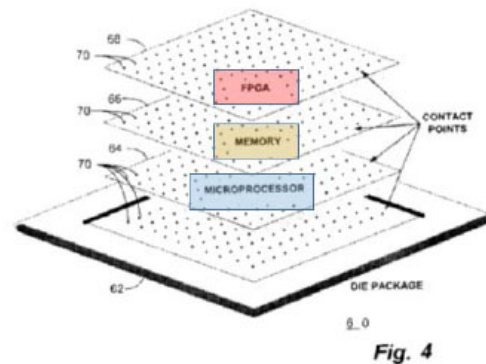
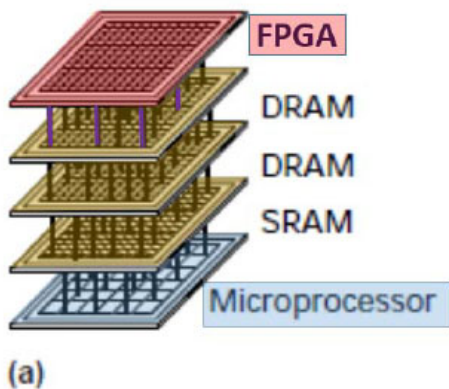
a. *Petitioner’s Contentions*

Claim 13’s preamble recites “[a] processor module comprising.” Petitioner relies on the combined teachings of Koyanagi and Cooke, providing evidence that Koyanagi discloses all elements of the claimed processor module, with the exception of the programmable array of limitation 13.1 and limitation 13.4’s “means for reconfiguring the programmable array within one clock cycle.” *See* Pet. 22–28.

Claim 13 also recites limitation 13.1, “at least a first integrated circuit die element including a programmable array,” limitation 13.2, “at least a

second integrated circuit die element stacked with and electrically coupled to said programmable array of said first integrated circuit die element,” and limitation 13.3, “at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively.” Petitioner contends that the combination of Koyanagi and Cooke renders these limitations obvious. Pet. 23–25. Petitioner relies in part on Cooke’s FPGA, citing Cooke’s teaching of a standard processor and a reconfigurable FPGA on a single chip. *Id.* at 23 (quoting Ex. 1008, 2:1–2).

Petitioner provides the following modified version of Koyanagi’s Figure 1(a) (on the left, termed “Figure 1M” by Petitioner) in a side-by-side comparison with the Petitioner-annotated version of the ’226 patent’s Figure 4 (on the right):



Id. at 23. Petitioner’s annotated version of Koyanagi’s Figure 1 shows a stack of dies with Cooke’s FPGA die replacing one of Koyanagi’s DRAMs, and the ’226 patent’s Figure 4 shows a structurally and functionally similar configuration. *Id.* Petitioner contends that in the proposed combination illustrated in the annotated version of Koyanagi’s Figure 1, the added FPGA from Cooke (in red) teaches the first integrated circuit die element of

limitation 13.1, the microprocessor (in blue) teaches the claimed second integrated circuit die element of limitation 13.2, and the DRAM dies teach the claimed third integrated die element of limitation 13.3, with the electrical coupling of the layers (in limitations 13.2 and 13.3) indicated by the vertical lines between layers. *Id.* at 23–26 (citing Ex. 1008 2:1–7; Ex. 1007, 17; Ex. 1002 ¶¶ 74–77). To additionally support this showing, Petitioner quotes Koyanagi: “More than 10^5 [100,000] interconnections per chip form in a vertical direction in these 3D LSI chips or 3D MCMs. Consequently, we can dramatically increase wiring connectivity while reducing the number of long interconnections.” *Id.* at 24 (citing Ex. 1002 ¶ 87).

Petitioner discusses how Cooke provides a tightly integrated FPGA with microprocessors and a “vertical stack” of memory planes. *Id.* at 18–19 (citing Ex. 1008, 2:40–55). Petitioner contends that Koyanagi’s 3D integration scheme is “agnostic to the type and functionality of the stacked dies.” *Id.* at 18 (citing Ex. 1007, 17; Ex. 1002 ¶ 66). Petitioner provides reasons why a person of ordinary skill in the art (POSITA) would have been motivated to employ Koyanagi’s 3D integration teachings to achieve the benefits of vertically stacking the functional components of an FPGA-based reconfigurable computer system, such as the one described in Cooke:

A POSITA would have been motivated to apply Koyanagi’s broadly applicable 3D integration scheme to integrate the FPGA, memory and microprocessor components of Cooke’s system into a compact single 3D chip because the stacked chip would save area, reduce power consumption, and improve performance. [Ex. 1002] ¶ 72. A POSITA would have found it obvious to try stacking the components of Cooke as taught by Koyanagi and would have had a reasonable expectation of success doing so because Cooke suggests a stacked system and Koyanagi provides broadly applicable, detailed teachings with regard to stacking different dies. *Id.*

Pet. 21–22.

Claim 13 recites element 13.4: “means for reconfiguring the programmable array within one clock cycle.” Petitioner relies upon Cooke’s disclosure of reconfiguring an FPGA in one clock cycle for the functional portion of limitation 13.4. Pet. 26 (citing Ex. 1002 ¶¶ 78–79; Ex. 1024, code (57); Ex. 1008, code (57), 2:47–48). For the corresponding structure, Petitioner relies on Koyanagi’s vertical interconnections between stacked memory and FPGA dies using contact points distributed throughout the dies, and Cooke’s disclosure that a large bandwidth allows configuration data from one memory plane to be shifted into the FPGA in a single cycle. *Id.* at 27–28 (citing Ex. 1007, 17, Fig. 1(a); Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1002 ¶ 79). Petitioner argues that Koyanagi as modified by Cooke “provides the same wide configuration data port” as described in the ’226 patent, and that Cooke teaches how large data bandwidth allows the shift of configuration data in one clock cycle. *Id.* at 26–27 (citing Ex. 1002 ¶ 79).

b. Patent Owner’s Arguments

Patent Owner argues that one of ordinary skill in the art would not have combined Koyanagi and Cooke, because such a combination would have taken undue experimentation to perform. PO Resp. 27–33; PO Sur-reply 13–14. Patent Owner cites Petitioner’s expert’s testimony that to stack chips “you don’t just slap it together without worrying about what connects to what” and contends that the asserted combination of Koyanagi and Cooke is such a “slap[ped-]together” combination. PO Resp. 27–33 (citing Ex. 2009 ¶¶ 67, 69–73; quoting Ex. 2014, 81:21–82:19 (Shanfield deposition) (emphasis omitted)). Patent Owner asserts that Petitioner has

not provided an adequate explanation as to how to combine Koyanagi and Cooke. PO Resp. 28; PO Sur-reply 17–21.

Patent Owner additionally argues that Petitioner overlooked thermal issues that “plagued” 3D stacked FPGA chips, and that there would not have been a reasonable expectation of success with respect to the proposed combination. PO Resp. at 33–39. Patent Owner argues that Cooke does not disclose stacking a vertical memory stack and a FPGA. *Id.* at 34 (citing Ex. 2009 ¶ 75; Ex. 2014, 74:17–75:6). Patent Owner discusses the Alexander reference, cited by Petitioner for its discussion of the benefits of FPGAs but also their “substantial performance penalty, due primarily to interconnect delay,” which Petitioner asserts would have motivated a configuration including an FPGA but with stacking to minimize interconnect delay. Pet. 42–43 (quoting Ex. 1006 (Alexander)); PO Resp. 34–35. Patent Owner contends that Alexander discusses mitigating thermal issues in 3D FPGA architectures, that these issues are “a critical concern in 3D integration,” and that such issues were well known and a skilled artisan would not have ignored them and would have been deterred from making the proposed combination by thermal issues. PO Resp. 34–39 (citing Ex. 1006, 3–4; Ex. 2009 ¶¶ 79–80). Patent Owner highlights Petitioner’s proposed modification to Koyanagi to include an FPGA in the stack, contending that Koyanagi’s solution to heat dissipation would not apply to a stack with an FPGA, which would have greater power consumption needs. *Id.* at 36–37 (citing Ex. 2009 ¶¶ 79–80).

Patent Owner also argues that Petitioner’s showing regarding limitation 13.4 is deficient because it does not detail the buffer cells Patent Owner argues are, by construction, required for this limitation, or because of

issues with the location of buffers in Cooke. *Id.* at 18–21; PO Sur-reply 10–12, 15–16. Patent Owner also argues that Petitioner has not identified a structure which corresponds to the identified function in Cooke or Koyanagi. PO Resp. at 21–25; PO Sur-reply 10–13. Petitioner asserts that the structure in Koyanagi constrains, rather than accelerates, the speed of data travelling through its TSVs and was subject to additional issues degrading device performance. PO Resp. at 23–24 (citing Ex. 2009 ¶¶ 59–60). Patent Owner asserts that Petitioner does not allege the corresponding structure in Cooke, and that both structure and function for the means-plus-function limitation must be found in one reference. *Id.* at 24–25.

c. Analysis and Conclusions – Claim 13

We do not find that Petitioner’s proposed combination would require undue experimentation. Dr. Shanfield’s deposition testimony relied upon by Patent Owner does not support Patent Owner’s argument that combining the teachings of Koyanagi and Cooke to arrive at the claimed processor module requires “undue experimentation.” In the passage that includes the quoted testimony that Patent Owner relies upon, Dr. Shanfield testifies as follows about Bertin – in response to being asked “[w]hen you’re stacking two different type[s] of chips using TSVs, does any thought need to be put into how those TSVs are interconnecting the chips, or is it – is it really just, you know, you can sandwich any kind of chips together and call it a day?”:

You have obviously got to have a circuit in mind that you’re wanting to create a system-level circuit, a module-level circuit; and so you’re going to need to consider which connections you want a TSV connecting to something below.

So you don’t just slap it together without worrying about what connects to what.

On the other hand, the putting together of the -- in Bertin, he describes the putting together of these chips and how that can

be done in detail. And that piece of it is -- I guess you could characterize that as something that comes with the process and in itself isn't something you think specifically about every one of 50,000 connections. They're all done by the process that he gives an example of.

Ex. 2014, 81:21–82:19.

Dr. Shanfield's deposition testimony does not indicate that Petitioner "slap[s] *Koyanagi* and *Cooke* together without worrying about what connects to what. . . . to arrive at a '3D integrated circuit' integrating 'an FPGA, memory, and microprocessor,'" or that arriving at the claimed invention would have required "undue experimentation." *See* PO Resp. 28–29. Rather, Dr. Shanfield's deposition testimony indicates that an artisan of ordinary skill readily would have been able to connect different die circuits together "obviously" with "a circuit in mind . . . to create a system-level circuit, [or] a module-level circuit . . . consider[ing] which [TSV] connections [she] want[s]." *See* Ex. 2014, 81:21–82:19. As Petitioner argues, "[n]othing in Dr. Shanfield's testimony, however, suggests that Petitioner 'slap[ped] together' *Koyanagi* and *Cooke*." Pet. Reply 18 (second alteration in original); Ex. 1030 ¶¶ 82–83 (testifying that Patent Owner took his (Dr. Shanfield's) deposition testimony "out of context" and "at the system or circuit design level, each TSV is an interconnection between specific circuits").

As Petitioner also argues and as summarized above, the Petition "provide[s] a detailed explanation of *how* *Koyanagi* and *Cooke* would have been combined to disclose each limitation of the challenged claims and *why* a POSITA would have been motivated to combine them—to create a 3D reconfigurable processor module with improved performance and area efficiency." Pet. 17–19, 21; Pet. Reply 18–19 (quoting Pet. 17). By way of

example, Petitioner's annotated Figure 1 (Pet. 21), which represents combined teachings of Koyanagi and Cooke, shows how to connect the dies together using a wide configuration data port as challenged claim 1 requires.

By teaching similar stacking techniques for similar circuits, Koyanagi and Cooke collectively evidence a reasonable expectation of success in arriving at the claimed invention. *See Otsuka Pharm. Co., v. Sandoz, Inc.*, 678 F.3d 1280, 1296 (Fed. Cir. 2012) ("The inventor's own path itself never leads to a conclusion of obviousness; that is hindsight. What matters is the path that the person of ordinary skill in the art would have followed, as evidenced by the pertinent prior art."). In other words, Petitioner shows that the claimed invention involves a routine combination of familiar elements, namely combining Koyanagi's die stack with Cooke's FPGA replacing a DRAM, maintaining the large bandwidth connection taught by Cooke through the 3D integration with contact points on the surface of the dies, as taught by Koyanagi. *See* Pet. 21–22.

With respect to thermal issues, we agree with Petitioner's contentions that this concern is mooted by Koyanagi's express description that "forming as many vertical interconnections" addresses heat generation issues, and that the vertical interconnections may act as heat pipes to remove generated heat. Pet. Reply 20 (citing Ex. 1007, 17; Ex. 1030 ¶¶ 62–63; Ex. 1035 256:6–15, 190:4–7). Specifically with respect to Alexander's discussion of thermal issues for FPGAs, Petitioner argues persuasively that "Alexander does not suggest that there are any particularly challenging thermal issues with 3D FPGAs, but rather states that heat dissipation is an important consideration in any chip design." Pet. Reply 21 (citing Ex. 1006, 3).

With respect to the propriety of identifying a structure and a function from different references, we consider what the combined teachings of the references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Patent Owner argues that “[i]t is improper for the Petitioner to rely on a function in one prior art system and a structure in a different prior art system without showing that the structure corresponds to the recited function.” PO Resp. 18–19, 21–22, 24–25 (citing *Fresenius USA, Inc. v. Baxter Int’l, Inc.*, 582 F.3d 1288, 1299 (Fed. Cir. 2009) and *Bennett Marine, Inc. v. Lenco Marine, Inc.*, 549 F. App’x 947, 954 (Fed. Cir. 2013)); PO Sur-reply 11. The relevant portion of *Fresenius* involved a dispute regarding whether claims with means-plus-function limitations were shown to be invalid. *Fresenius*, 582 F.3d at 1293–1294. Our reviewing court found that there was no evidence of what the correct corresponding structure was for certain means-plus-function limitations, and no comparison of structure in the specification to those present in the prior art. *Id.* at 1299–1300. While the Federal Circuit took the opportunity to stress that, for showing invalidity of a claim with a means-plus-function limitation, both the function and the corresponding structure must be found to be present in the prior art, we do not see any indication in this case relating to Patent Owner’s assertion of impropriety in finding structure and function in an asserted combination based on the combined teachings of two references. The situation is similar in *Bennett Marine*. In that case, there was a failure to identify corresponding structure in the specification of the challenged patent, and the Federal Circuit confirmed that a means-plus-function limitation is limited to the corresponding structure disclosed in the specification. *Bennett Marine*, 549 F. App’x at 954–955.

In any case, for this ground of asserted unpatentability, Petitioner identifies the structure as taught in the vertical interconnections of Koyanagi in its stacked die modules and in the large bandwidth interface of Cooke providing shifting into the FPGA function in a single cycle as teaching or suggesting the structure of the wide configuration data port. Pet. 20–21, 27 (citing Ex. 1007, 17, 19; Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1002 ¶¶ 68–71, 79); Tr. 91:3–14; *see* Dec. on Inst. 30. Therefore, Patent Owner’s argument that Petitioner finds the structure in Koyanagi and the function exclusively in Cooke is not commensurate with the Petition’s assertions. *See* Pet. 27–28.

Based on the foregoing discussion and a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claim 13 obvious.

4. Claim 22

Petitioner’s showing with respect to claim 22 is similar to its showing with respect to claim 13. Pet. 36–38. Notably, claim 22’s first limitation is to “at least a first integrated circuit die element including a programmable array and a plurality of logic configuration cells,” which Petitioner describes as being taught or suggested in Cooke’s programmable array with logic cells. *Id.* at 36 (citing Ex. 1008, 6:40–42; Ex. 1002 ¶ 90). Otherwise, the showing for this claim is substantially similar to that for claim 13. Pet. 36–38.

Patent Owner presents no separate argument with respect to claim 22. For the reasons given with respect to this first limitation and for the same reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claim 22 obvious.

5. Claims 14 and 23

Claim 14 depends from claim 13 and specifies that the "reconfiguring means" of claim 13 "comprises a wide configuration data port." Ex. 1001, 7:23–24. Claim 23 depends from claim 22 and specifies that the "updating means" of claim 22 "comprises a wide configuration data port." *Id.* at 8:18–19. Patent Owner presents no separate arguments with respect to these claims.

We have determined that the structure for each means-plus-function limitation described includes a wide configuration data port and discussed above Petitioner's showing that this would have been obvious over the combination of Koyanagi and Cooke.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claims 14 and 23 obvious.

6. *Claims 16, 17, 25, and 26*

Claims 16 and 17 depend from claim 13 and specify that the processor of the second integrated circuit die element comprises a microprocessor (claim 16) and that the third integrated circuit die element comprises a memory array (claim 17). Ex. 1001, 7:28–33. Claims 25 and 26 further limit claim 22 in the same way. *Id.* at 8:23–28.

Petitioner argues that Koyanagi teaches a die element that is a microprocessor. Pet. 29 (citing Ex. 1007, 17; Ex. 1002 ¶ 81). Petitioner further argues that Koyanagi teaches a die element that is a DRAM memory die, and that one of ordinary skill in the art would have known this would include a memory array. *Id.* at 29–30 (citing Ex. 1002 ¶ 82). Petitioner further argues that Cooke discloses portions of a memory array from one of its memory planes. *Id.* at 30 (citing Ex. 1008, 2:47–55, 4:20–21, Figs. 7A–7F). Petitioner reiterates these arguments with respect to claims 25 and 26. *Id.* at 38–39.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claims 16, 17, 25, and 26 obvious.

7. Claims 18 and 27

Claim 18 depends from claim 13 and specifies that the programmable array is configurable as a processing element. Ex. 1001, 7:34–35. Claim 27 further limits claim 22 in the same way. *Id.* at 8:29–30.

Petitioner argues that Cooke teaches configuring and reconfiguring the FPGA used in the asserted Koyanagi/Cooke combination to perform different functions. Pet. 31–33 (citing Ex. 1008, 1:58–67, 2:58–60, 4:66–5:19, Figs. 9A, 9B; Ex. 1002 ¶¶ 84–85). Petitioner reiterates these arguments with respect to claim 27. *Id.* at 39.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claims 18 and 27 obvious.

8. Claims 19–21 and 28–30

Claim 19 depends from claim 13 and specifies that the first, second, and third integrated circuit die elements “are electrically coupled by a number of contact points distributed throughout the surfaces of the die elements.” Ex. 1001, 7:36–39. Claim 20 depends from claim 19 and recites that the contact points “traverse said die elements through a thickness thereof.” *Id.* at 7:40–42. Claim 21 depends from claim 20 and specifies that the “die elements are thinned to a point at which said contact points traverse

the thickness of said die elements.” *Id.* at 8:1–3. Claims 28–30 provide similar limitations (and similar interdependencies) from claim 22. *Id.* at 8:31–40.

Petitioner argues that Koyanagi teaches the further limitations of claim 19 in its teaching of large numbers of contact points distributed throughout the surfaces of die elements electrically coupling those die elements. Pet. 32–33 (citing Ex. 1007, 17; Ex. 1002 ¶ 86). Petitioner further argues that Koyanagi teaches that the contact points traverse the die elements throughout their thickness. *Id.* at 33–34 (citing Ex. 1007, 17, Fig. 5; Ex. 1002 ¶ 87). With respect to the thinning of the die elements, Petitioner further argues that Koyanagi teaches thinning of die elements at the points where the connections are created, from 270 μm to a thickness of 70 μm . *Id.* at 35 (citing Ex. 1007, 19–20, Fig. 5; Ex. 1002 ¶ 88).

Petitioner reiterates these arguments with respect to claims 28, 29, and 30. *Id.* at 39–40.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Koyanagi and Cooke would have rendered claims 19–21 and 28–30 obvious.

E. Obviousness, Bertin and Cooke 13, 14, 16–23, and 25–30

1. Petitioner's Contentions – Claim 13

Petitioner contends claims 13, 14, 16–23, and 25–30 would have been obvious over the combination of Bertin and Cooke. *See* Pet. 40–62. Similar to Koyanagi, Bertin teaches stacking different types of chips, including logic chips, microprocessors, and controllers to minimize latency and maximize bandwidth and heat dissipation, using through-chip conductors. *See* Pet. 40–41 (citing Ex. 1009, 1:20–57, 6:49–52, 7:17–34; Ex. 1002 ¶¶ 102–104).

Bertin does not disclose an FPGA. Petitioner relies on Cooke to describe stacking chips, including FPGAs, microprocessors, and memory planes. *See* Pet. 41–42 (citing Ex. 1008, 2:3–12, 2:40–55, 3:13–18, Figs. 1, 2, 8A; Ex. 1002 ¶¶ 105–106). Petitioner contends it would have been obvious to use FPGAs in Bertin's 3D stacks to improve performance, area-efficiency, packing densities, and speed, and avoid interconnect delays. *See* Pet. 42–43 (citing Ex. 1001, 1:36–2:9; Ex. 1006, 1; Ex. 1009, 2:61–65, 6:49–52; Ex. 1002 ¶¶ 106–107). Petitioner also reads the claim limitations of the challenged claims on the combined teachings of Bertin and Cooke, providing a detailed showing, supported by the references and expert testimony. *See id.* at 43–62.

Bertin describes the following:

FIGS. 21 and 22 illustrate the ability to stack similar chips while providing high speed chip-to-chip connections through the silicon. As seen in FIG. 21, a stack of chips 142, 144, 146 and 148 is mounted directly on device 140, such as a logic chip, carry-card, microprocessor, controller, etc., to minimize latency between the device and chips and to maximize bandwidth.

Ex. 1009, 7:16–22. Petitioner's interpretation of Bertin is that a variety of chips such as the recited logic chip or a microprocessor may be included in

one stack of chips. *See* Pet. 16; Ex. 1002 ¶ 102. Bertin describes chips that differ, for example, in requiring different heights of chip-to-chip connectors, and it is not clear what similarity is required for the embodiment of Figures 21 and 22 in Bertin. *See* Ex. 1009, 6:49–7:15.

Petitioner argues a combination of the teachings of Cooke with respect to a reconfigurable processor system including a processor, FPGA logic, and memory with Bertin’s stacked chips interconnected using through-chip connectors. Pet. 40–41 (citing Ex. 1009, 6:49–52, 7:17–34, Figs. 21, 22; Ex. 1008, 2:3–12, 2:40–55, 3:13–18; Ex. 1002 ¶¶ 101–108). Petitioner argues that one of ordinary skill in the art would have made this combination to achieve the packing densities and high performance inter-chip, the intra-chip communication, and the heat dissipation described in Bertin. Pet. 42 (citing Ex. 1009, 2:61–65). Petitioner argues that one of ordinary skill would have tried this combination and had a reasonable expectation of success in light of Cooke’s suggestions regarding a stacked system and Bertin’s broadly-applicable teachings with regard to stacking processors, memories, and logic chips. *Id.* at 43 (citing Ex. 1002 ¶ 108).

Petitioner argues that this combination would yield a processor module, as in the preamble of claim 13. Pet. 43–44 (citing Ex. 1009, 7:16–34; Ex. 1002 ¶¶ 109–110). Petitioner further argues, with respect to limitations 13.1, 13.2, and 13.3, that the functional components of Cooke teach such a module including the first, second, and third integrated circuit die elements of claim 13. *Id.* at 45–47 (citing Ex. 1008 2:40–43; Ex. 1009, 7:16–34; Ex. 1002 ¶¶ 111–113). Lastly for claim 13, Petitioner asserts that the combination teaches or suggests limitation 13.4, in its teaching of a wide configuration data port in the large number of contact points distributed

throughout the dies. Pet. 47–49 (citing Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1009, 2:61–65, 4:57–60; Ex. 1002 ¶¶ 114–116); Pet. Supp. Br. 5–6. Petitioner argues that Bertin teaches a very large number of through-chip conductors to provide high performance inter-chip communication. Pet. 48 (citing Ex. 1009, 2:61–65, 4:57–60; Ex. 1002 ¶ 115). Petitioner notes that one of ordinary skill would have understood the shifting of configuration data stored in memory into the FPGA in a single cycle using through-chip conductors distributed throughout the surface of a die, with memory cells containing configuration bits would be connected in parallel to the logic cells of the FPGA die using the interconnections. Pet. 48–49 & n.10 (citing Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1002 ¶ 115); Pet. Supp. Br. 7 (citing Ex. 1014, 151–152 (describing cells in a memory)).

2. Patent Owner's Arguments – Claim 13

With respect to Petitioner's arguments regarding the unpatentability of claim 13 over Bertin and Cooke, Patent Owner argues that neither Cooke nor Bertin teaches or suggests the corresponding structure for limitation 13.4. PO Resp. 41–42. Additionally, Patent Owner argues that Petitioner impermissibly relies on a structure taught in Bertin and a function taught in Cooke. *Id.* at 42–43.

Patent Owner additionally contends that Petitioner has not shown that one of ordinary skill in the art would have been motivated to combine Bertin and Cooke, recapitulating and at times referencing the arguments Patent Owner presents with respect to the combination of Koyanagi and Cooke. *Id.* at 44–54. Patent Owner again argues that Petitioner oversimplifies the technology at issue, “slaps together” the teachings, and does not explain how the combination would be achieved, while asserting that the '226 patent

provides such detail. *Id.* at 45–50 (citing Ex. 1001, 4:45–65). Patent Owner also asserts that the combination of Bertin and Cooke would be subject to the same thermal problems discussed with respect to the combination of Koyanagi and Cooke. *Id.* at 51–54.

3. Analysis and Conclusions – Claim 13

We determine that Petitioner has shown that claim 13 would have been obvious over Bertin and Cooke. With respect to Patent Owner’s arguments, which are similar to or recapitulate the arguments made with respect to Koyanagi and Cooke, we refer to our analysis of that ground of unpatentability, with the following exceptions.

First, with respect to the question of whether Bertin teaches buffer cells, this argument fails because it is not commensurate with the claim constructions of “wide configuration data port” and limitation 13.4, which do not require such buffer cells. *See* II.C.2.

With respect to Patent Owner’s repeated argument that it is error to find structure for a means plus function claim in one reference and function in a second reference, we reiterate that we consider what the combined teachings of the references would have suggested to those of ordinary skill in the art. *Keller*, 642 F2d. at 425. In this case, we agree with Petitioner that one of ordinary skill in the art would have combined the references as illustrated in the annotated version of Figure 22 of Bertin. Pet. 43. As Petitioner argues, the combination would have taught a wide configuration data port as per our construction of limitation 13.4, and that that wide configuration data port would perform the function described, that of reconfiguring the programmable array within one clock cycle. Pet. 47–49

(citing Ex. 1008, code (57), 2:47–48, 8:11–15; Ex. 1009, 2:61–65, 4:57–60; Ex. 1002 ¶¶ 114–116).

With respect to the assertion that Petitioner’s argument is a “vast oversimplification” and that Petitioner has failed to demonstrate how the combination would be effected or used the challenged claims as a roadmap, we reiterate our response to the same argument with respect to the combination of Koyanagi and Cooke, as discussed *supra* Section II.D.3.c. Our determination is that Petitioner has supplied the necessary level of detail, detailing the similarities between the teachings of Bertin and Cook, each describing stacking to create a processor system, and providing an annotated version of Figure 22 of Bertin. *See* Pet. 40–43.

With respect to Patent Owner’s arguments asserting thermal issues would have prevented Petitioner’s proposed combination of Bertin and Cooke, Patent Owner correctly points out that a person of ordinary skill would have possessed “an understanding of the known thermal issues as recognized by Alexander and other skilled artisans.” PO Resp. 53. This supports Petitioner’s showing that an artisan would have addressed the known thermal issues, given the teachings of the prior art of record, including those in Bertin and Cooke. *See* Pet. 46–50 (addressing motivation and known thermal issues including Bertin’s teaching of “high performance” and “heat dissipation” (quoting Ex. 1009, 2:61–65)). The record shows that such an artisan would have had a reasonable expectation of success based on known via heat conductor solutions as admitted by Dr. Chakrabarty (as discussed above, § II.D.3), and would have been motivated to employ those via and FPGA teachings for myriad beneficial reasons, including speed gains (based on increased bandwidth and short via connections), compactness, and

known benefits with the use of FPGAs. *See* Pet. 4 (arguing that “expected advantages of 3D stacks of chips are ‘high packing density,’ ‘high speed,’ ‘parallel signal processing,’ and ‘integration of many functions on a single chip’ (quoting Ex. 1010, 1704; citing Ex. 1002 ¶ 39)), 40–43 (providing evidence that reasons to combine the similar stacked logic chips of Bertin and Cooke include to maximize bandwidth, minimize latency, eliminate performance degradation, improve heat dissipation, and provide high system packing densities and high performance communication, where Bertin’s structure generically accommodates different sizes and structures (citing Ex. 1002 ¶¶ 102–118; Ex. 1009, 1:20–57, 2:61–65, 6:49–52, 7:17–34, Figs. 21–22; Ex. 1006, 1; Ex. 1008, 2:3–11, 2:40–55, 3:13–18, Fig. 8A)).

Further regarding the known thermal issues, Patent Owner’s argument ignores that Patent Owner agrees that Bertin teaches a “broad invocation of logic chips.” PO Resp. 52. Regarding operability, Petitioner cites Dr. Chakrabarty’s admission that “Bertin pays a lot of attention to the thermal issues” and Bertin uses many TSVs “as heat pipes.” *See* Pet. Reply 27 (quoting Ex. 1035, 247:10–15, 246:14–247:2). Accordingly, Petitioner persuasively shows that the combination would “provide high system packing densities, [as well as] high performance inter-chip and intra-chip communication and heat dissipation.” Ex. 1009, 2:61–65 (quoted at Pet. 17).

Based on the foregoing discussion and a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence

that the combination of Bertin and Cooke would have rendered claim 13 obvious.

4. Claim 22

Petitioner's showing with respect to claim 22 is similar to its showing with respect to claim 13. Pet. 57–59. Again, Petitioner describes the first limitation of claim 22 as being taught or suggested in Cooke's programmable array with logic cells. *Id.* at 58 (citing Ex. 1008, 6:40–42; Ex. 1002 ¶ 131). Otherwise, the showing for this claim is substantially similar to that for claim 13. *Id.* at 57–59.

Patent Owner presents no separate argument with respect to claim 22. For the reasons given with respect to this first limitation and for the same reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Bertin and Cooke would have rendered claim 22 obvious.

5. Claims 14 and 23

These dependent claims further specify that the “reconfiguring means” (claim 14) or “updating means” (claim 23) of the respective independent claim from which each depends “comprises a wide configuration data port.” Ex. 1001, 7:23–24, 8:18–19. Patent Owner presents no separate arguments with respect to these claims.

We have determined that the structure for each means-plus-function limitation described includes a wide configuration data port and discussed above Petitioner's showing that this would have been obvious over the combination of Bertin and Cooke.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Bertin and Cooke would have rendered claims 13 and 23 obvious.

6. Claims 16, 17, 25, and 26

For the teaching that the processor of the second integrated circuit die element comprises a microprocessor (claim 16), Petitioner argues that Bertin teaches a stacked chip element that is a microprocessor. Pet. 50 (citing Ex. 1000, 7:16–34; Ex. 1002 ¶ 118).

For the teaching that the memory of the third integrated circuit die element comprises a memory array (claim 17), Petitioner asserts this is taught in Bertin's teaching of a memory comprising a memory array accessed through array lines of a memory chip. *Id.* at 51 (citing Ex. 1009, 6:38–48; Ex. 1002 ¶¶ 119). Petitioner reiterates these arguments with respect to claims 25 and 26. *Id.* at 60.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Bertin and Cooke would have rendered claims 16, 17, 25, and 26 obvious.

7. Claims 18 and 27

For the additional limitations of claims 18 and 27, Petitioner again asserts that Cooke teaches configuring and reconfiguring the FPGA used in the asserted combination to perform different functions. Pet. 52–53 (citing Ex. 1008, 1:58–67, 2:58–60, 4:66–5:18, Figs. 9A, 9B; Ex. 1002 ¶¶ 120–122). Petitioner reiterates these arguments with respect to claim 27. *Id.* at 61.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner’s evidence and arguments as presented in the Response, Sur-reply, and Patent Owner’s Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Bertin and Cooke would have rendered claims 18 and 27 obvious.

8. Claims 19–21 and 28–30

With respect to claim 19’s limitation that the integrated circuit die elements be electrically coupled by a number of contact points distributed throughout the surfaces of the die elements, Petitioner argues that Bertin teaches contact points distributed throughout the surfaces of the dies to provide inter-chip communication. Pet. 53–55 (citing Ex. 1009, 2:61–65, 4:57–60, 6:38–48, Figs. 18, 22; Ex. 1002 ¶¶ 124–125).

With respect to claim 20, Petitioner further argues that Bertin teaches that the contact points traverse the die elements throughout their thickness. *Id.* at 33–34 (citing Ex. 1009, Fig. 22; Ex. 1002 ¶ 126). With respect to the

thinning of the die elements to a point at which the contact points traverse the thickness of the die elements, Petitioner argues that one of ordinary skill in the art would know that Bertin's disclosed through-chip conductors, formed by a conventional semiconductor process, would require thin dies, because the aspect ratio of holes that form these conductors is proportional to the thickness of the die element. *Id.* at 56–57 (citing Ex. 1009, 3:21–40, Figs. 3, 4; Ex. 1002 ¶¶ 128–129).

Petitioner reiterates these arguments with respect to claims 28, 29, and 30. *Id.* at 61–62.

Patent Owner presents no separate arguments with respect to these claims. We find that Petitioner has shown the additional claim limitations present in the asserted combination.

Therefore, for the reasons discussed above, based on a review of the record, including a consideration of Patent Owner's evidence and arguments as presented in the Response, Sur-reply, and Patent Owner's Supplemental Brief, Petitioner persuasively establishes by a preponderance of the evidence that the combination of Bertin and Cooke would have rendered claims 19–21 and 28–30 obvious.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.⁸ In summary:

⁸ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg.

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent- able
13, 14, 16– 23, 25–30	103	Koyanagi, Cooke	13, 14, 16– 23, 25–30	
13, 14, 16– 23, 25–30	103	Bertin, Cooke	13, 14, 16– 23, 25–30	
Overall Outcome			13, 14, 16– 23, and 25– 30	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 13, 14, 16–23, and 25–30 of the '226 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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