

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-01315
Patent 8,373,455 B1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Dismissing Patent Owner's Motion to Exclude
37 C.F.R. § 42.64(c)

I. INTRODUCTION

A. BACKGROUND

Advanced Micro Devices, Inc., (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1–14 (“the challenged claims”) of U.S. Patent No. 8,373,455 B1 (Ex. 1001, “the ’455 patent”). Monterey Research, LLC, (“Patent Owner”) filed a Preliminary Response. Paper 6. We instituted review. Paper 7 (“Institution Decision” or “Inst.”).

Patent Owner filed a Response. Paper 11 (“PO Resp.”). Petitioner filed a Reply. Paper 14 (“Pet. Reply”). Patent Owner filed a Sur-Reply. Paper 16 (“PO Sur-Reply”). We held a hearing on November 30, 2021, and a transcript appears in the record. Paper 26 (“Tr.”).

This is a final written decision as to the patentability of the challenged claims. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–14 of the ’455 patent are unpatentable.

B. RELATED MATTERS

The parties identify the following matter related to the ’455 patent: *Monterey Research, LLC v. Advanced Micro Devices Inc.*, No. 1:19-cv-02149-NIQA-LAS (D. Del.). Pet. 2; Paper 3, 1.

C. REAL PARTIES IN INTEREST

Petitioner identifies itself and ATI Technologies ULC, an indirect wholly owned subsidiary of Petitioner, as the real parties in interest. Pet. 2. Patent Owner identifies itself and IPValue Management as the real parties in interest. Paper 3, 1.

D. THE '455 PATENT

The '455 patent describes an output buffer circuit using a variable current supply to control the gate of the driver transistor. Ex. 1001, code (57). It characterizes prior buffers as having “limited flexibility in meeting variations arising from different applications.” *Id.* at 1:48–50. According to the '455 patent, such conventional buffers could be tuned for certain conditions but could not adapt to changing conditions. *Id.* at 1:50–62.

To accommodate that need, the '455 patent describes a buffer circuit using a variable current source to control how quickly the gates of the output driver transistors change state. *Id.* at 2:43–3:37. Figure 1 is reproduced below:

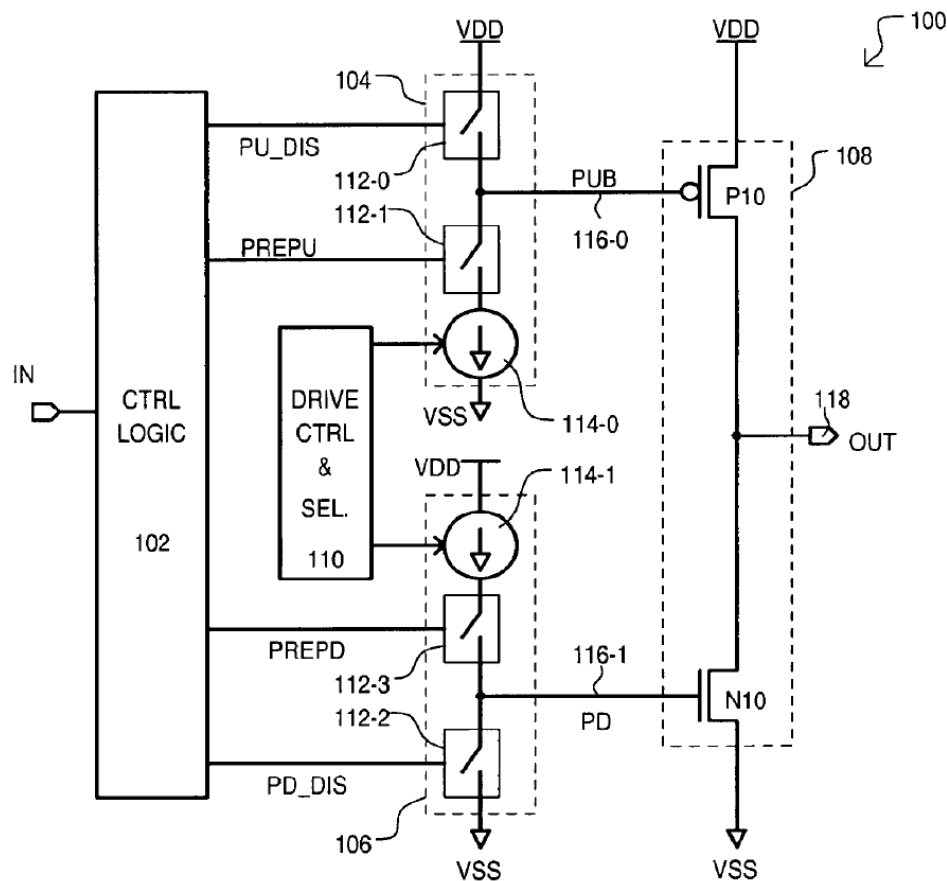


FIG. 1

Id., Fig. 1. Figure 1 depicts output buffer 100 with pull-up predriver circuit 104, pull-down predriver circuit 106, and driver section 108; pull-up predriver circuit 104 includes variable current source 114-0. The variable current source allows the drive strength of the driver transistors to “be varied without increasing or decreasing the number of driver devices, as is done in some conventional approaches.” *Id.* at 3:31–37. One implementation of the pull-up predriver circuit is shown in Figure 2A, reproduced below:

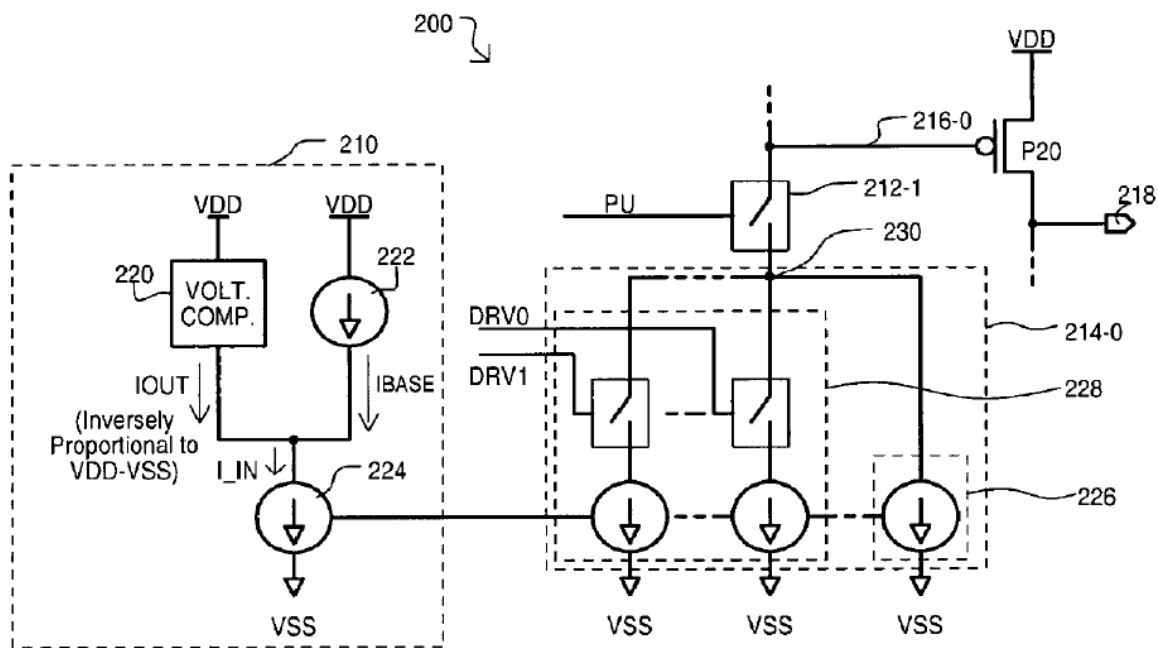


FIG. 2A

Id., Fig. 2A. Figure 2A depicts variable current source 214-0, controlled by current control section 210 and connected to the gate of output driver PFET [p-channel insulated gate field effect transistor]¹ P20 through switch element 212-1. *Id.* at 3:38–51. The described variable current source includes static section 226 and programmable section 228. *Id.* at 3:64–4:3. Programmable

¹ Ex. 1001, 2:62–63.

section 228 uses control signals DRV0 and DRV1 to allow additional transistors to sink current in parallel to static section 226. *Id.* at 4:3–12.

By configuring the variable current supply to sink or source a current that varies with power supply voltage levels, the '455 patent's buffer circuit may maintain desired rise and fall times for the output. *Id.* at 6:27–31.

E. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. An output driver circuit, comprising:
 - at least a first driver transistor having a source-drain path coupled between a first power supply node and an output node;
 - a first variable current supply that generates a current having at least one component that is inversely proportional to a power supply voltage; and
 - a first driver switch element coupled in series with the first variable current supply between a gate of the at least first driver transistor and a second power supply node, wherein the first driver switch and the first variable current supply are configured to control a rise time of the output driver circuit.

Ex. 1001, 7:13–25. Claims 2–6 and 14 depend, directly or indirectly, from claim 1. Challenged claim 7 is independent and is reproduced below:

7. An output driver circuit, comprising:
 - a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;
 - a first switch element coupled between the first driver control node and a first power supply node; and
 - a selectable current source coupled between the first driver control node and a second power supply node, the

selectable current source generating a drive current that varies in response to a drive select value,

wherein the selectable current source includes a plurality of selectable current legs, each connected to a current control node and enabled to provide a current to the current control node in response to a corresponding drive control signal.

Id. at 8:5–19. Claims 8–10 and 13 depend, directly or indirectly, from claim 7. Claim 11 is independent and recites elements similar to those of claim 7, and claim 12 depends from claim 11.

F. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:²

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	7, 8, 10, 13	102	Ozguc ³
2	7, 8, 10, 13	103	Ozguc
3	7, 8, 10–13	103	Ozguc, Huber ⁴
4	9	103	Ozguc, Wu ⁵
5	9	103	Ozguc, Huber, Wu
6	11, 12	102	Huber
7	11, 12	103	Huber
8	1–6, 14	103	Ozguc, Huber, Wu

Pet. 3–4. Petitioner also relies on the Declaration of R. Jacob Baker, Ph.D., Ex. 1002.

² The challenged claims have an effective filing date prior to March 16, 2013, the effective date of the applicable provisions of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), and therefore the pre-AIA versions of 35 U.S.C. §§ 102 and 103 apply to this Decision.

³ US 6,037,811 (issued Mar. 14, 2000) (Ex. 1006).

⁴ US 7,170,324 B2 (issued Jan. 30, 2007) (Ex. 1007).

⁵ US 5,994,945 (issued Nov. 30, 1999) (Ex. 1008).

II. ANALYSIS

A. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner proposes that a person of ordinary skill “would have had a bachelor’s degree in electrical or computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of circuits, related hardware design.” Pet. 13–14 (citing Ex. 1002 ¶ 52). Patent Owner adopts that definition. PO Resp. 13. We adopt the agreed upon level of ordinary skill as it appears to be consistent with the level of skill reflected by the specification and in the asserted prior-art references.

B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019).

Patent Owner argues that we should construe “low impedance path” in claims 7 and 11, and “driver transistor” in all challenged claims. PO Resp. 14–27. Petitioner submits that neither term requires express construction. Tr. 8:8–9.

1. “low impedance path”

In the Institution Decision, we construed “low impedance path” as “a path that permits current flow, not necessarily one with zero or non-variable impedance.” Inst. 10–11. Patent Owner submits that construction is incorrect and that a “low impedance path” is properly understood as “a path between two points that includes zero impedance.” PO Resp. 14.

One initial point warrants discussion. Patent Owner uses the nonrestrictive term “includes” in its proposed construction, and argues that Petitioner “seeks to exclude ‘zero impedance’ from the possible values of ‘low impedance.’” PO Sur-Reply 2. Indeed, Patent Owner characterizes Petitioner’s position as one of excluding zero impedance from the scope of a “low impedance path.” *Id.* That is inaccurate. Petitioner argues that a “low impedance path” is one that permits current flow, and that construction does not exclude a device with zero impedance. Tr. 14:4–20 (“[I]f you were to have a circuit element that has zero impedance, we do not believe that’s excluded by the scope of the claim.”). During the hearing, Patent Owner clarified that its view of “a low impedance path essentially is a range of resistances that can -- the driver transistor should be able to provide.” Tr. 45:8–11. Stated otherwise, Patent Owner argues that a “driver transistor that provides a low impedance path to an output node” must be able to provide a zero impedance path to the output node.

Patent Owner recognizes that the specification discusses a “low impedance path” in connection with first switch element 112-0, not with a driver transistor. PO Resp. 14–15. In that regard, the specification states that “first switch element 112-0 can provide a low or high impedance path between a high power supply node VDD and a first driver control node 116-0 in response to signal PU_DIS.” Ex. 1001, 2:35–38. Thus, the specification uses “low impedance path” as the counterpart to a “high impedance path,” to distinguish when a switch element (transistor) conducts electricity from when it does not conduct electricity.

Patent Owner argues that when first switch element 112-0 is enabled, “the drain and source of the PMOS transistor will be both at VDD.”

PO Resp. 17; *see* Ex. 1001, Fig. 1. Patent Owner relies on its contention that a transistor creating a low-impedance path will have no voltage drop between its drain and source, and further points to the specification's statement that "FIG. 5 shows . . . a conventional output buffer 500 that can drive an output 506 between a high (e.g., VDD) and low (e.g., VSS) level in response to an input signal IN." PO Resp. 18 (quoting Ex. 1001, 1:22–25, Fig. 5) (emphasis omitted). Patent Owner interprets that disclosure to establish that an output driver transistor must cause the drain or output node to fully reach the voltage provided to the source or input node. Patent Owner submits that the output node reaching the supply voltages means the driver transistor has zero impedance. *Id.* at 19.

Petitioner submits that no FET⁶ can actually have zero impedance, as they have an internal resistance. Pet. Reply 6–7 (citing Ex. 1018, 81:16–23, 82:10–13). A device such as a transistor will experience a voltage drop across the device when current flows through it; when no current flows, there will be no voltage drop. But that doesn't mean the device has zero impedance when there is no voltage drop across the device because no current is flowing through the device. *See* Tr. 11:22–13:11 (discussing the discontinuity in Patent Owner's theory of zero impedance; citing Ex. 2004 (defining impedance as including a resistance component); Ex. 2005 (same)). Rather, the impedance of a transistor changes depending on its gate voltage, and expresses the relationship between current flow and voltage

⁶ Field-effect transistor, a device that uses electric field to control current flow. *See* Ex. 1011, 111, 747–48 (page numbers as added by Petitioner).

difference across the device. *See* Ex. 1002 ¶ 19; Pet. Reply 5–6.⁷ We agree with Petitioner that a transistor does not have “zero impedance” simply because it has no source-drain voltage difference, and that a “low impedance path” does not require a transistor with zero impedance.

Indeed, Petitioner’s view of a low impedance path is consistent with the specification. Petitioner points out that the specification describes that “a variable current source 114-0 can source a current from first control node 116-0 (provided switch element 112-1 is in a low impedance state).” Ex. 1001, 2:44–46; *see* Pet. Reply 3–4. Thus, the specification describes switch element 112-1 as operating in a “low impedance state” notwithstanding that the current flowing through it would experience some

⁷ Patent Owner submits also that the Institution Decision incorrectly viewed the specification’s description of an output buffer’s variable drive strength. PO Resp. 23–24 (discussing Ex. 1001, 3:34–37). Drive strength refers to how quickly an output buffer can transition between voltages. Ex. 2001 ¶ 82 (“the drive strength of the output buffer (i.e., how quickly it can transition from VDD to ground and vice versa)”). According to Patent Owner, when the specification discloses that “drive strength of the output driver can vary according to how the current from current source 114-0 is varied,” it refers only to the currents flowing in or out of the “driver control node,” i.e., the output driver gate (*see* Ex. 1001, 2:66–67). PO Resp. 24. Although variable currents in or out of a driver transistor’s gate—through current sources 114-0 and 114-1, for example—do not themselves represent variable drive strength, those gate currents are how the ’455 patent proposes to effect variable drive strength. Ex. 1001, 3:31–37. As Petitioner’s expert, Dr. Baker, explains, a transistor’s “source-drain impedance depends on the voltage difference between the gate and source terminals (V_{GS}).” Ex. 1002 ¶ 23. We credit that testimony, which supports that the driver transistor’s gate-source voltage affects the drive strength by affecting the driver transistor’s impedance.

voltage drop. The specification does not clearly establish that a driver transistor uses a different definition of “low impedance path.”

Patent Owner asserts that Petitioner’s expert agreed that a “low impedance path” requires a transistor capable of zero impedance. PO Resp. 20–21. We do not agree. Petitioner’s expert, Dr. Baker, agreed that a transistor (in the example he considered, a P-channel MOSFET, or PMOS, with its gate voltage held low) would have its source and drain at the same voltage only when no current is flowing in the device. Ex. 2003, 49:4–50:3. Patent Owner reasons that that supports that “a ‘low impedance path’ includes the case where there is zero voltage drop between the source and drain, or zero impedance.” PO Resp. 22. As an initial matter, Dr. Baker did not equate zero voltage drop with zero impedance. Moreover, Patent Owner’s conclusion that a low impedance path may include a device with zero voltage drop is beside the point—that is not in dispute. As discussed above, the dispute is whether a “low impedance path” *requires* zero impedance. Dr. Baker’s testimony does not support Patent Owner’s position in that regard.

In our view, the correct construction for “low impedance path” recognizes that neither the claims nor the specification provide a special meaning for the path through the driver transistors. Rather, the claim language uses “low impedance path” to indicate that a driver transistor allows current to flow to influence the driver transistor’s output node voltage. We maintain our construction from the Institution Decision that a “low impedance path” is “a path that permits current flow, not necessarily one with zero or non-variable impedance.”

2. “driver transistor”

Claim 1 recites “at least a first driver transistor having a source-drain path coupled between a first power supply node and an output node,” and claims 7 and 11 recite “a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node.” Ex. 1001, 7:14–16, 8:6–8, 8:41–43. Patent Owner argues that “driver transistor,” as used in all challenged claims, means “a transistor that can provide a low impedance path to an output node.” PO Resp. 25–26. Petitioner submits that Patent Owner’s proposed construction “replaces a simple term with additional limitations not recited by the claim language” and that no construction is required. Pet. Reply 8.

We decline to construe “driver transistor” because, as explained below, we do not agree that the prior art lacks a “low impedance path” as we have construed it above. Thus, whether a driver transistor must provide a low-impedance path has no bearing on our unpatentability determination.

C. ANTICIPATION BY OZGUC

Ozguc discloses a “current-controlled output buffer circuit.” Ex. 1006, code (57). Ozguc’s circuit uses a charging circuit and discharging circuit to control the output signal, where “[t]he charging circuit is configured to receive the charging signal and, in response, supplies a charging current to an output terminal; the magnitude of the charging current produces a signal rise time.” *Id.* at 1:44–47. The discharging circuit operates similarly, controlling the signal fall time. *Id.* at 1:47–51. Ozguc’s Figure 1 is reproduced below:

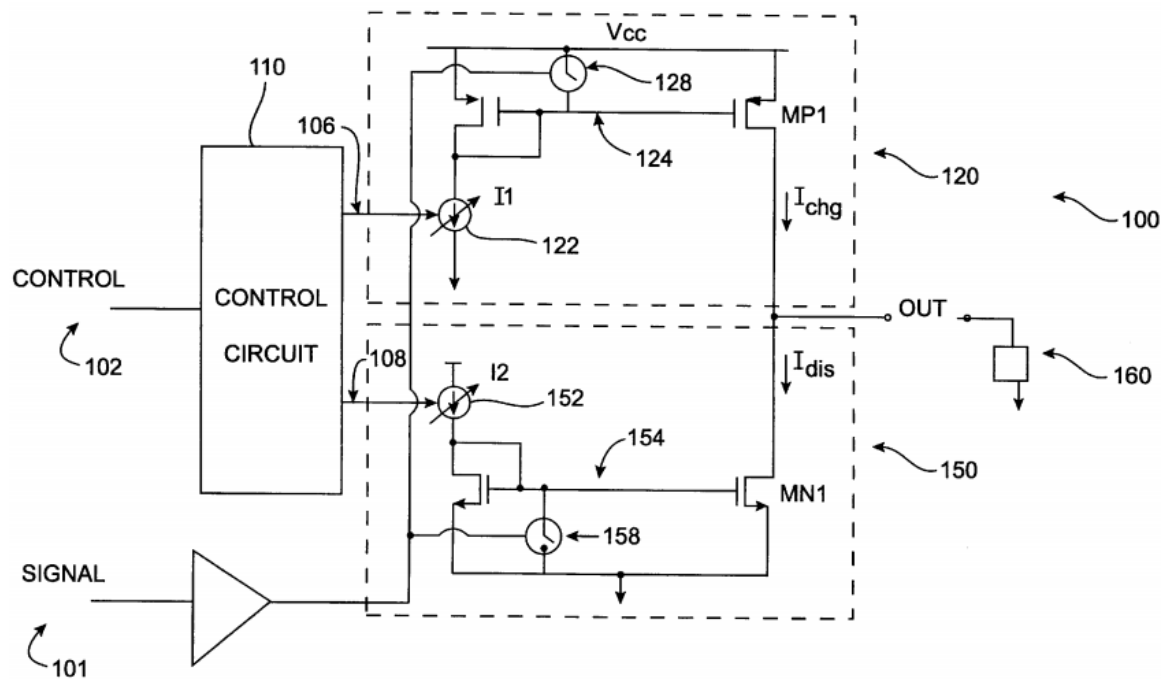
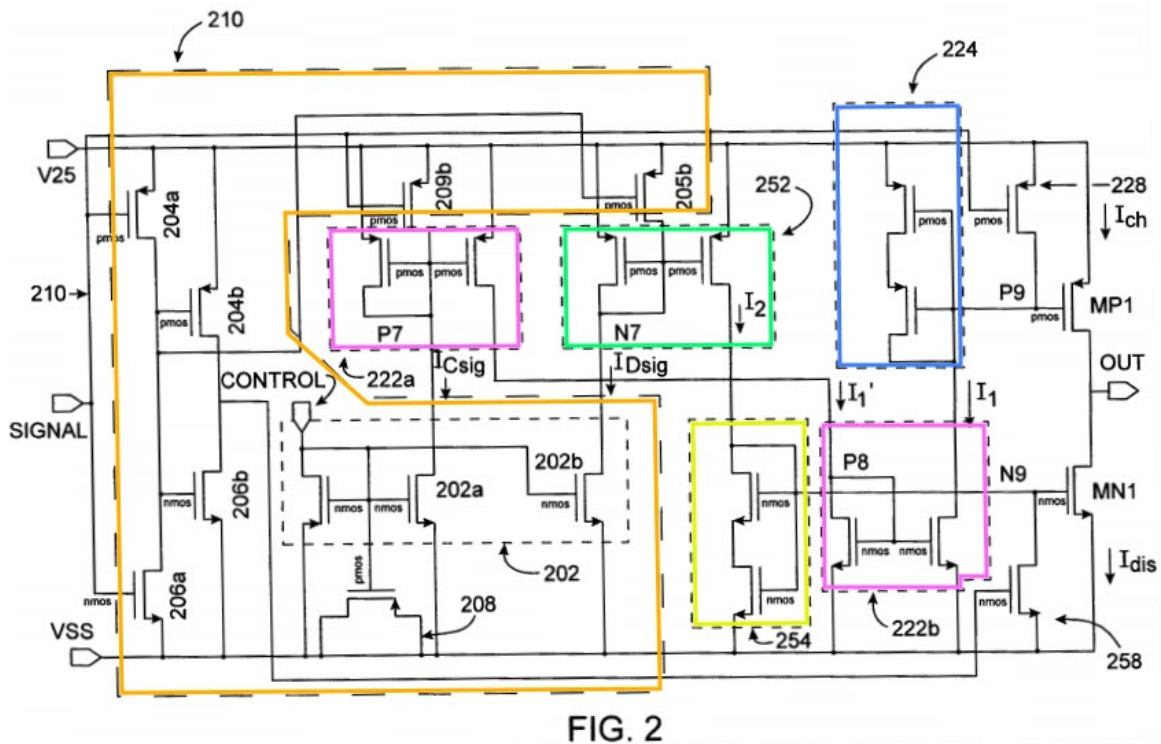


FIG. 1

Id., Fig. 1. Figure 1 depicts a simplified block diagram of the current-controlled output driver circuit 100, including control circuit 110, charging transistor MP1, discharging transistor MN1, first adjustable current source 122, and second adjustable current source 152. *Id.* at 1:66–2:20. Input signal 101 “controls switches 128 and 158 to alternately activate the charging and discharging transistors MP1 and MN1.” *Id.* at 2:21–30. By varying the gate voltages of those transistors, the charge and discharge current provided to the output terminal may be controlled, therefore controlling the rise and fall times of the output signal. *Id.* at 2:8–44. Ozguc discloses an exemplary circuit implementation in Figure 2, reproduced below:



Id., Fig. 2 (colored annotations added). Figure 2 depicts control circuit 210 (annotated in orange), first adjustable current source 222 (annotated in pink), current mirror 224 (annotated in blue), second adjustable current source 252 (annotated in green), current mirror 254 (annotated in yellow), charging transistor MP1, and discharging transistor MN1. *Id.* at 2:45–65. Through operation of the adjustable current sources and current mirrors, Ozguc’s Figure 2 circuit allows control signal CONTROL to define the rise and fall times of the output signal at OUT by controlling charging current I_{ch} and discharging current I_{dis} .⁸ *Id.* at 2:66–4:9.

⁸ Ozguc uses I_{ch} in Figure 2 and I_{chg} in the written description, both referring to the output charging current through transistor MP1. *See* Ex. 1006, 3:7–4:9, Fig. 2.

1. Claim 7

Petitioner maps the claimed first driver transistor to Ozguc's charging transistor MP1. Pet. 19–20. It maps the claimed first switch element to Ozguc's switch 128, and the claimed selectable current source to Ozguc's first adjustable current source 122. *Id.* at 20–23. As to the selectable current source including a plurality of selectable current legs as claimed, Petitioner relies on Ozguc's Figure 3 as showing the details of its current source. *Id.* at 24–26.

Patent Owner argues that Ozguc does not disclose a “driver transistor that provides a low impedance path” as recited in claims 7 and 11 because Ozguc's charging transistor MP1, which Petitioner maps to the claimed driver transistor, does not have zero impedance. PO Resp. 36–43. As discussed above, we do not agree with Patent Owner's proposed construction. *See supra* at 7–11. Thus, we do not agree with Patent Owner's argument that Ozguc lacks a low impedance path because its charging transistor does not achieve zero impedance.⁹

Patent Owner argues also that Ozguc lacks the claimed driver transistor even under Petitioner's construction because Ozguc's MP1 gate

⁹ Petitioner argues that Ozguc operates the same as the '455 patent's disclosed embodiments, in that (1) Ozguc's output (like the '455 patent's) would reach Vdd, the positive power-supply voltage, when driving a capacitive load or no load; and (2) the '455 patent's output (like Ozguc's) would not reach Vdd when driving a resistive load. Pet. Reply 8–16. While our unpatentability determination relies on the reasoning discussed elsewhere in this Decision, we note that Petitioner provides persuasive evidence to support its argument (e.g., Ex. 1018, 57:10–59:2, 61:16–62:12, 63:24–64:8), and that the claimed circuits are not limited to a particular load. This provides an additional basis on which we would conclude at least that Ozguc anticipates claims 7, 8, 10, and 13.

connects to Vcc through a PMOS transistor (unlabeled in Ozguc's Figure 1) and connects to ground through current source 122. PO Resp. 46. Thus MP1's gate voltage depends on the voltage drop across the PMOS transistor and the voltage drop across current source 122. *Id.* In Patent Owner's view, Petitioner's expert, Dr. Baker, relied on MP1's gate being *at* ground (not merely close to it) in order to assert that MP1 provided a "low impedance path" to the output node. *Id.* (citing Ex. 2003, 50:4–11). Patent Owner submits that because MP1's gate is never exactly at ground voltage, it "will never be 'fully on.'" *Id.* at 46, 48–49.

We do not agree with Patent Owner. There is no requirement, in the claim language or in our construction for "low impedance path," that a transistor provide its lowest-possible impedance. Dr. Baker refers to a PMOS transistor conducting when its gate voltage is "low," and explained that means "generally ground." Ex. 2003, 39:4–24.

We find nothing inconsistent between Dr. Baker's explanation and Ozguc's disclosures. Although Ozguc's current source 122 may result in MP1's gate having a slight voltage difference from ground, Ozguc discloses that, "[w]hen the input signal 101 is high, switch 128 is turned off, allowing the charging transistor MP1 to conduct." Ex. 1006, 2:24–26. When MP1 conducts, it creates a "low impedance path" as claimed. *See supra* at 7–11. We agree with Petitioner that Patent Owner's argument would require a claim construction that we have not adopted. *See* Pet. Reply 17–18.¹⁰

¹⁰ Patent Owner raises the same argument as to Ozguc's MN1. PO Resp. 49. We reach the same conclusion, for the same reasons, as discussed regarding Ozguc's MP1.

Patent Owner does not otherwise dispute Petitioner’s anticipation contentions for claim 7. We conclude Patent Owner has waived any such arguments. *See* Paper 8, 8 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”); *In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016); PTAB Consolidated Trial Practice Guide 52 (Nov. 2019) (“CTPG”), *available at* <https://www.uspto.gov/about-us/news-updates/consolidated-trial-practice-guide-november-2019>.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that Ozguc anticipates claim 7. Pet. 14–26.

2. Claims 8, 10, and 13

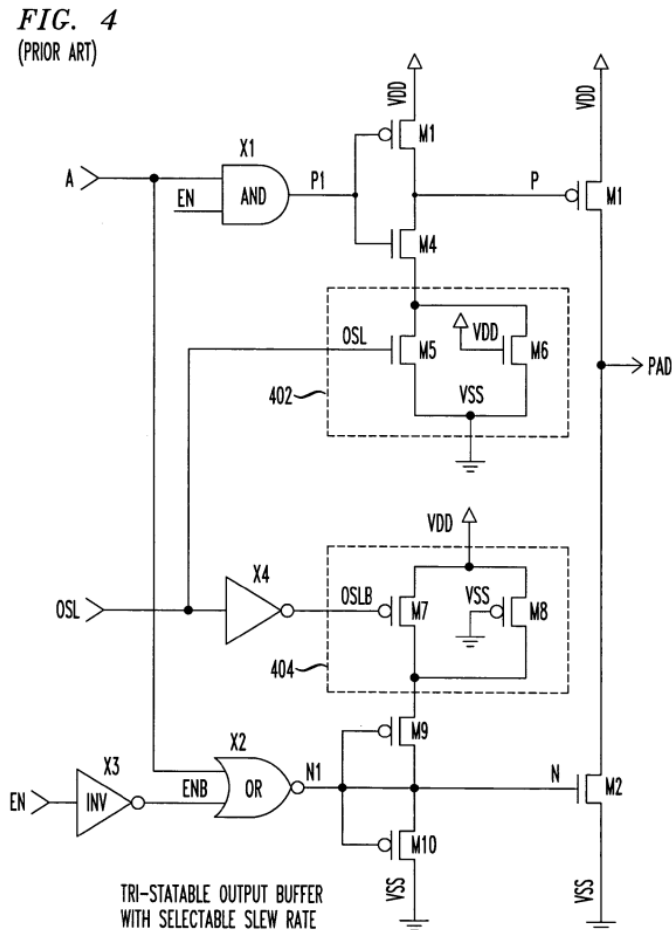
Petitioner challenges also dependent claims 8, 10, and 13 as anticipated by Ozguc. Pet. 26–38. Other than as discussed regarding claim 7, Patent Owner does not dispute Petitioner’s anticipation contentions for claims 8, 10, or 13. *See* PO Resp. 35–49. We conclude Patent Owner has waived any such arguments. *See* Paper 8, 8; *NuVasive, Inc.*, 842 F.3d at 1380–81; CTPG 52.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that Ozguc anticipates claims 8, 10, and 13. Pet. 26–38.

D. OBVIOUSNESS OVER OZGUC AND HUBER

Huber describes an output buffer with adjustable slew rate control. Ex. 1007, code (57). Huber explains that slew rate refers to the “maximum rate that the output voltage of a buffer can change” (*id.* at 1:36–37) and that prior-art designs permitted output slew rate “to be switched between two

pre-determined values” (*id.* at 1:46–48). Huber’s Figure 4 depicts a prior-art output buffer with slew rate control and is reproduced below:



Id., Fig. 4. Figure 4 depicts slew rate control circuit 402, with transistor M4 connecting the gate of output transistor M1 (node P) to slew rate control circuit 402, which uses transistors M5 and M6 in parallel to connect the gate of output transistor M1 to ground (turning on transistor M1). *Id.* at 2:4–12 (describing Figure 3, which includes the aspects of Figure 4 other than slew rate control), 2:51–3:57. Huber discloses that “[t]he slew rate of the output signal PAD from the buffer is controlled by the speed at which nodes N and P are switched.” *Id.* at 2:3–5. Huber notes that because prior designs used a slew rate control circuit in series with transistor M4, the sizes of the

transistors had to be increased to allow the same current flow. *Id.* at 3:7–16, 3:58–61. Thus, Huber proposes a different arrangement, depicted in Figure 1, where the slew rate control circuit is integrated with the transistors that selectively connect the output transistors’ gates to their control voltages. *Id.* at 4:3–29, 5:1–6:31, Fig. 1.

For obviousness of the subject matter of claims 7, 8, and 10–13, Petitioner primarily relies on Ozguc as discussed above regarding anticipation, and argues that skilled artisans had reason “to modify Ozguc’s buffer circuit in view of Huber to improve performance, including (1) the buffer’s ability to control the rise and fall times of the output without unintended delays, and (2) power efficiency.” Pet. 43 (citing Ex. 1002 ¶ 100); *accord id.* at 48. Petitioner explains that the critical performance metric relates to “how fast a buffer can alternate between the pull-up and pull-down operations.” *Id.* And Petitioner explains how Ozguc’s “shut-off delay leads to potential power waste and unintended delays in output transition.” *Id.* at 44. Thus, Petitioner proposes a combination in which Huber’s transistor M4 is added to Ozguc’s circuit, as shown in an annotated version of Ozguc’s Figure 1, reproduced below:

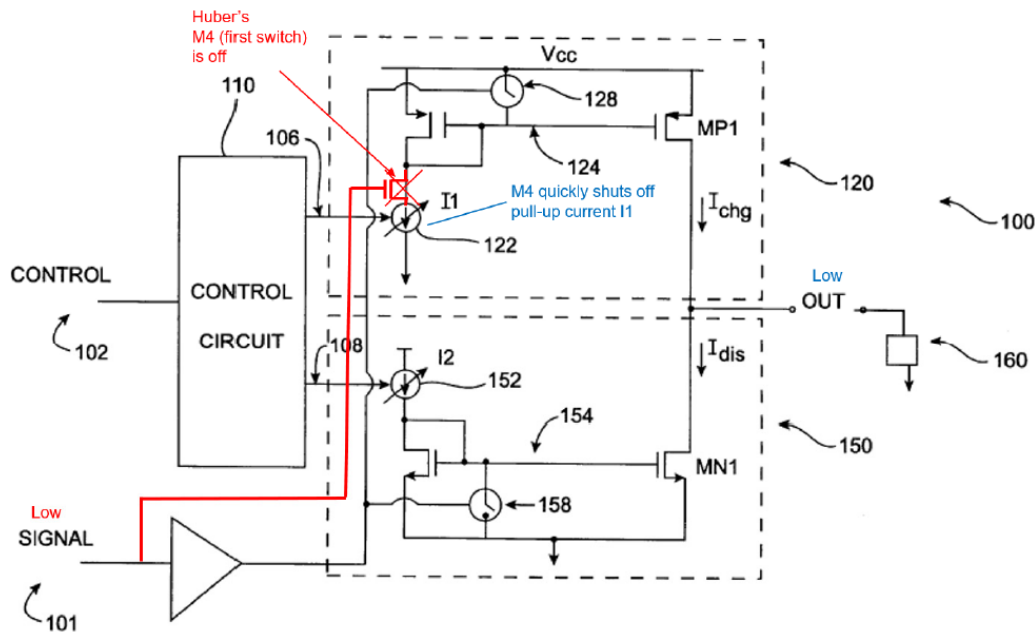


FIG. 1

Pet. 47. The annotated figure depicts Huber's transistor M4 in red, added to Ozguc's circuit between adjustable current source 122 and the power supply Vcc. Petitioner reasons that the modification would make it possible "to shut off the pull-up current (I_1) with minimal delay." *Id.* at 46.

Patent Owner challenges whether a skilled artisan would have had reason to modify Ozguc as Petitioner asserts. Patent Owner asserts that Petitioner improperly relies on Huber to assert that transistor M4 (which is in Huber's pull-up circuit) will allow the pull-down circuit to pull the output pad low quickly. PO Resp. 55.

We conclude that Petitioner's reliance is not improper. While Huber discloses a circuit with multiple interacting elements, Petitioner reasonably explains that using transistor M4 to quickly shut off the pull-up current when the input transitions low minimizes interference with the pull-down circuit. Pet. 45 (citing Ex. 1002 ¶ 104). Although other circuit elements—such as Huber's M7 and M2—actively pull the output pad low, that M4 plays a role

in that transition is both logical and supported by Dr. Baker. Ex. 1002 ¶ 104. Moreover, Petitioner connects the modification to a specific deficiency in Ozguc's circuit—that a chain of circuit elements delays shut off of the pull-up drive current. Pet. 44 (citing Ex. 1002 ¶ 103).

Patent Owner argues that because the proposed combination places Huber's transistor M4 in the same location (above the pull-up circuit current source) as depicted in the '455 patent, Petitioner's combination evidences hindsight. PO Resp. 56–57. We, however, agree with Petitioner that the desire to isolate Ozguc's current source 122 motivates the location of Huber's transistor M4 in the combination. *See* Pet. Reply 21–24.

Next, Patent Owner argues that Huber teaches away from the proposed combination, because it discloses that adding additional transistors in series with M4 would require increasing the size of the transistors to maintain drive strength (thus increasing the size of the overall circuit). PO Resp. 59–61. We recognized that aspect of Huber in the Institution Decision. Inst. 13. While Huber addresses the potential size increase by proposing a parallel, rather than series, arrangement of transistors (Ex. 1007, 5:39–44), that does not necessarily teach away from the proposed combination. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (“A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.”). As Petitioner points out, Huber teaches that implementing adjustable slew rate with a series transistor arrangement offers advantages that may be maintained with its proposed parallel arrangement. Ex. 1007, 5:1–6; Pet. Reply 21. We agree with Petitioner that Huber does

not teach away from the series arrangement that uses transistor M4. Additionally, while there may be some disadvantage to the proposed combination (increased circuit size), that does not undermine the reason that a skilled artisan would have made the combination. *Winner Int'l Royalty Corp. v. Wang*, 202 F. 3d 1340, 1349 n.8 (Fed. Cir. 2000) (“The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another.”). We find that skilled artisans had reason to modify Ozguc with Huber’s transistor M4 for the reasons discussed, notwithstanding that doing so would have increased the circuit size.

Patent Owner argues also that adding Huber’s transistor M4 would have increased power dissipation, by causing an additional voltage drop when current is flowing through adjustable current source 122. PO Resp. 62–63. As with the potential increase in circuit size, we find that the potential of increased on-state power dissipation does not outweigh the advantage in switching speed and off-state power consumption. In that regard, we agree with Petitioner that the proposed combination addresses the off-state and transition behavior of Ozguc’s circuit. *See* Pet. Reply 18–21. The factual basis for that conclusion is supported by testimony from Patent Owner’s expert, Mr. Robert Zeidman, explaining that a switch would eliminate off-state current in current source 122. *Id.* at 20–21 (citing Ex. 1018, 41:4–42:1).

Finally, Patent Owner argues that using Huber’s transistor M4 in isolation, without transistors M5 and M6, would not work. PO Resp. 63–65. We do not agree. Huber explains that M5 and M6 implement part of the “slew rate control circuit 402,” which is used to control the speed at which

the gates of the output drivers transition. Ex. 1007, 2:4–5, 2:44–46, 2:59–61. In the proposed combination, variable drive strength is achieved with Ozguc’s adjustable current source 122 (Ex. 1006, 2:8–14), so there would be no need for Huber’s transistor’s M5 and M6.

Patent Owner offers no further arguments contesting the obviousness of the subject matter of claims 7, 8, or 10–13 over Ozguc and Huber. We conclude Patent Owner has waived any such arguments. *See* Paper 8, 8; *NuVasive, Inc.*, 842 F.3d at 1380–81; CTPG 52.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that the combination of Ozguc and Huber renders obvious the subject matter of claims 7, 8, and 10–13. Pet. 39–56.

E. OBVIOUSNESS OVER OZGUC AND WU

Claim 9 depends from claim 7 and recites “the selectable current source further includes a reference current source that provides a reference current having at least one component that is inversely proportional to a power supply voltage, and each of the selectable current legs provides a current proportional to the reference current.” Ex. 1001, 8:27–32. Petitioner submits that Wu discloses that additional limitation and that skilled artisans had reason to incorporate Wu’s relevant circuitry into Ozguc’s device. Pet. 57–66.

Wu discloses a circuit for compensating for variations in both temperature and power-supply voltage. Ex. 1008, code (57). To that end, Wu’s compensation circuit includes multiple current sources, “each of which generates a corresponding compensation current.” *Id.* at 1:62–67. In one of the disclosed compensation circuits, the control current has “a negative slope

with respect to the V_{CC} supply voltage.” *Id.* at 2:60–63. Wu states that its circuit is applicable to compensate “input/output buffer circuits.” *Id.* at 2:33–36.

Petitioner asserts that it would have been obvious to modify Ozguc’s circuit to use Wu’s current-compensation circuit, which supplies a stable current for buffer circuits such as Ozguc’s. Pet. 57–63. Doing so, in Petitioner’s view, would result in an output-driver circuit in which the reference current has a “component that is inversely proportional to a power supply voltage,” as claimed. *Id.* at 64–65. Petitioner reasons that Ozguc discloses a reference “CONTROL” current is provided to its circuit but “does not disclose how this current is generated.” *Id.* at 60. Petitioner contends that using Wu’s compensation circuit to provide the current would “improve the consistency of [the circuit’s] performance (*e.g.*, the rise/fall times) under a variety of operating conditions (*e.g.*, temperature or supply voltage variation).” *Id.* at 60–61.

Patent Owner argues that a skilled artisan would not have been motivated to combine Wu with Ozguc. In Patent Owner’s view, Wu’s compensation circuit outputs voltage, not current, and therefore could not have been combined as Petitioner asserts. PO Resp. 71–74. Patent Owner argues additionally that following Petitioner’s purported combination would render Wu’s compensation circuit inoperable. *Id.* at 75–77.

Wu depicts its “compensation circuit 230” as part of a larger circuit to control current provided to an output node. Ex. 1008, Figs. 2, 3. Wu discloses that the combined circuit results in a target current that is the combination of four different compensation components. *Id.* at 5:27–33. Wu, however, states that its compensation circuit 230 includes four compensating

current sources 301–304 and a summing circuit 310, and that the compensation currents “are added within summing circuit 310, thereby creating a total compensation current I_{target} .” *Id.* at 5:24–31.

Petitioner responds that it clearly relies on Wu’s current output, not the compensation circuit in isolation. Pet. Reply 30–32. We agree with Petitioner. The Petition identifies that one of Wu’s compensation current components, I_C , is inversely proportional to the V_{CC} supply voltage. Pet. 58 (citing Ex. 1008, 6:28–57; Ex. 1002 ¶¶ 121–123). It identifies that Wu’s compensation circuit is designed to provide stable current for buffers like Ozguc’s. *Id.* at 60 (citing Ex. 1008, 2:28–48, 6:42–57). And the Petition asserts that “Wu’s compensation circuit can be used to feed a compensated control current (I_{Total}) to Ozguc’s buffer,” as depicted in annotated versions of Ozguc’s Figures 1 and 2. *Id.* at 61–63. The Petition asserts that it would also have been obvious “to use Wu’s compensated current (I_{Total}) as a source for Ozguc’s pull-down current I_2 .” *Id.* at 63.

Although Patent Owner argues that Petitioner gets details of the combination wrong by not specifying precisely which of Wu’s transistors would be included and where they would be located in Ozguc’s circuit (PO Resp. 73–74), the Petition’s contentions are both logical and readily understandable. Petitioner’s exemplary circuits are properly understood as schematic in nature, and need not include all details of a final implementation. *Cf. In re ICON Health and Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) (“[W]e do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art.”) (holding that skilled artisans would appropriately configure a prior-art device when incorporating it into a new context). For the same reason, we do

not agree with Patent Owner that the proposed combination would render Wu's circuit inoperable. *See* PO Resp. 75–77. A skilled artisan would understand from Wu's cited disclosures that its compensation circuit is capable of creating the desired current and would have been able to apply Wu's circuit in combination with Ozguc. Ex. 1002 ¶¶ 122–123, 128–129, 131–132. We disagree with Patent Owner's arguments to the contrary. We find that skilled artisans had reason to combine Wu and Ozguc as Petitioner asserts, and that doing so would have resulted in claim 9's circuit.

Accordingly, we conclude that Petitioner has shown by a preponderance of the evidence that the combination of Ozguc and Wu renders obvious the subject matter of claim 9.

F. OBVIOUSNESS OVER OZGUC, HUBER, AND WU

Claim 1 recites, *inter alia*, “a first variable current supply that generates a current having at least one component that is inversely proportional to a power supply voltage,” a limitation that closely parallels that of claim 9, discussed above. *See supra* at 23. Petitioner asserts that skilled artisans would have combined Wu's teachings regarding its compensation circuit with Ozguc's circuit, and that the combination discloses the above limitation. Pet. 75–77.

Claim 1 also recites “a first driver switch element coupled in series with the first variable current supply between a gate of the at least first driver transistor and a second power supply node, wherein the first driver switch and the first variable current supply are configured to control a rise time of the output driver circuit.” Petitioner asserts that skilled artisans would have found it obvious to add Huber's transistor M4 to Ozguc's circuit

for the same reasons discussed above regarding the similar limitation in claim 7. *See supra* at 17–20; Pet. 77–78.

For the other limitations of claim 1, Petitioner relies on Ozguc’s disclosures, as for the similar limitations in claim 7. Pet. 74. Thus, Petitioner reasons that the combination of Ozguc, Huber, and Wu renders claim 1 obvious. Patent Owner contests that conclusion for the same reasons discussed above regarding obviousness over Ozguc and Wu and over Ozguc and Huber. PO Resp. 83–84. Patent Owner additionally argues that the asserted combination lacks a “driver transistor” under Patent Owner’s proposed construction. *Id.* at 84; *see supra* at 12. For the reasons already discussed, we conclude that Petitioner’s arguments are persuasive and do not agree with Patent Owner’s arguments to the contrary.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that the combination of Ozguc and Huber renders obvious the subject matter of claims 1–6 and 14. Pet. 74–105.

G. PATENT OWNER’S MOTION TO EXCLUDE

Patent Owner moves to exclude a portion of the transcript from Dr. Baker’s deposition (Ex. 2003, 82:4–92:2), which Patent Owner asserts exceeded the proper scope of redirect examination and improperly presented new opinions. Paper 19. We do not rely on the objected-to portion of the transcript in reaching this Decision. Accordingly, we dismiss Patent Owner’s motion as moot.

III. CONCLUSION¹¹

For the reasons discussed, we conclude:

Claim(s)	35 U.S.C. §¹²	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
7, 8, 10, 13	102	Ozguc	7, 8, 10, 13	
7, 8, 10, 13	103	Ozguc		
7, 8, 10–13	103	Ozguc, Huber	7, 8, 10–13	
9	103	Ozguc, Wu	9	
9	103	Ozguc, Huber, Wu		
11, 12	102	Huber		
11, 12	103	Huber		
1–6, 14	103	Ozguc, Huber, Wu	1–6, 14	
Overall Outcome			1–14	

¹¹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

¹² We do not reach grounds 2, 5, 6 or 7 (*see supra* at 6) because doing so would not change the overall outcome of this Decision. See *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. Apr. 30, 2020) (nonprecedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding” and, thus, agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

IV. ORDER

It is

ORDERED that Petitioner has proven that claims 1–14 of the '455 patent are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed* as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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