

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

IPR2020-01336
Patent 7,012,463 B2

Before JEFFREY S. SMITH, SCOTT A. DANIELS, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

DANIELS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

On July 20, 2020, Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–7, 10–17, and 29 of U.S. Patent No. 7,012,463 B2, issued on March 14, 2006 (Ex. 1001, “the ’463 patent”). Paper 2 (“Pet.”). Analog Devices, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Following our Institution Decision, (Paper 9, “Inst. Dec.”), Patent Owner filed a Response. Paper 12 (“PO Resp.”). Petitioner filed a Reply. Paper 15 (“Reply”). Patent Owner filed a Sur-Reply. Paper 18 (“PO Sur-Reply”). A hearing was held on November 4, 2021. A transcript of the hearing has been entered as Paper 23 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claims 1, 2, 4, and 6 are unpatentable and that claims 3, 5, 7, 10–17 and 29 are not unpatentable.

B. Additional Proceedings

The parties identify the following district court proceeding concerning the ’463 patent: *Analog Devices, Inc. v. Xilinx, Inc.*, No. 1:19-cv-02225-RGA (D. Del.). Pet. 1; Paper 4.

C. Real Party-in-Interest

The Petition identifies Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. as real parties-in-interest. Pet. 1. Patent Owner identifies itself as the real party-in-interest. Paper 4.

D. The '463 Patent (Ex. 1001)

The '463 patent relates to an integrated circuit having dual mode differential amplifiers and switched capacitor circuitry including a common-mode feedback loop for reducing the common-mode gain. Ex. 1001, 1:6–29. The '463 patent explains that

[w]hen the switched capacitor circuit is coupled to the differential amplifier, the capacitors can sense the average or common-mode of the output and then compare the average with a desired common-mode. The difference between the average common-mode and the desired common-mode can be used in a feedback loop which drives the difference to zero.

Id. at 1:33–40. The '463 patent further describes that errors occur in the common mode feedback loop producing common-mode error gain that varies between one clock phase and the next. *Id.* at 1:41–49. According to the '463 patent, it is desirable to reduce such variation and “to have the same common-mode when switching between phases to minimize the dependence of the output signal on the common-mode.” *Id.* at 1:54–57. This variation from one clock phase to another is also referred to in the '463 patent as the “signal offset level.” *Id.* at 2:40–41, 14:11–15.

To solve this problem the '463 patent describes a common-mode circuit utilizing differential amplifiers to obtain an output, a common-mode corrector circuit including a common-mode feedback circuit for determining a feedback signal offset level, and an impedance matching error correcting circuit connected to the common-mode corrector circuit that adjusts, *i.e.*, corrects, the signal offset level. *Id.* at 2:3–12. Figure 1 of the '463 patent is reproduced below.

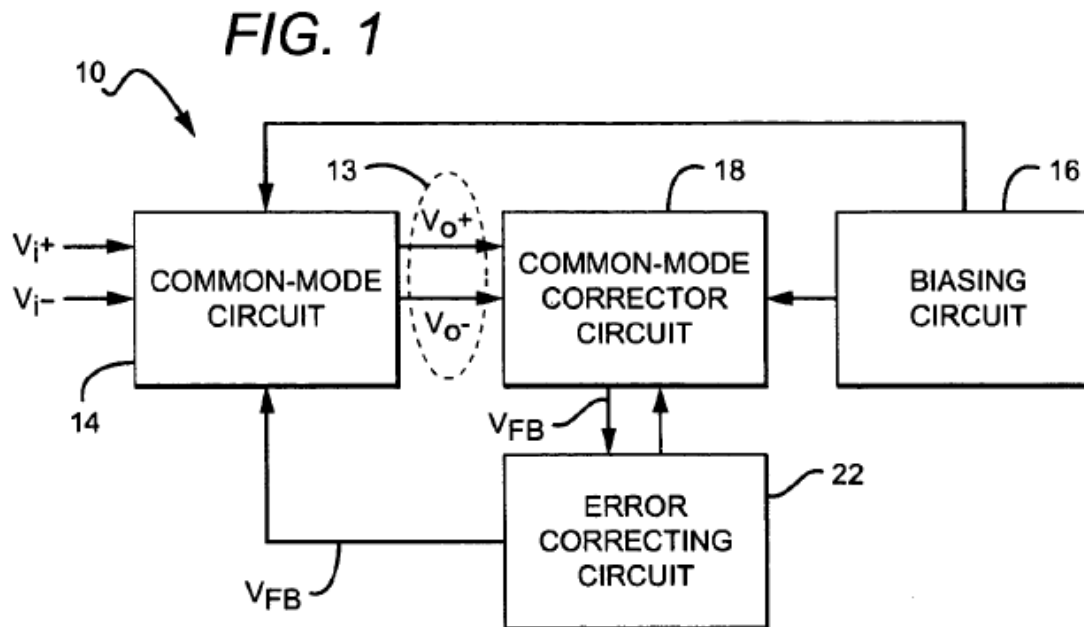


Figure 1 of the '463 patent, above, illustrates a block diagram of signal conditioning system 10 having common-mode circuit 14 including differential input terminals V_{i+} and V_{i-} , and having differential output terminals V_{o+} and V_{o-} (defining output port 13) connected to common-mode corrector circuit 18. *Id.* at 3:13–24. Common-mode corrector circuit 18 determines a feedback signal V_{FB} for common-mode circuit 14 and error correcting circuit 22 is coupled between corrector circuit 18 and common-mode circuit 14 to provide feedback signal error correction. *Id.* Biasing circuit 16 is coupled to corrector circuit 18 and common-mode circuit 14 and provides power and a set operating point to common-mode circuit 14. *Id.* at 3:24–27.

E. Illustrative Claims

Of the challenged claims, claims 1 and 11 are independent. Each of dependent claims 2–7 and 10 depend from claim 1, and claims 12–17 and 29 depend from claim 11. Claims 1 and 11 illustrate the claimed subject matter

and are reproduced below with particular limitations of importance highlighted (bracketed limitation numbering added):

1. [1A] A circuit with a common-mode dual output comprising:
 - [1B] a common-mode circuit with an output portion;
 - [1C] a common-mode corrector circuit connected to alternate the states of said output portion between an average output level and a desired common-mode level, the difference between the average and desired levels being proportional to a signal offset level; and
 - [1D] *an error correcting circuit connected to said common mode corrector circuit to adjust the signal offset level;*wherein said common-mode corrector circuit further includes:
 - [1E] a common-mode voltage terminal connected to said output portion through a first pair of switches, said first pair of switches being responsive to alternating clock cycles which alternate the states of said output portion;
 - [1F] a bias terminal providing a bias level, said bias terminal being connected to a first control terminal in said common-mode circuit through a second pair of switches, said second pair of switches being responsive to the alternating clock cycles,
 - [1G] a precharging capacitor which stores the difference between the desired common-mode level and the bias level during a first clock cycle in the alternating clock cycles, and
 - [1H] a common-mode capacitor which stores the average output level during the first clock cycle, said common-mode capacitor and said precharging capacitor being connected in parallel during a second clock cycle in the alternating clock cycles.
11. [11A] An integrated circuit, comprising:
 - [11B] a differential amplifier circuit with an output portion and a current sinking portion, said output portion including dual outputs which provide an average output level;

[11C] a common-mode feedback circuit coupled to said output portion, said feedback circuit providing a desired common-mode level in a first operational mode *and generating a feedback signal proportional to the difference between the average output level and the desired common-mode level in a second operational mode*, the feedback signal being coupled to said current sinking portion; and

[11D] *an impedance matching circuit connected to said feedback circuit to adjust the feedback signal*;

[11E] wherein the desired common-mode signal is provided to a precharging capacitor in the first operational mode, said precharging capacitor including a terminal coupled to said impedance matching circuit.

Ex. 1001, 14:9–51, 15:23–40 (emphases added).

F. Level of Ordinary Skill in the Art

Petitioner, supported by the testimony of Dr. Holberg, argues that a person of ordinary skill in the art

would have at least a Master’s Degree in Electrical Engineering or equivalent field, including studies in the area of analog circuitry, or at least a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuitry design.

Pet. 33 (citing Ex. 1002 ¶¶ 18–19).

Patent Owner does not address the level of ordinary skill in its Response. *See generally* PO Resp. Patent Owner’s declarant, Dr. Peter Kinget, testifies that Petitioner’s proposed level of education and experience for a person of ordinary skill is reasonable. Ex. 2002 ¶ 9.

For purposes of this decision, we adopt Petitioner’s proposal because it is consistent with the ’463 patent and the asserted prior art and not disputed by Patent Owner.

G. Claim Construction

We interpret claims in the same manner used in a civil action under 35 U.S.C. § 282(b) “including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. §42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)).¹ Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner contends it has construed all claim terms according to this standard, but does not propose any express constructions. *See* Pet. 32–33 (citing Ex. 1002 ¶¶ 20, 22, 134–135). Patent Owner does not expressly address claim construction of any claim terms in its Response. *See generally* PO Resp. We determine that no formal constructions of any specific terms or words in the claim are necessary in this proceeding.

H. Grounds Asserted

Petitioner asserts that claims 1–7, 10–17, and 29 are unpatentable on the following grounds:

¹ This rule change applies to the instant Petition because it was filed after November 13, 2018. *See id.*

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 6, 11, 13, 29	103(a) ²	Oliaei ³
1–7, 10–17, 29	103(a)	Oliaei, Vittoz ⁴

Petitioner relies on testimony from Dr. Douglas Holberg (Ex. 1002; Ex. 1022) and Patent Owner relies on the testimony of Dr. Peter Kinget (Ex. 2002).

II. ANALYSIS

A. Legal Standards of Obviousness

Section 103(a) forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, objective evidence such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *see*

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the ’463 patent issued was filed before this date, the pre-AIA version of § 103 applies.

³ Ex. 1007, US Patent No. 6,697,001 (Feb. 24, 2004).

⁴ Ex. 1012, Eric A. Vittoz, “Dynamic Analog Techniques,” *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, 97–124 (José Franca and Yannis Tsividis eds., 2nd ed. Prentice Hall, 1994).

KSR, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”). The Court in *Graham* explained that these factual inquiries promote “uniformity and definiteness,” for “[w]hat is obvious is not a question upon which there is likely to be uniformity of thought in every given factual context.” *Graham*, 383 U.S. at 18.

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. To reach this conclusion, however, it is not enough to show merely that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.” *Id.*

A claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why one of skill in the art would have modified the prior art to obtain the claimed invention. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1307 (Fed. Cir. 2006). And, as a factfinder, we also must be aware “of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.” *KSR*, 550 U.S. at 421. This does not deny us,

however, “recourse to common sense” or to that which the prior art teaches.
Id.

B. Obvious over Oliaei (Claims 1, 2, 4, 6, 11, 13, 29)

1. Overview of Oliaei (Ex. 1007)

Oliaei discloses an operational amplifier circuit with a common-mode feedback circuit in Figure 10, reproduced below.

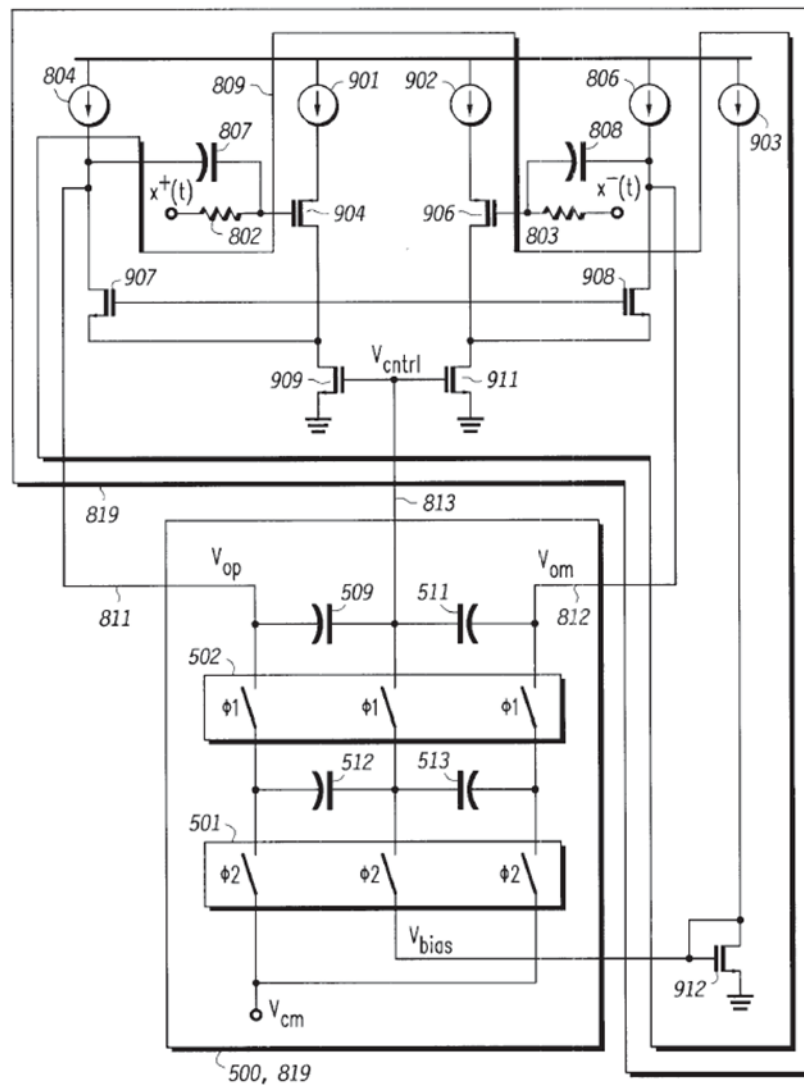


FIG. 10

Figure 10 of Oliaei, above, illustrates an operational amplifier circuit 809 with a switched capacitor common-mode feedback circuit 500. Ex. 1007, 3:22–25. The inputs to the op-amp circuit 809 are the differences between $x^-(t)$ and $x^+(t)$. *Id.* at 6:55–56. Op-amp circuit output signals 811 ($w^-(t)$), and 812 ($w^+(t)$), are provided to common mode feedback circuit 500 and compared to reference common-mode voltage V_{cm} to produce output V_{cntrl} , which is used in the operational amplifier circuit 809 to modify op-amp output signals 811 ($w^-(t)$), and 812 ($w^+(t)$) towards a desired value. *Id.* at 6:59–7:63.

Describing in more detail the switched capacitor common-mode feedback circuit 500, Oliaei refers to Figure 5 reproduced below, explaining that when switches 502 at phase $\phi 1$ are open, switches 502 are closed, and *vice versa* for phase $\phi 2$. *Id.* at 5:44–46.

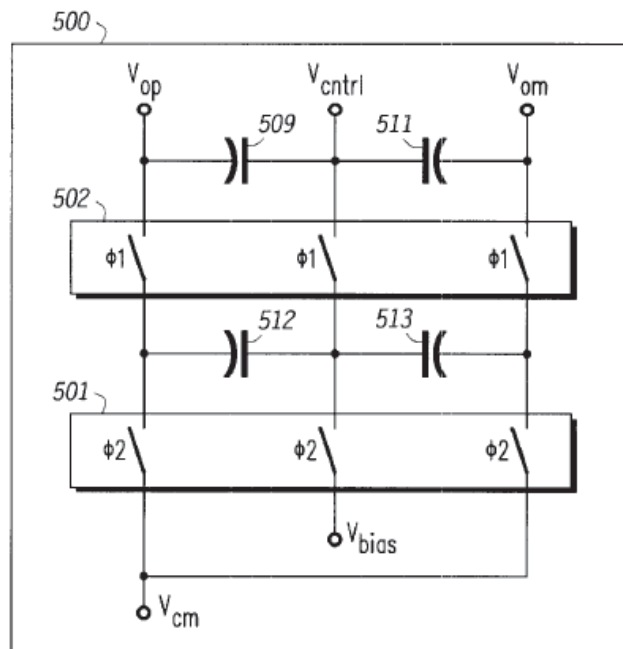
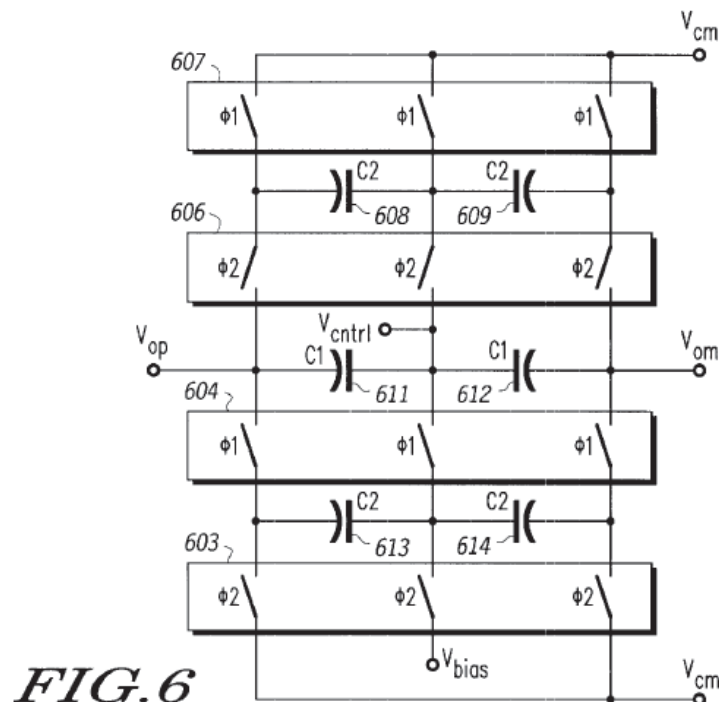


FIG.5

Figure 5 of Oliaei, above, illustrates switched capacitor common-mode feedback circuit 500. Oliaei explains that “[t]his switching measures the common mode components of signals V_{op} and V_{cm} as needed to adjust V_{cntrl} the control voltage that is fed back to produce the desired common mode voltage in the integrator circuits.” *Id.* at 5:56–59.

Figure 6 of Oliaei, reproduced below, illustrates an alternative switched capacitor common-mode feedback circuit 600.



Oliaei’s Figure 6, above, illustrates switched capacitor common-mode feedback circuit 600. Oliaei explains that “capacitors 611-614 and switches 603-604 is the same as that of FIG. 5. The remaining circuit elements, including capacitors 608-609 and switches 606-607, have been added to maintain the amplifier capacitive load constant.” *Id.* at 6:10–15.

2. Claims 1, 2, 4, 6, 11, 13, 29

Petitioner, relying on the testimony of Dr. Douglas Holberg, contends that claims 1, 2, 4, 6, 11, 13, and 29 would have been obvious over Oliaei. Pet. 33–76; Ex. 1002.

a. Independent Claims 1 and 11

i. Petitioner’s Arguments (Claim 1)

Considering the preamble of claim 1, element [1A] recites “a circuit with a common-mode dual output,” Petitioner argues that to the extent it is limiting, Oliaei’s Figure 10 discloses a common-mode integrator. Pet. 33 (citing Ex. 1002 ¶ 145). Petitioner asserts that “[a]ctive RC integrator 819 has dual outputs V_{op} and V_{om} [], which outputs generate a common-mode component.” *Id.*

Petitioner argues that limitation [1B] “a common-mode circuit with an output portion,” is disclosed by Oliaei’s “differential amplifier [that] is an example of a common-mode circuit.” *Id.* at 34 (citing Ex. 1002 ¶ 146). Petitioner asserts that the differential amplifier includes “dual outputs that provide the output signals vo^+/vo^- .” *Id.*

Limitation [1C] recites

a common-mode corrector circuit connected to alternate the states of said output portion between an average output level and a desired common-mode level, the difference between the average and desired levels being proportional to a signal offset level.

Ex. 1001, 14:1–15. Petitioner argues that Oliaei discloses common-mode corrector circuit 500, and when compared to the ’463 patent’s common mode corrector circuit, “the circuits are element-by-element the same.” Pet. 36 (citing Ex. 1002 ¶¶ 148–159 (Tables II, III)).

Dr. Holberg testifies that “[t]he common-mode feedback circuit of Oliaei is element-by-element the same as the common-mode corrector circuit 18 disclosed in the ’463 patent (Table II) and operates in the same way (Table III) as shown in the following [tables].” Ex. 1002 ¶ 148.

Dr. Holberg’s Table II, reproduced below, compares the elements of Oliaei’s feedback circuit corresponding with those in the ’463 patent.

Circuit Element	The ’463 Patent	Oliaei
Common-mode circuit	14	809
Common-mode corrector circuit	18	500
Output portion	V_o^+ / V_o^-	V_{op} / V_{om}
Average output level	$(V_o^+ + V_o^-)/2$	$(V_{op} + V_{om})/2$
Desired common-mode level	V_{cm}	V_{cm}
Precharging capacitors	C_{fly}^a / C_{fly}^b	512 / 513
Feedback capacitors	C_{cmfb}^a / C_{cmfb}^b	509 / 511
Feedback node	V_{FB}	V_{cntrl}

Table II

Dr. Holberg’s Table III, reproduced below, describes how the corresponding feedback circuit and elements in Oliaei operate in the same way as that of ’463 patent.

Operation	The '463 Patent	Oliaei
First phase	C_{cmfb}^a is between V_o^+ and V_{FB}	509 is between V_{op} and V_{cntrl}
	C_{cmfb}^b is between V_o^- and V_{FB}	511 is between V_{om} and V_{cntrl}
	C_{fly}^a is between V_{cm} and V_{Bias}	512 is between V_{cm} and V_{bias}
	C_{fly}^b is between V_{cm} and V_{Bias}	513 is between V_{cm} and V_{bias}
	C_{fly}^a and C_{fly}^b are charged to $V_{cm} - V_{Bias}$	C512 and C513 are charged to $V_{cm} - V_{bias}$
	State of output portion (V_o^+ and V_o^-) is at average output level	State of output portion (V_{op} and V_{om}) is at average output level
Second phase	C_{cmfb}^a and C_{fly}^a are connected in parallel between V_o^+ and V_{FB}	509 and 512 are connected in parallel between V_{op} and V_{cntrl}
	C_{cmfb}^b and C_{fly}^b are connected in parallel between V_o^- and V_{FB}	511 and 513 are connected in parallel between V_{om} and V_{cntrl}
	State of output portion (V_o^+ and V_o^-) at the desired common-mode level	State of output portion (V_{op} and V_{om}) at the desired common-mode level

Table III

Paragraph 148 of Dr. Holberg's declaration includes Tables II and III, above, and compares the corresponding elements and functions between Oliaei's Figure 10 and the '463 patent. Based on Tables II and III as well as Oliaei's Figure 10, Dr. Holberg testifies that "the common-mode feedback circuit arrangement of Oliaei is the same as in the '463 Patent." Ex. 1002 ¶ 156.

Petitioner further contends that the common-mode corrector circuit 500 shown in Oliaei's Figure 10 is the same as that disclosed in Oliaei's Figure 5 and, is also embodied in the alternative switched capacitor circuit 600 of Figure 6. Pet. 43–44. As discussed in more detail below, Petitioner argues that because Oliaei's circuit 600 of Figure 6, below, includes all elements of Oliaei's Figure 5, circuit 600 likewise discloses claim element [1C] when combined with Figure 10. *Id.* (citing Ex. 1002 ¶ 156).

As for limitation [1D], Petitioner relies on Dr. Holberg's testimony as to Oliaei's Figure 6. Petitioner argues that Oliaei discloses an error

correcting circuit illustrated in Figure 6 cooperating with the same elements of the common mode corrector circuit as shown and described with respect to Figure 5. Pet. 45 (citing Ex. 1002 ¶ 159). Dr. Holberg testifies that “Figure 6 discloses the common-mode corrector circuit 500 of Oliaei’s Figure 5, but with the addition of balancing capacitors 608 and 609 and balancing switches 606 and 607.” Ex. 1002 ¶ 159 (citing Ex. 1007, Figs. 5, 6, 4:4–15). Dr. Holberg further testifies that “Oliaei notes, ‘[u]sing a symmetric SC-CMFB 600 as in FIG. 6, it may be possible to balance the capacitive load of the amplifier. . . . [C]apacitors 608–609 and switches 606–607, have been added to maintain the amplifier capacitive load constant.’” *Id.* ¶ 161 (citing Ex. 1007, 6:4–15).⁵ According to Dr. Holberg, by balancing the capacitive load Oliaei provides for impedance matching and thus, “Oliaei’s balancing capacitors 608, 609 provide [the] same functionality as the error correcting circuit of the ’463 Patent – that of maintaining a constant common-mode error gain in both phases of the clock signals,” and thus, “the capacitors 608/609 operate to adjust the signal offset level.” *Id.* ¶¶ 164–165 (citing Ex. 1007, Fig. 6, 6:4–20).

For limitation [1E] Petitioner argues that Oliaei discloses a common-mode voltage terminal. Pet. 51–52 (citing Ex. 1002 ¶ 171). Dr. Holberg testifies that Figure 10 of Oliaei illustrates a common-mode voltage terminal V_{cm} connected to the V_{om} node of output line 182. Ex. 1002 ¶ 171 (citing Ex. 1007, Fig. 10). According to Dr. Holberg, “[t]he common mode voltage terminal V_{cm} is connected to the V_{om} node through a first pair of switches

⁵ Throughout this Decision acronyms “SC-CMFB” and “CMFB” circuit refer to “switched capacitor-common mode feedback” and “common mode feedback” circuits respectively.

rightmost 501 and rightmost 502,” and “[s]witch 501 is responsive to clock ϕ_2 ,” “switch 502 is responsive to clock ϕ_1 ,” “with clock ϕ_2 and clock ϕ_1 alternating.” *Id.* (citing Ex. 1007, Fig. 10). Further, according to Dr. Holberg, “[s]witches 501 and 502 are labeled as switches 603 and 604, respectively, in Oliaei’s Figure 6.” *Id.* (citing Ex. 1007, Fig. 10).

For limitation [1F] Petitioner argues that Oliaei discloses a bias terminal. Pet. 54–55 (citing Ex. 1002 ¶ 174). Dr. Holberg testifies that Figure 10 of Oliaei illustrates bias terminal V_{bias} connected to control node V_{cntrl} through a second pair of switches middle 501 and middle 502. Ex. 1002 ¶ 174 (citing Ex. 1007, Fig. 10). According to Dr. Holberg, “[s]witch middle 501 is responsive to clock ϕ_2 ,” “switch middle 502 is responsive to clock ϕ_1 ,” “with clock ϕ_2 and clock ϕ_1 alternating.” *Id.* (citing Ex. 1007, Fig. 10). Further, according to Dr. Holberg, “[s]witches 501 and 502 are labeled as switches 603 and 604, respectively, in Oliaei’s Figure 6.” *Id.* (citing Ex. 1007, Fig. 10).

For limitation [1G] Petitioner argues that Oliaei discloses precharging capacitors. Pet. 56–57 (citing Ex. 1002 ¶ 177). Dr. Holberg testifies that “Oliaei . . . discloses precharging capacitors 512 and 513 which are connected across a desired common-mode level node V_{cm} and a bias level node V_{bias} during a first clock phase . . . and hence store a charge which is proportional to the difference between the desired common-mode level node V_{cm} and the bias level node V_{bias} during the first clock phase, as illustrated in Figure [10].” Ex. 1002 ¶ 177. According to Dr. Holberg, “[t]hese precharging capacitors are also illustrated in Figure 6 and are labeled as 613 and 614.” *Id.*

For limitation [1H], Petitioner argues that Oliaei discloses a common-mode capacitor. Pet. 59–60 (citing Ex. 1002 ¶ 179). Dr. Holberg testifies that “Oliaei . . . discloses capacitors 509 and 511 which are connected between the output portion and the control node during the first clock pages,” where “[t]hese same capacitors are disclosed in Figure 6 and are labeled as capacitors 611 and 612.” Ex. 1002 ¶ 179. According to Dr. Holberg, Figure 6 shows that “during the second clock phase, common-mode capacitor 509 . . . is connected in parallel (between nodes V_{op} and V_{cntrl}) with precharging capacitor 512 . . . and similarly common-mode capacitor 511 . . . is connected in parallel (between nodes V_{om} and V_{cntrl}) with precharging capacitor 513.” *Id.*

ii. *Petitioner’s Arguments (Claim 11)*

Because many of the limitations and elements are similar between claims 1 and 11 we focus on two particular limitations [11C] and [11D] that differ from claim 1 and are critical to our analysis.

Limitation [11C] requires:

a common-mode feedback circuit coupled to said output portion,
said feedback circuit providing a desired common-mode level *in a first operational mode*

Ex. 1001, 15:27–29 (emphasis added). Petitioner argues that in Oliaei’s first operational mode “the feedback circuit provides the desired common-mode level v_{cm} at node V_{cm} .” Pet. 66 (citing Ex. 1002 ¶ 188).

Limitation [11C] also requires:

generating a feedback signal proportional to the difference between the average output level and the desired common-mode level *in a second operational mode*, the feedback signal being coupled to said current sinking portion;

Id. at 15:29–34 (emphasis added). Petitioner contends that in Oliaei’s “second operational mode, precharging capacitors 512/513 (613/614 in Figure 6) – which received the desired common-mode level v_{cm} in the first operational mode – are connected in parallel with feedback capacitors 509/511 (611/612 in Figure 6) – to which the average output level was applied in the first operational mode.” *Id.* at 67–68 (citing Ex. 1002 ¶ 189). Petitioner argues that “[a]s a result, a signal proportional to the difference between the average output level and the desired common-mode level is generated by connecting these capacitors in parallel. *Id.* at 68.

Limitation [11D] recites:

an impedance matching circuit connected to said feedback circuit to adjust the feedback signal;

Ex. 1001, 15:35–36. Petitioner argues that Oliaei’s “[c]apacitors 608 and 609 act as an impedance matching circuit.” Pet. 70 (citing Ex. 1002 ¶ 190). Petitioner explains that “when capacitors 608/609 are added to the circuit (the circuit of Figure 6 is the same circuit as Figure 5 but with the addition of capacitors 608/609 and their associated switches 606/607), then the impedance seen from feedback control node V_{ctrl} is the same in the first clock phase (equal to $C611+C612+C608+C609$) and the second clock phase (equal to $C611+C612+C613+C614$).” *Id.*

b. Patent Owner’s Arguments

Patent Owner provides the majority of its argument directed towards independent claim 11, and stating with respect to independent claim 1 that, “claim 1 recites an ‘error correcting circuit’ that adjusts the ‘signal offset level’ from the common mode corrector circuit. These features are analogous to claim 11’s impedance matching circuit adjusting the feedback

signal generated by the common mode feedback circuit.” PO Resp. 50 (citing Ex. 2002 ¶ 69), *see also id.* at 33–51.

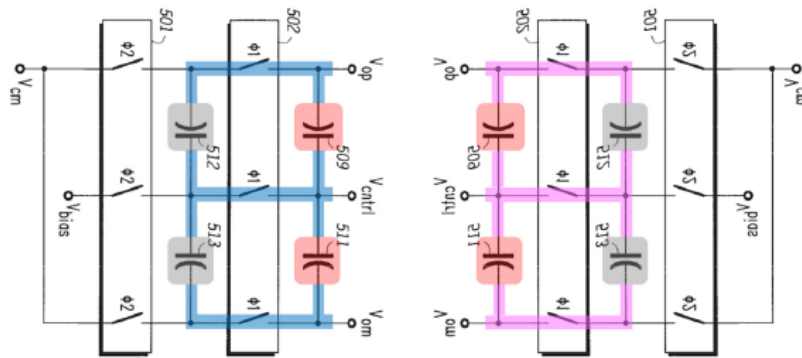
With this in mind, Patent Owner’s main argument is that Oliaei’s Figures 5 and 6 teach conventional switched capacitor common-mode feedback circuits and do not teach or disclose an “error correcting circuit” as recited in independent claim [1D], or an “impedance matching circuit” as recited in independent claim [11D]. *Id.* at 4. Patent Owner argues specifically that compared to conventional CMFB circuits as in Oliaei, “The ’463 patent improves on the earlier common mode feedback circuits (‘CMFBs’) by placing an impedance matching circuit, including *an additional capacitor, at a specific terminal within the CMFB circuit.*” *Id.* at 13 (citing Ex. 1001, 7:32–43).

Patent Owner contends that “Oliaei provides no hint or suggestion that Figure 5 depicts anything other than a conventional SC-CMFB circuit.” PO Resp. 25–26 (citing Ex. 1005, 12; Ex. 2002 ¶ 38). Patent Owner argues that for Figure 5 the feedback capacitors are connected in clock phase $\Phi 1$ and disconnected in clock phase $\Phi 2$. *Id.* at 27 (citing Ex. 1007, 5:51–53).⁶ Patent Owner explains that “[t]his switching operation causes the CMFB circuit to “measure[] the common mode components of signals V_{op} and V_{om} as needed to adjust V_{ctrl} , the control voltage that is fed back to

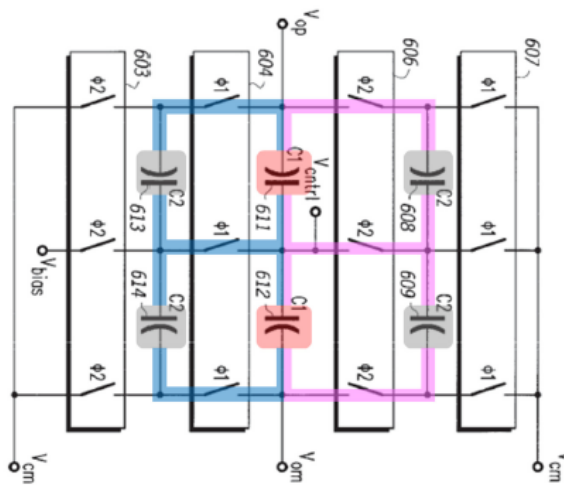
⁶ The font symbols Φ (phi) used by Patent Owner, and ϕ used by Petitioner, are used interchangeably in this Decision to refer to the circuit clock phase function.

produce the desired common mode voltage.” *Id.* (citing Ex. 1007, 5:56-60; Ex. 2002 ¶ 39).⁷

Patent Owner argues that Oliaei’s Figure 6 “is simply two sets of the Figure 5 embodiment.” *Id.* at 29 (citing Ex. 1007, 6:8–10). Reproduced below are Patent Owner’s annotated Figures 5 and 6.



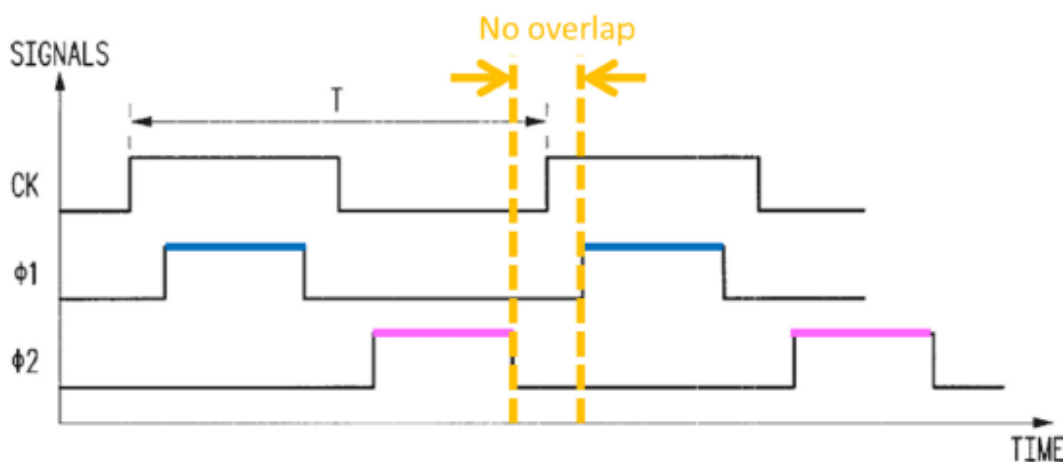
Ex. 1007, Fig. 5 (two copies, rotated)



Ex. 1007, Fig. 6 (rotated)

⁷ Patent Owner highlights and color codes certain terms in its Response and in Dr. Kinget's Declaration (Ex. 2002) to coincide with its annotated figures. Unless necessary for reference to an annotated figure we do not in this Decision reproduce the highlighting and color coding in quotations from the Response or Dr. Kinget's Declaration.

Patent Owner's annotated Figures 5 and 6, above, illustrate the symmetric nature of Oliaei's SC-CMFB circuit in Figure 6, as compared to Figure 5. Patent Owner argues that for Figure 6, in clock phase $\Phi 1$ switches 604 are closed and, with switches 606 open, just the first circuit including capacitors 611–614 provides a feedback signal. According to Patent Owner, in clock phase $\Phi 2$ the opposite occurs, switches 604 are open, switches 606 are closed and only the second circuit including capacitors 608, 609, 611 and 612 provides the feedback signal. Patent Owner provides annotated Figure 7 of Oliaei, reproduced below, illustrating that phases $\Phi 1$ and $\Phi 2$ as a function of time, do not overlap.



Oliaei's Figure 7, above, as annotated by Patent Owner depicting clock signals $\Phi 1$ and $\Phi 2$ as a function of time. Patent Owner argues that Oliaei does not “improve on conventional CMFB circuits in any way” and that Figure 6 is simply Oliaei's conventional CMFB circuit of Figure 5 arranged so as to be activated for each phase. *Id.* at 30 (citing Ex. 2002 ¶ 42).

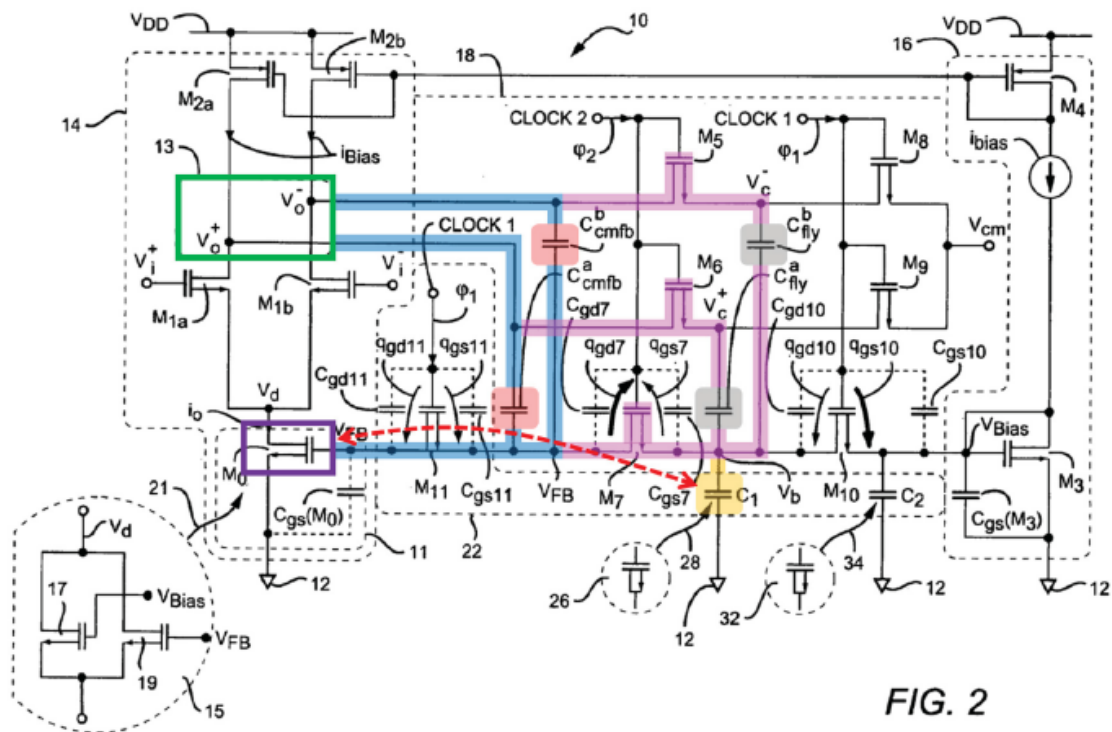
Patent Owner argues specifically that “Oliaei's scant description does not even describe these capacitors, let alone suggest they are an impedance matching circuit.” *Id.* at 34. Contrary to Petitioner's assertion that Oliaei's

Figure 6 discloses an impedance matching circuit, Patent Owner alleges “that these are *precharging* capacitors responsible for receiving the desired common mode V_{cm} , in clock phase $\Phi 1$.” *Id.* at 34–35 (citing Ex. 2002 ¶ 48). Patent Owner asserts that in $\Phi 2$, the precharging capacitors available in $\Phi 1$ are disconnected, and *vice versa*, thus “Figure 6 has two switched capacitor common mode feedback circuits, not one common mode feedback circuit and another impedance matching circuit, as claimed.” *Id.* at 35 (citing Ex. 2002 ¶ 48).

c. Whether Oliaei discloses an “error correcting circuit” as recited in independent claim 1

The declarants generally agree as to the function and structure of the error correcting circuit 22 and impedance matching described in the ’463 patent. For example, the ’463 patent describes that error correcting “[c]ircuit 22 further includes a balancing capacitor C_1 and a balancing capacitor C_2 ” and that “[c]apacitors C_1 and C_2 provide impedance matching between terminals V_b and V_{Bias} and adjacent terminals such as terminal V_{FB} .” Ex. 1001, 5:21–22, 7:51–53, *see* Ex. 1002 ¶ 70 (Dr. Holberg testifying that “[b]alancing capacitors C_1 and C_2 provide impedance matching between terminals of the circuit, such as V_{Bias} , V_b , and V_{FB} [] by balancing the capacitive load seen by those terminals,”) *see also* Ex. 2002 ¶ 23 (Dr. Kinget testifying that “[t]he capacitance of capacitor C_1 matches the impedance at the feedback terminal (V_{FB}). [] By coupling this impedance matching capacitor C_1 to terminal V_b , the capacitor C_1 adjusts the feedback signal at terminal V_{FB} generated by the CMFB circuit during the clock phase $\Phi 2$ ”).

Figure 2 of the ’463 patent as annotated by Patent Owner is reproduced below.



Annotated Figure 2 of the '463 patent, above, illustrates how impedance matching circuit, including capacitor C1, adjusts the feedback signal in clock phase $\Phi 2$. Dr. Kinget explains that “[t]he [common mode feedback circuit] generates the feedback signal at terminal V_{FB} during both clock phases, but . . . during the second clock phase that feedback signal is adjusted in the second clock phase by the precharging capacitors and the impedance-matching circuit.” Ex. 2002 ¶ 24.

Dr. Kinget testifies that the result of the error correcting circuit, i.e., impedance matching circuit, “enables the error gain of the CMFB during each of the clock phases to be the same (including during transition periods between non-overlapping clocking cycles, when both clocking signals are low), which reduces common-mode variation.” Ex. 2002 ¶ 25 (citing Ex. 1001, 7:61–8:8). Similarly, Dr. Holberg testifies that “by balancing the

capacitive load seen by those terminals [V_{Bias} , V_b , and V_{FB}] during switching of the capacitor network of the common-mode feedback circuit . . . the common-mode error gain remains constant and charge injection errors associated with switches in the feedback circuit can be minimized.” Ex. 1002 ¶ 70 (citing Ex. 1001, 7:67–8:1; 8:66–9:2). Thus, there is little disagreement over how the claimed invention functions. On the other hand, as we discuss below, the declarants substantively disagree as to the function of Oliaei.

Compared to the common mode feedback circuit 500 in Figure 5, Petitioner argues that Oliaei’s circuit 600 in Figure 6 teaches adding balancing capacitors 608 and 609 and balancing the capacitive load, i.e., matching the impedance, of the amplifier seen at node V_{FB} , between clock phase $\Phi 1$ and clock phase $\Phi 2$. Pet. 47 (citing Ex. 1002 ¶ 161). Petitioner points out that Oliaei expressly states “using a symmetric SC-CMFB 600 as in FIG. 6, it may be possible to balance the capacitive load of the amplifier . . . [t]he remaining circuit elements, including capacitors 608-609 and switches 606-607, have been added to maintain the amplifier capacitive load constant.” *Id.* (quoting Ex. 1007, 6:7–15). Thus, Petitioner asserts “the error correcting circuit functions as an impedance matching circuit.” *Id.* at 44.

This is confirmed, Petitioner argues, by considering Oliaei’s circuit from Figure 6 in the same capacitive balancing equation (1) set forth in the ’463 patent (Ex. 1001, 8:5) and reproduced below. *Id.* at 47 (citing Ex. 1002 ¶¶ 162–165).

$$\frac{c_{gs}(M_0)}{(c_{cmfb}^a + c_{cmfb}^b)} = \frac{(c_{gs}(M_0) + c_1)}{(c_{cmfb}^a + c_{cmfb}^b + c_{fly}^a + c_{fly}^b)} \quad (1)$$

Dr. Holberg testifies that “during the first clock phase the capacitance ratio is:

$$[C_{gs}(909) + C_{gs}(911)] / [C611 + C612 + C608 + C609]$$

and during the second clock phase that capacitance ratio is:

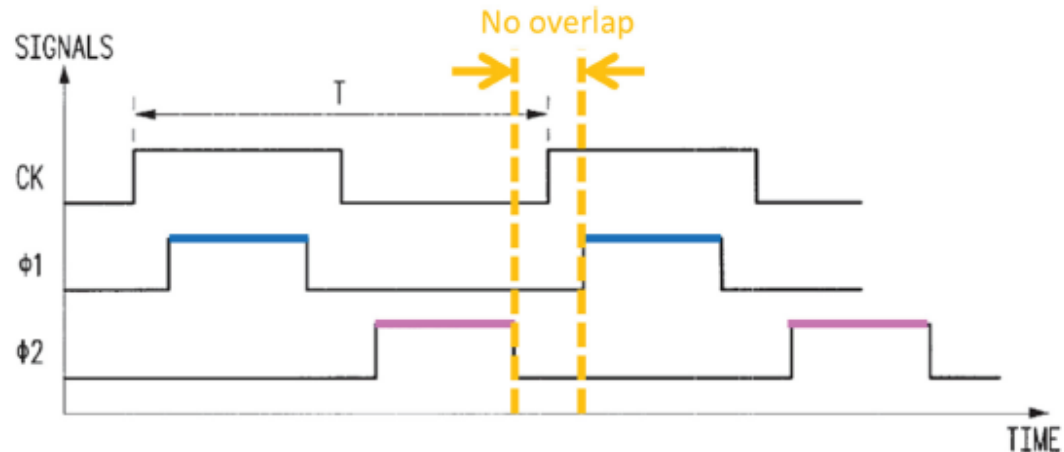
$$[C_{gs}(909) + C_{gs}(911)] / [C611 + C612 + C613 + C614].$$

Because C608 = C613 and C609 = C614 (as required for symmetry), the two capacitance ratios are equal and hence common-mode error gain is the same in both clock phases.” Ex. 1002 ¶ 164 (citing Ex. 1007, Fig. 6; 6:4–20). Dr. Holberg explains that “[b]ecause the common-mode gain remains constant in both phases, a signal offset level will not be induced due to different load impedances in each phase (as was the case for the circuit of Figure 5).

Hence, the capacitors 608/609 operate to adjust the signal offset level.” *Id.* ¶ 165.

Patent Owner argues that Oliaei’s Figure 6 discloses a symmetrical combination of a first and second conventional common mode feedback circuits that “are alternately connected and disconnected on clock phases, $\Phi 1$ and $\Phi 2$,” in a switching operation. PO Resp. 27 (citing Ex. 1007, 5:51–53, 5:56–60; Ex. 2002 ¶ 39). Patent Owner argues that the switching operation “provides a nominally identical load at the output terminal on different clock phases.” *Id.* (citing Ex. 1007, 6:7–15). Patent Owner’s declarant, Dr. Kinget, testifies that “[d]uring phase $\Phi 1$, switches 606 are open, meaning the second circuit is disconnected from the first circuit and thus prevented from

adjusting the feedback signal.” Ex. 2002 ¶ 41. Annotating Oliaei’s Figure 7, reproduced below, Dr. Kinget testifies that “[t]his configuration is reversed during clock phase $\Phi 2$,” and thus “clock phase $\Phi 1$ and $\Phi 2$ are non-overlapping, meaning there is no moment in time when both sets of switches 604 and switches 606 are closed.” *Id.*



(Ex. 1007, Fig. 7.)

Oliaei’s Figure 7, above, as annotated by Patent Owner depicting clock signals $\phi 1$ and $\phi 2$ as a function of time illustrating no time-overlap of the signals generated during clock phase $\Phi 1$ and $\Phi 2$.

We appreciate, as Dr. Kinget points out, that Oliaei’s symmetric common mode feedback circuit 600 shown in Figure 6 switches between clock phase $\Phi 1$ and $\Phi 2$ without overlap of the feedback signal generated during each clock phase. Ex. 2002 ¶ 41. And we acknowledge, as Dr. Kinget testifies, that because clock phase $\Phi 1$ and $\Phi 2$ do not overlap as shown in Figure 7, in each clock phase $\Phi 1$ and $\Phi 2$ the disconnected capacitors in feedback circuit 600 are “prevented from adjusting the feedback signal,” that is— *Vcntrl* *Id.* However, claim 1 does not recite a

“feedback signal” limitation or a specific functional limitation of “adjusting the feedback signal.” Limitation 1[C] recites:

a common-mode corrector circuit connected to alternate the states of said output portion between an average output level and a desired common-mode level, the difference between the average and desired levels being proportional to a signal offset level;

Ex. 1001, 14:11–15. Claim 1 expressly defines “a signal offset level” that is proportional to the difference between the average and desired common mode signal. *Id.* Claim 1 does not recite any temporal limitation with respect to when and how the average and desired common mode signals are generated by the common mode corrector circuit, only that the difference between them defines the “signal offset level.” Limitation 1[D] recites:

an error correcting circuit connected to said common mode corrector circuit to adjust the signal offset level;

Id. at 14:15–16. The express function of the error correcting circuit is “to adjust the signal offset level.” *Id.* A plain reading of the claim does not recite adjusting or modifying a “feedback signal” nor even recite how the adjustment of the signal offset level is performed, the claim requires simply that the error correcting circuit “adjust the signal offset level.”

Dr. Holberg explains persuasively how Oliaei’s symmetric common mode feedback circuit 600 shown in Figure 6, as it switches between clock phase $\Phi 1$ and $\Phi 2$, adjusts the signal offset level so that “the capacitive load impedance seen by the op-amp’s differential output is the same in both phases.” Ex. 1002 ¶ 99. Dr. Holberg testifies that “Oliaei’s circuit of Figure 6 (switches 606 and 607 and capacitors 608 and 609) balances the capacitive load seen by the amplifier, and also balances the capacitive load that is seen at the feedback control node V_{cntrl} .” Ex. 1002 ¶ 101. Dr. Holberg testifies

that “[h]ence Oliaei discloses reducing variation in common-mode error gain,” to adjust the signal offset level as required in claim 1. *Id.*; *see also* Ex. 1001, 3:41–45 (The ’463 patent explaining “[t]he desired common-mode signal or level at a terminal V_{cm} will be referred to as v_{cm} and the difference between signals V_{cm}^{avg} and v_{cm} (i.e. $V_{cm}^{avg} - V_{cm}$) will be referred to as the common mode variation, . . . the difference between the average and the desired levels is proportional to a signal offset level.”).

We are persuaded by Petitioner’s arguments and Dr. Holberg’s testimony that Oliaei discloses a common mode correcting circuit 600 connected to an error correcting circuit, e.g., balancing capacitors 608, 609 and switches 606, 607, to “adjust the signal offset level” as recited in claim 1, elements [1C]-[1D], between a desired common mode level and an average output level and thus reduce common-mode error gain variation in the common mode correcting circuit 600. Pet. 34–50 (citing Ex. 1002 ¶¶ 145–169); *see also* Ex. 1007, 6:12–15 (Oliaei stating that “[t]he remaining circuit elements, including capacitors 608-609 and switches 606-607, have been added to maintain the amplifier capacitive load constant.”).

Patent Owner does not substantively argue the limitations of elements [1A]-[1B] and [1E]-[1H]. PO Resp. 33–35, 50–51. As set forth above in Section II.B.2.a.i., we find persuasive Petitioner’s arguments and evidence, including the testimony of Dr. Holberg, that Oliaei discloses these limitations of claim 1. *See* Ex. 1002 ¶¶ 92–105, 136–179. Having considered the entire record and all the evidence and arguments from both parties, for the reasons explained above we are persuaded that Oliaei discloses all the limitations of claim 1. The Petition and supporting

testimony of Dr. Holberg has shown by a preponderance of the evidence that claim 1 would have been obvious over Oliaei.

d. Whether Oliaei discloses an “impedance matching circuit . . . to adjust the feedback signal” as recited in independent claim 11

Different from the “error correcting circuit” in claim 1, claim 11 requires an “impedance matching circuit.” Ex. 1001, 15:35–36. Notably, claim 11 also recites “a feedback signal”:

a common mode feedback circuit . . . providing a desired common-mode level in a first operational mode and generating *a feedback signal* proportional to the difference between the average output level and the desired common-mode level *in a second operational mode*,

Id. at 15:28–32 (emphasis added). Claim 11 requires that the feedback signal generated in the second operational mode, i.e., a second clock phase, is proportional to the difference between the average output level and the desired common mode level. Claim 11 then recites

an impedance matching circuit connected to said feedback circuit to adjust *the feedback signal*;

Id. at 15:35–36 (emphasis added). According to Petitioner, the claimed “generating a feedback signal . . . in a second operational mode” occurs in the second operational mode, but the claimed function “adjust[ing] the feedback signal” can occur during the first operational mode, during the second operational mode, or during both modes. Reply 6–7. Patent Owner contends that Petitioner’s argument is inconsistent with the plain language of claim 11, which recites that the claimed “feedback signal” is generated “in a second operational mode,” and that feedback signal is “the feedback signal” that is adjusted by the impedance matching circuit. PO Sur-Reply 5–6.

There is clear antecedent basis in claim 11 for “*the feedback signal*”

being “a feedback signal . . . in a second operational mode,” and thus we agree with Patent Owner. *Compare Ex. 1001*, 15:30 (“a feedback signal”), *with id.* at 15:32–33, 36 (“the feedback signal”).

Recognizing that claim 11 plainly requires “adjust[ing] the feedback signal” in the second operational mode or second clock phase, the question remains whether Oliaei’s error correcting circuit, (a) acts as an impedance matching circuit and (b) adjusts the feedback signal in the second operational mode? We find Patent Owner’s arguments and evidence the most persuasive.

Petitioner contends that “during the first operational mode, Oliaei’s impedance matching circuit (capacitors 608/609) adjusts the feedback signal (voltage on node V_{cntrl}) that was generated by the feedback circuit (capacitors 611-614, etc.) during the second operational mode. This is what claim 11 requires.” Reply 9. Even if we were to accept Petitioner’s factual premise as correct, Petitioner’s conclusion is incorrect. Claim 11 requires adjusting the feedback signal during the second operational mode, not during the first operational mode.

As discussed above, we are persuaded, as Petitioner and Dr. Holberg assert, that “Oliaei’s capacitors 608/609 provide the same functionality as the error correcting circuit of the ’463 Patent – that of maintaining a constant common-mode error gain in both phases of the clock signals.” Pet. 48 (citing Ex. 1002 ¶ 165). Dr. Holberg’s opinion is that the impedance of the circuit in each clock phase is balanced, i.e., matched, as would be seen at Oliaei’s node V_{cntrl} , between clock phase $\Phi 1$ and clock phase $\Phi 2$. Dr. Holberg testifies that a person of ordinary skill in the art would understand

such balancing of the impedance across each circuit is impedance matching. Ex. 1002 ¶ 161.

However, claim 11 recites an impedance matching circuit “to adjust the feedback signal” during the second operational mode. Ex. 1001, 15:36. We agree with Patent Owner that reducing the signal offset by capacitive balancing of two distinct common mode feedback circuits as taught in Oliaei “is not the same as the claimed invention, which requires an impedance matching circuit to be ‘*connected* to . . . *adjust* the feedback signal’ generated by a common mode feedback circuit during the ‘second operational mode’ of that common mode feedback circuit.” PO Resp. 35 (quoting Ex. 2002 ¶ 49). Also, we are persuaded by Dr. Kinget’s testimony that a person of ordinary skill in the art “would recognize that operating two sets of SC-CMFB circuits in this manner is not the same as the claimed invention, which requires an impedance-matching circuit to be ‘connected to . . . adjust the feedback signal’ provided by a common-mode-feedback circuit.” Ex. 2002 ¶ 48. Dr. Kinget testifies persuasively, that claim 11 is consistent with the ’463 patent specification, describing that the common mode feedback signal being adjusted is *the* feedback signal in the “second operational mode.” *Id.* ¶¶ 50–51 (citing Ex. 1001, 7:52–60; 8:9–18). Figure 2 of the ’463 patent as annotated by Dr. Kinget is reproduced below.



Figure 2 of the '463 patent, above, highlights impedance matching circuit C1 at terminal V_b of precharging fly capacitors C^a_{fly}, C^b_{fly}. Dr. Kinget testifies persuasively that, as shown by annotated Figure 2 above, and different from Oliaei, “feedback occurs when the feedback capacitors and the fly capacitors are coupled together (i.e., in the claimed ‘second operational mode’). Claim 11 then recites an ‘impedance-matching circuit’ that is ‘connected to [the] feedback circuit to *adjust* the feedback signal’ generated by *that* feedback circuit.” *Id.* ¶ 50. Acknowledging that Oliaei and '463 patents present a similar result, Dr. Kinget explains persuasively how the circuits accomplish the task differently:

Oliaei describes Figure 6 as two sets of conventional CMFB circuits that provide a constant load to the output of an integrator in a sigma-delta modulator. When one CMFB circuit is generating a feedback signal, the other circuit is precharging, and vice versa. Because of their non-overlapping roles, neither circuit

performs impedance matching to adjust the feedback signal of the other.

Id. ¶ 57. In other words, although the result of the circuits described in Oliaei and the '463 patent may be reducing variation in common-mode error gain, we credit Dr. Kinget's testimony that a person of ordinary skill in the art "would understand that [Oliaei's] Figure 6 has two switched-capacitor common-mode-feedback circuits, not one common-mode feedback circuit and another impedance-matching circuit." *Id.* ¶ 48. Thus, Oliaei teaches a different circuit structure than the one expressly required by claim 11.

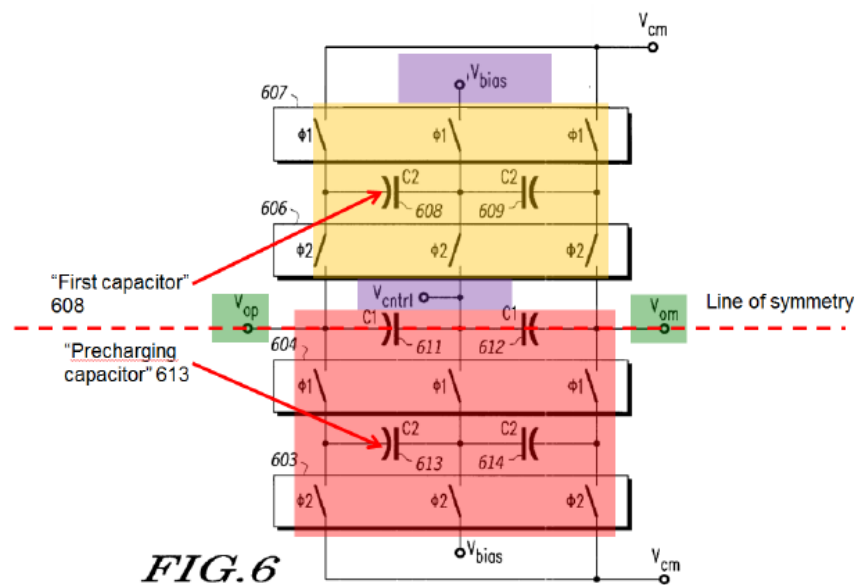
Whether a person of ordinary skill in the art would have understood that Oliaei's error correcting circuit, (a) acts as an impedance matching circuit, we are not persuaded that Oliaei discloses an impedance matching circuit that (b) adjusts the feedback signal in the second operational mode as required by claim 11. Petitioner has not shown sufficiently that Oliaei's symmetrical switched capacitor-common mode feedback circuits, even though the two circuits are balanced by symmetrical capacitors 608, 609, and 613, 614, which arguably reduce common-mode error gain variation by matching impedances at node V_{cntrl} , teach the particular structure required by claim 11, i.e., "an impedance matching circuit connected to said feedback circuit to adjust the feedback signal" in the second operational clock phase. Ex. 1001, 15:35–36.

e. Dependent Claims 2, 4, and 6

Claim 2 depends from independent claim 1 and recites "wherein said error correcting circuit includes a first capacitor coupled to said common-mode corrector circuit to reduce the difference between the average and desired levels." Ex. 1001, 14:51–54. Similarly, claim 4 recites "wherein said error correcting circuit includes a second capacitor coupled to said bias

terminal to reduce the difference between the average and desired levels.”
Id. at 14:55–58. Petitioner argues that capacitors 608 and 609 in Oliaei’s Figure 6 correlate to the claimed first and second capacitors, and “operate to reduce the difference between the average $((V_{op}+V_{om})/2)$ and desired (V_{cm}) levels. Pet. 62 (citing Ex. 1002 ¶¶ 180–183); *see also* Ex. 1007, 6:12–15 (Oliaei stating that “[t]he remaining circuit elements, including capacitors 608–609 and switches 606–607, have been added to maintain the amplifier capacitive load constant”).

Claim 6 depends from independent claim 1 and recites “wherein a capacitance of said precharging capacitor is chosen to be proportional to a capacitance of said first capacitor.” Ex. 1001, 15:1–3. Petitioner argues that because Oliaei’s circuit 600 is symmetric, “the capacitor values on the ‘top’ half of the circuit are the same as the capacitor values of the ‘bottom’ half of the circuit.” Pet. 63 (citing Ex. 1002 ¶ 184). Petitioner’s annotated Figure 6 from Oliaei is reproduced below.



Ex.1002, ¶184

Petitioner's annotated Figure 6 from Oliaei is reproduced above indicating capacitor 608 as the "first capacitor" and symmetric capacitor 613 as the proportional "precharging capacitor." *Id.*

Patent Owner does not argue separately dependent claims 2, 4, and 6, but instead relies on arguments presented for claim 1, which we find unpersuasive as discussed in our analysis of claim 1 above. Petitioner's analysis for claims 2, 4, and 6, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 180–184), which we credit, is persuasive that Oliaei discloses the limitations of dependent claims 2, 4, and 6.

f. Dependent claims 13 and 29

Claims 13 depends from claim 12, which depends from claim 11, and 29 depends directly from claim 11. Ex. 1001, 15:45–48, 16:60–62. Because Petitioner has not shown by a preponderance of the evidence that claim 11 would have been obvious in view of Oliaei, we are likewise not persuaded that claims 13 and 29 would have been obvious in view of Oliaei.

3. Conclusion as to Obviousness Based on Oliaei

Based on the complete trial record in the proceeding, for the reasons above we are persuaded that claims 1, 2, 4, and 6, would have been obvious in view of Oliaei. We are not persuaded that claims 11, 13, 17, and 29 would have been obvious in view of Oliaei.

C. Obvious over Oliaei and Vittoz (Claims 1–7, 10–17, 29)

1. Overview of Vittoz (Ex. 1012)

Vittoz describes that switching circuits, such as a sample switch and a hold capacitor, suffer from non-idealities such as charge injection, and further describes multiple remedies to compensate for charge injection. Ex.

1012, 97, 100–102. In a first solution, impedance matching in the form of balancing capacitance is applied to the circuit to control the flow of charge injection away from sensitive nodes. *Id.* at 100–102. This solution is illustrated in Figure 7, reproduced below.

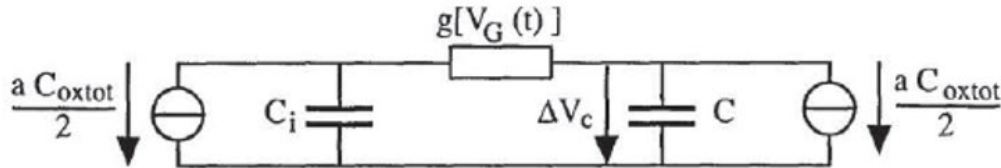


Fig. 7: Final sample-and-hold model for the analysis of charge injection.

Figure 7, above, illustrates adding capacitance on an input side of the switch (the left-hand side in the above drawing) to reduce the impedance of that side relative to the output side of the switch (the right-hand side in the above drawing), where charge injection is directed away from the sample capacitor C. *Id.* at 102–104. Specifically, and with reference to Figure 7, Vittoz teaches to “choose $C_i \gg C$ and β very large, in order to let all the released charge flow back into C_i (which behaves as a voltage source).” *Id.* at 103.

A second solution disclosed by Vittoz is to equalize the capacitance on both sides of a switch and further to use “dummy switches” to compensate for charge injection introduced by a main switching element. *Id.* at 104. This solution is illustrated in Figure 9, reproduced below.

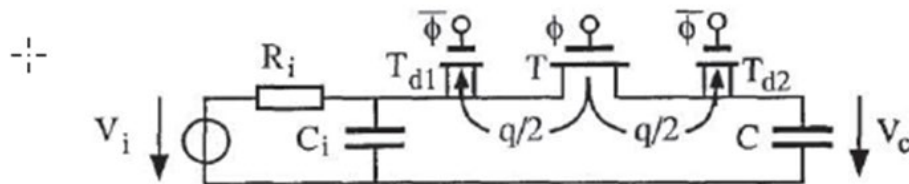


Fig. 9: Compensation of charge injection by half-sized dummy switches.

Figure 9, above, illustrates adjusting capacitance to ensure “ $C_i = C$.” *Id.* Further, dummy switches T_{d1} and T_{d2} are deployed, respectively, on either

side of the switching transistor T so that “[i]f the transistor is itself perfectly symmetrical, half the charge q flows into C and can be compensated by half-sized dummy switches which absorb the released charge.” *Id.* Vittoz also notes that the dummy switches can be employed whether or not the capacitances C_i and C are equal. *Id.*

2. Claims 1–7, 10–17, 29

Petitioner, relying on the testimony of Dr. Douglas Holberg, contends that claims 1–7, 10–17, and 29 would have been obvious over Oliaei and Vittoz. Pet. 77–107; Ex. 1002. For the reasons below, we determine that Petitioner has not provided persuasive evidence and reasoning sufficient to show that a person of ordinary skill in the art would have combined Oliaei and Vittoz.

a. Petitioner’s Arguments

Petitioner relies upon Oliaei for teaching the elements of claim 1, as described above. Pet. 83, 89–90 (citing Ex. 1002 ¶¶ 220–231, 240–249). To the extent Oliaei does not teach or disclose an error correcting or impedance matching circuit Petitioner turns to Vittoz which, according to Petitioner, “discloses an error correcting / impedance matching circuit,” and “provides well-documented models for analyzing charge injection and its effects on circuits.” Pet. 78–79.

Relying on Dr. Holberg’s testimony, Petitioner contends Vittoz discloses “an error correcting circuit connected to said common-mode corrector circuit to adjust the signal offset level,” as called for in claim 1. Pet. 84–89 (citing Ex. 1002 ¶¶ 232–239). Dr. Holberg testifies that Vittoz “teaches error correcting circuitry used to compensate for errors (charge injection) arising from switched-capacitor circuits.” Ex. 1002 ¶ 233 (citing

Ex. 1012, 101–105). More specifically, Dr. Holberg testifies that “with regard to Figure 9 . . . Vittoz discloses placing balancing capacitance C_i on one side of a switch T in order to match the impedance C on the other side of the switch T . . . so that the charge injection from switch T is distributed equally on both sides of the switch,” and Vittoz further discloses that “[a] half-sized dummy switch T_{d2} is added on the critical node side (the output side V_c) of switch T to correct for charge injection into that critical node.” Ex. 1002 ¶ 233 (citing Ex. 1012, 101–105, Fig. 9). Additionally, as explained by Dr. Holberg, “Vittoz teaches placing a dummy switch T_{d1} on the other side of switch T in order to compensate for the charge injection on that node as well.” Ex. 1002 ¶ 233.

b. Patent Owner’s Arguments

Patent Owner argues that the combination of Oliaei and Vittoz is “motivated purely by hindsight and contrary to Oliaei’s express teachings.” PO Resp. 53 (citing Ex. 2002 ¶ 74). Patent Owner argues that Petitioner’s asserted motivation for combining Vittoz and Oliaei, that is—the desire to reduce charge injection, is conclusory and unsupported. *Id.* Patent Owner asserts that Dr. Kinget’s “simulations confirm that Petitioner’s proposed combination would have performed worse than Oliaei’s unmodified teachings—precisely the reason that experts and literature caution against applying charge injection compensation to switches without a specific and compelling reason to do so.” *Id.*

Patent Owner argues that “charge injection naturally occurs at **every** switch in a switched capacitor circuit. Accordingly, it does not follow that a POSITA would be motivated from this fact alone to add charge injection compensation circuitry to every switch in the circuit.” *Id.* at 54 (citing Ex.

2003, 39:8–22). Patent Owner asserts that “the known downsides of charge injection circuitry—including increased complexity, extra clocking circuitry, and the possibility of making the problem worse—means that a POSITA would **not** use such circuitry gratuitously.” *Id.* at 57 (citing Ex. 2002 ¶ 77). According to Patent Owner, Petitioner’s declarant, Dr. Holberg, “admitted on cross-examination that Oliaei **does not disclose any charge injection problem** in Figure 5.” *Id.* at 57 (citing Ex. 2003, 72:19–25).

Patent Owner argues that Oliaei expressly indicates that charge injection was not an issue in its common mode feedback circuit. *Id.* at 61 (citing Ex. 1007, 5:17–22 Ex. 2002 ¶ 80.). Patent Owner argues that Oliaei states explicitly that “clock-feedthrough glitches [from the switched capacitor CMFB circuit] give rise to a spectral component at the sampling frequency $1/T$ which **does not affect the system performance**.” *Id.* (quoting Ex. 1007, 5:17–22). According to Dr. Kinget, “clock-feed through glitches” are understood by those of ordinary skill in the art as charge injection, and that “relatively few circuits warrant circuitry to compensate for charge injection. In fact, given the known downsides of charge-injection compensation circuitry discussed above, the vast majority of switches—though simulated to determine the impact of charge injection—have no compensation circuitry whatsoever.” Ex. 2002 ¶ 82. Based on this, Dr. Kinget concludes that “a POSITA would have been motivated to accept Oliaei’s comments that charge injection in its CMFB did not impact performance, and would not have been motivated to modify Oliaei.” *Id.*

c. Analysis

Dr. Holberg testifies that a person of ordinary skill in the art “would recognize that the addition of Vittoz’s balancing capacitors and dummy

switches would not substantively change the operation of Oliaei's circuit (other than to improve its performance by reducing effects of charge injection)." Ex. 1002 ¶ 202. Dr. Holberg explains that Vittoz's balancing capacitors and switches would function in the same way if incorporated into Oliaei's CMFB circuit concluding, "[h]ence, it would [have been] obvious to combine the elements of Oliaei and Vittoz by known methods to yield predictable results." *Id.* Dr. Holberg testifies that Vittoz acknowledges the effects of charge injection on common mode offset compensation, and adding Vittoz's balancing capacitors and switches to Oliaei is simply a known technique involving "the use of compensating components in order to reduce the effects of charge injection that arise from the switches." *Id.* ¶ 207 (citing Ex. 1012, 108). Dr. Holberg concludes that because "[t]he techniques for impedance matching and reducing charge injection disclosed by Vittoz had been recognized and studied for well over ten years prior to the filing date of the '463 Patent . . . a POSITA would have had a reasonable expectation of success in following the suggestions in Oliaei and Vittoz to combine their respective teachings." *Id.* ¶ 217 (citing Ex. 1012, 101–105).

On the complete record before us, we do not find Petitioner and Dr. Holberg's evidence and reasoning sufficient to support a combination of Oliaei and Vittoz. We appreciate that charge injection caused by turning off the switch in a sample-and-hold circuit was known to those of ordinary skill in the art to affect the sampled voltage V_C across the capacitor, as discussed for example in Vittoz. Ex. 1012, 101. This is confirmed by Patent Owner's declarant, Dr. Kinget, testifying that "Vittoz explains that at the moment the switch turns off, charge stored in the channel of the switch is released, causing the sample-and-hold circuit to deviate from its ideal behavior." Ex.

2002 ¶ 45. Yet, Dr. Kinget testifies that “[c]harge injection naturally occurs at every switch in a switched capacitor circuit, and . . . a POSITA would only add charge-injection compensation circuitry, if at all, at select locations where charge injection is known to adversely impact system performance.” *Id.* ¶ 75.

A person of ordinary skill in the art would not simply add charge injection circuitry, Dr. Kinget testifies, “because charge-injection circuitry is accompanied by many known downsides, including increased complexity, extra clocking circuitry to control the dummy switches, and the possibility of making the problem worse. *Id.* (citing Ex. 1013, 22–23). In support of this position, Dr. Kinget points to a text book, CMOS ANALOG CIRCUIT DESIGN, 2nd Ed., authored by Dr. Holberg, that states “known methods for addressing charge injection “never completely remove[] the feedthrough and in some cases may worsen it. Also, it is necessary to generate an inverted clock, which is applied to the dummy switch . . . Typically, these solutions will create problems in other areas.” *Id.* (quoting Ex. 1012, 22–23).

Dr. Kinget explains that absent a known circuit performance problem a person of ordinary skill in the art would not apply charge injection compensation to a circuit, and to the extent there was a concern, “they would have at the very least performed simulations to determine the impact of charge injection on a circuit before taking a remedial action.” *Id.* ¶ 77. Dr. Kinget again points to Dr. Holberg’s text book, which explains that

[c]harge injection involves a complex process whose resulting effects depend on a number of factors such as the layout of the transistor, its dimensions, impedance levels at the source and drain nodes, and gate waveform. It is hopeless to attempt to address all of these effects precisely analytically—we have computers to do that!

Id. (quoting Ex. 1013, 18). We find Dr. Kinget's testimony, explanations, and references to Dr. Holberg's testimony, persuasive as to issues surrounding adding charge injection circuitry. When questioned about adding charge injection circuitry in his deposition, Dr. Holberg confirmed that a person of ordinary skill in the art understood would not simply add charge injection circuitry to another circuit:

Q: So in the cases where you looked into charge injection and decided whether it was or was not an issue, what types of questions did you ask?

[]

A: I don't remember what questions I did ask, but I think the highest level is, would you ask yourself does charge -- would charge feedthrough error impact your performance, you know, the intended performance of the chip at the system level.

And if it would, you would address it. If it wouldn't, then you might just leave it be.

Q: Why would you leave it be?

A: Well, partly because it's simplicity. If you put a dummy switch next to every switch, the dummy switch has to be driven by the -- the inverse clock. And oftentimes it's a non-overlapping clock.

So you know, that's a lot of -- that's a lot of traces that you've got to run, a lot of extra circuitry that you'd add. And why do that if it's not necessary?

Ex. 2003, 34:7–35:5. Dr. Holberg further explained that a person of ordinary skill in the art understood that not all switched capacitors needed charge injection compensation and charge injection circuitry was only added by necessity:

Q: Is the idea that every switch in a switch capacitor circuit injects charge?

Is that correct?

A: I would say so.

Q: In the circuits that you designed, had you ever included charge injection compensation circuitry on every switch in that circuit?

A: I – I’m sure I’ve never put charge compensation circuitry on every switch. I’m sure of that. I’m sure that I have not done that.

I want to make sure that’s clear.

Q: And -- and why is that?

A: Because it wasn’t necessary.

Ex. 2003, 39:8–22.

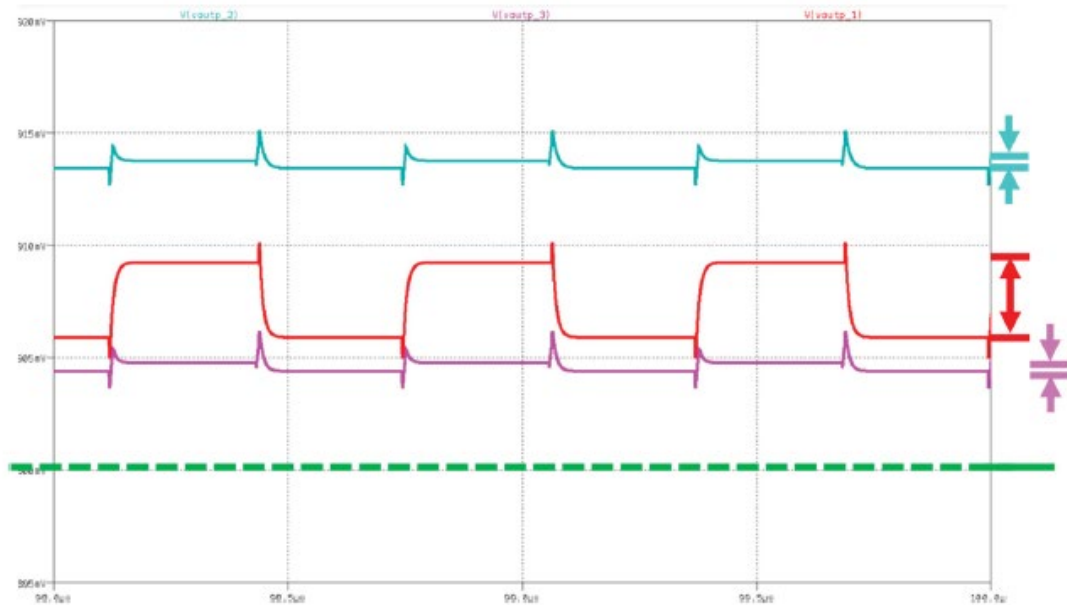
Overall, we find Dr. Holberg’s testimony particularly telling, and not very persuasive, with respect to combining Oliaei and Vittoz. Dr. Holberg makes clear that a person of ordinary skill in the art would have analyzed Oliaei’s circuit, and in particular any switches that were of concern, before implementing charge injection compensation circuitry. *See, e.g., id.* at 25:8–26:22 (Dr. Holberg describing for a pacemaker amplifier circuit he designed “I definitely did a lot of analysis because I had to deal with the DC value, so I did a lot of analysis on the charge injection impact.”). Dr. Holberg did not, however, provide any technical analysis or circuit performance simulations in his original declaration showing that Oliaei would benefit from Vittoz’s charge injection compensation circuitry. *See* Ex. 1002 ¶¶ 200–218.

Also, in his original Declaration, Dr. Holberg testified that “[a] POSITA *could have* combined the common-mode circuit and the common-mode feedback circuit of Oliaei with the impedance matching circuit of Vittoz using the known modeling methods disclosed by Vittoz.” Ex. 1002

¶ 202 (citing Ex. 1012, 101–105, Fig. 7). The mere fact that the prior art reference could be modified does not satisfy the requirements for a finding of obviousness. Indeed, even if Vittoz’s charge injection circuit could be implemented in Oliaei’s CMFB circuit, and “a POSITA would recognize Vittoz’s balancing capacitors and dummy switches would operate in substantially the same way, whether in the system disclosed by Vittoz or the system disclosed by Oliaei,” as Dr. Holberg testifies, this does not explain persuasively *why* a person of ordinary skill in the art would have added Vittoz’s charge injection circuitry into Oliaei’s CMFB circuit.

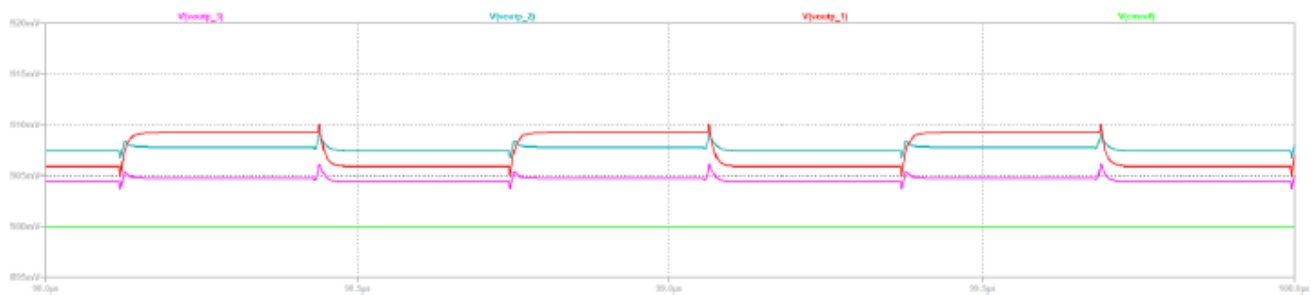
On the other hand, with Patent Owner’s Response, Dr. Kinget provided simulation evidence comparing (a) Oliaei’s unmodified CMFB circuit in Figure 5, (b) Petitioner’s asserted modified CMFB circuit using two capacitors C1 and C2, and (c) a third CMFB circuit according to the ’436 patent. Ex. 2002 ¶¶ 87–90. Dr. Kinget described the component specifications for his simulations, including sizing the precharging capacitors at 1/10 that of the feedback capacitors for the (a) unmodified and (b) Petitioner’s modified circuits. *Id.* at ¶¶ 97–98 (citing Ex. 1005, 12).⁸ For the simulation of the ’463 patent CMFB circuit, Dr. Kinget used the capacitor sizes described in the specification. *Id.* ¶ 98 (citing Ex. 1001, 8:9–18, 8:34–58). In all the circuit simulations, Dr. Kinget set the desired common mode to 900 mV (i.e., half the supply voltage of 1.8V). The results of Dr. Kinget’s simulations for all three circuits is reproduced in the graph below.

⁸ Ex. 1005, Jones & Martin, ANALOG INTEGRATED CIRCUIT DESIGN, 1997.



The graph above from Dr. Kinget's declaration shows in relation to desired common mode voltage (green), the comparison of (a) Oliaei's unmodified CMFB circuit in Figure 5, (red), (b) Petitioner's asserted modified CMFB circuit using capacitors C1 and C2, (light blue), and (c) a third CMFB circuit steady state output curve (purple) according to the '463 patent. *Id.* ¶ 99. Comparing the simulations, Dr. Kinget testifies that (c) the '463 patent's CMFB circuit (purple), performs best, while the difference between (b) Petitioner's modified CMFB in Oliaei (light blue) and the desired common mode is significantly larger on average than even (a) the unmodified CMFB circuit (red)— "[t]hat is, Petitioner's proposed modification performs worse than the unmodified circuit." *Id.* Based on these simulations, Dr. Kinget testifies that "[a] POSITA would not have modified Oliaei's CMFB in a way that provides a less accurate average common-mode level than the unmodified CMFB. Thus, my simulations confirm that a POSITA would not have combined Oliaei and Vittoz in the manner proposed in the Petition." *Id.* ¶ 100.

Dr. Holberg responds, testifying that Dr. Kinget’s parameters “are not unreasonable values – but certainly are not the only reasonable values that a POSITA would consider in order to evaluate the performance of the Oliaei/Vittoz Circuit.” Ex. 1022 ¶ 5. Dr. Holberg performed similar simulations to Dr. Kinget, but sizing the precharging capacitors at 1/4 that of the feedback capacitors, as also taught in the Jones & Martin text book. Ex. 1005, 291. Dr. Holberg’s results are reproduced below.



Dr. Holberg’s results indicate an improved common mode level performance for the modified Oliaei circuit (light blue) compared to Dr. Kinget’s results. Ex. 1022 ¶ 17. Dr. Holberg testifies further that “[i]n my personal experience of circuit design, I would anticipate running many such simulations before reaching any conclusions regarding the feasibility or performance of a proposed circuit modification.” *Id.* ¶ 19.

Based on both declarants’ testimony we are apprised that a person of ordinary skill in the art, if they had undertaken an analysis of charge injection compensation for the CMFB loops in Oliaei, might determine certain parameters that show improvement in the common mode level performance, as well as parameters that did not improve the circuit performance. Thus, although the evidence is somewhat split, we find that if a person of ordinary skill in the art were to analyze the charge injection for

Oliaei's CMFB circuits, applying Vittoz's charge injection compensation, the common mode feedback level and the common mode variability might be improved. This evidence, however, only answers part of the question as to why a person of ordinary skill in the art would have combined Oliaei and Vittoz. It perhaps shows that after performing many circuit analyses, the combination could potentially provide a better result than the unmodified circuit, depending on the parameters used.

Although we give this evidence some weight towards Petitioner's position, the simulation evidence still does not address fully why, where Dr. Holberg testifies every switch capacitor is naturally afflicted with charge injection, a person of ordinary skill in the art would have undertaken charge injection compensation analyses of Oliaei's common mode feedback circuits in the first place. Ex. 2003, 39:8–22. Neither Petitioner nor Dr. Holberg point to any persuasive evidence that Oliaei and its CMFB circuits have charge injection problems that would lead one of ordinary skill in the art to undertake such analyses. In fact, Oliaei addresses charge injection, expressly stating that “clock-feedthrough glitches [charge injection] generated by the CMFB give rise to a spectral component at the sampling frequency $1/T$ which does not affect the system performance.” Ex. 1007, 5:24–27. Oliaei describes further that

[n]umerous electrical simulations performed for a second-order continuous-time modulator including discrete-time common-mode feedback circuits have shown that discrete-time adjustment of the common-mode has no harmful effect on the output spectrum of the system.

Id. at 5:27–32. Oliaei thus not only states that there were no charge injection issues with its circuit in the first place, but goes on to explain that the inventors undertook numerous simulations showing that there was “no

harmful effect” due to charge injection. *Id.* We agree with Patent Owner that a person of ordinary skill in the art, given a plain reading of Oliaei, would most likely not undertake any charge injection analyses of the CMFB circuits. Therefore, along with the express disclosure in Oliaei, we credit Dr. Kinget’s testimony as the most persuasive, specifically that

a POSITA would have appreciated that all switches in theory cause some charge injection, but would also realize that the charge injection does not affect the system performance in Oliaei – indeed relatively few circuits warrant circuitry to compensate for charge injection. In fact, given the known downsides of charge-injection compensation circuitry discussed above, the vast majority of switches—though simulated to determine the impact of charge injection—have no compensation circuitry whatsoever.

Ex. 2002 ¶ 81.

Considering all the evidence of record, we agree with Patent Owner that Petitioner has not asserted sufficient rationale for the combination of Oliaei and Vittoz. *See* PO Resp. 51–77; Ex. 2002 ¶¶ 71–103. Petitioner alleges similarities between Oliaei and Vittoz and that the resulting combination, based on a desire to compensate for charge injection, would have predictably yielded the claimed system. Pet. 77–81. The arguments and evidence are deficient, however, for several reasons. First, as discussed above, we considered Petitioner’s assertion that a person of skill in the art would consider charge injection as a reason to look to Vittoz. Pet. 77. The evidence from both Dr. Holberg and Dr. Kinget is clear, however, that charge injection is not always necessary or compensated for in every switched capacitor circuit. *See, e.g.*, Ex. 2003, 39:16–18 (Dr. Holberg stating that “I’m sure I’ve never put charge compensation circuitry on every switch. I’m sure of that.”). Second, Petitioner’s evidence including

simulations of the combined Oliaei and Vittoz teachings, together with Patent Owner's simulation evidence, illustrate that there are no clear-cut improvements in Oliaei's circuit. The experts' simulations, as a whole, show that by choosing particular parameters Oliaei's circuit performance might be improved, and choosing other reasonable parameters would not improve circuit performance. With results of the simulations going both ways, the evidence is not persuasive that the combination would have yielded a predictable result. Third, the alleged rationale of adding charge injection compensation does not address sufficiently the reason a person of ordinary skill in the art would combine the relevant teachings of Oliaei and Vittoz. Oliaei expressly discloses that the inventors undertook "numerous" simulations to address issues of clock-feedthrough glitches, i.e., charge injection, and that the results showed no impact of charge injection on system performance. Ex. 1007 5:17–32. Without sufficient explanation, Petitioner and Dr. Holberg have failed to present a persuasive rationale for the alleged combination.

In highly developed fields such as the design of common mode feedback circuits and switched capacitors, small differences may produce a nonobvious advance. *See Outside the Box Innovations, LLC v. Travel Caddy, Inc.*, 695 F.3d 1285, 1298 (Fed. Cir. 2012); *see also Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360–61 (Fed. Cir. 2011) (providing that the inquiry under § 103 is not whether the claimed invention is "sufficiently simple to appear obvious to judges after the discovery is finally made"). "The emphasis on nonobviousness is one of inquiry, not quality" of the advance. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The reason this inquiry is important is because "[j]udicial hindsight must be avoided."

Orexo AB v. Actavis Elizabeth LLC, 903 F.3d 1265, 1271 (Fed. Cir. 2018); *see also KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”). Here, Petitioner’s rationale and circuit simulations applying certain parameters that show some modicum of improvement in the CMFB circuit seem to be simply working back Patent Owner’s claims to arrive at the claimed invention, which we decline to do. *See Orexo*, 903 F.3d at 1271 (“It is inappropriate to use the template provided by the inventor, to render the inventor’s contribution obvious.”).

d. Conclusion Regarding Oliaei and Vittoz

Based on the Petition and the evidence of record, we find insufficient evidence to establish that a person of ordinary skill would have had reason to combine the teachings of Oliaei and Vittoz to arrive at the inventions of independent claims 1 and 11. Accordingly, Petitioner has not shown by a preponderance of the evidence that claims 1 and 11, nor dependent claims 2–7, 10, 12–17, and 29, are unpatentable over Oliaei and Vittoz.

III. CONCLUSION

Petitioner has proved by a preponderance of the evidence that claims 1, 2, 4, and 6 of the ’463 patent would have been obvious over Oliaei.⁹

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Petitioner has not shown by a preponderance of the evidence that claims 11, 13, and 29 are obvious over Oliaei. Petitioner has not shown by a preponderance of the evidence that claims 1–7, 10–17, and 29 would have been obvious over Oliaei and Vittoz.

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 4, 6, 11, 13, 29	103	Oliaei	1, 2, 4, 6	11, 13, 29
1–7, 10–17, 29	103	Oliaei, Vittoz		1–7, 10–17, 29
Overall Outcome			1, 2, 4, 6	3, 5, 7, 10–17, 29

IV. ORDER

For the reasons given, it is

ORDERED that, based on a preponderance of the evidence claims 1, 2, 4, and 6 of the '463 patent have been shown to be unpatentable;

ORDERED that claims 3, 5, 7, 10–17, and 29 have not been proven by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, any party to the proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01336
Patent 7,012,463 B2

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