

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INC.
and STMICROELECTRONICS, INC.,¹

Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-01492
Patent 6,651,134 B1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ STMicroelectronics, Inc., which filed a petition in IPR2021-00702, has been joined as a party to this proceeding. *See* Paper 23.

I. INTRODUCTION

A. BACKGROUND

Qualcomm Inc., (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1–7 and 9–21 (“the challenged claims”) of U.S. Patent No. 6,651,134 B1 (Ex. 1001, “the ’134 patent”). Pet. 6. Monterey Research, LLC, (“Patent Owner”) filed a Preliminary Response. Paper 6. After our email authorization, Petitioner filed a Preliminary Reply (Paper 7) and Patent Owner filed a Preliminary Sur-Reply (Paper 8). We instituted review. Paper 9 (“Institution Decision” or “Inst.”).

After institution, STMicroelectronics, Inc. (“STM”) was joined as a party. Paper 23. In *Advanced Micro Devices, Inc. and STMicroelectronics, Inc. v. Monterey Research, LLC*, IPR2020-00985, Paper 31 (Nov. 30, 2021), we determined that STM showed by a preponderance of the evidence that claims 1–21 of the ’134 patent are unpatentable. Thus, STM is estopped from challenging the patentability of those claims in this proceeding. *See* 35 U.S.C. § 315(e)(1). Thus, our use of “Petitioner” in this decision, including the Order below, refers solely to Qualcomm.

Patent Owner filed a Response (Paper 16, “PO Resp.”), Petitioner filed a Reply (Paper 21, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 24, “PO Sur-Reply”). An oral hearing was held on December 7, 2021, and a transcript appears in the record. Paper 30 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that claims 1–7 and 9–21 of the ’134 patent are unpatentable.

B. RELATED MATTERS

As required by regulation, the parties identify matters related to the '134 patent. Pet. 2–3; Paper 3, 1–2. Of note is *Advanced Micro Devices, Inc. v. Monterey Research, LLC*, IPR2020-00985, in which AMD challenged all claims of the '134 patent. We issued a final written decision in that proceeding on November 30, 2021, determining all claims unpatentable. IPR2020-00985, Paper 31. Additionally, the district-court case involving Qualcomm is identified as *Monterey Research, LLC v. Qualcomm Inc. et al.*, No. 1:19-cv-02083 (D. Del. 2019), whereas the case involving AMD is identified as *Monterey Research, LLC v. Advanced Micro Devices Inc.*, No. 1:19-cv-02149 (D. Del. 2019). Paper 3, 1; Pet. 3.

C. REAL PARTIES IN INTEREST

Petitioner identifies itself, Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific Pte Ltd. as real parties in interest. Pet. 2. Patent Owner identifies itself and IPValue Management as real parties in interest. Paper 3, 1.

D. THE '134 PATENT

The '134 patent is titled Memory Device with Fixed Length Non Interruptible Burst. Ex. 1001, code (54). The patent discloses that “the data burst transfers of conventional memories can be interrupted and single access made,” and proposes a memory device “that has a fixed burst length.” *Id.* at 1:37–45.

Figure 1 is reproduced below:

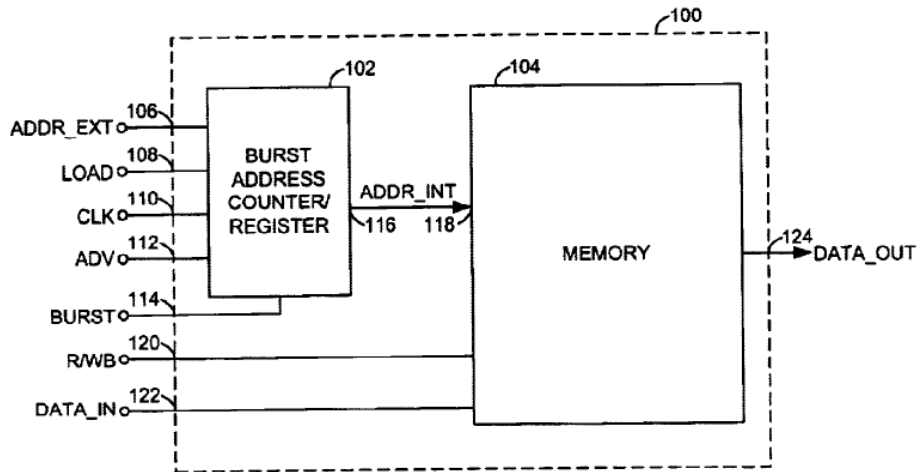


FIG. 1

Ex. 1001, Fig. 1. Figure 1 depicts circuit 100 configured as a fixed burst memory, in which circuit 102 accepts external signals including external address signal ADDR_EXT, and “generate[s] the signal ADDR_INT as a fixed number of addresses in response to the signal CLK.” *Id.* at 3:21–22. The ’134 patent states that “[o]nce the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).” *Id.* at 3:25–28.

The ’134 patent depicts two embodiments for circuit 102, in Figures 2 and 3. Figure 2 is reproduced below:

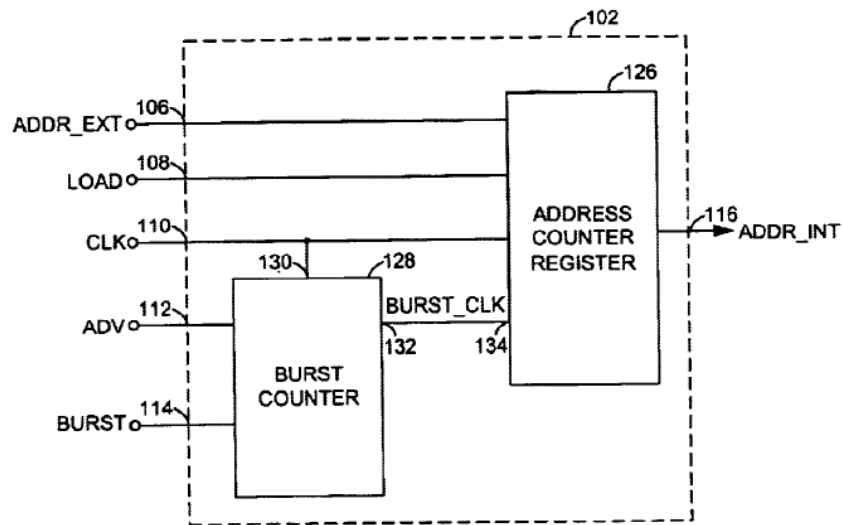


FIG. 2

Id. Fig. 2. Figure 2 shows burst counter 128 receiving signal CLK (a clock signal), signal ADV, and signal BURST, and providing signal BURST_CLK. “When the signal ADV is asserted, the burst counter 128 will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST.” *Id.* at 4:10–14. Figure 3 and the associated description disclose an alternative circuit, in which “counter 138 may be configured to generate a number of addresses in response to the signals CLK, BURST[,], and ADV” and where “[t]he number of addresses generated by the counter 138 may be programmed by the signal BURST.” *Id.* at 4:29–34. The ’134 patent describes more generally that, “[w]hen the signal ADV is asserted, the circuit 100 will generally generate a number of address signals” and that “[t]he address signals will generally continue to be generated until the Nth address signal is generated.” *Id.* at 4:42–48.

E. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. A circuit comprising:
 - a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and
 - a logic circuit configured to generate a predetermined number of said internal address signals in response to
 - (i) an external address signal, (ii) a clock signal and
 - (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

Ex. 1001, 5:22–32. Independent claim 16 recites limitations similar to those of claim 1, expressed as means-plus-function elements. *Id.* at 6:20–30.

Independent claim 17 recites limitations similar to those of claim 1, expressed as a “method of providing a fixed burst length data transfer.” *Id.* at 6:31–39. Claims 2–7 and 9–15 depend, directly or indirectly, from claim 1. *Id.* at 5:33–6:19. Claims 18–21 depend, directly or indirectly, from claim 17. *Id.* at 6:40–48.

F. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1–5, 7, 9, 10, 12–18, 20, 21	102	Schaefer ²
1–7, 9, 10, 12–21	103	Schaefer, Fujioka ³
11	103	Schaefer, Lysinger ⁴

² U.S. Patent No. 5,600,605 (Ex. 1017).

³ U.S. Patent No. 6,185,149 (Ex. 1006).

⁴ U.S. Patent No. 5,784,331 (Ex. 1009).

Claim(s) Challenged	35 U.S.C. §	References/Basis
11	103	Schaefer, Lysinger, Fujioka

Pet. 6–7. Petitioner also relies on the Declaration of Robert Murphy.
Ex. 1015.

II. ANALYSIS

A. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner proposes that a person of ordinary skill “would have had at least a degree in electrical or computer engineering, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 14 (citing Ex. 1015 ¶ 48). Patent Owner does not dispute this definition of a person of ordinary skill. PO Resp. 21.⁵ We adopt Petitioner’s proposed level of ordinary skill as it appears to be consistent with the level of skill reflected by the specification and in the asserted prior art references.

B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Petitioner proposes constructions for the following terms: “non-interruptible,” “internal address signal,”

⁵ As discussed below, Patent Owner does challenge the credibility of Petitioner’s expert witness based on his testimony in a district-court litigation supporting a slightly different level of ordinary skill in the art for the ’134 patent. See PO Resp. 21; *infra* at 12 n.6.

“predetermined number of [said] internal address signals,” “fixed burst length,” “means for reading data” and “means for generating a predetermined number of said internal address signals.” Pet. 21–27.

In the Institution Decision, we adopted the parties’ construction for “non-interruptible”—“cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated.” Inst. 7. The parties do not dispute that construction (*see* PO Resp. 22), and we maintain it for this decision.

We also adopted the parties agreed constructions for the two “means for” terms in claim 16. Inst. 8–9. Patent Owner expressly confirms it agrees with those constructions. PO Resp. 22–23. We maintain those constructions here. Thus, we apply the “means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals” to require a corresponding structure of a memory array 104, or equivalents. We apply the “means for generating a predetermined number of said internal address signals . . .” to require a corresponding structure of burst address counter/register 102, as depicted in either Figure 2 or Figure 3 of the ’134 patent, or equivalents.

As to the remaining terms for which Petitioner proposes a construction, none affects a dispute in this proceeding and therefore none warrants construction. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

C. ANTICIPATION BY SCHAEFER

Schaefer discloses a “synchronous dynamic random access memory (SDRAM)” in which command signals and address bits cause a controller to access memory cells in a variety of ways. Ex. 1017, code (57). Schaefer

explains that “a SDRAM requires separate commands for accessing and precharging a row of storage cells in the SDRAM memory array.” *Id.* at 1:33–35. That precharge operation “deactivate[s] and precharge[s] a previously accessed bank memory ar[ra]y” and may result in wasted time between read and write operations. *Id.* at 1:42–54. Schaefer discloses the ability to use an “AUTO-PRECHARGE command feature” so that “a manual PRECHARGE command does not need to be issued during the functional operation” of the SDRAM. *Id.* at 7:29–40. “The AUTO-PRECHARGE command insures that the precharge is initiated at the earliest, valid stage within a burst cycle.” *Id.* at 7:40–42. When the AUTO-PRECHARGE command is used in conjunction with a READ or WRITE command, “[t]he user is not allowed to issue another command until the precharged time (t_{RP}) is completed.” *Id.* at 7:42–44. To that end, “[a] no operation (NOP) command can be provided to SDRAM 20 to prevent other unwanted commands from being registered during idle or wait states.” *Id.* at 8:8–10. Schaefer depicts the timing of a read operation using the auto-precharge option in Figure 4, reproduced below:

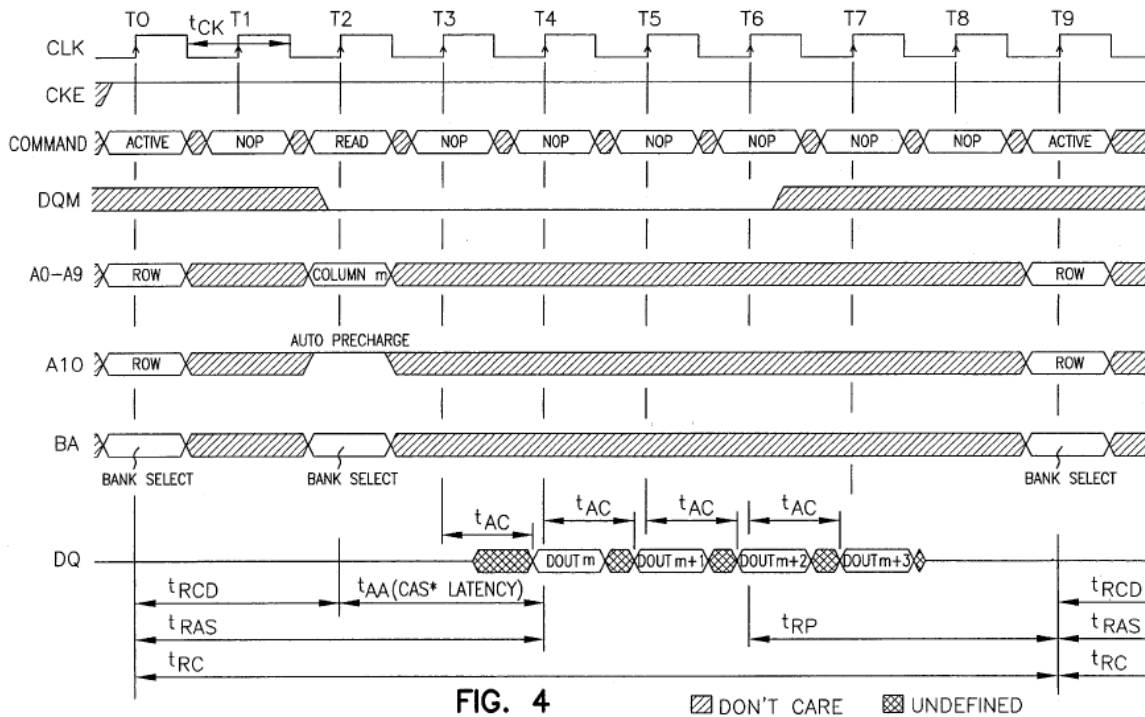


Figure 4 depicts a four-cycle burst transfer read operation, in which the READ command is given at time t_2 , the first cycle of data is output at time t_4 , and the precharge period t_{RP} runs from time t_6 to time t_9 . *Id.* at 8:37–9:1, Fig. 4.

Petitioner contends that Schaefer’s SDRAM memory discloses the circuit elements (e.g., memory, logic circuit) required by the challenged claims. Pet. 36–38 (quoting Ex. 1017, Fig. 1). In Petitioner’s view, by disclosing burst read and write operations that use the AUTO-PRECHARGE feature, Schaefer also discloses generating a predetermined number of internal address signals such that the generation is non-interruptible. Pet. 40–43.

Patent Owner does not dispute that Schaefer discloses the circuit elements required by the challenged claims. Instead, Patent Owner contends that Schaefer does not disclose non-interruptible address generation because

it discusses burst interruption in certain contexts and prohibits user commands only during the precharge period. PO Resp. 29–30.

As to Schaefer’s discussion of burst interruptions, Patent Owner points out that Schaefer discloses a “full-page burst,” which “will wrap around and continually restart the ‘burst’ operation until a BURST TERMINATION command or PRECHARGE command is indicated by command controller 28 or until interrupted with another burst operation.” Ex. 1017, 5:15–19; *see* PO Resp. 30–31. Patent Owner submits that those burst-termination options are required for a full-page burst, i.e., that a full-page burst *must* be terminated by user command. PO Resp. 31–32.

As to prohibiting commands only during the precharge period, Patent Owner argues that Schaefer’s concern for wasted clock cycles between bursts motivated its focus on “reducing the amount of time required to perform the PRECHARGE and ACTIVE command operations necessary for proper SDRAM operation.” *Id.* at 33. According to Patent Owner, when a user desires to read a data series shorter than an available burst length, terminating the burst once the desired data have been read would save clock cycles. *Id.* at 34–36. Thus, Patent Owner reasons that Schaefer’s prohibition on user commands when an AUTO-PRECHARGE option has been issued would apply only once the precharge time has started, not before then. *Id.* at 36.

Thus, the parties dispute whether Schaefer’s prohibition on user commands begins with the issuance of a read or write command using the AUTO-PRECHARGE option (time t_2 in Figure 4) as Petitioner contends, or instead begins only when the resulting precharge operation begins (time t_6 in

Figure 4) as Patent Owner contends. *Id.* at 36–37; Pet. Reply 7; PO Sur-Reply 4.

Patent Owner asserts that because Schaefer “is directed to eliminating wasted cycles *in between* bursts by reducing the amount of time necessary to complete PRECHARGE and ACTIVE command operations,” Schaefer’s disclosures relate to completing the precharge operation before immediately activating a row. PO Resp. 38–39. Patent Owner reasons that because interrupting precharge or row-activation operations would interfere with memory operation, preventing interruption during those operations makes sense. PO Resp. 40–45. That aspect of Schaefer’s operation, however, is not in dispute—the question is whether Schaefer’s prohibition on interruption begins before the precharge operation begins.

Patent Owner’s arguments fail to overcome Schaefer’s express statement that, when a READ or WRITE command is issued with the AUTO-PRECHARGE feature, “[t]he user is not allowed to issue *another* command until the precharged time (t_{RP}) is completed.” Ex. 1017, 7:32–44 (emphasis added). In this context, *another* command refers to any user command other than or in addition to the user command that initiated a burst address generation (e.g., READ at time t_2 in Figure 4). Thus, Schaefer’s statement prohibiting *another* command until the end of the precharge period also precludes issuing a burst terminate command before the precharge period begins (time t_6 in Figure 4).

Petitioner’s expert supports this interpretation of Schaefer, explaining that a device could be designed to allow interruptions before the precharge period, but that doing so “would have been more costly (more circuitry) and may have detrimentally impacted the speed of operation.” Ex. 1015 ¶ 83. In

light of that tradeoff—a classic engineering decision balancing features against cost—it is logical and reasonable to interpret Schaefer’s statement according to its plain words. We agree with Petitioner that although Schaefer’s system could have been designed to behave as Patent Owner asserts it does, that is not what Schaefer describes. Pet. Reply 9. Although Patent Owner criticizes Petitioner’s expert, Mr. Murphy, for not definitively stating that allowing interruptions would have impaired the circuit’s speed of operation (PO Sur-Reply 9), we do not view his testimony as flawed for that reason. The actual effect on a circuit depends on many aspects beyond the scope of Schaefer’s disclosures and we see no reason to require that Petitioner show actual impacts of potential redesigns, beyond a credible expert testifying as to the principles underlying Schaefer’s choice.⁶

Patent Owner argues that because Schaefer states that “[t]he AUTO-PRECHARGE command insures that the precharge is initiated at the earliest, valid stage within a burst cycle,” its prohibition on user commands “until the precharged time (t_{RP}) is completed” begins only when precharge is initiated. PO Sur-Reply 5–6 (quoting Ex. 1017, 7:38–44 (emphasis omitted)). According to Patent Owner, the reference to t_{RP} not only defines the end of the prohibition period, but also defines the start of the prohibition. *Id.* We do not agree. The quoted passage repeats the benefit of using an

⁶ Patent Owner argues that the opinions of Petitioner’s expert, Mr. Murphy, should be accorded little weight because he gave a different opinion on the level of ordinary skill in the art when testifying in another proceeding. PO Resp. 23–28. We do not agree that the differences in Mr. Murphy’s testimony suggest bias, unreliability, or any other characteristic that would undermine his credibility. As Petitioner explains, Mr. Murphy adopted the level of skill proposed by AMD in IPR2020-00985, which also involved the ’134 patent. Pet. Reply 5–6.

AUTO-PRECHARGE option with a burst command—the precharge operation begins at the earliest possible stage. But identifying when the precharge operation begins does not identify when the prohibition against issuing *another* command begins. Rather, the statement that a “user is not allowed to issue another command” connects the prohibition to the last issued user command, which is the READ or WRITE command with AUTO-PRECHARGE. Ex. 1017, 7:38–44. Thus, we do not agree with Patent Owner’s strained interpretation of Schaefer’s plain language. *See* PO Sur-Reply 7–8.

Further, we agree with Petitioner that additional evidence supports that Schaefer does not permit termination of fixed-length burst operations with the AUTO-PRECHARGE option selected. *See* Pet Reply 12–15. Schaefer discusses burst termination, but only for “full page” (as opposed to fixed-length) bursts, which do not use the AUTO-PRECHARGE option. *See id.* at 12–13 (citing Ex. 1017, 5:15–19, 5:59–62; Ex. 1029, 34:8–23, 36:5–37:12, 38:17–39:8). Because full-page bursts require termination, Schaefer discusses the need for user-issued burst-terminate commands. Ex. 1017, 5:15–19; Ex. 1029, 36:5–18. Likewise, because fixed-length bursts complete automatically and do not require user termination, Schaefer does not discuss user-issued burst-terminate commands in the context of fixed-length burst commands. Moreover, there is no inherent requirement that Schaefer permit such commands in that context. Pet. Reply 13. In short, we agree with Petitioner that the evidence is consistent with Schaefer’s prohibition of user commands from the time a fixed-length burst is initiated with the AUTO-PRECHARGE selected. According to Schaefer’s plain words, in fixed-length bursts with AUTO-PRECHARGE, any user command (“another”)

after the initial burst command is prohibited until precharge is complete. Ex. 1017, 7:42–44. Therefore, Schaefer’s address generation is non-interruptible as claimed.

Patent Owner does not otherwise dispute Petitioner’s anticipation contentions for claims 1–5, 7, 9, 10, 12–18, 20, or 21. *See* PO Resp. 29–52; Pet. Reply 15; PO Sur-Reply 4.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that Schaefer anticipates claims 1–5, 7, 9, 10, 12–18, 20, and 21.

D. OBVIOUSNESS OVER SCHAEFER AND FUJIOKA

Petitioner contends that claims 1–7, 9, 10, and 12–21 are obvious over the combination of Schaefer and Fujioka. Pet. 64–77. Fujioka discloses a memory circuit that generates bursts, and includes embodiments with mode-selection circuitry that enables burst length to be set during the fabrication process. Ex. 1006, 4:24–25, 14:55–15:24. Petitioner argues that skilled artisans would have had reason to use Fujioka’s mode-selection circuitry to set Schaefer’s burst length because it “would have reduced the amount of circuitry required in Schaefer’s mode register 40, the initialization time before burst operations, and the testing time, all while still providing a degree of programmability.” Pet. 66 (citing Ex. 1015 ¶ 133); *id.* at 66–67 (providing additional reasons for the combination). Other than as relates to Schaefer’s disclosures discussed above, Patent Owner does not contest Petitioner’s contentions. *See* PO Resp. 52–53.

We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence

that the combination of Schaefer and Fujioka renders obvious the subject matter of claims 1–7, 9, 10, and 12–21. *See* Pet. 64–77.

E. OBVIOUSNESS OVER SCHAEFER AND LYSINGER

Claim 11 depends from claim 1 and recites that the “predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.” Ex. 1001, 6:4–7. Petitioner submits that claim 11 would have been obvious over the combined disclosures of Schaefer and Lysinger. Pet. 77–82.

Lysinger discloses a memory circuit with a burst controller that increments memory addresses. Ex. 1009, 2:5–7. As one approach, Lysinger teaches delaying the transmission of a new address until the end of a possible “timing window” such that the memory device may “perform other functions such as accessing other memory devices or interfacing with the microprocessor.” *Id.* at 26:34–49.

Petitioner asserts that skilled artisans “would have understood the advantage of increased data throughput by being able to access additional memory arrays by using the address and control busses that were freed.” Pet. 80 (citing Ex. 1015 ¶ 168).

Other than as relates to Schaefer’s disclosures discussed above, Patent Owner does not contest Petitioner’s contentions. *See* PO Resp. 53. We have considered Petitioner’s contentions in light of the full record and conclude that Petitioner has shown by a preponderance of the evidence that the combination of Schaefer and Lysinger renders obvious the subject matter of claim 11. *See* Pet. 77–82.

III. CONCLUSION⁷

For the reasons discussed, we conclude:

Claim(s)	35 U.S.C. §⁸	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–5, 7, 9, 10, 12–18, 20, 21	102	Schafer	1–5, 7, 9, 10, 12–18, 20, 21	
1–7, 9, 10, 12–21	103	Schaefer, Fujioka	1–7, 9, 10, 12–21	
11	103	Schaefer, Lysinger	11	
11	103	Schaefer, Lysinger, Fujioka		
Overall Outcome			1–7, 9–21	

⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

⁸ We do not reach the ground based on Schaefer, Lysinger, and Fujioka (*see supra* at 6) because doing so would not change the overall outcome of this Decision. See *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. Apr. 30, 2020) (nonprecedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding” and, thus, agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

IV. ORDER

It is

ORDERED that Petitioner has proven that claims 1–7 and 9–21 of the '134 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 6,651,134 B1

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