

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INC.,

Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-01493
Patent 6,765,407 B1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. BACKGROUND

Qualcomm Incorporated, (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1–3, 7–10, and 14–17 (“the challenged claims”) of U.S. Patent No. 6,765,407 B1 (Ex. 1001, “the ’407 patent”). After preliminary briefing, we instituted review. Paper 11.

Patent Owner filed a Response (Paper 15, “PO Resp.”), Petitioner filed a Reply (Paper 19, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 22, “PO Sur-Reply”). An oral hearing was held on December 7, 2021, and a transcript appears in the record. Paper 29 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that claims 1–3, 8–10, and 15–17 of the ’407 patent are unpatentable, but has not demonstrated that claims 7 or 14 are unpatentable.

B. RELATED MATTERS

As required by regulation, the parties identify matters related to the ’407 patent. Pet. 2; Paper 5, 1. Of note is *Advanced Micro Devices, Inc. v. Monterey Research, LLC*, IPR2020-00989 (“the AMD proceeding”), in which AMD challenged claims 1–3, 6–10, 13–17, and 20 of the ’407 patent. We issued a final written decision in that proceeding on November 30, 2021, determining claims 1–3, 6–10, 13–17, and 20 unpatentable. IPR2020-00989, Paper 42.

Additionally, the district-court case involving Qualcomm is identified as *Monterey Research, LLC v. Qualcomm Inc. et al.*, No. 1:19-cv-02083

(D. Del. 2019), whereas the case involving AMD is identified as *Monterey Research, LLC v. Advanced Micro Devices Inc.*, No. 1:19-cv-02149 (D. Del. 2019). Paper 5, 1; Pet. 2.

C. REAL PARTIES IN INTEREST

Petitioner identifies itself, Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific Pte Ltd. as real parties in interest. Pet. 2. Patent Owner identifies itself and IP Value Management as the real parties in interest. Paper 5, 1.

D. THE '407 PATENT

The '407 patent describes a “digital configurable macro architecture.” Ex. 1001, code (57). To that end, it describes “programmable digital circuit blocks” that are “8-bit circuit modules that can be programmed to perform any one of a variety of predetermined digital functions by changing the contents of a few registers therein.” *Id.* at 2:4–7. As examples, the '407 patent states that its programmable blocks can be configured as “timers, counters, serial communication ports, cyclic redundancy generators/checkers (CRC), or pseudo random sequence generators (PRS).” *Id.* at 2:14–17. The blocks may also be “coupled in series or in parallel to handle more complex digital functions.” *Id.* at 2:21–23; *accord id.* at 6:29–43.

A particular block is configured in the '407 patent “by changing the contents of the configuration registers.” *Id.* at 2:35–37; *accord id.* at 4:55–57. Thus, explains the patent, “configuration of the programmable digital circuit block is fast and easy.” *Id.* at 2:34–35; *accord id.* at 4:59–63. In that regard, the description contrasts the '407 patent with field programmable gate array (FPGA) devices, which it states “need to have their look-up tables

re-programmed in order to enable them to implement a new digital function, which is a time consuming task.” *Id.* at 1:55–57; *accord id.* at 5:1–5.

E. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. A programmable digital device comprising:
a programmable digital circuit block that is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

Ex. 1001, 8:35–39. Claims 8 and 15 are independent and recite similar limitations; claim 8 requiring an array of programmable digital circuit blocks, and claim 15 expressing the elements as steps of a method. *Id.* at 9:5–10, 10:5–15. The remaining challenged claims depend from one of the independent claims. *Id.* at 8:35–10:37.

F. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1, 3, 7, 8, 10, 14, 15, 17	102	PIC16C7X Datasheet ¹
2, 9, 16	103	PIC16C7X Datasheet, AN594 ²

Pet. 5. Petitioner also relies on the Declaration of John Villasenor, Ph.D.
Ex. 1010.

¹ PIC16C7X Datasheet, Microchip Technology Inc., 1997 (Ex. 1008).

² AN594 Application Note, Microchip Technology Inc., 1997 (Ex. 1009).

II. ANALYSIS

A. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner proposes that a person of ordinary skill “would have had at least a bachelor’s degree in electrical or computer engineering, or a similar field with at least two years of experience in digital circuit and computer design, or a person with a master’s degree in electrical or computer engineering, or a similar field with a specialization in digital circuit and computer design.” Pet. 7 (citing Ex. 1010 ¶ 32). Patent Owner adopts that definition of a person of ordinary skill. PO Resp. 10. We adopt Petitioner’s proposed level of ordinary skill as it appears to be consistent with the level of skill reflected by the specification and in the asserted prior-art references.

B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Petitioner discusses the construction of an “array of programmable digital circuit blocks,” recited in claim 8, and notes that the term should not exclude “two or more identical or similar programmable digital circuit blocks.” Pet. 11–14. Patent Owner asserts that neither “array” nor any other term requires express construction. PO Resp. 10–11.

In Patent Owner’s view, Petitioner applies “programmable digital circuit block” in a way “that deviates from the plain requirements of the Challenged Claims.” *Id.* at 10. Patent Owner does not, however, explain that assertion in a manner that distinguishes prior-art features from the claim language. *See id.* at 10–11. While we discuss the parties’ differing

viewpoints below in context, we conclude that no express claim construction beyond that addressed in our analysis below is required in this proceeding. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

C. ANTICIPATION BY PIC16C7X DATASHEET

PIC16C7X Datasheet (“PIC16”) discloses the operational details of the PIC16C7X family of microcontrollers. Ex. 1008, 1. Within the family, some devices include a richer set of features than others. Relevant here, the PIC16C73 includes a number of peripheral features, “including: three timer/counters, two Capture/Compare/PWM modules and two serial ports.” *Id.* at 5; *accord id.* at 11 (Figure 3-2, depicting CCP1 and CCP2); *see* Pet. 15 (“The below grounds focus on the PIC16C7X models that contain two CCP modules, such as the PIC16C73.”).

Each Capture/Compare/PWM (CCP) module may be configured to operate in one of three modes. Ex. 1008, 71. Capture mode “captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1.” *Id.* at 72. “In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value” and, “[w]hen a match occurs, the RC2/CCP1 pin is” driven high, driven low, or remains unchanged (depending on the value of control bits), and an interrupt flag bit is set. *Id.* at 73. “In Pulse Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output.” *Id.* at 74.

Each CCP module has a dedicated configuration register—CCP1 is configured by CCP1CON and CCP2 is configured by CCP2CON. *Id.* at 71. PIC16’s Figure 10-1 is reproduced below:

FIGURE 10-1: CCP1CON REGISTER (ADDRESS 17h)/CCP2CON REGISTER (ADDRESS 1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: Unimplemented: Read as '0'

bit 5-4: CCPxX:CCPxY: PWM Least Significant bits
Capture Mode: Unused
Compare Mode: Unused
PWM Mode: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0: CCPxM3:CCPxM0: CCPx Mode Select bits
0000 = Capture/Compare/PWM off (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set; CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled))
11xx = PWM mode

Ex. 1008, 72. Figure 10-1 shows the functions of the bits in the CCP1CON/CCP2CON configuration registers, of which bits 7-6 are unimplemented, bits 5-4 are used only in PWM mode to control the duty cycle, and bits 3-0 control the CCP module's mode.

Petitioner maps claim 1's "programmable digital circuit block" to PIC16's Capture/Compare/PWM modules (CCP1 and CCP2). Pet. 15–35. Petitioner asserts each CCP module is "configured with a single register write operation" because the registers used to control the module—CCP1CON for CCP1 and CCP2CON for CCP2—select the operational mode. *Id.* at 20–21 (citing Ex. 1008, 71–72). We, like the parties, use CCPxCON to refer to the CCP configuration registers nonspecifically. Petitioner reasons that, when the PIC16 device is first powered on, the values of the CCP configuration registers are zero. Pet. 21 (citing Ex. 1008,

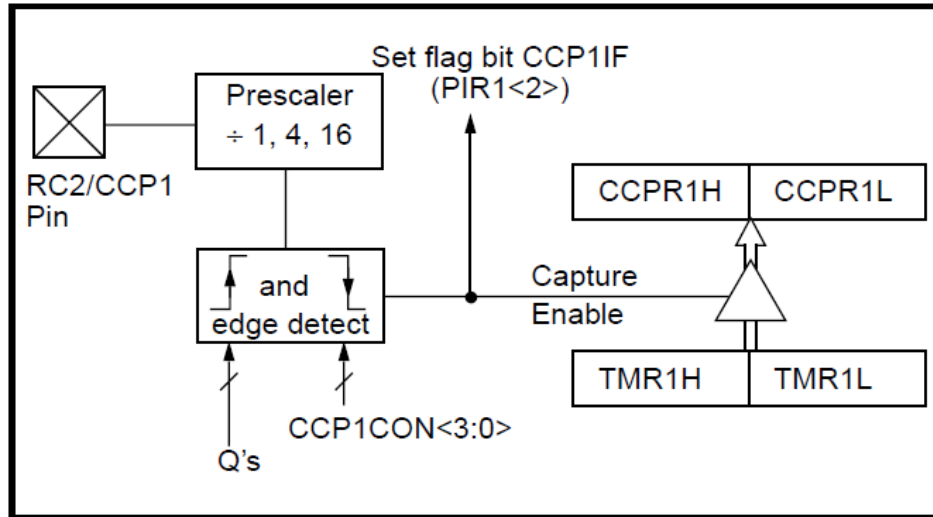
25; Ex. 1010 ¶ 80). Because a single instruction is able to set the values of the bits (bits 2 and 3) that cause a CCP module to begin its capture (01xx), compare (10xx), or PWM (11xx) function, Petitioner asserts that the modules are configurable by a single register write operation. *Id.* at 23–31. Petitioner gives several examples of single instructions that would configure one of PIC16’s CCP modules to operate in capture, compare, or PWM mode. *Id.*

1. Claim 1

Patent Owner argues that PIC16’s CCP cannot be the claimed programmable digital circuit block because other components are necessary to perform the capture, compare, and PWM modes. PO Resp. 12–22. We do not agree. In this regard, it is important to recognize the claim requires a circuit block “configurable to perform any one of a plurality of predetermined digital functions” and Petitioner identifies PIC16’s CCP module as that block, configurable to perform its capture, compare, or PWM function. Pet. 31–32. Patent Owner contends that because PIC16’s Figures 10-2, 10-3, and 10-4 depict components that “are required for the capture, compare, and PWM modes” and also “depict and involve components in addition to the CCP,” the CCP module cannot perform the asserted functions. PO Resp. 12–13.

We use the capture mode for our consideration of this argument, but reach the same conclusion for all three of the CCP functions that Petitioner relies on. PIC16 states that, “[i]n Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1.” Ex. 1008, 72. PIC16’s Figure 10-2 is reproduced below:

**FIGURE 10-2: CAPTURE MODE
OPERATION BLOCK
DIAGRAM**



Id. Figure 10-2 depicts block elements for the described capture-mode functionality. Although the operation block diagram depicts certain elements, such as an input pin (RC2/CCP1) or timer registers (TMR1H and TMR1L), that does not mean that the capture function is performed by all of the elements depicted. Rather, consistent with the described functionality, the CCP module itself will copy the value of TMR1H and TMR1L into CCPR1H and CCPR1L, respectively. *See id.*, 72, Fig. 10-2. PIC16 describes that the capture is performed “when an event occurs on pin RC2/CCP1” and further explains that the event may be “every falling edge,” “every rising edge,” “every 4th rising edge,” or “every 16th rising edge.” *Id.* at 72.

Viewing the capture (recognizing a trigger condition and copying one register value to another register) as the claimed “digital function” is consistent with the claim language and specification, neither of which limit the “predetermined digital functions” to require a scope broader than the capture itself. *See* Pet. Reply 3–4 (citing Ex. 1001, 4:3–6). As Petitioner

notes, unchallenged dependent claims 4, 5, 11, 12, 18, and 19 recite particular functions, but are not at issue in this proceeding. Pet. Reply 4 n.1. Thus, we agree with Petitioner that PIC16 discloses that the CCP module performs the capture, compare, and PWM functions.

Patent Owner argues that PIC16's CCP module is not "configurable to perform" a digital function because the CCP module's functions require a properly configured timer, but the timer is neither part of the CCP module nor configured with the CCP module. PO Resp. 15–22. In particular, Patent Owner relies on PIC16's statement that "Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature." Ex. 1008, 72. Because a timer must be configured to run in a particular mode for each of the three CCP functions Petitioner relies on, Patent Owner argues that the CCP is not "configurable to perform" those functions because other components (the timers) must also be configured. PO Resp. 15–22. We do not agree. PIC16's timer modules are themselves separate modules described by the reference. Ex. 1008, 11 (depicting timer modules separately from CCP1 and CCP2); *accord* Ex. 1022, 79:23–80:1 (Patent Owner's expert agreeing). We agree with Petitioner that the timer modules provide an input for the CCP modules to use for their selected function, but do not perform the capture or compare functions themselves.³ See Pet. Reply 5–6. We further agree that PIC16's block diagrams

³ The question may be somewhat different for the CCP module's PWM function, in that it requires clearing the Timer2 module during each PWM period. See Ex. 1008, 74. We need not address Patent Owner's arguments directed to the PWM function, however, because the claim language requiring a plurality of predetermined digital functions is satisfied by the CCP module's capture and compare functions.

(Ex. 1008, Figures 10-2, 10-3, and 10-4) do not define the elements that perform the relevant function, but instead show the interactions between the CCP modules and other elements such as input pins and timer modules. *See* Pet. Reply 7–8.

In this regard, we agree with Petitioner that the claim language does not require that the programmable digital circuit block performs a particular function “by itself.” Pet. Reply 8–10; *see* PO Resp. 15 (“[I]t is undisputed that the CCP cannot perform any of those functions by itself.”). Figure 1 of the ’407 patent depicts a programmable digital circuit block with multiple inputs including “configurable inputs 20,” “cascade inputs 70,” “clock input 80, and “system input 90.” Ex. 1001, Fig. 1, 5:6–13.⁴ The specification does not support a programmable digital circuit block that must operate without inputs from other circuit elements. *E.g.*, Ex. 1001, 6:23–25 (“Moreover, the selectable logic circuits 30 realize any one of the variety of predetermined digital functions by using the data registers 40 to receive data, load data, capture data, etc.”). PIC16’s CCP module is no different—requiring a functioning timer input to the module does not mean that the module does not perform the capture or compare functions.

Patent Owner argues additionally that the CCP module is not configured with “a single register write operation,” in light of the configuration steps required to put non-CCP elements in their required states

⁴ Patent Owner contends that, *inter alia*, “input 20” and “data registers 40” are “within the PDCB” of Figure 1, which is therefore consistent with the programmable digital circuit block itself performing a function. PO Sur-Reply 5. Those elements, however, represent external interactions and support that the claimed circuit block need not perform a function without such interactions.

before the CCP module can perform the capture or compare functions.

PO Resp. 23–44. To that end, Patent Owner asserts PIC16 is silent on the “write sequence for configuring the capture or compare modes.”

PO Resp. 24. But Patent Owner’s expert agreed that skilled artisans would understand from “the PIC data sheet” how to set up the peripherals of the microcontroller described by PIC16, including the relevant CCP functions. Ex. 1022, 73:11–74:3, 92:8–21. Thus, we agree with Petitioner that PIC16 discloses configuring the capture and compare modes. *See* Pet. Reply 21.

Patent Owner’s argument regarding PIC16’s PWM mode frames the dispute about configuration. Patent Owner points to PIC16’s disclosure of “set-up for PWM operation,” which instructs that certain “steps should be taken when configuring the CCP module for PWM operation.”

PO Resp. 24–26 (quoting Ex. 1008, 75). That disclosure includes two steps particular to PWM mode—setting the PWM period and duty cycle. *Id.* at 25–26. Additionally, PIC16 discloses making the CCP1 pin an output by writing to the TRISC register, then configuring and starting Timer2 by writing to the T2CON register. Ex. 1008, 75 (*see* PO Resp. 26). For the capture and compare CCP modes, Patent Owner argues that one must write to the T1CON register to configure and start Timer1. PO Resp. 27–28.

Petitioner, on the other hand, submits that because the timer is not part of the CCP module (the claimed circuit block), whatever configuration the timer requires is not relevant to the claim language because the claim restricts only how the claimed circuit block be configured. Pet. Reply 13. Petitioner further points to the ’407 patent’s disclosure of setting PWM period and duty cycle through register write operations that are not part of the claimed “single register write operation.” *Id.* at 14–16 (citing Ex. 1001,

7:37–56 (describing multiple data registers used to configure PWM period and duty cycle), Fig. 5). When asked about the discrepancy, Patent Owner’s expert testified that although the ’407 patent shows separate registers for setting the PWM period and duty cycle (distinct from the configuration register to select a mode), “nothing in the patent says that [writing to additional registers] configures the logic to perform the PWM.” Ex. 1022, 85:2–19; *accord id.* at 81:18–19 (“[T]here’s nothing in the patent that says that that is part of the configuration.”) This testimony supports Petitioner’s contention that PIC16’s additional registers (beyond CCPxCON) are not relevant to the claim language, because they do not change the CCP module’s logic operation. *Cf.* Ex. 1022, 47:3–48:3 (testifying that a circuit block requiring multiple register writes would not be within the claims’ scope if those writes are required “to change the configuration of the logic from Figure 3 to Figure 4” of the ’407 patent).

Petitioner additionally points to the ’407 patent’s Provisional Application, which is incorporated by reference. Pet. Reply 16; *see* Ex. 1001, 1:4–13; Ex. 1021. As Petitioner describes, the Provisional Application’s disclosures are consistent with the ’407 patent’s specification in relevant part. *Compare* Ex. 1001, Fig. 3, *with* Ex. 1021, 65. The Provisional Application describes configuring a programmable digital circuit block using multiple register writes, only one of which selects the block’s function, while others establish parameters for operation. Pet. Reply 16–20 (citing Ex. 1021, 66, 113–114, 134; Ex. 1022, 136:25–137:22, 170:21–171:1). Petitioner separately notes that the Provisional Application distinguishes between “Personalization” and “Parameterization,” where the former refers to selecting a block’s function while the latter refers to

modifying operational details such as a timer's period. Pet. Reply 13 n.3 (citing Ex. 1021, 45, 46); *see* Ex. 1021, 25.

Patent Owner takes the position that the Provisional Application does not overcome claim language to the contrary. PO Sur-Reply 24–28. We agree with that principle, but the question is whether the claimed “single register write operation” restricts additional register writes beyond selecting the block's function. Alternatively phrased, the question is whether a block is “configurable to perform” a function when writing to a register that selects that function or instead only upon writing all parameters to all registers involved in that function. On this question, the Provisional Application supports Petitioner's view that selecting a block's function is distinct from establishing parameters involved in that function. Ex. 1021, 25, 64, 65.⁵ In that way, the Provisional Application is consistent with the '407 patent's figures, which show multiple data registers used to control the parameters (“parameterization”) involved in particular operational modes (“personalizations”). Ex. 1001, Figs. 3–6; Ex. 1022, 48:7–18 (recognizing that DR1 and DR2 are data registers).

⁵ Patent Owner contends that when the Provisional Application states that “not all DMFBs [(Digital Multi-Function Blocks)] may have this capability,” it is referring to using a “single register write . . . to change form a Timer to a PWM or to a CRC function.” PO Sur-Reply 25 (quoting Ex. 1021, 25); Tr. 40:17–26. We, however, agree with Petitioner that the more natural reading of that statement limits “the communication functions” that are included in certain, but not all, programmable blocks, rather than limiting the single-register-write configurability. *See* Tr. 44:16–45:19. Indeed, the '407 patent describes certain programmable digital circuit blocks (e.g., timers, counters, PWMs) that have their “digital communication functions . . . eliminated to further reduce [their] size.” Ex. 1001, 4:30–33.

As discussed above, we conclude that PIC16's timers are not part of the CCP module that Petitioner maps to the claimed programmable digital circuit block. *See supra* at 9–11. Accordingly, we agree with Petitioner that setting up a timer does not implicate the requirement for configuring the circuit block with a single register write operation. *See* Pet. Reply 12–13, 20–21; PO Resp. 28–33. We reach the same conclusion regarding PIC16's pin configuration, which sets up hardware pins to function as inputs or outputs. *See* Ex. 1008, 48. The patent discloses that configuration data includes “bits for configuring and selecting the configurable inputs 20 and the configurable outputs 10” but, significantly, those are inputs to and outputs from the block itself, not inputs and outputs of the digital device as a whole. Ex. 1001, 5:28–33, Fig. 1. We do not read the '407 patent as restricting how circuit elements outside the programmable digital circuit block must be configured. Thus, we do not agree with Patent Owner that configuring one of PIC16's pins (which are inputs/outputs to the microcontroller, not just the CCP module) as an input or output is part of configuring the CCP module itself to perform a selected function. *See* PO Resp. 33–38.

Patent Owner asserts that, in the CCP compare mode, establishing the register value to be compared against the timer input represents another required write operation that takes the CCP module outside the claim scope. PO Resp. 38–40. For the same reasons discussed, we do not agree. The compare registers provide information the CCP module uses to perform a comparison, but do change the CCP module's functionality. Accordingly, providing the CCPR1 registers with values does not configure the CCP module to perform a particular function.

Beyond writes to additional registers to provide parameters for CCP operation, Patent Owner argues that multiple write operations to the CCPxCON register are required for the CCP module to perform a function. PO Resp. 44–63. The argument takes two forms: that no single instruction can configure the CCP module; and that addressing the register requires multiple write operations.

Petitioner identifies three instructions that PIC16 discloses for writing to the CCPxCON registers in a single operation. Pet. 26–31. Two of those are BSF and COMF; BSF refers to “Bit Set f,” in which a bit in a designated register is set to a particular value.⁶ Ex. 1008, 150; Pet. 27–28. Petitioner submits that, after the microcontroller is first powered on (such that the CCPxCON registers are set to all zeros), using BSF to set bit 2 in the CCP1CON register “will cause the CCP1 module to perform the Capture function.” Pet. 29 (citing Ex. 1008, 72). *See ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018) (“[A] prior art reference may anticipate or render obvious an apparatus claim . . . if the reference discloses an apparatus that is reasonably capable of operating so as to meet the claim limitations, even if it does not meet the claim limitations in all modes of operation.”). Similarly, Petitioner submits that the instruction could be used instead to set bit 3 in the CCP1CON register, which “will cause the CCP1 module to perform the Compare function.” *Id.* (citing Ex. 1008, 72).

Petitioner further explains that a different instruction, COMF, refers to “Compliment f,” in which a register’s bits are complimented (i.e., inverted),

⁶ In light of our findings regarding the BSF and COMF instructions, we need not address the parties’ contentions regarding the MOVWF instruction. *See* Pet. 26–27; PO Resp. 49–53.

and may be stored back in the designated register. Pet. 29 (citing Ex. 1008, 153). Thus, using COMF to invert the CCPxCON register's values after a power-on reset, a single instruction would configure the CCP module to use PWM mode. *Id.* at 30–31; Ex. 1008, 72 (Figure 10-1 (showing that if CCPxCON bits 3–0 are set to 11xx, the module will use PWM mode)).

Patent Owner argues that “[b]ecause a BSF after a power-on-reset cannot configure PWM mode,” the CCP is not ““configurable to perform any one of’ capture, compare, or PWM mode” with a single register write operation. PO Resp. 46 (emphasis omitted). We do not agree, because nothing in the claim language requires the *same instruction* be used to configure the claimed programmable digital circuit block. Rather, it requires that only one operation be used to select the circuit block's function from at least two possible functions. Because the BSF instruction uses a single write operation to set a bit in the CCPxCON register that can select either the capture or compare function, the claim language is satisfied. Moreover, even if Petitioner had to show that the CCP module must be configurable to function in any of the three modes with a single operation, Petitioner has done so. That the PWM mode is selected using a different instruction (COMF) than the capture or compare modes (BSF) does not take PIC16's disclosures outside the challenged claims.

Patent Owner submits that even a single operation used to set one or more bits in the CCPxCON register actually requires more than a single register write operation because PIC16's register addressing requires first writing to PIC16's STATUS register (to select the memory bank for directly addressing the CCPxCON register). PO Resp. 53–63. Petitioner submits that because the STATUS register does not configure the CCP module, it is not

relevant to a register write operation that configures the module. Pet. Reply 24. We need not determine the persuasiveness of that argument, however, because we agree with Petitioner’s second argument—that the STATUS register’s memory-bank selection bits default to zero with power-on reset, and therefore are already correctly configured to address the CCPxCON register. *Id.* at 24–25; *see ParkerVision*, 903 F.3d at 1361. Patent Owner’s expert agreed that “after a power-on reset bank 0 will be selected.” Ex. 1022, 113:5–21. Thus, a single operation would then directly address the CCPxCON register with no change to the STATUS register. Pet. Reply 24–25; Ex. 2009, 282:23–283:20 (Petitioner’s expert testifying that addressing bank 0 requires no change to the STATUS register after power up, and that CCPxCON is addressed with bank 0). Although Patent Owner points to an example in AN594 using the CCP’s PWM mode, where bank 0 is selected in the STATUS register after power-on reset, that example does not contradict the default behavior supported by both experts’ testimony. *See* PO Sur-Reply 22–23 (citing Ex. 1009, 9, 15); *see also* Ex. 1009, 2 (“Appendix A is a program which generates up to a 10-bit PWM output.”). Setting bits to the value they are expected to have already does not mean such an operation was required.

Finally, Patent Owner argues that the CCPxCON register does not “configure” the CCP module, but instead controls its operation once configured. PO Resp. 64–73. According to Patent Owner, because the same bits in CCPxCON both set the CCP module for capture mode and also select a prescaler setting, and because PIC16’s block diagram shows those bits being provided to the prescaler element (Ex. 1008, 72 (Fig. 10-2)), PIC16’s disclosures indicate that there are no bits in CCPxCON to set a particular

mode. PO Resp. 64–67; *accord id.* at 67–73 (making similar arguments for compare and PWM modes). We do not agree that because the CCPxCON register’s bits may both select an operational mode and also configure certain aspects of that mode, the register fails to configure the CCP module as claimed. For the reasons discussed, we find that, through the CCPxCON register, the CCP module is configurable with a single register write operation to perform at least capture or compare operations.

Accordingly, having reviewed the parties’ contentions and the evidence presented, we find that Petitioner has shown by a preponderance of the evidence that claim 1 is anticipated by PIC16.

2. Claims 7 and 14

Claim 7 depends from claim 1 and is reproduced below:

7. The programmable digital device as recited in claim 1 wherein said programmable digital circuit block further comprises:
 - a configuration register for receiving and storing a plurality of configuration data corresponding to any of said plurality of predetermined digital functions, and
 - a plurality of selectable logic circuits which perform any of said plurality of predetermined digital functions, wherein said predetermined digital functions determine size and arrangement of said selectable logic circuits.

Ex. 1001, 8:62–9:4. Claim 14 depends from claim 8 and recites the same additional limitations as claim 7. *Id.* at 9:33–10:4.

Petitioner asserts that PIC16 discloses the first additional limitation of claims 7 and 14 because the CCPxCON registers store configuration data as bits, including bits 3 and 2, which determine the function for each CCP module. Pet. 38. Petitioner asserts that PIC16 discloses the second additional

limitation because the CCP module includes logic circuits including “a prescaler, an edge detect circuit, comparators, output logic, and flip-flops.” *Id.* at 39 (citing Ex. 1008, 72–74). Petitioner continues that the predetermined digital functions determine the size and arrangement of the logic circuits because “different logical circuits are selected and arranged in a particular way depending on the selected function.” *Id.* (citing Ex. 1008, 72–74).

Patent Owner argues that the CCPxCON registers are not part of the CCP modules, because the registers are implemented as static RAM, which PIC16 shows as a separate block. PO Resp. 77–79 (citing Ex. 1008, 11 (Fig. 3-2)). Patent Owner relies on the ’407 patent’s depiction of “configuration registers 50” as part of Figure 1’s “programmable digital circuit block” to contrast with PIC16’s disclosure of a separate RAM block. *Id.* at 77.

Petitioner contends that the ’407 patent does not require a physical relationship between the claimed configuration register and the programmable digital circuit block, instead requiring only a logical relationship. Pet. Reply 28–29 (citing Ex. 1022, 120:2–8); *accord id.* (citing Ex. 1022, 40:13–25) (arguing the ’407 patent does not require a particular physical layout). Petitioner relies on testimony from Patent Owner’s expert. *Id.* at 28–29. The expert was asked whether “Claim 7 require[s] a particular physical configuration of the logic that is a programmable digital circuit block” and responded that, in his opinion, it does not. Ex. 1022, 120:2–8. In Petitioner’s view, that supports that the claim requires a logical and not physical relationship between the programmable digital circuit block and the configuration register. Pet. Reply 28–29. Patent Owner views the testimony

differently, arguing that Patent Owner’s expert actually “rejected the premise” that Petitioner seeks (a logical rather than physical relationship imposed by the claim). PO Sur-Reply 29 (citing Ex. 1022, 120:2–8). We agree with Patent Owner, in that its expert testified that claim 7 does not require “a particular physical configuration” of logic, but does require that “whatever is identified as the digital circuit block includes a configuration register.” Ex. 1022, 120:2–8.

The dispute regarding claim 7 fundamentally turns on claim construction. We read the plain language of a “programmable digital circuit block” as using “block” to suggest circuitry considered as a unit. Ex. 1001, 8:35–39. While a “block” of circuitry could apply to a logical block, as under Petitioner’s view, the specification counsels in favor of considering the block as a physical structure.

The specification describes configuration of “programmable digital circuit blocks . . . by changing the contents of a few registers *therein*,” suggesting that a block’s configuration registers are located physically within the block. Ex. 1001, 2:4–7 (emphasis added). Further, it describes how certain design approaches can “minimize the size of the programmable digital circuit block.” *Id.* at 2:9–13; *accord id.* at 4:15–16 (“[T]he programmable digital circuit block 100 is highly efficient in terms of die area.”), 4:26–34 (describing an embodiment with limited functionality “to further reduce the size of the programmable digital circuit block 100”). By referencing size, the specification directly implicates that a block is a physical circuit unit.

Further, while Figures 3–9 each depict a “block diagram” that does not represent a physical implementation, Figure 1 is not a block diagram and

instead “illustrates a programmable digital circuit block.” Ex. 1022, 40:10–25 (Patent Owner’s expert agreeing that Figure 3 does not show an implementation of physical logic); Ex. 1001, Fig 1, 2:55–3:18. Figure 1 shows that configuration registers are within the circuit block, consistent with a physical relationship imposed by claim 7’s language directed to a programmable digital circuit block that comprises a configuration register. *Id.*, Fig. 1; PO Resp. 77.

Thus, based on the claim language and the specification, we construe the “digital programmable circuit block” to be a physical structure such that a block comprising a configuration register must include the register within the block’s boundaries.

PIC16’s configuration registers, the CCPxCON, are implemented in the RAM File Registers. Ex. 1008, 11 (Fig. 3-2), 21 (Fig. 4-5), 23 (“These [special function] registers are implemented as static RAM.”); Ex. 2009, 307:16–20 (Petitioner’s expert agreeing). Petitioner has not provided evidence or argued that PIC16’s CCPxCON registers would satisfy Patent Owner’s view of claim 7 requiring a physical relationship between the programmable digital circuit block and its configuration register. *See* Pet. 38; Pet. Reply 28–29.

We have reviewed the parties’ contentions and the evidence presented and conclude that Petitioner has not shown by a preponderance of the evidence that claim 7 or 14 is anticipated by PIC16.

3. Additional claims

For claims 3, 8, 10, 15, and 17, Petitioner provides contentions showing how PIC16 teaches each of the recited elements. Pet. 35–50. Other than as addressed above regarding claims 1, 7, and 14, Patent Owner does

not challenge Petitioner’s contentions regarding PIC16’s disclosures with respect to claims 3, 8, 10, 15, or 17. *See* PO Resp. 11–79. We determine Patent Owner has waived any such argument regarding these claims. *See* Paper 12, 8 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”); *In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016); Consolidated Trial Practice Guide 52 (Nov. 2019). We have reviewed the parties’ contentions and the evidence presented and conclude that Petitioner has shown by a preponderance of the evidence that each of claims 3, 8, 10, 15, and 17 is anticipated by PIC16.

D. OBVIOUSNESS OVER PIC16C7X DATASHEET AND AN594

Claim 2 depends from claim 1 and further requires that the “programmable digital circuit block is configurable into a serial arrangement.” Ex. 1001, 8:40–42. Claims 9 and 16 depend from claims 8 and 15, respectively, and recite similar limitations. *Id.* at 9:11–13, 10:16–18. Petitioner relies on AN594 to disclose the additional limitations.

AN594 is an application note published by the same entity as PIC16 and “discusses the operation of a Capture/Compare/PWM(CCP) module, and the interaction of multiple CCP modules with the timer resources.” Ex. 1009, 1. AN594 discusses that, “[w]hen two or more CCP modules exist on a device, there can be an interaction between the CCP modules.” *Id.* at 5. AN594 includes example programs for each mode of operation, and “[t]he software example for the Capture mode, also uses a second CCP module in Compare mode to generate the signal to capture.” *Id.* at 1. Petitioner relies on that example as teaching the claimed serial arrangement. Pet. 52–53. Petitioner asserts skilled artisans had reason to follow AN594’s exemplary configuration because PIC16 “expressly instructs the reader to refer to the

AN594 Application Note for further information.” *Id.* at 51 (citing Ex. 1008, 71 (“For use of the CCP modules, refer to the Embedded Control Handbook, ‘*Using the CCP Modules*’ (AN594).”)).

Patent Owner relies on secondary considerations of non-obviousness to support the patentability of claims 2, 9, and 16. Specifically, Patent Owner argues that these claims are patentable over the asserted art because the ’407 patent’s claimed invention “solved a long-felt need . . . for a configurable computer architecture without the programming overhead and inefficiency of an FPGA.” PO Resp. 80–83. Patent Owner asserts benefits of the ’407 patent’s approach, citing exclusively to the specification.⁷ *Id.* Patent Owner then concludes that “[t]hese benefits, which were not provided in the prior art, support the nonobviousness of the claimed invention.” *Id.* at 83 (citing Ex. 2008 ¶ 198 (Patent Owner’s expert, repeating the same statement without additional support)).

As discussed above, we agree with Petitioner that PIC16 discloses configuration of a programmable digital circuit block using a single register write operation. *See supra* at 6–19. PIC16 therefore solved the need that Patent Owner asserts, prior to invention of the ’407 patent.⁸

⁷ Patent Owner’s expert repeats Patent Owner’s claims, but provides no additional support. Ex. 2008 ¶¶ 194–197.

⁸ Even if we had not concluded that Patent Owner’s asserted need was already met before the challenged patent, Patent Owner has not identified objective evidence to support its view. Citations to the challenged patent’s specification do not offer a reliable basis on which to conclude that the claims were nonobvious, and Patent Owner’s declarant provides no additional evidence to support his statements. *See* Ex. 2008 ¶¶ 194–197; 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

We have considered Patent Owner's assertions regarding objective indicia of nonobviousness, together with Petitioner's submissions regarding PIC16 and AN594, and conclude that the subject matter of claims 2, 9, and 16 would have been obvious over PIC16 and AN594 for the reasons given by Petitioner.

III. CONCLUSION⁹

For the reasons discussed, we conclude:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 3, 7, 8, 10, 14, 15, 17	102	PIC16C7X Datasheet	1, 3, 8, 10, 15, 17	7, 14
2, 9, 16	103	PIC16C7X Datasheet, AN594	2, 9, 16	
Overall Outcome			1–3, 8–10, 15–17	7, 14

IV. ORDER

It is

ORDERED that Petitioner has proven that claims 1–3, 8–10, and 15–17 of the '407 patent are unpatentable;

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that Petitioner has not proven that claim 7 or 14 of the '407 patent is unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For PETITIONER:

Eagle H. Robinson
Daniel S. Leventhal
Richard S. Zembek
Daniel Prati
NORTON ROSE FULBRIGHT US LLP
eagle.robinson@nortonrosefulbright.com
daniel.leventhal@nortonrosefulbright.com
richard.zembek@nortonrosefulbright.com
dan.prati@nortonrosefulbright.com

For PATENT OWNER:

Theodoros Konstantakopoulos
Yung-Hoon Ha
Ryan G. Thorne
DESMARAIS LLP
tkonstantakopoulos@desmaraisllp.com
yha@desmaraisllp.com
rthorne@desmaraisllp.com