

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

IPR2020-01561
Patent 7,719,452 B2

Before JEFFREY S. SMITH, SCOTT A. DANIELS, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

DANIELS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background*

On September 1, 2020, Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively, “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–4, 8, 9, 12–16, 19, and 20 of U.S. Patent No. 7,719,452 B2, issued on May 18, 2010 (Ex. 1001, “the ’452 patent”). Paper 1 (“Pet.”). Analog Devices, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

Following our Institution Decision (Paper 10, “Inst. Dec.”), Patent Owner filed a Response. Paper 13 (“PO Resp.”). Petitioner filed a Reply. Paper 19 (“Reply”). Patent Owner filed a Sur-Reply. Paper 20 (“PO Sur-Reply”). A hearing was held on December 9, 2021. A transcript of the hearing has been entered as Paper 26 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claims 1–4, 8, 9, 12–16, 19 and 20 are unpatentable.

B. *Additional Proceedings*

The parties indicate that the ’452 patent has been asserted against Petitioner in *Analog Devices, Inc. v. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd.*, Case No. 1:19-cv-02225 in the United States District Court for the District of Delaware. Pet. 97; Paper 5, 2. Patent Owner also states that “Petitioner[] filed petitions for *Inter Partes* Review of U.S. Patent No. 10,250,250 (Case No. IPR2020-01210), U.S. Patent No. 8,487,659 (Case No. IPR2020-01219), U.S. Patent No. 7,012,463 (Case No. IPR2020-01336), U.S. Patent No. 7,286,075 (Case No. IPR2020-01559), and U.S. Patent No. 6,900,750 (Case Nos. IPR2020-01483, IPR2020-01484, and IPR2020-01564), which are also at issue in the above litigation.” Paper 5, 2.

C. Real Parties in Interest

The Petition identifies Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. as Real Parties in Interest. Pet. 97. Patent Owner identifies itself as the Real Party in Interest. Paper 5, 2.

D. The '452 Patent (Ex. 1001)

The '452 patent describes analog to digital converter (ADC) systems that convert analog signals to digital signals. Ex. 1001, 1:10–12. More specifically, the '452 describes a “pipelined” or “cascade” signal converter that uses lower resolution converter stages to achieve higher signal resolution at greater sampling speeds. *Id.* at 1:12–16. The '452 patent explains that

[e]ach stage of a pipelined system quantizes that stage's input signal to a predetermined number of digital bits and forms an analog output signal which is presented to a succeeding stage for further signal processing.

Id. at 1:16–19. Figure 1 of the '452 patent, reproduced below, illustrates an embodiment of such a pipelined ADC system.

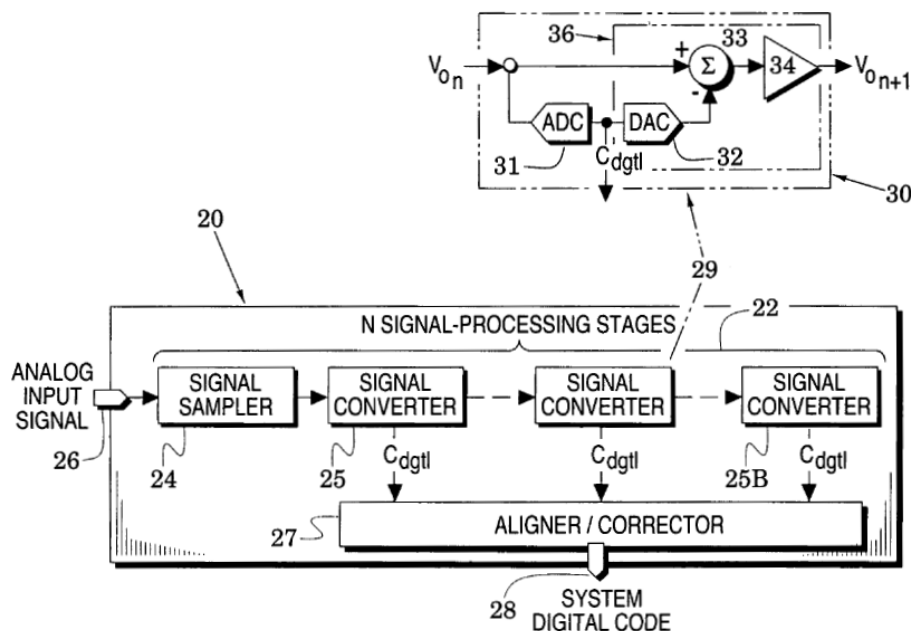


FIG. 1

Figure 1 of the '452 patent, reproduced above, illustrates a block-diagram of a pipelined ADC system including analog input signal 26, signal sampler 24, N signal processing stages 25[N], alignor/corrector 27 and system digital code output 28. A circuit diagram, Figure 2, reproduced below, illustrates an exemplary signal converter circuit structure according to the '452 patent. *Id.* at 3:32–34.

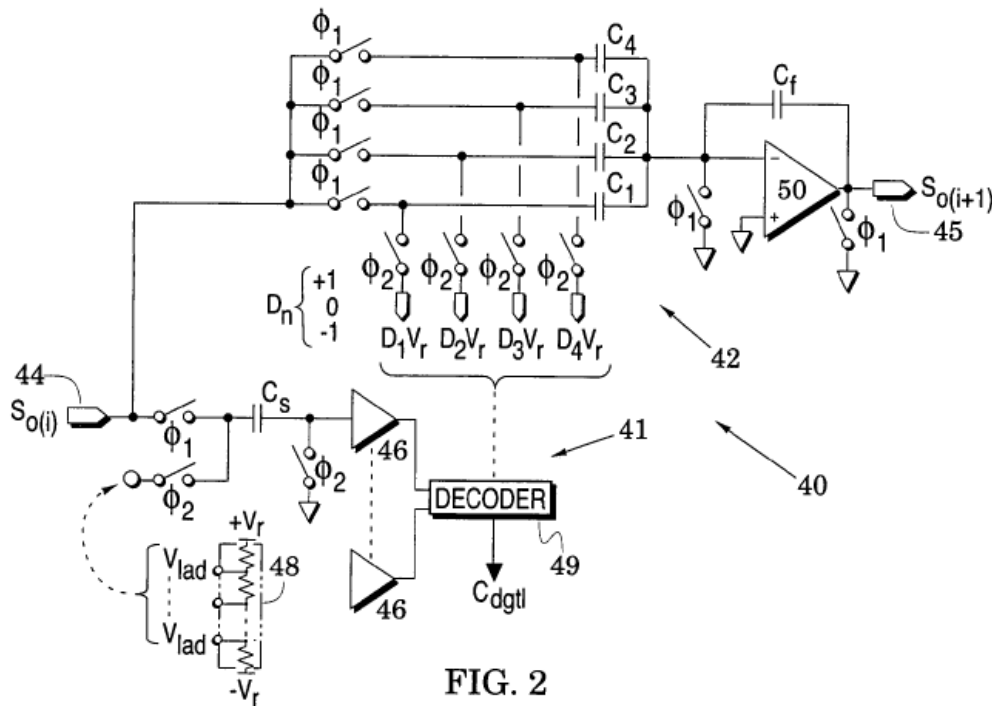


Figure 2 of the '452 patent, above, shows an embodiment of signal converter 40 including a multiplying digital-to-analog converter 42 (MDAC) and switched-capacitor signal comparator 41. *Id.* at 3:40–42.

The '452 patent further describes a problem with such systems where “converter nonlinearity” between the stages of a pipelined signal converter “can significantly degrade the conversion of low-level dynamic signals.” *Id.* at 1:25–26. A goal of the ADC system described in the '452 patent is to provide “pipelined converter systems with enhanced linearity.” *Id.* at 1:51–

52. The '452 patent explains that better linearity addresses the problem where

the signal converter **40** of FIG. 2 will introduce undesirable symmetrical INL [integral nonlinearity] errors (e.g., as exemplified by segments **74** of the INL **70**) into the transfer function of the converter system **20** of FIG. 1. Although these symmetrical transfer function errors have been described above to originate from incorrect feedback capacitor C_f size and insufficient amplifier gain, they can also originate from other system errors (e.g., signal setting errors).

Id. at 5:49–56. To account for these, and other such errors, the '452 patent describes the addition of pseudo-random (PN) generator 81, and also PN generator 85, to system 20, as illustrated in Figure 6 reproduced below.

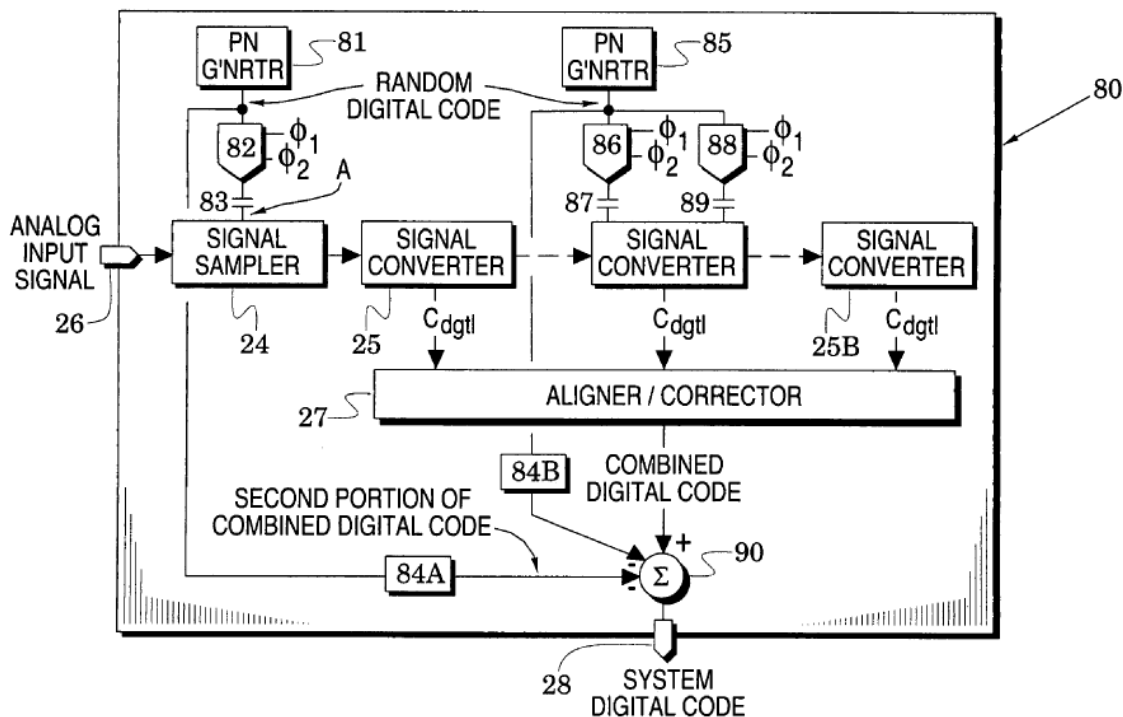


FIG. 6

Figure 6 of the '452 patent, above, shows PN generator 81, digital analog converter (DAC) 82, and dither capacitor 83 for injecting analog dither

signals into signal sampler 24. According to the '452 patent, the analog dither signals and analog input to signal sampler 24 are combined and

the combined signal is processed down randomly-selected signal-processing paths of the converter system which induce different magnitudes and signs of INL errors. The average error of these processing paths is reduced to thereby provide significant improvements in system linearity . . . these linearity improvements are realized by simultaneous processing of two combined analog signals-the input signal at the input port 26 and the injected dither signal.

Id. at 6:17–26. The '452 patent explains further that

[a]s shown in FIG. 6, this processing provides a combined digital code at the output of the aligner/corrector 27. A first portion of this combined digital code at the digital back-end of the signal converter corresponds to the analog input signal that was earlier received into the input port 26 but a second portion of the combined digital code corresponds to the injected analog dither signal. In the converter system 80, the final system digital code at the output port 28 is realized by subtracting out the second portion in a differencer 90.

Id. at 6:26–35.

The '452 patent also describes that a similar ADC signal resolution process can occur for downstream signal converter 25, also shown in Figure 6, having PN generator 85, DAC 86, 88, and respective dither capacitors 87, 89 providing analog dither signals for combination with the input analog signal. *Id.* at 6:44–67.

E. Illustrative Claim

Of the challenged claims, claims 1 and 13 are independent. Each of dependent claims 2–4, 8, 9, and 12 depend from claim 1, and claims 14–16, 19, and 20 depend from claim 13. Claim 1 illustrates the claimed subject matter and is reproduced below with certain limitations of interest highlighted in italics (bracketed limitation numbering added):

1. [1A] An analog-to-digital converter system to convert an analog input signal to a system digital code, comprising:

[1B] a sampler to provide samples of said analog input signal;

[1C] signal converters arranged and configured to successively process said samples;

[1D] at least one digital-to-analog converter configured to respond to a random digital code *and inject analog dither signals into at least a selected one of said sampler and said signal converters* which process said samples and said analog dither signals into a plurality of digital codes;

[1E] an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals; and

[1F] a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code;

[1G] *said samples thus processed along different signal-processing paths of said signal converters to thereby enhance linearity of said system.*

Ex. 1001, 15:63–16:18 (emphasis added).

F. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include: (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. *Env'tl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.

Id. Moreover, these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

In determining a level of ordinary skill, we also may look to the prior art, which may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Additionally, the Supreme Court informs us that “[a] person of ordinary skill is also a person of ordinary creativity, not an automaton.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421.

Petitioner, supported by the testimony of Dr. Holberg, proposes that a person of ordinary skill in the art (“POSITA”):

would have at least a Master’s Degree in Electrical Engineering or equivalent field, including studies in the area of analog circuitry, or at least a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuitry design.

Pet. 16–17 (citing Ex. 1002 ¶¶ 16–19).

Patent Owner’s declarant, Dr. Moon states that Petitioner’s asserted level of ordinary skill in the art is “reasonable.” Ex 2002 ¶ 13.

Petitioner’s proposed level of ordinary skill in the art is consistent with our review and understanding of the technology and descriptions in the ’452 patent and the prior art references that disclose electronic circuits including pipelined analog-to-digital converters and discussion of the nonlinearity problems due to offset, gain, and aperture mismatches in analog to digital signal conversion. And, because the parties generally agree, we apply Petitioner’s proposed level of ordinary skill in the art.

G. Claim Construction

We interpret claims in the same manner used in a civil action under 35 U.S.C. § 282(b) “including construing the claim in accordance with the

ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. §42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2020)).¹ Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner relies on the opinion testimony of Dr. Douglas R. Holberg (Ex. 1002). Patent Owner’s arguments are supported by the testimony of Dr. Un-Ku Moon (Ex. 2002).

“said signal converters”

Claim limitations 1[B]–[D] and [G] recite:

[1B] a sampler to provide samples of said analog input signal;

[1C] signal converters arranged and configured to successively process said samples;

[1D] at least one digital-to-analog converter configured to respond to a random digital code and inject analog dither signals into *at least a selected one of said sampler and said signal converters* which process said samples and said analog dither signals into a plurality of digital codes

...

[1G] said samples thus processed along different signal-processing paths of *said signal converters* to thereby enhance linearity of said system.

¹ This rule change applies to the instant Petition because it was filed after November 13, 2018. See *id.*

Ex. 1001, 15:65–16:6.

We determined in our Institution Decision that claim 1 “only requires that samples be processed along different signal-processing paths of *at least one* stage of the pipelined converter.” Inst. Dec. 24. In this Decision, based on the parties’ arguments and evidence, and for the reasons explained below, we clarify our claim construction.

Patent Owner argues that claim 1[C] “recites that the conversion is performed by a series of ‘signal converters’ arranged and configured to ‘successively process’ samples of the analog input signal into a ‘plurality of digital codes.’” PO Resp. 25. Patent Owner argues that each of the signal converters is “a different **stage** in the pipelined converter system.” *Id.* at 26 (citing Ex. 1001, 1:10–19, 2:48–57, Fig. 1; Ex. 2002 ¶ 54). Patent Owner then asserts for claim 1[D] “that dither is injected into the sampler or the signal converters.” *Id.* In this way, Patent Owner argues for claim limitation 1[G] that “the injected dither propagates through **all** of the stages, causing the samples to be processed along different signal-processing paths of all of the converter stages.” *Id.* at 26–27.

Patent Owner contends that the Specification of the ’452 patent supports their construction. PO Resp. 29–34. Patent Owner argues specifically that as shown by comparing Figures 7A and 7B, the ’452 patent confirms that, compared to known systems, the novelty of the claims lies in “propagation of dither through **all** stages of the converter system.” *Id.* at 31 (citing Ex. 1001, 8:53–56, 10:65–67, 11:59–65, 14:5–9, 39–55). Figure 7A illustrates one embodiment where only some of the signal converters, i.e., stages 1 and 2, process the respective combined signal (101–102) at different operating points, while Figure 7B illustrates another embodiment where all

stages 1–5 processes the combined signal (101–105) at different operating points. *Id.*

Patent Owner also relies on Dr. Moon’s testimony that “in the context of the patent specification and claims, the phrase ‘said signal converters’ in limitations [1G] and [13F] . . . refers back to the multiple ‘signal converters arranged and configured to successively process samples’ in limitation [1C] and [13B].” *Id.* at 36–36 (citing Ex. 2002 ¶ 54). Dr. Moon surmises that

a POSITA would have understood the reference to “said signal converters” in limitations [1C] and [13B] to refer to all the signal converters in an ADC pipeline, because each of them generates a different digital code reflecting a different portion of the input analog signal. Using fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.

Ex. 2002 ¶ 55.

In sum, the argument presented by Patent Owner is that independent claims 1 and 13 recite, structurally, a plurality, or multiple “signal converters,” and therefore functionally require, “that the input samples be processed along different signal-processing paths in *each* of the *multiple* stages of the converter system.” *Id.* at 25.

We agree that “said signal converters” in claim 1[G] is plural and the antecedent basis is found in the recitation of “signal converters” in claim limitation 1[C]. Ex. 1001, 15:66–16:17. What we are not persuaded by is Patent Owner’s arguments and evidence that limitation 1[G] should be read as “*all* said signal converters.”

As an initial matter, on its face, claim 1[G] does not recite “all,” or “each of” said signal converters. Given a plain reading of the claim, we are not apprised that the language, on its face, limits the claim to processing the combined input and dither sample “along different signal-processing paths

of [all] *said signal converters*.” We acknowledge that there is proper antecedent basis in the claim 1[C] for “said signal converters,” but Patent Owner has not explained persuasively how merely having successive pipelined signal converters extends to the functional requirement of signal samples being “processed along different signal-processing paths of [all] said signal converters.” Indeed, as Patent Owner points out, the Specification explains that “[i]n a feature of the present disclosure, however, dither points propagate through the converter stages and cover a substantial portion of ***each converter subrange as shown in FIG. 7B***.” PO Resp. 20–21 (citing Ex. 1001, 14:39–52; Ex. 2002 ¶ 50). Because this feature, or embodiment, of the invention was clearly discussed in the Specification of the ’452 patent, it would have been an elementary matter for the claim to have been similarly drafted to specify this limitation, e.g., by writing the limitation as “*all* said signal converters,” or alternatively “*each of* said signal converters.” This, however, is not the case.

The Specification of the ’452 patent provides a description of the figures, including:

FIG. 6 is a diagram of a converter system embodiment of the present disclosure;

FIG. 7A illustrate transfer functions of signal-processing stages in the system of FIG. 6 and possible dither levels in these stages;

FIG. 7B is similar to FIG. 7A and illustrates preferred dither levels;

Ex. 1001, 2:1–7. Thus, in the disclosed embodiment of Figure 6, the converter system embodiment can provide “possible dither levels” as shown in Figure 7A, or “preferred dither levels,” as shown in Figure 7B. Figures 7A and 7B are reproduced below.

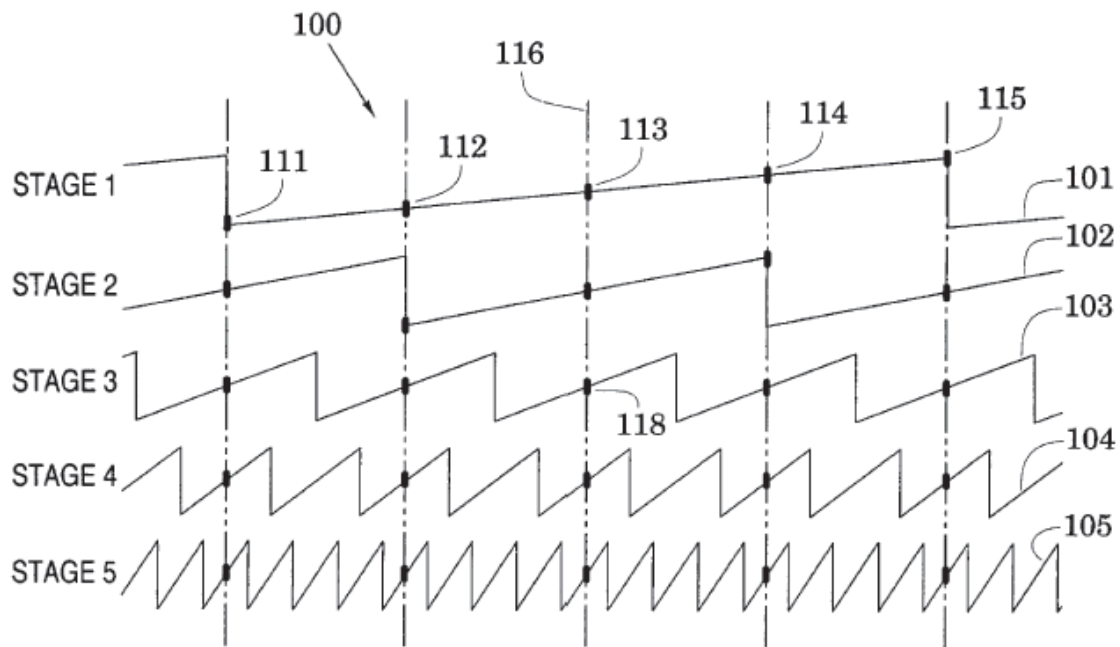


FIG. 7A

Figure 7A, above, illustrates one embodiment of the converter system in Figure 6 where stages 1 and 2 process the respective combined signal (101–102) at different operating points. But, in each of stages 3–5, the signal is processed at the same operating points. *See id.* at 7:52–56 (The written description explaining that “the operating point in subsequent stages 3-5 remains at the operating point prior to application of dither.”).

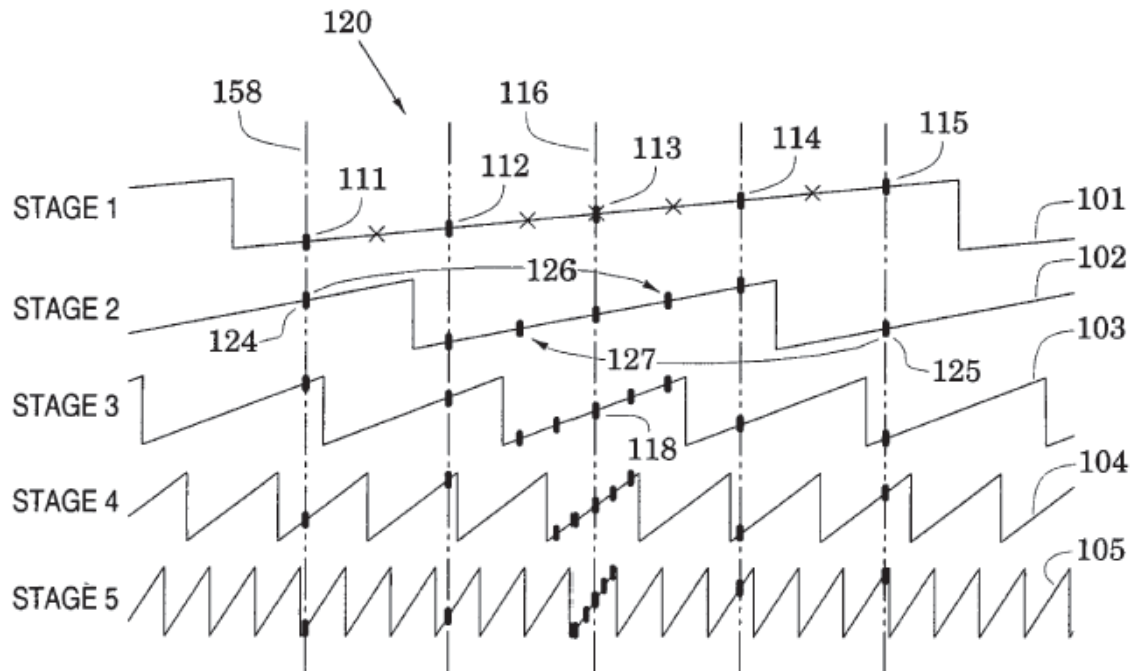


FIG. 7B

Figure 7B, above, illustrates, compared to Figure 7A, a preferred result of the converter system illustrated in Figure 6 where each stage 1–5 processes the combined signal (101–105) at different operating points. Patent Owner asserts that the difference between Figures 7A and 7B illustrates the problem of “dither exhaustion.” PO Resp. 10.

Because both Figures 7A and 7B are embodiments of the signal converting structure shown in Figure 6, we appreciate that Figure 7B shows a preferable result where the processing of the input signal along more stages having different signal processing paths helps improve the system linearity and achieve a more accurate signal conversion result. Yet we do not read the Specification and the embodiments of Figures 6, 7A, and 7B as being such disparate embodiments that they cannot be covered by the claim language or, that the comparison is somehow a disavowal of claim scope. We acknowledge that the Specification discusses the embodiment of Figure

7B, having more processing paths, being the most preferred. *See, e.g., id.* at 10:65–67 (“The different operating points in FIG. 7B illustrate the processing advantages of dither structure embodiments of the present disclosure.”). We would agree that Figure 7A is mainly described as a less preferred embodiment of the converter system shown in Figure 6 where “dither exhaustion” may occur. Yet, the ’452 patent does not describe Figure 7A as representative of the prior art or distinguish it in a way other than to be less preferred than Figure 7B. Overall, the Specification mainly describes that the embodiment of Figure 7B is preferred over that of Figure 7A, and does not specify any persuasive description or statements limiting “signal converters” to meaning “*all* signal converters” in the context of processing the combined input and dither sample “along different signal-processing paths of *said signal converters*,” as recited in claim 1. We also do not find a disavowal of the embodiment in Figure 7A because disavowal of claim scope generally requires an express disavowal or disclaimer. *See Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1306 (Fed. Cir. 2011) (The Federal Circuit explaining that “[t]o disavow claim scope, the specification must contain ‘expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.’”) (quoting *Epistar Corp. v. Int’l Trade Comm’n*, 566 F.3d 1321, 1335 (Fed. Cir. 2009)).

Patent Owner further contends that during prosecution of the application which became the ’452 patent “[i]n the Notice of Allowance, the Examiner specifically referred to the ‘different signal-processing paths in said signal converters’ limitation as being one of the novel features in the claims.” PO Resp. 24 (citing Ex. 1003, 165–166). The Examiner’s reasons for allowance stated that “prior art considered individual or combination

does not teach an analog-to-digital converter system comprising,” and then essentially copied claim limitations 1[E]–[G], and similarly claim limitations 13[E]–[G], as the noted reasons for allowance. Ex. 1003, 165–166. The Examiner’s reasons for allowance did not indicate in any express way that “said signal converters” was interpreted as “[all] said signal converters,” or “[each of] said signal converter.” *Id.*

Dr. Moon’s testimony does not persuasively support Patent Owner’s construction because it mainly reiterates what we understand from a plain reading of the ’452 patent, that “[u]sing fewer than all the digital codes output by all the signal converters would result in digital output of the converter that does not correctly reflect the input analog signal.” Ex. 2002 ¶ 55. In other words, the more signal converters that operate over different operating points, the better. Overall, Dr. Moon’s testimony is consistent with our understanding from reading the Specification, that the embodiment of Figure 7B is better and preferred because it would result in a more accurate signal conversion than the Figure 7A embodiment. In our view, even considering the issue of “dither exhaustion” which is not expressly recited in the ’452 patent, Patent Owner has not pointed to persuasive evidence either in the claims, Specification, prosecution history, or Dr. Moon’s testimony as to why a person of ordinary skill in the art would read the claim language as excluding the embodiment in Figure 7A or, that the ’452 patent expressly disavows embodiments which alter the signal processing paths in less than all the signal converters.

We find that Patent Owner’s construction depends improperly on reading limitations, namely that dither propagates through *all* the converter stages, from the Specification into the claims. *See* PO Resp. 31, *see also Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014)

(The Federal Circuit explaining that “[w]hile we read claims in view of the specification, of which they are a part, we do not read limitations from the embodiments in the specification into the claims.”). Accordingly, we alter our claim construction from our Institution Decision, and determine that for limitations 1[G] and 13[F], “said samples thus processed along different signal-processing paths of *said signal converters* to thereby enhance linearity of said system,” is not limited to, or properly interpreted as, processing samples along “*all* said signal converters” in the claimed analog-to-digital converter systems.

H. Grounds Asserted

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 8, 9, 13–16	103(a)	Cesura ²
12, 19, 20	103(a)	Cesura, Lewis, ³ and Bjornsen ⁴
1–4, 8, 9, 13–16	103(a)	Fu ⁵ and Lewis
12, 19, 20	103(a)	Fu, Lewis, and Bjornsen

II. ANALYSIS

A. Legal Standards of Obviousness

Section 103(a) forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such

² Ex. 1004, US Patent No. 6,970,125 B2 (Nov. 29, 2005).

³ Ex. 1006, Stephen H. Lewis and Paul R. Gray, “A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter,” *IEEE Journal of Solid State Circuits*, Vol. SC-22, No. 6, Dec. 1987.

⁴ Ex. 1007, US Patent No. 7,129,874 B2 (Oct. 31, 2006).

⁵ Ex. 1005, Daihong Fu et al., “A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters,” *IEEE Journal of Solid State Circuits*, Vol. 33, No. 12, Dec. 1998.

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR*, 550 U.S. at 406.

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, objective evidence such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); see *KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”). The Court in *Graham* explained that these factual inquiries promote “uniformity and definiteness,” for “[w]hat is obvious is not a question upon which there is likely to be uniformity of thought in every given factual context.” *Graham*, 383 U.S. at 18.

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. To reach this conclusion, however, it is not enough to show merely that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.” *Id.*

A claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why one of skill in the art would have modified the prior art to obtain the claimed invention. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1307 (Fed. Cir. 2006). And, as a factfinder, we also must be aware “of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.” *KSR*, 550 U.S. at 421. This does not deny us, however, “recourse to common sense” or to that which the prior art teaches. *Id.*

B. Obviousness over Cesura, claims 1, 2, 8, 9, 13–16

Petitioner argues that claims 1, 2, 8, 9, and 13–16 of the ’452 patent would have been obvious over Cesura. As discussed below, and having reviewed the full record now before us, including the relevant portions of the supporting testimony of Dr. Holberg and Dr. Moon we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Cesura.

1. Overview of Cesura (Ex. 1012)

Cesura discloses a pipelined ADC system shown for example in Figure 1, reproduced below, labeled “Prior Art,” where ADC system 100 includes pipelined converter stages 105₃–105₀ for successively processing the sampled analog signal IN. Ex. 1004, 2:61–67.

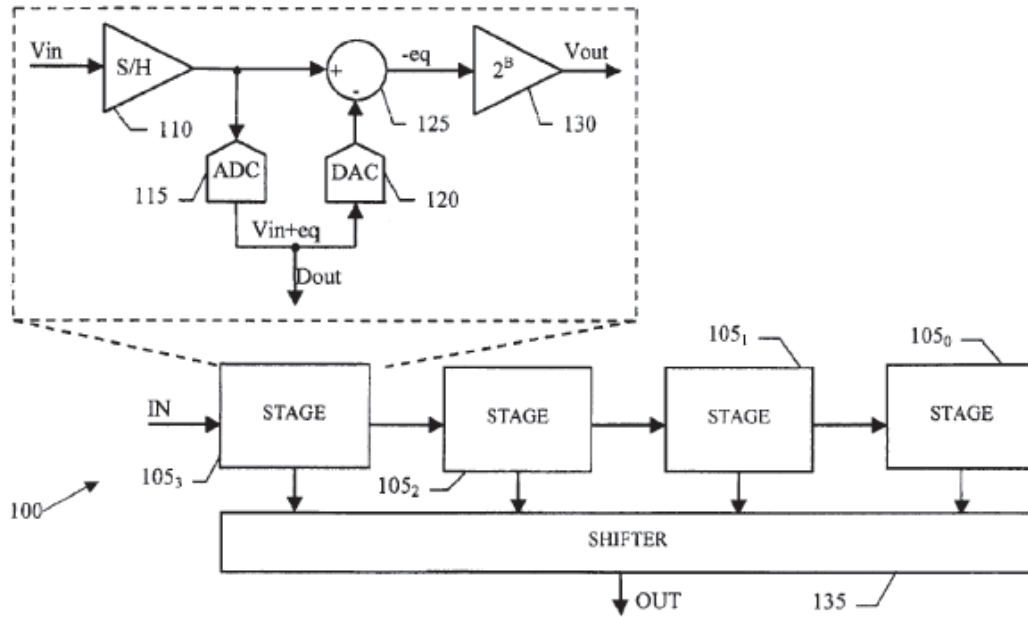


FIG. 1
(Prior Art)

Cesura's Figure 1, above, schematically illustrates a pipeline ADC system including that converter stages 105₃–105₀ determine respective analog outputs Dout that are combined and processed by shifter 135 into digital output signal OUT. *Id.*

Figure 2 of Cesura, reproduced below, reveals a schematic of an embodiment of an ADC converter.

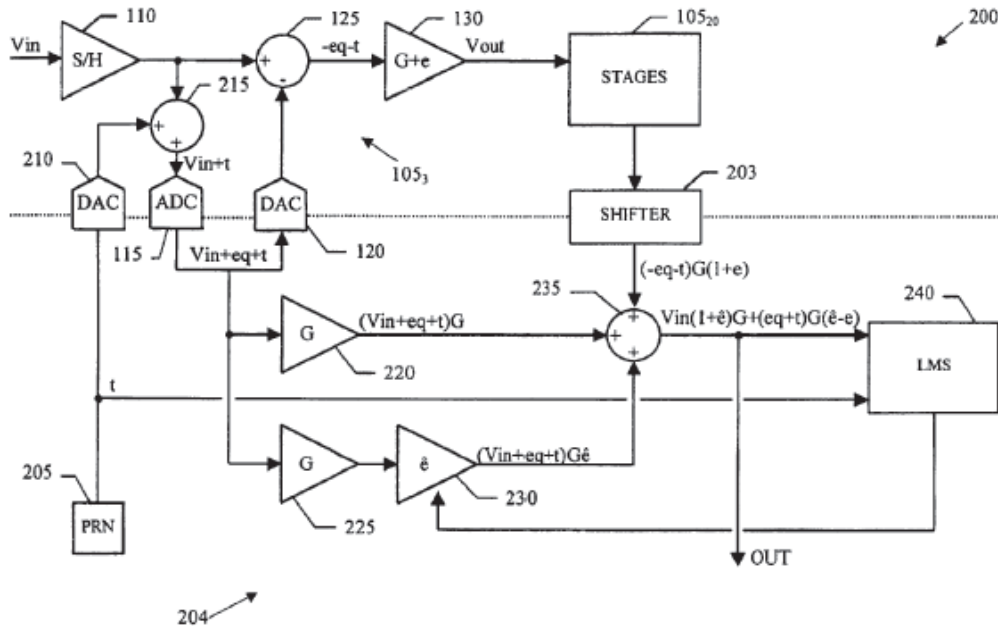


FIG. 2

Cesura's Figure 2, above, illustrates an embodiment of pipelined ADC converter 200 including pseudo-random noise (PRN) generator 205 that provides via DAC 210, a test analog signal t that is combined in adder 215 with analog input signal V_{in} , from sampler 110. *Id.* at 4:8–14. Adder 215 thus provides through amplifier 130 analog V_{out} that is a combination of test analog PRN signal t and the sampled analog V_{in} input signal. *Id.* at 4:12–18.

In the embodiment of Figure 2, stages 105₂₀ produce digital output signals and shifter 203 combines these digital output signals into a combined digital output signal that is sent to adder 235. *Id.* at 4:23–33. Cesura states that “[t]he digital signal $V_{in}(1+e)G+(eq+t)G(e-e)$ from the adder 235 represents the digital output signal OUT of the whole converter 200.” *Id.* at 4:55–57. In conjunction with adder 235, logic module 240 receives the digital test signal directly from PN generator 25 and Cesura states that “the additive term (including the digital test signal t) due to the analog error e of the amplifier 130 providing the inter-stage gain is deleted.” *Id.* at 4:59–61. Cesura explains that “[t]he solution of the invention substantially reduces the

distortion (in the digital signal generated by the converter) caused by the analog error in the inter-stage gain.” *Id.* at 6:30–33.

2. *Independent Claims 1 and 13*

Considering elements [1A]-[1G] of claim 1, as reproduced above, and independent claim 13, we address below the respective arguments of both parties as to claim 1.

a) *Petitioner’s Arguments*

(1) *Preamble [1A]*

Petitioner argues that to the extent the preamble is limiting, “Cesura discloses in Figure 2, [] a pipelined analog-to-digital converter 200 that converts analog input signal ‘Vin’ [] into a corresponding digital output code ‘OUT.’” Pet. 17 (citing Ex. 1002 ¶¶ 92–93).

(2) *Limitation [1B]*

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura’s ADC system 200 includes “sample/hold (S/H) amplifier 110” that samples the input signal Vin and provides the sampled signal to flash ADC 115. Pet. 18 (citing Ex. 1002 ¶ 94).

(3) *Limitation [1C]*

With respect to “signal converters arranged and configured to successively process said samples,” Petitioner argues that Cesura’s signal converters 105₃–105₀ are arranged and configured to successively process the sample input signal. Pet. 18. Dr. Holberg testifies that this is demonstrated “by the input signal ‘IN’ also shown as the signal ‘Vin’ . . . being fed to a first signal converter stage 105₃, the output of which is fed to signal converter stage 105₂, the output of which is fed to signal converter stage 105₁, etc.” Ex. 1002 ¶ 95 (citing Ex. 1004, Fig. 1, 2:60–3:45). According to Dr. Holberg, “[i]n Figure 2 of Cesura . . . the first signal converter stage 105₃

is illustrated in detail with its constituent components, whereas the remaining signal converter stages 105_2 , 105_1 , and 105_0 are illustrated collectively by the box ‘STAGES’ 105_{20} .” *Id.* (citing Ex. 1004, Fig. 2, 3:46–4:32).

(4) Limitation [1D]

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura’s DAC 210 responds to a random digital code generated by pseudo random noise generator 205 to generate analog dither signals. Pet. 20 (citing Ex. 1002 ¶¶ 96–97). Petitioner argues that the analog dither signals from DAC 210 are injected into the first signal converter stage 105_3 , as functionally illustrated by being summed with the analog input signal V_{in} at the input node of flash ADC 115 in stage 105_3 . *Id.* (citing Ex. 1002 ¶¶ 96–97). Petitioner additionally argues Cesura discloses that the “resulting analog signal $V_{in}+t$ is applied to the ADC 115, so as to be converted into a corresponding digital signal $V_{in}+eq+t$ (wherein eq is the residue introduced by the quantization error of the ADC 115),” and, thus, signal converter stage 105_3 processes the samples and the analog dither signals into a plurality of digital codes. *Id.* at 21 (citing Ex. 1002 ¶ 98). According to Petitioner, because the stages $105_3 - 105_0$ are connected consecutively in a pipeline, the successive stages $105_2 - 105_0$ will likewise process the samples and analog dither signals. *Id.* (citing Ex. 1002 ¶ 98).

(5) Limitation [1E]

Petitioner argues that Cesura’s shifter 203, amplifier 220, and adder 235 collectively teach an aligner/corrector as claimed. Pet. 22–24 (citing Ex. 1002 ¶¶ 99–100). Petitioner additionally argues that, to the extent Cesura’s elements 203/220/235 do not expressly provide an “aligner/corrector” function, it would have been obvious to do so, at least in

part, because “shifter 135 (**orange**) provides an aligner/corrector function by correcting for differing amounts of inter-stage gain at the respective signal converter stages 1053, 1052, 1051, *etc.* (that feeds through to the respective digital codes output from the respective stages). *Id.* at 24 (citing Ex. 1002 ¶ 101).

(6) Limitation [1F]

Petitioner argues that Cesura discloses a decoder comprising amplifier 225, amplifier 230, and LMS logic module 240. Pet. 26 (citing Ex. 1002 ¶ 103). As argued by Petitioner, amplifier 225 receives as its input the signal $V_{in} + eq + t$, applies a gain G thereto, and outputs the amplified signal to amplifier 230, which applies a gain of $\hat{e}$ to the signal. *Id.* (citing Ex. 1002 ¶ 103). Thus, according to Petitioner, amplifiers 225/230 apply a transfer function of $G\hat{e}$ to the $V_{in} - eq + t$ digital signal, including the recited “second portion,” t , that is the random digital code. *Id.* (citing Ex. 1002 ¶ 103). Petitioner further argues that the output of amplifiers 225/230 is applied to adder 235, which “differences” the signals coming from the amplifiers 225/230 with the combined digital code coming collectively from shifter 203 and amplifier 220. *Id.* at 27 (citing Ex. 1002 ¶ 104). According to Petitioner, Cesura’s logic module 240 “calculates the digital correction signal $\hat{e}$ that approximates the digital representation of the analog error e minimizing their difference according to a Least Mean Square Algorithm (LMS)” to ensure that $\hat{e} = e$. *Id.* at 28 (citing Ex. 1002 ¶ 105).

(7) Limitation [1G]

Relying on Dr. Holberg’s testimony, Petitioner argues that Cesura discloses injecting analog dither signals t into the ADC 115 along with the analog input signal V_{in} . Pet. 28 (citing Ex. 1002 ¶ 106). Dr. Holberg testifies that Cesura’s analog dither signals cause at least one, and

undoubtedly the first and second stages of its pipeline ADC to operate at different operating points, depending on the value of the dither signal at any given moment. Ex. 1002 ¶ 106 (citing Ex. 1004, Fig. 2, 4:8–33); Ex. 2003, 85:9–86:25. Dr. Holberg further testifies that each operating point in the respective stages represents a signal processing path, and thus, the samples processed by the ADC are processed along a different signal-processing path depending on the value of the dither signal. *Id.* ¶ 106 (citing Ex. 1004, Fig. 2, 4:8–33). Thus, according to Dr. Holberg, Cesura discloses that, as a result of dithering, the samples are processed along different signal-processing paths of said signal converters. *Id.*

(8) Independent Claim 13

Claim 13 differs from claim 1 mainly by eliminating the limitation of “a sampler” as recited in claim [1B], and thus claim [13C] recites, “inject[ing] corresponding analog dither signals into at least a selected one of said signal converters.” Ex. 1001, 17:10–12. The parties acknowledge the main difference “being that in claim [1D] dither can be injected into either the sampler or one of the signal converters.” Pet. 36 (citing Ex. 1002 ¶¶ 120–121); *see also* PO Resp. 41 (Patent Owner confirming that “[c]laim 13 has different phrasing, stating that the dither is injected into one of the converters.”).

b) Patent Owner’s Arguments

Patent Owner’s arguments are premised mainly on their incorrect claim construction that claims 1 and 13 require “dither injected into **one** of the ADC’s sampler or pipelined stages would propagate through **all** of the downstream stages of the pipelined converter system.” PO Resp. 1–2. Patent Owner argues that “[n]either the Petition nor the art itself contains any discussion of whether the cited art’s purported ‘dither signals’ cause the

input samples to be processed along different signal-processing paths in *all* stages of a pipelined converter system.” *Id.* at 2.

As discussed above in our claim construction analysis, Patent Owner applies a name for the problem alleged to be solved by the ’452 patent, that is—“dither exhaustion.” *Id.* at 10 (citing Ex. 2002 ¶ 30). Patent Owner argues specifically that “[t]he ’452 inventors demonstrate the problem addressed by the patent—dither exhaustion—in Figures 7A and B of the patent.” *Id.* Patent Owner provides the annotated Figure 10 from the ’452 patent, reproduced below, to illustrate “dither exhaustion.”

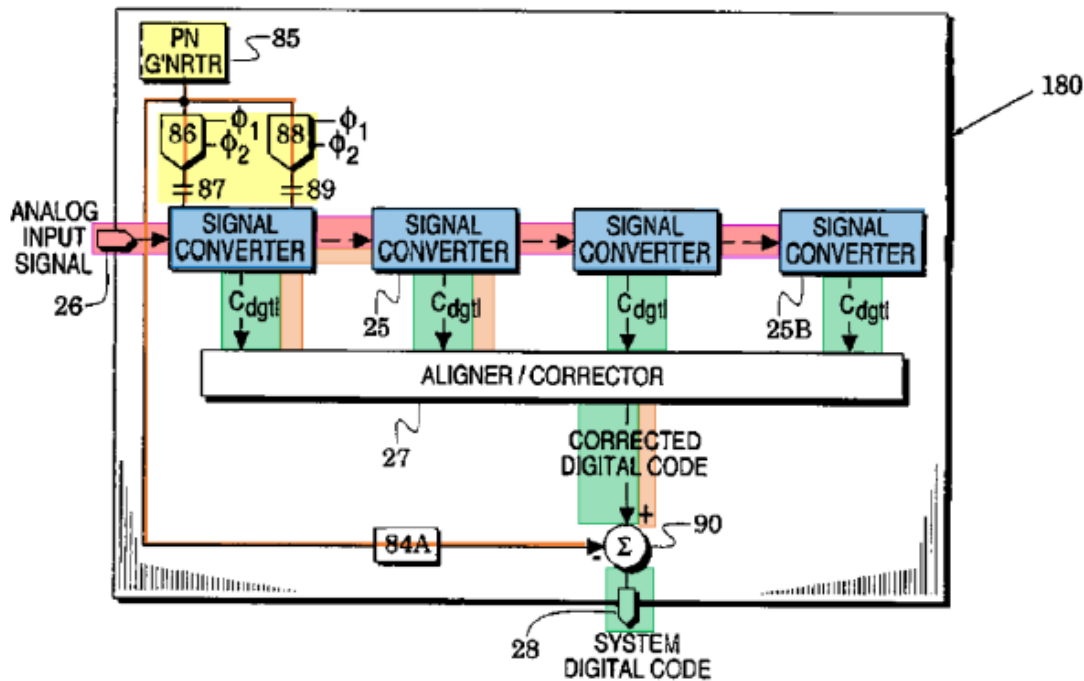


Figure 10 of the ’452 patent, as annotated by Patent Owner, illustrates a pipelined converter system with PN generator 85 adding a dither signal into the first signal converter via DACs 86, 88. *Id.* at 12. Patent Owner argues that “in this example, the dither is exhausted by the third converter stage (and for all

subsequent converter stages), and from the perspective of these stages, it is as though dither was never injected into any stage of the pipeline.”⁶ *Id.* (citing Ex. 2002 ¶ 32).

Similar to its arguments with respect to claim construction, Patent Owner argues that Figure 7A, reproduced below as annotated by Patent Owner, illustrates the problem of dither exhaustion. *Id.* at 16.

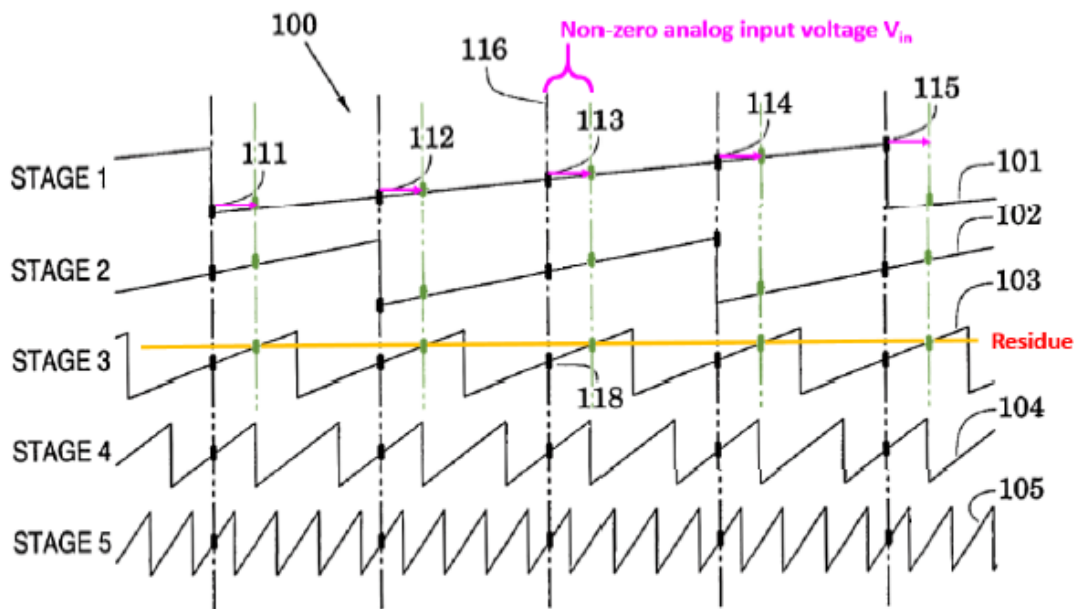


FIG. 7A

Figure 7A, as annotated by Patent Owner, illustrates one embodiment of the converter system in Figure 6 where stages 1 and 2 process the respective combined signal (101–102) at different operating points. *Id.* Patent Owner contends that Figure 7A “shows that the residue value in converter stage 3 is the same regardless of the dither level injected into stage 1, which indicates that the dither has been exhausted.” Ex. 2002 ¶ 43.

⁶ Patent Owner’s brief includes color-coded wording coordinated with the colors in the drawings. We do not reproduce the color-coded wording in this Decision.

Patent Owner argues that the problem of dither exhaustion is solved by the claimed invention and is illustrated by annotated Figure 7B reproduced below.

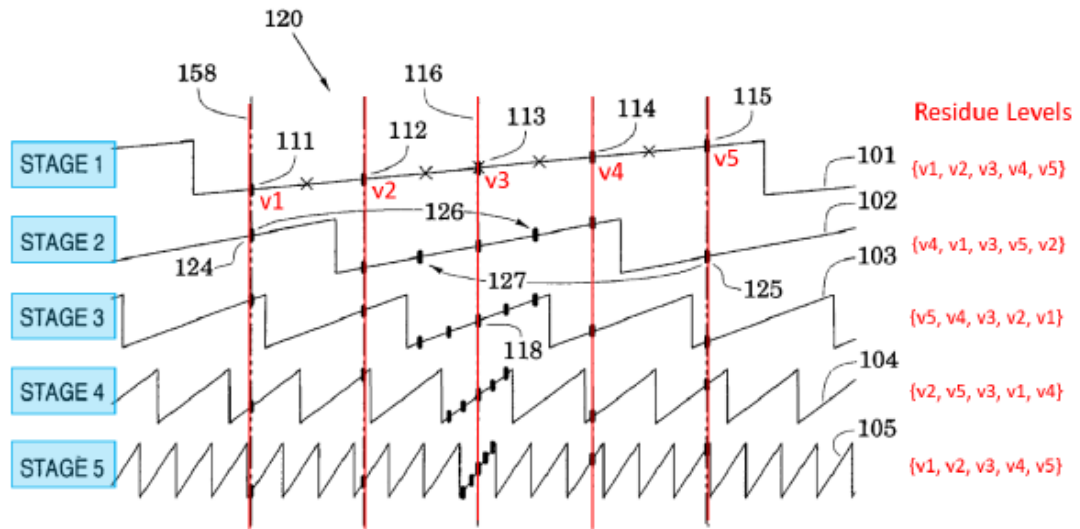


FIG. 7B

Figure 7B, above, illustrates, compared to Figure 7A, a preferred result where each stage 1–5 processes the combined signal (101–105) at different operating points. PO Resp. 17. Patent Owner argues that “Figure 7B depicts the operation of the claimed pipelined converter in which *all* of the pipelined stages receive the randomizing, error-averaging benefits of dither.” *Id.* at 16.

In addition to the “dither exhaustion” and intertwined claim construction arguments noted here, Patent Owner makes additional arguments with respect to Cesura as it pertains to independent claims 1 and 13 which we address in our analysis below.

c) Analysis

With respect to claim limitations [1A]–[1C] and [1E], we have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that Petitioner sufficiently establishes that Cesura

discloses these limitations. Patent Owner's arguments mainly pertain to limitations [1D], [1F], and [1G], which we address below.

It is very helpful in our analysis to understand *why*, according to the '452 patent, a better or more preferred result is obtained in Figure 7B.

The '452 patent explains that for Figure 7A

[i]t is further assumed that the PN generator **81**, DAC **82** and at least one capacitor **83** are configured to dither this operating point over five operating points **111**, **112**, **113**, **114** and **115** (in FIG. **SA**, each operating point is indicated by an oblong marker) wherein operating points **111** and **115** coincide with the ends of the converter subrange.

Ex. 1001, 7:23–29. Thus, according to the '452 patent, the five dithered operating points 111–115 shown in Figure 7A, “coincide with the ends of the converter subrange,” i.e., at the lowest and highest sawtooth points (111, 115), in stage 1, and therefore span the output-signal window. *Id.*

Configuring PN generator 81, DAC 82 and capacitor 83, in this way results, apparently, in “the dither fail[ing] to alter the signal processing path through these latter stages.” *Id.* at 7:56–57.

To resolve this problem, the '452 patent describes that in Figure 7B “the five dithered operating points are now arranged so that they span substantially 4/5 of the output signal window, i.e., the span between operating points 111 and 115 is substantially 4/5 of the output-signal window.” *Id.* at 7:64–66. Observing Figure 7B, the operating points in stage 1 are now configured to *not* coincide with the lowest and highest sawtooth, and therefore span the 4/5 of the output signal window. The '452 patent sums this up by explaining that it is beneficial to select

a predetermined dither range which sufficiently differs from the output-signal window of the selected stage so that, in each of

succeeding stages, the respective dither range covers a substantial portion of the respective output-signal window

Ex. 1001, 8:55–59.

Considering these examples and the written description and figures of the '452 patent, we agree with Patent Owner's statement that "[a]s the inventors observed, the use of such specific configurations of dither signals could ensure that an injected dither signal would propagate to each converter stage in the pipeline." PO Resp. 20 (citing Ex. 1001, 14:39–52). However, notably, neither of the independent claims 1 or 13 include any limitations relating to a dither range covering any portion of the output-signal window.

In any event, as discussed above, the proper claim construction for limitation 1[G] is not limited to processing samples along "*all* said signal converters" in the claimed analog-to-digital converter system. Therefore, we disagree with Patent Owner's overall conclusion that "[b]oth independent claims capture this invention." *Id.* at 21.

Turning to Cesura, Patent Owner argues that "Cesura contains no mention of a digital-to-analog converter (DAC) configured to inject dither signals in a manner that ensures *all* pipeline stages of the ADC benefit from the randomizing effect of the dither signal (i.e., that the dither does not exhaust after some stages of processing)." PO Resp. 36–37. The proper claim construction, however, does not require "*all* pipeline stages of the ADC benefit from the randomizing effect of the dither signal," as Patent Owner argues. *Id.* at 37.

Besides reiterating that Patent Owner's claim construction is erroneous, Petitioner replies that Dr. Holberg's testimony unmistakably explains, both in his original declaration and subsequently under cross-examination, that Cesura discloses successive stages 105₂–105₀ processing

the input signal samples and dither injected into Cesura's first stage 105₃.

Dr. Holberg's testifies in his original declaration that

signal converter stage 105₃ "process[es] said analog samples and said analog dither signals into a plurality of digital codes" as recited by this claim element. Because the stages 105₃ - 105₀ are connected consecutively in a pipeline (the output of one stage feeding the next stage), the successive stages 105₂ - 105₀ will likewise process the samples and analog dither signals into respective digital codes.

Ex. 1002 ¶ 98. During Dr. Holberg's deposition, Patent Owner's counsel asked whether Cesura's Figure 2 showed processing of the combined input signal residue and dither signal by the successive stages 105₂ - 105₀:

Q: So in Figure 2, Stages 105/20 represent Stages 105/2, 105/1, and 105/0, shown in the prior art Figure 1, correct?

A: Correct.

Q: And so Figure 2 does not represent an embodiment where the correction circuitry is applied to Stages 105/2, 105/1, or 105/0, correct?

A: [T]his figure doesn't.

Ex. 2003, 83:1–9. Although agreeing that Cesura's Figure 2 did not show processing by the successive stages 105₂ - 105₀, Dr. Holberg explained with more clarity why Cesura, as a whole, does disclose that the successive stages 105₂ - 105₀, in addition to the initial stage 105₃, also process the combined input sample $V_{in} + t$ (where t is the added dither signal):

Q. Did you do any analysis of whether Stages 105/2, 105/1, and 105/0 process their analog input signals down different paths based on test signal t ?

...

A. Well, claim 1G of '452 says, "samples thus processed along different signal-processing paths of signal

converters to thereby enhance linearity of said system.” So I said, “Cesura discloses injecting an analog to the signal t into the ADC 115 along with the analog input signal. Cesura’s analog dither signals will cause at least one stage of the pipeline to operate at different points depending on the value of the dither signal in any given moment . . . [“] So, I mean, I said here that at least one of the stages. But, you know, sitting here today, you know, looking at it, you know, in a different light, based upon your question, it appears that Cesura, as I read in the passage, you know, he says that you can apply the tests over one or more stages. And the output of the first stage has the -- has the test signal embedded in it, which is something I really didn’t think about before. But that signal is patched onto the subsequent stages as well.

Id. at 85:9– 86:25.

In this line of questioning by Patent Owner’s counsel, Dr. Holberg was consistent, explaining that because the output of the first stage 105₃ included dither signal t output to second stage 105₂, then the dither signal would indeed be applied to multiple stages:

Q. So I’m talking about an embodiment in which test signal t is inserted only into Stage 105/3. Okay? In that embodiment, would Stage 105/1 process a signal down different paths based on test signal t ?

. . .

A: Well, given -- it might, given that the output V_{out} is G plus e times the quantity negative e_q minus t . So V_{out} has t in it, and that’s going to the subsequent stages.

Id. at 88:8–18. Dr. Holberg was clear in his deposition that although Figure 2, which is a circuit diagram, does not show specific processing being carried out by subsequent stages, a person of ordinary skill in the art would understand that this is undoubtedly occurring:

Q. And today you have no idea whether the output of Stage 105/2 includes a component based on t , do you?

A. That's not described in this figure. But a POSITA looking at it would -- and reading that paragraph that I just read that the algorithm could apply to one or more stages, that maybe it does.

Id. at 89:4–11.

Patent Owner's declarant, Dr. Moon, testifies that "Cesura . . . says nothing about processing an injected random signal in **any** succeeding stage of an ADC, much less a DAC configured to inject a dither signal that is processed by **all** the succeeding stages." Ex. 2002 ¶ 64. We appreciate that Cesura discusses mainly that dither signal t is added via PRN generator 205 and DAC 210 to initial stage 105₃, however, we find Dr. Holberg's testimony on this point more persuasive, specifically that in Cesura "the output voltage of one stage is the input voltage of the next stage. We can't dispute that. And [] that output voltage has a t in it." Ex. 2003, 90:22–24. Indeed, we have no persuasive testimony from Dr. Moon that the combined input and test dither signal *would not* be processed by subsequent stages. For example, Dr. Moon testifies that "Cesura does not teach or suggest that its test signals propagate to downstream stages 105₁ and 105₀, and provides no reason to believe that they would." Ex. 2002 ¶ 67. Dr. Moon essentially repeats Patent Owner's "dither exhaustion" argument, yet conspicuously does not include stage 105₂, which immediately follows the initial stage 105₃ in Cesura's pipelined converter. Ex. 1004, Fig. 1. This is, in effect, consistent with Dr. Holberg's testimony that the output of initial stage 105₃ includes the test signal and thus a person of ordinary skill in the art would have understood that it is also the input signal to be processed by subsequent stage 105₂.

We are persuaded by the arguments and evidence of record that a person of ordinary skill in the art would have understood that Cesura's test signal *t* is applied to multiple stages of the signal converter system.

Besides the issue of claim construction and the interpretation of Cesura's disclosure, Patent Owner makes several other arguments with respect to Cesura. First, that "Cesura does not teach or suggest processing dither through all the signal converters in an ADC system." PO Resp. 40–44. Second, Patent Owner argue that "Cesura does not teach or suggest 'said samples thus processed along different signal-processing paths of said signal converters'" as recited in independent claim 1G and 13F. *Id.* at 44–46. Third, Patent Owner argues that "Cesura does not teach or suggest 'an aligner/corrector . . . to process said plurality of digital codes into a combined digital code'" as recited in claims 1E and 13D. *Id.* at 46–48. Fourth, Patent Owner argues that "Cesura does not teach or suggest 'a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code'" as recited in claim limitations 1F and 13E. *Id.* at 48–57. We address these arguments in turn.

(1) Whether Cesura teaches processing dither through all the signal converters in an ADC system

The issue of whether or not Cesura teaches processing dither through all the signal converters in an ADC system is based on Patent Owner's erroneous claim construction. *Id.* at 41. As discussed above, the claim language does not require that dither is processed through "*all* said signal converters," and we are persuaded that a person of ordinary skill in the art would have understood that Cesura teaches processing combined input and dither samples through multiple signal converters in an ADC system.

(2) *Whether Cesura teaches “said samples thus processed along different signal-processing paths of said signal converters”*

This argument is also based on Patent Owner’s erroneous claim construction, that independent claims 1 and 13 “be construed to require that the input samples be processed along different signal-processing paths in **each** of the **multiple** stages of the converter system.” *Id.* at 44. For the same reasons as discussed above, we do not find this argument persuasive.

(3) *Whether Cesura teaches “an aligner/corrector . . . to process said plurality of digital codes into a combined digital code”*

Patent Owner argues that Petitioner has failed to show that Cesura’s elements shifter 203, multiplier 220, and adder 235, correspond to an aligner/corrector as recited in independent claims 1 and 13. *Id.* at 46. The reason Patent Owner contends is that “in Figure 2 of Cesura adder 235 combines **three** inputs, not **two**, to create an output signal OUT that is represented by the expression ‘ $V_{in}(1 + \hat{e})G + (eq + t)G(\hat{e} - e)$ ’. **Nowhere** does Cesura describe forming the combined digital code alleged by the Petition.” *Id.* at 46–47.

The Petition explains that Cesura’s shifter 203 is coupled to multiple converter stages 105₂₀, and processes the digital code which has two terms, the first term corresponding to the input signal samples, and the second term corresponding to the analog dither signals. Pet. 22 (citing Ex.1002 ¶ 99). According to Petitioner, amplifier 220 processes a digital code from the first signal converter 105₃, this code also including a first term corresponding to the input samples, and a second term corresponding to the analog dither signals. *Id.* at 23. Dr. Holberg testifies that

Adder 235 combines the digital code from amplifier 220 with digital codes from shifter 203 together to form a combined digital code, namely $[(-eq-t)G(l+e)] + [(V_{in} + eq + t)G] = [(GV_{in} - G(e)(eq)) - G(e)(t)]$, that includes a first portion, $(GV_{in} - G(e)(eq))$, corresponding to said samples and a second portion, $-G(e)(t)$, corresponding to said analog dither signals.

Ex. 1002 ¶ 100 (citing Ex. 1004, 3:46–4:32, Fig. 2).

The '452 patent describes that “aligner/corrector 27” receives the digital codes from all the signal converter stages and “only after the aligner/corrector 27 has received the digital codes C_{dgtl} from all of the signal converters 25, does it provide a system digital code at an output port 28 that corresponds to the original sample.” Ex. 1001, 3:6–10. Similarly, we understand from a plain reading of claim 1 that the claimed aligner/corrector “process[es] said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals.” *Id.* at 16:8–11. The claim language does not recite any limitations as to specifically *how* the process of a combined digital code is carried out, what order the signals are added to provide the output digital code, or that the output digital code is limited to only two inputs. Therefore, we find that a person of ordinary skill in the art would have understood that Cesura teaches an aligner/corrector as claimed, and Patent Owner’s explanation, evidence and arguments are unpersuasive.

(4) Whether Cesura teaches “a decoder having a transfer function configured to convert said random digital code to said second portion”

Patent Owner explains that “a decoder converts the initial random digital code used to generate the injected analog dither signal into a ‘second portion,’ which is then subtracted from the combined digital code to derive the final ‘system digital code’ corresponding to the analog sample.” PO

Resp. 48. But, According to Patent Owner, “nothing in Cesura corresponds to a decoder that applies a transfer function to ‘t’ to generate the claimed ‘second portion’ or differences that ‘second portion’ from a ‘combined digital code.’” *Id.* at 50.

In the Petition, Petitioner explained that in Cesura’s Figure 2 amplifiers 225 and 230 together apply a transfer function $G\hat{e}$ to input $V_{in}+e_q+t$, including the dither signal t , resulting in $(V_{in}+e_q+t)G\hat{e}$. Pet. 26 (citing Ex. 1002 ¶ 103). Dr. Holberg testifies persuasively that

Figure 2 also illustrates that the output of amplifiers 225/230 is applied to adder 235, which “differences” the signals coming from the amplifiers 225/230 with the combined digital code coming, collectively, from shifter 203 and amplifier 220 . . . it is self-evident that the summing of the “t” component (from the amplifiers 225/230) and the “-t” component (from the shifter 203) is equivalent to the difference in the magnitudes of the respective “t” components.

Ex. 1002 ¶ 104.

Patent Owner argues that different from the claimed invention “Cesura requires that the ADC output (the OUT signal) **contain** a component corresponding to the test signal so that LMS module 240 may correlate the test signal with the ADC output to drive the estimation of ‘ $\hat{e}$ ’”. PO Resp. 49. In other words, Patent Owner argues that test signal t has not been removed from the Cesura’s output signal, because to do so would eliminate feedback to amplifier 230 as shown in Cesura’s Figure 2.

Petitioner responds in two ways, first, pointing out that contrary to Patent Owner’s assertion Cesura explicitly states that

[i]n the ideal condition wherein $e=e$, the digital output signal OUT is then equal to $V_{in}(1+e)G$. In this way, the additive term (including the digital test signal t) due to the analog error e of the amplifier **130** providing the inter-stage gain *is deleted*; therefore,

the harmonic distortion caused by the imprecision of the inter-stage gain is eliminated, or at least substantially reduced.

Reply 11 (citing Ex. 1004, 4:57–63) (emphasis added). Second, to the extent that the ideal condition does not exist and the test signal is not deleted, Petitioner points out persuasively that the claims do not recite that the dither must be deleted or “removed.” *See id.* (Petitioner arguing that the independent claims “only recite ‘differencing’ the second portion (which corresponds to the dither signal) with the combined digital code.”). We find Dr. Holberg’s testimony on this point persuasive. Dr. Holberg testifies that

[i]ndeed, Cesura’s logic module 240 “calculates the digital correction signal $\hat{e}$ that approximates the digital representation of the analog error e minimizing their difference according to a Least Mean Square Algorithm (LMS)” to ensure that $\hat{e}=e$. []. Stated another way, the portion of the digital output code corresponding to the dither signal “ t ” that was injected into the pipeline is effectively removed by the transfer function of amplifiers 225/230 and LMS logic module 240. Hence, Cesura discloses this claim limitation.

Ex. 1002 ¶ 105.

Patent Owner argues also that Petitioner has taken inconsistent positions as to what exactly is the claimed “second portion,” i.e., whether the “second portion” is $G(e)(t)$ or $-G(e)(t)$. PO Resp. 51 (citing Pet. 23). Patent Owner argues that “the sign of ‘ $-G(e)(t)$ ’ is negative, not positive. As such, ‘ $-G(e)(t)$ ’ cannot comprise a portion of anything, because the ‘ $-$ ’ sign indicates this [] term is *missing* from that output.” *Id.*

Petitioner responds that such an assertion is unsupported by Cesura’s disclosure and inconsistent with the electrical convention and the understanding of a person of ordinary skill in the art. Reply 11–12. Petitioner contends that a person of ordinary skill in the art “would readily understand that a ‘ $-$ ’ sign indicates a signal having a magnitude that can be

summed and/or differenced with other signals.” *Id.* at 12 (citing Ex. 1002 ¶ 104). Petitioner points out that Cesura’s Figure 2 explicitly discloses the output of shifter 203 includes a signal having an -eq-t component. *Id.* (citing Ex. 1004, Fig. 2). Dr. Holberg testifies

that the “eq” component and the “t” component of the digital signal from shifter 203 are both of opposite polarity (*i.e.*, “-eq” and “-t”) relative to the “eq” and “t” components of the signals coming from the amplifiers 225/230 (and also from amplifier 220) - *and hence adder 235 results in the difference of the respective components when they are added together.*

Ex. 1002 ¶ 104 (emphasis added). We find more persuasive Dr. Holberg’s testimony that the “-” sign is an indication of polarity, not that it is “missing” as Dr. Moon testifies. *See* Ex. 2002 ¶ 72 (Dr. Moon stating that “‘-G(e)t)’ cannot comprise a portion of anything, because the ‘-’ sign indicates this is term is **missing** from that output.”). The specification clearly describes voltage signals as comprising positive and negative components. *See, e.g.*, Ex. 1004, 4:18–22 (Cesura explaining that test signal t could be “for example, -10 mV for the logic value 0 and +10 mV for the logic value 1”). Our review of Cesura is more consistent with Petitioner and Dr. Holberg’s assertions that Cesura considers the “-” sign as a sign of polarity.

Claim limitation 1[F] requires that the decoder convert the “random digital code” (that generates the dither signal in limitation 1[C]), into “said second portion” of the combined digital code that corresponds to the analog dither signals. Considering Cesura’s Figure 2, Petitioner explains that this limitation is encompassed by Cesura’s adder 235 receiving signal $(V_{in} + eq + t)G_e$ from amplifiers 225/230, and adding this to the signal $(-eq - t)G_l$ from shifter 203, to generate the

combined digital code output of the ADC that is “ $V_{in}(1+\epsilon)G+(e_q+t)G(\epsilon-e)$ ”. Reply 12 (citing Ex. 1002 ¶ 4). Overall, we find persuasive Petitioner’s position with respect to the decoder’s “differencing” function as recited in limitation [1F], that “Cesura discloses adding signals having opposite polarity ($A+(-B)$), which is equivalent to the claimed element of “differencing” two signals ($A-B$), as Holberg demonstrated.” Reply 13 (citing Ex. 1002 ¶¶104–105).

One last thing on this particular argument by Patent Owner. To the extent that Patent Owner is arguing that Petitioner is asserting two different signals from Cesura, i.e., “ $-G(e)(t)$ ”, and “ $+G(e)(t)$ ” for the “second portion” this argument misinterprets Patent Owner’s own claim language. On its face, claim limitation [1E] clearly recites that the “second portion” corresponds to the claimed analog dither signals, not any particular value or signal. See Ex. 1001, 16:10–11 (Claim 1 reciting “a second portion that corresponds to said analog dither signals”). Indeed, if this were not the case, it is unclear how the “combined digital code” in limitation [1E] could be “differenced” with itself, in order to determine a final “system digital code.” We do not find Patent Owner’s arguments here compelling.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 1 and 13 would have been obvious over Cesura.

3. Claims 2 and 14

Claims 2 and 14 require “a differencer to difference said second portion and said combined digital code to provide said system digital code.” Patent Owner argues that Cesura discloses only adder 235 “and does not

calculate a difference between any of its input values.” Patent Owner contends that no matter the values processed by adder 235, the “adder 235 still performs only **additions** on those components and does not performing any differencing as required by the claim.” PO Resp. 57 (citing Ex. 2002 ¶ 79).

Petitioner responds, arguing that the ’452 patent uses the terms “summer” and “differencer” interchangeably. *See* Reply 15 (citing Ex. 1001, 7:46–61) (the ’452 patent describing element 90 in Figure 6 as a “summer”); *see also id.* at 13:36–41 (the ’452 patent describing element 90 in Figure 6 as a “differencer”). Petitioner contends that the difference between a “differencer,” a “summer,” and an “adder,” “is in fact a distinction without a difference” and points out that regardless of the terminology used, both the ’452 patent at Figure 6 and Cesura show a similar conventional schematic symbol to represent this element. *Id.* at 15–16. Petitioner argues that no matter what you call the summing element, “a POSITA would understand that Cesura’s adding of two signals (having opposite polarity) is functionally the same as finding a difference of two signals of the same polarity.”

We acknowledge that addition is a different mathematical operation from subtraction, and “differencing.” However, Petitioner’s position is compelling that a person of ordinary skill in the art would understand that an “adder” as described by Cesura, and a “differencer” as recited in the claims of the ’452 patent, are functionally and structurally equivalent. The ’452 patent clearly conflates the element of summer 90, and differencer 90. *Compare* Ex. 1001, 7:46–61, *with id.* at 13:36–41. With respect to Cesura calling a similar element an “adder 235,” Dr. Holberg explains persuasively that “[b]ecause the “t” components of these signals have opposite polarity

(“t” and “-t”) adding the signals results in the difference in the magnitude of the respective components. Hence, adder 235 is a “differencer” as claimed.” Ex. 1002 ¶ 110. Although Cesura does not call “adder 235” a “differencer,” we credit Dr. Holberg’s testimony on this point. Moreover, Patent Owner does not explain persuasively that there is any tangible structural or functional difference between these elements. Accordingly, we are persuaded that Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would understand Cesura’s adder as a summer element that is at least equivalent functionally to the claimed “differencer.” It is well-settled that “[a] reference need not teach a limitation *in haec verba*.” *In re Bode*, 550 F.2d 656, 660 (CCPA 1977).

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 2 and 14 would have been obvious over Cesura.

4. Claims 8, 9, 15, and 16

Petitioner argues for claims 8 and 15, similar to limitation [1D], that “Cesura’s signal converters (stages 105₃-105₁) are configured to provide analog output signals to succeeding signal converters.” Pet. 32 (citing Ex. 1002 ¶ 113. Petitioner explains that because Cesura’s pipelined converters 105₂-105₁ are configured to receive an input signal from a preceding converter “each converter stage (except the last one) provides a residue signal with an amplitude limited to an output-signal window (*i.e.*, the input range of the next stage). *Id.* at 33–34 (citing Ex. 1002 ¶ 114).

Petitioner argues for claims 9 and 16, that Cesura teaches a dither range “lower than a half LSB of the ADC 115.” *Id.* at 35 (citing Ex. 1002 ¶ 116). Petitioner contends that

Cesura further discloses that stage 105₃, which contains the ADC 115 is a four bit stage. [] Since +/-10 mV is a half LSB for this ADC, then one LSB is +/- 20 mV. Hence, the stage must be capable of an output window of at least +/- 320 mV, meaning that the predetermined dither window of +/-10 mV is less than this output-signal window.

Id.

Patent Owner argues that claims 8, 9, 15, and 16 depend either directly or indirectly from independent claims 1 and 13, and are not obvious for the same reasons as the independent claims. PO Resp. 57.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner's showing as to claims 8, 9, 15, and 16, as set forth in the Petition and summarized above, as our own. *See* Pet. 32–35, 38. Accordingly, we are persuaded by Petitioner's arguments and evidence that claims 8, 9, 15, and 16 would have been obvious over Cesura.

C. Obviousness over Cesura, Lewis, and Bjornsen

Petitioner argues that claims 12 and 19–20 would have been obvious over the combination of Cesura, Lewis, and Bjornsen. Pet. 38–52. Having reviewed the information provided by Petitioner, including the relevant portions of the supporting Holberg Declaration, we are persuaded, on the current record, that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Cesura, Lewis, and Bjornsen.

1. Lewis (Ex. 1006)

Lewis describes a pipelined, 5-Msample/s, 9-bit analog-to-digital (A/D) converter designed and fabricated in CMOS technology. Ex. 1006,

954.⁷ An example of the pipelined A/D converter is illustrated in Figure 1, reproduced below.

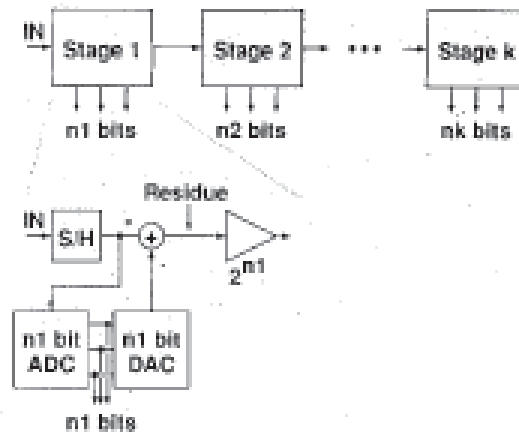


Fig. 1. Block diagram of a general pipelined A/D converter.

Figure 1, above, illustrates a block diagram of a general pipelined A/D converter with k stages. *Id.* Each stage contains an S/H circuit, a low-resolution A/D subconverter, a low-resolution D/A converter, and a differencing fixed-gain amplifier. *Id.* Each stage then does a low-resolution A/D conversion on the held input, and the code just produced is converted back into an analog signal by a D/A converter. *Id.* Finally, the D/A converter output is subtracted from the held input, producing a residue that is amplified and sent to the next stage. *Id.*

Figure 4, reproduced below, illustrates an example of a two-stage pipelined A/D converter.

⁷ We refer here, to the actual IEEE Journal page numbers.

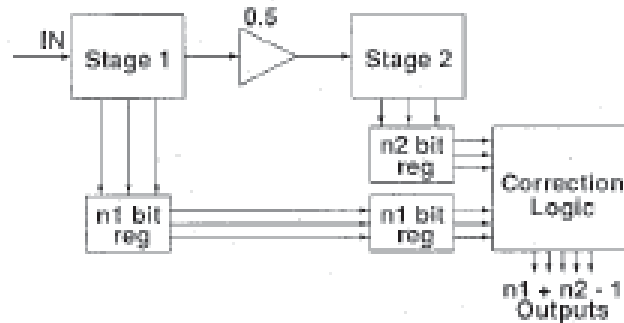


Fig. 4. Block diagram of a two-stage pipelined A/D converter with digital correction.

Figure 4, above, illustrates a block diagram of a two-stage pipelined A/D converter with digital correction. *Id.* at 956. The new elements in this diagram are the pipelined latches, the digital correction logic circuit, and the amplifier with a gain of 0.5. *Id.*

Lewis describes that 1 bit from the second stage is saved to digitally correct the outputs from the first stage; the other $n2-1$ bits from the second stage are added to the overall resolution. *Id.* After the pipelined latches align the outputs in time so that they correspond to one input, the digital correction block detects overrange in the outputs of the second stage and changes the output of the first stage by 1 LSB at $n1$ -bit level if overrange occurs. *Id.*

2. Bjornsen (Ex. 1007)

Bjornsen describes an analog-to-digital converter (ADC) circuit that converts an analog input signal into a digital output signal, where the ADC circuit includes a noise shaping first stage cascaded with a pipelined second stage. Ex. 1007, 2:53–56. The first stage includes a sample-and-hold circuit and a first order modulator, where the first order modulator includes a noise shaping filter, a FLASH ADC and a feedback digital-to-analog converter (DAC). *Id.* at 2:56–59. A digital dither generator is used to provide a dither signal to the ADC circuit. *Id.* at 2:59–60.

Figure 6, reproduced below, illustrates an example circuit diagram of a multiplying and integrating DAC (MDAC) used in a first order modulator.

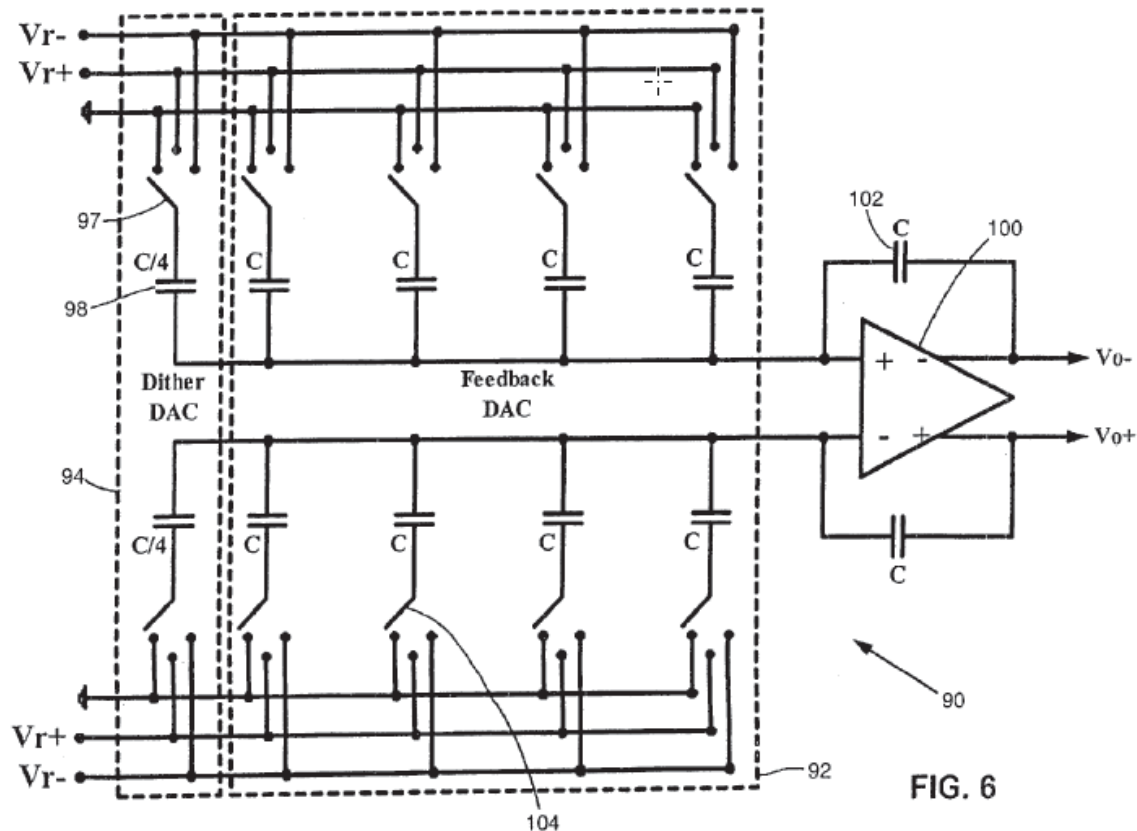


Figure 6, above, shows a MDAC 90 be in used in a feedback phase of a modulator 50. *Id.* at 6:57–59, 7:3–4. The MDAC 90 consists of a regular feedback DAC 92 and a dither DAC 94. *Id.* at 6:59–60. The regular feedback DAC 92 includes unit capacitor 96, each having the size of C , and the dither DAC 94 include dither capacitors 98, each having a size of $C/4$. *Id.* at 6:60–63. Dither capacitors 98 provide a dither signal to dither DAC 94. *Id.* at 7:23–26.

3. Dependent claims 12, 19, and 20

Claim 12 depends directly from claim 8 and recites

wherein said selected signal converter includes at least first and second dither capacitors and said digital-to-analog converter is configured to switchably couple different voltages to said first

dither capacitor to thereby contribute to said analog dither signals and switchably couple different voltages to said second dither capacitor to thereby contribute to a respective one of said plurality of digital codes.

Ex. 1001, 16:63–17:3. Claims 19 and 20 each depend directly from claim 15 and recite similar limitations. *Id.* at 18:20–29. Petitioner argues Cesura discloses DAC 210 that injects analog dither signals “t” into the first stage 105₃ of the pipeline. Pet. 45 (citing Ex. 1002 ¶¶ 146, 153, 156). While Petitioner concedes, “Cesura provides no details regarding the specific circuitry in order to realize these functions,” Petitioner further argues “Lewis and Bjornsen provide the type of circuit details that Cesura does not.” *Id.* at 46 (citing Ex. 1002 ¶¶ 147, 154, 157). Petitioner further contends that Dr. Holberg identifies several different reasons why a person of ordinary skill in the art would have been motivated to combine Cesura, Lewis, and Bjornsen. *Id.* at 39–43 (citing Ex. 1002 ¶¶ 132–144).

Dr. Holberg testifies that as shown by Cesura, ADCs typically employ a sample and hold circuit, a sub-ADC circuit, sub-DAC circuit, and an adder. Ex. 1002 ¶ 129. According to Dr. Holberg these are well-known circuits and components of an ADC to those of ordinary skill in the art, and “[a] POSITA would require no details regarding the specific elements (capacitors, operational amplifiers, and the like) to understand the respective elements’ purpose and function.” *Id.* Dr. Holberg explains however, that Lewis and Bjornsen “do provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Cesura.” *Id.* Dr. Holberg testifies further that the specifics of these type of ADC components were well-known and that

Lewis discloses the details regarding, *e.g.*, a basic switched capacitor implementation for the components. Ex. 1006, pp. 954–

959. Similarly, Bjornsen also discloses an ADC system employing common switched capacitor techniques for implementing the circuit components, and further discloses using a switched capacitor circuit for, *e.g.*, injecting dither signals into the system.

Id. ¶ 132 (citing Ex. 1007, Figs. 2, 5, 6, 9). Based on the level of ordinary skill in the art, as well as the asserted well-known technology and circuit structure of such components, Dr. Holberg testifies that “[t]hese types of circuits are basic building blocks for analog circuits and are readily substituted one for another. . . the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 134.

Patent Owner does not expressly dispute the combination of Cesura, Lewis, and Bjornsen, but argues that neither Lewis nor Bjornsen teach or discloses “configuring a DAC to ensure that the injected dither propagates to all stages of a pipelined converter.” PO Resp. 58 (citing Ex. 2002 ¶ 81).

Because, as discussed above, we do not agree with Patent Owner’s claim interpretation, and now having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner’s showing as to claims 12, 19, and 20, as set forth in the Petition and summarized above, as our own. *See* Pet. 38–52. Based on the entire record, we are persuaded that Petitioner has shown by a preponderance of the evidence that claims 12, 19, and 20 would have been obvious over Cesura, Lewis, and Bjornsen.

D. Obviousness over Fu and Lewis

Petitioner argues that claims 1–4, 8, 9, and 13–16 of the ’452 patent would have been obvious over Fu and Lewis. Having reviewed the information provided by Petitioner, including the relevant portions of the supporting Holberg Declaration, we are persuaded, on the current record,

that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been unpatentable over Fu and Lewis.

1. *Fu (Ex. 1005)*

Fu describes a 10-bit 40-Msample/s two-channel parallel pipelined analog-to-digital (ADC) with monolithic digital background calibration. Ex. 1005, 1904. The ADC consists of M ADC's in parallel, an analog demultiplexer at the input and a digital multiplexer at the output. *Id.* Each ADC operates at an overall sampling rate f_s divided by M . *Id.* During operation, the analog demultiplexer selects each ADC in turn to process the input signal. *Id.* The corresponding digital multiplexer selects the digital output of each ADC periodically and forms a high-speed ADC output. *Id.* An example ADC is illustrated in Figure 4, reproduced below.

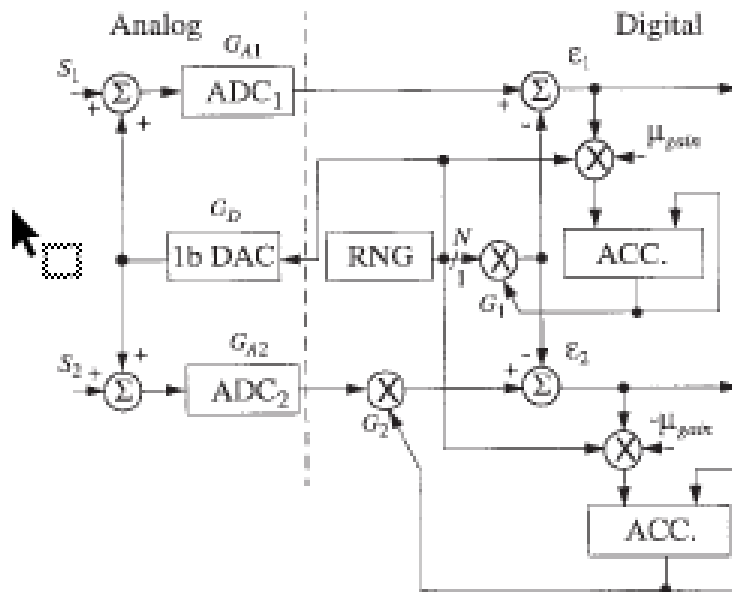


Fig. 4. Modified gain calibration system for two time-interleaved ADC's.

Figure 4, above, shows a modified gain calibration system an ADC comprising two time-interleaved ADCs. *Id.* at 1906. The ADC receives an analog signal S_1 and generates a combined digital code ϵ_1 . *Id.* at 1905–1907.

Figure 7, reproduced below, illustrates an example of a pipelined ADC.

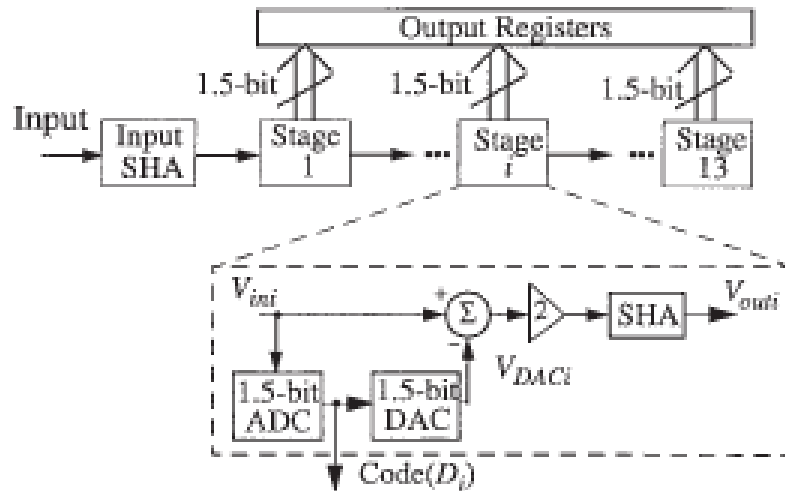


Fig. 7. Block diagram of the 14-bit pipelined ADC.

Figure 7, above, illustrates a block diagram of one pipelined ADC. *Id.* at 1907. The ADC includes a sampler (“Input SHA”) that samples an incoming analog signal (“Input”) and a plurality of signal converter stages (“Stage 1, Stage i . . . Stage 13”) that successively process the samples. *Id.* The stages process the analog samples and dither signals and generate respective digital codes (“1.5 bit”), which are fed to output registers (“Output Registers”). *Id.* at 1905.

2. Independent Claims 1 and 13

Petitioner argues the combination of Fu and Lewis teach or suggest the limitations of claims 1–4, 8, 9, and 13–16. Pet. 58–86. Petitioner argues that both Fu and Lewis disclose an “analog to digital converter system” as recited in claim [1A]. *Id.* at 58 (citing Ex. 1002 ¶¶ 177–179). Petitioner argues that at least Fu discloses “a sampler” for providing input signal samples as called for in claim [1B]. *Id.* at 60 (citing Ex. 1002 ¶¶ 181–182). Petitioner argues for claim [1C] that both Fu and Lewis disclose pipelined

signal converters for processing signal samples. *Id.* at 62–63 (citing Ex. 1002 ¶¶ 185–187). Considering claim [1D], Petitioner argues that Fu teaches “the 1b DAC is configured to ‘inject’ the dither signals into the pipelines ADC,” and “the pipelined ADC is processed by a first signal converter stage ‘Stage 1’ of the pipeline, which includes a sampler circuit ‘SHA.’” *Id.* at 66 (citing Ex. 1002 ¶ 190). Petitioner argues with respect to element [1E] that a person of ordinary skill in the art understood that Fu’s “Output Registers at least logically combine the digital codes “D_i” into a combined digital code.” *Id.* at 68 (citing Ex. 1002 ¶¶ 193–194). Petitioner argues for limitation [1F] that “Fu teaches multiplying the output of the random number generator “RNG” [] by a variable gain “G1” [] for subsequent subtraction from ADC1 with a differencer []. *Id.* at 72 (citing Ex. 1002 ¶¶ 198–199). For limitation [1G], Petitioner argues that “Fu’s analog dither signals will cause at least one stage of its pipelined ADC to operate at different operating points,” and that in Fu’s “time-interleaved architecture, each successive sample x(t) would be processed by a different ADC (*i.e.*, ADC0 – ADCM-1).” *Id.* at 73–74 (citing Ex. 1002 ¶¶ 200–201).

Petitioner contends that Dr. Holberg identifies several different reasons why a person of ordinary skill in the art would combine the teachings of Fu and Lewis. *Id.* at 53–58 (citing Ex. 1002 ¶¶ 159–165, 229–233). Dr. Holberg testifies that “Fu discloses a pipelined signal converter stage includes a SHA, a sub-ADC, and a sub-DAC - but these elements are illustrated simply using symbols to represent their respective functions.” Ex. 1002 ¶ 159 (citing Ex. 1005, Fig. 7). Dr. Holberg testifies that these ADC components and their structural circuitry are well-known, but, “Lewis, on other hand, does provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Fu.” *Id.* (citing

Ex. 1006, Figs 6(a) and 9). Dr. Holberg reasons that “[g]iven that the performance and function of such circuits were well known, the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 164.

Patent Owner does not expressly dispute the combination of Fu and Lewis, but argues that “neither Fu nor Lewis contains any teaching or suggestion regarding a pipelined converter in which dither propagates through all the converter stages as claimed, the combination of Fu and Lewis likewise fails to anticipate any of the challenged claims.” PO Resp. 59 (citing Ex. 2002 ¶¶ 82–83). Patent Owner argues, as it has throughout this proceeding, that due to “dither exhaustion,” there “is no basis for Petitioner’s suggestion – contrary to the ’452 patent’s teachings— that Fu’s injected signal would propagate to downstream converter stages.” *Id.* at 62 (citing Ex. 2002 ¶ 91).

We determine that Petitioner has shown that a person of ordinary skill in the art, considering the teachings in Fu, would have looked to Lewis in order to determine more specifically a circuit structure for implementing the teachings in Fu. Pet. 53–58. Petitioner explains that Lewis provides “detailed disclosure to fill in details that Fu presumably considered too well-known and/or too trivial to provide.” Pet. 53 (citing Ex.1002 ¶ 159). Dr. Holberg testifies that in view of the level of ordinary skill in the art “[b]ecause such details are not necessary to understand the invention disclosed by Fu, presumably, they were omitted. Lewis, on other hand, does provide the circuit details that a POSITA would naturally look to in order to implement the functionality disclosed by Fu.” Ex.1002 ¶ 159 (citing Ex. 1006, Figs 6(a) and 9). Dr. Holberg’s testimony is essentially un rebutted on this point. Dr. Holberg also offers several rationales explaining why a person of ordinary skill in the art would have combined Fu and Lewis. Dr.

Holberg testifies, for example that like Fu, Lewis “discloses at the system level a pipelined ADC system employing similar components. . . [a]dditionally, Lewis discloses the details regarding, *e.g.*, basic switched capacitor circuit implementations for some of the components. *Id.* ¶ 162 (citing Ex.1006, Figs. 6(a), 9; pgs. 957–959). Dr. Holberg explains persuasively that a person of ordinary skill in the art would have known to substitute or use Lewis’s disclosed circuit structures with Fu’s higher level disclosure because Lewis’s “circuits are basic building blocks for analog circuits and are readily substituted for one for another. Given that the performance and function of such circuits were well known, the results of such substitution would have been predictable to a POSITA.” *Id.* ¶ 164. Patent Owner and Dr. Moon do not expressly dispute Dr. Holberg’s testimony as to the rationale to combine and we are persuaded that a person of ordinary skill in the art would have been motivated to look to Lewis in order to determine more specific circuit structures to carry out the more functional teachings in Fu.

We turn next to the parties’ express arguments and evidence pertaining to the teachings of Fu and Lewis as they relate to independent claims 1 and 13.

Patent Owner again relies on its erroneous claim construction “that the analog input signals be processed along ‘different signal-processing paths’ of *each* of the **multiple** signal converters in the analog-to-digital converter.” *Id.* at 63. As discussed above, we do not find this argument persuasive because the claims do not require that the dither portion of the combined sampled input signals propagates through all, or each, stage of the converter system. Section II. G. Patent Owner next argues that Fu “show[s] the addition of a random analog value using **summing nodes** located *before* the

pipelined ADC stages,” and thus does not inject a dither signal into a converter stage as required by independent claims [1D] and [13C]. *Id.* at 61 (citing Ex/ 2002 ¶ 89).

In light of Patent Owner’s second argument here, we address the following question.

- a) *Whether Fu teaches injecting dither signals “into at least a selected one of said signal converters”*

Patent Owner argues specifically that “Fu teaches injecting a random signal into a converter system at a point **before** an ADC pipeline, and not **into** a converter stage of an ADC pipeline. PO Resp. 64 (citing Ex. 2002 ¶ 96). Patent Owner asserts that a diagram provided by Petitioner, ostensibly combining Fu’s Figures 4 and 7, and alleged to show injection of dither signal into a first pipelined stage “was **fabricated** by Petitioner and is **not** found anywhere in Fu. In fact, the **actual** diagrams in Fu clearly show that the SHA prior to the first stage is separate from the first signal converter stage of the ADC pipeline.” *Id.* at 65–66.

Petitioner responds, arguing that Patent Owner’s argument “fails to recognize how a POSITA would understand the prior art.” Reply 19 (citing *KSR*, 550 U.S. 398. Petitioner contends that Patent Owner’s argument is mainly based on Fu’s figure 4, for example, as reproduced below, depicting a summer, or adder, illustrated prior to the ADC.

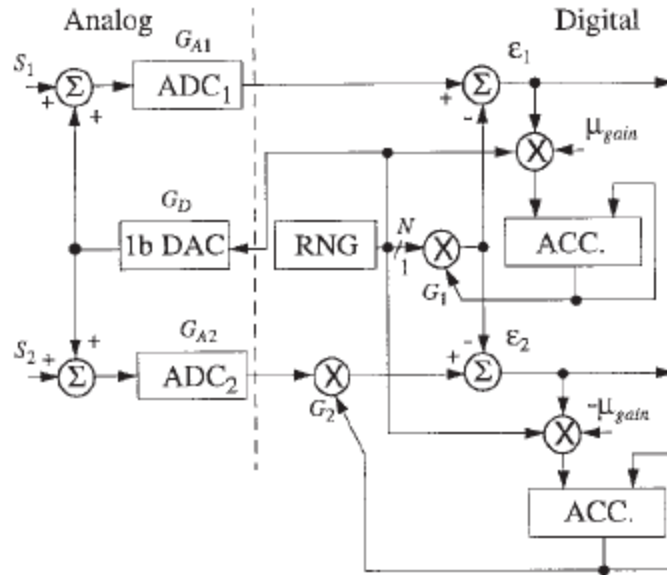


Fig. 4. Modified gain calibration system for two time-interleaved ADC's.

Figure 4 illustrates a random number generator RNG applying dither via 1b DAC to an input signal S_1 . Petitioner argues that Patent Owner's argument is a narrow reading of Fu's disclosure and teaching, and Petitioner relies on Dr. Holberg, who explains that "Fu's adder is symbolically represented for clarity of illustration, and . . . simply represents the *function* of combining signals (such as the dither signal and the analog input signal), *e.g.*, by applying the two signals onto a common capacitor or capacitors." Reply 19 (citing Ex. 1002 ¶ 220).

For Patent Owner, Dr. Moon testifies that according to Figure 4, "Fu adds a random signal to the analog signal that is input into an ADC pipeline, not into a signal converter stage of the ADC pipeline." Ex. 2002 ¶ 97. In other words, Dr. Moon's point is that "Fu clearly injects its random analog signal upstream of the ADC pipeline, and not into any signal converter stage of the pipeline." *Id.*

Considering the level or ordinary skill in the art, we find Dr. Holberg's testimony more persuasive. Considering Figure 4, above, Fu

discloses functionally, (as opposed to structurally with a specific circuit) combining a dither signal from 1b DAC with input signal S_1 and entering into ADC_1 . We acknowledge that Figure 4 illustrates diagrammatically summing the digital signal and then sending it to ADC_1 , but Dr. Holberg explains persuasively that a person of ordinary skill in the art would understand that dither is injected into Stage 1 of the ADC_1 by combining it with the input signal S_1 , and then providing that signal to a sampler circuit, SHA, for Stage 1 of Fu. Dr. Holberg testifies that Fu's "combining function is a form of injecting, and thus Fu teaches the 1b DAC is configured to 'inject' the dither signals into the pipelined ADC." Ex. 1002 ¶ 190. Dr. Holberg summarizes that a person of ordinary skill in the art would have understood "Fu's b1 DAC thus 'inject[s]' the analog dither signals into the 'signal converters' . . . which as noted above, each contain a sampler." *Id.*

Although Patent Owner argues that Fu's Figures 4 and 7 have been altered and misrepresent Fu teachings, considering the level of ordinary skill in the art, we find Patent Owner and Dr. Moon's analysis of Fu too narrow. PO Resp. 65–66. We are persuaded by Dr. Holberg's testimony that a person of skill in the art would have understood Fu in a similar manner to Petitioner's combination of Fu's Figures 4 and 7, reproduced below.

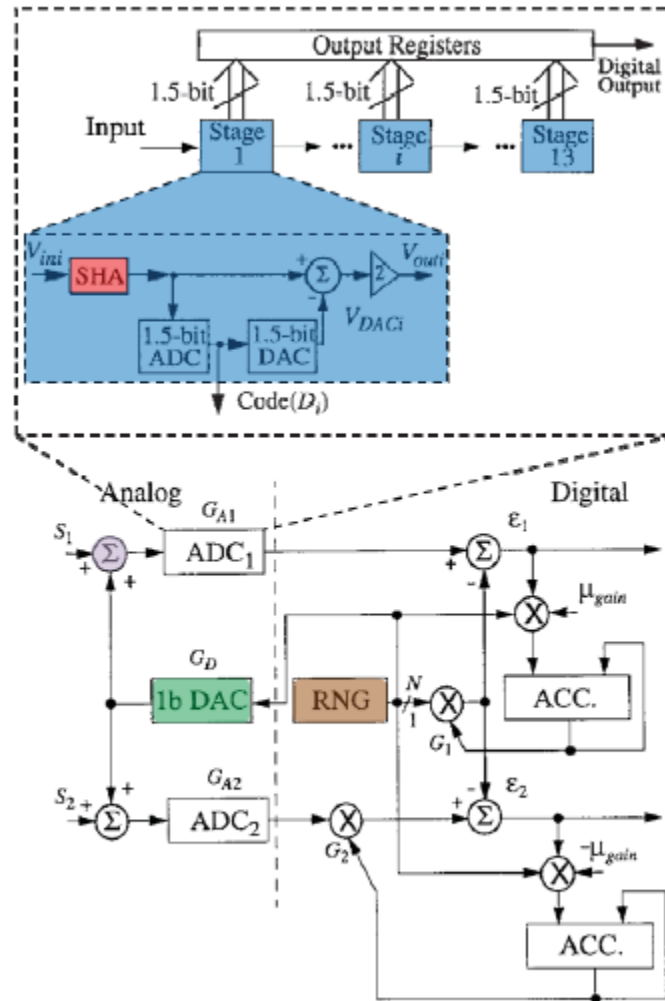


Figure C (combined teachings of Fu Figs. 4 and 7).

Petitioner’s combination of the teachings in Fu’s Figures 4 and 7 is reproduced above, and illustrates injecting dither, combined with the input signal, into a sampler circuit of Stage 1 in Fu. Pet. 67. Fu’s Figure 7 depicts each Stage of its pipelined signal converter including a sampler circuit SHA. Ex. 1005, 1907, Figure 7; *see also* Ex. 1002 ¶ 184 (Dr. Holberg testifying that “[a] POSITA would recognize that a S/H circuit samples an incoming signal and provides samples of that signal to circuitry at its output.”).

Considering all the evidence before us, including the competing testimony of Dr. Moon and Dr. Holberg, we are persuaded that a person of ordinary skill

in the art would have understood that Fu, as a whole, and considering the level of ordinary skill in the art, teaches “inject[ing] analog dither signals into at least a selected one of [said sampler and] said signal converters which process said samples and said analog dither signals into a plurality of digital codes,” as called for in independent claims 1 and 13.

Having considered the entire record now before us, including the arguments and evidence presented by both parties, we are persuaded by Petitioner’s arguments and evidence that claims 1 and 13 would have been obvious over Fu and Lewis.

3. *Dependent claims 2–4, 8, 9, and 14–16*

Petitioner argues that Fu discloses a pseudorandom number generator providing a random digital code to the DAC, as well as a differencer as called for in claim 2. Pet. 76–77. Petitioner argues for claim 3 that a person of ordinary skill in the art would have understood that dither is added via a sampler circuit into each of Fu’s converter stages. *Id.* at 77–78 (citing Ex. 1002 ¶ 208).

For claim 4, Petitioner argues that Fu discloses using 25% of signal amplitude for dither which is less than the output signal window of the converter stages *Id.* at 79–80 (citing Ex. 1002 ¶ 210). Petitioner argues that the limitations of claim 8 are similar to those of claim [1D] and “in Fu, the analog dither signal output from the DAC is injected into the sampler ‘SHA,’ which is part of the first converter stage ‘Stage 1.’” *Id.* at 80 (citing Ex. 1002 ¶¶ 211–212). Petitioner argues that claim 9, which depends from claim 8, is similar to claim 4 and that Fu discloses a dither range, e.g., 25% of the signal amplitude which is less than the full output signal window. *Id.* at 82 (citing Ex. 1002 ¶ 215). For claims 14, 15, and 16, which ultimately depend from independent claim 13, Petitioner argues these claims are

substantively the same as claims 2, 8 and 9 and therefore obvious over Fu and Lewis for the same reasons as previously discussed. *Id.* at 86 (citing Ex. 1002 ¶¶ 226–228).

Patent Owner argues that these dependent claims would not have been obvious for the same reasons as the respective independent claims 1 and 13, from which they depend. PO Resp. 67. Patent Owner offers no substantive rebuttal arguments or testimony contradicting that of Petitioner and Dr. Holberg as to these dependent claims. *Id.* Having considered the entire record now before us, including the arguments and evidence presented by both parties, we adopt and incorporate Petitioner’s showing as to claims 2–4, 8, 9, and 14–16, as set forth in the Petition and summarized above, as our own. *See* Pet. 76–82, 86. Accordingly, we are persuaded by Petitioner’s arguments and evidence that claims 2–4, 8, 9, and 14–16 would have been obvious over Fu and Lewis.

4. Conclusion as to Obviousness Based on Fu and Lewis

Based on the complete trial record in the proceeding, for the reasons above we are persuaded that claims 1–4, 8, 9, and 13–16 would have been obvious in view of Fu and Lewis. Because, together with the challenges based on Cesura, as well as Cesura, Lewis, and Bjornsen, we determine that all the challenged claims of the ’452 patent are unpatentable and we do not reach Petitioner’s challenge asserting that claims 12, 19, and 20 would have been obvious based on Fu, Lewis, and Bjornsen.

III. CONCLUSION

As summarized in the table below, the Petition and supporting evidence has shown by a preponderance of the evidence that claims 1–4, 8, 9, 12–16, 19, and 20 of the '452 patent would have been obvious.⁸

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 8, 9, 13–16	103	Cesura	1, 2, 8, 9, 13–16	
12, 19, 20	103	Cesura, Lewis, and Bjornsen	12, 19, 20	
1–4, 8, 9, 13–16	103	Fu and Lewis	1–4, 8, 9, 13–16	
12, 19, 20	103 ⁹	Fu, Lewis, and Bjornsen		
Overall Outcome			1–4, 8, 9, 12–16, 19, 20	

⁸ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

⁹ As explained above, because we determined that all the challenged claims of the '452 patent are unpatentable based on the other grounds, we do not reach Petitioner's challenge asserting that claims 12, 19, and 20 would have been obvious based on Fu, Lewis, and Bjornsen.

IV. ORDER

For the reasons given, it is

ORDERED that, based on a preponderance of the evidence claims 1–4, 8, 9, 12–16, 19, and 20 of the '452 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, any party to the proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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