

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. AND XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

IPR2020-01564
Patent 6,900,750 B1

Before JEFFREY S. SMITH, SCOTT A. DANIELS, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

On September 1, 2020, Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 2, 4–8, and 12 of U.S. Patent No. 6,900,750 B1, issued on May 31, 2005 (Ex. 1201, “the ’750 patent”). Paper 1. Petitioner filed a corrected Petition on November 3, 2020, to correct typographical errors. Paper 8 (“Pet.”). Analog Devices, Inc. (“Patent Owner”) filed a Response. Paper 21 (“PO Resp.”). Petitioner filed a Reply. Paper 27 (“Reply”). Patent Owner filed a Sur-Reply. Paper 29 (“PO Sur-Reply”). A hearing was held on December 10, 2021. Paper 33.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claim 12 is unpatentable, and that claims 1, 2, and 4–8 are not unpatentable.

BACKGROUND

A. *The ’750 Patent (Ex. 1201)*

The ’750 patent relates to adjusting gain and offset mismatches in a signal conditioning system having interleaved analog-to-digital converters (ADCs). Ex. 1201, 1:9–14, 5:28–29, 6:63–66. Interleaving multiple ADCs provides the advantage of increasing the sampling rate proportionally to the number of ADCs. *Id.* at 6:63–7:4. For example, if the clock frequency of each ADC is f_c and the number of interleaved ADCs is M , then the sampling rate of the system is $f_s = M \cdot f_c$. *Id.* The interleaved ADCs often have mismatches in offset and gain, however, which affect the Signal-to-Noise and Distortion ratio. *Id.* at 1:26–37. To correct the offset mismatches of the interleaved ADCs, the system includes an offset sensor coupled with the ADCs to sense and adjust an offset signal difference. *Id.* at codes (54), (57), 3:41–47, 7:5–21, Figs. 1–4. To correct the gain mismatches, the system includes a gain sensor coupled with the ADCs to sense a gain difference, and

a gain corrector coupled with the gain sensor to adjust the gain difference.
Id. at codes (54), (57), 3:41–47, 10:12–21, 10:40–65, 11:26–52, Figs. 6–8.

Figure 4 below shows a block diagram illustrating a signal conditioning system 140 including interleaved ADCs. Ex. 1201, 3:44–46, 8:15–23.

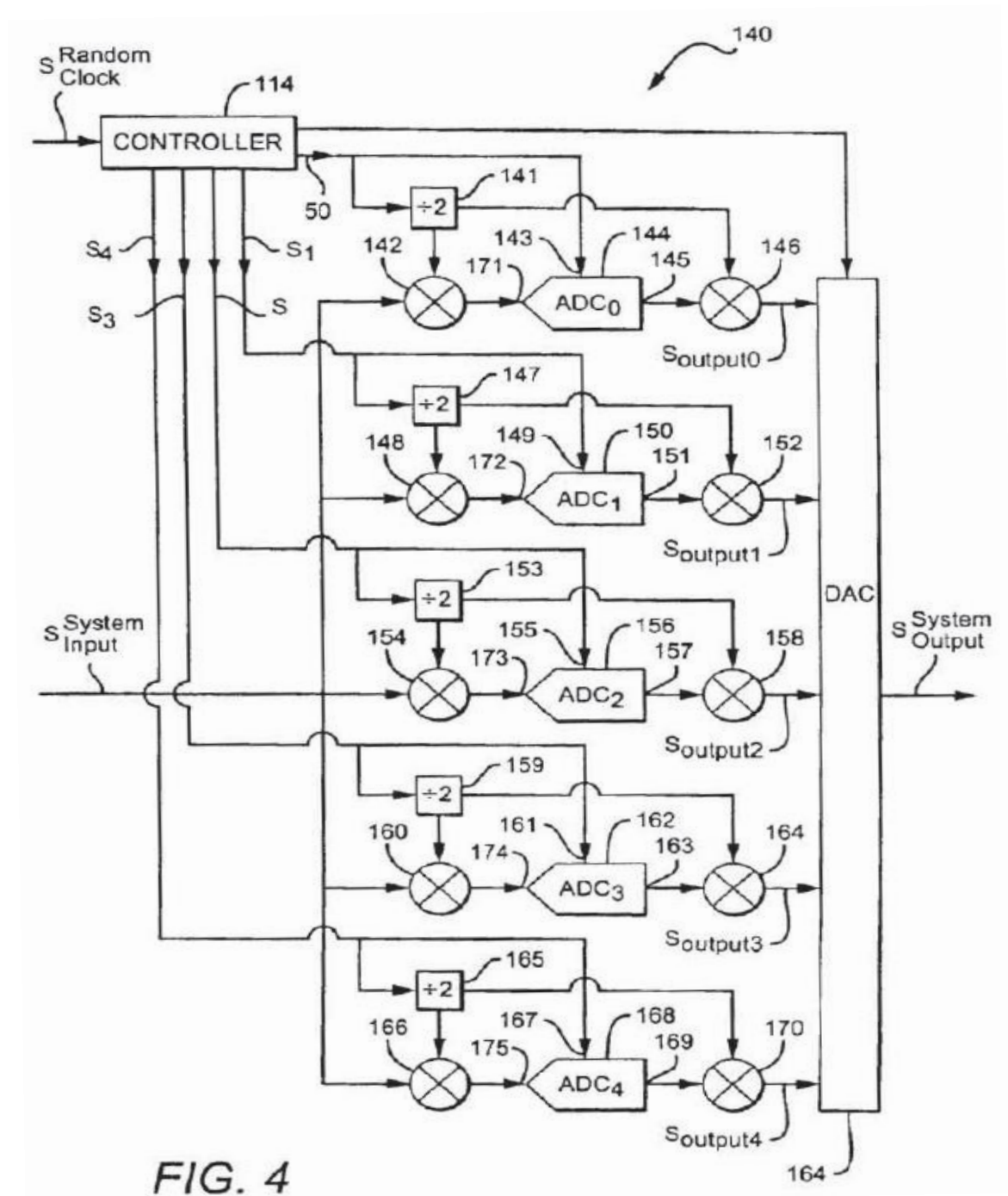


FIG. 4

As shown in Figure 4 above, signal conditioning system 140 includes interleaved ADCs 144, 150, 156, 162, and 168. Ex. 1201, 8:24–25. Each of the ADCs is a zero offset ADC, in which the offset signal is subtracted from an analog input signal to condition a digital output signal. *Id.* at 9:7–13; see *id.* at 5:17–45, Fig. 1. Controller 114 provides a random select or clock signal to each ADC through respective ADC select terminals. *Id.* at 8:51–54. For example, controller 114 provides random clock signal S_0 to ADC 144 through ADC select terminal 143. *Id.*

Each ADC has a modulator coupled to its input and a demodulator coupled to its output. *Id.* at 8:25–48. For example, modulator 142 is coupled to input 171 of ADC 144, and demodulator 146 is coupled to output 145 of ADC 144. *Id.* at 8:25–27. The modulators and demodulators are coupled to the controller through a respective divider. *Id.* at 8:25–48. For example, controller 114 is connected to modulator 142 and demodulator 146 through divider 141. *Id.* at 8:27–29.

Inputs of the modulators are configured to randomly receive the system input signal. *Id.* at 8:58–60. Each modulator multiplies the system input signal by the divided random clock prior to being converted by the corresponding ADC, and each demodulator multiplies the output of the corresponding ADC by the divided random clock to form each output signal $S_{\text{output}0}$ to $S_{\text{output}4}$. *Id.* at 8:41–67. The outputs of the demodulators are coupled to digital-to-analog converter (DAC) 164, which converts the digitized output into an analog signal. *Id.* at 9:1–6.

B. Illustrative claim

As noted above, Petitioner challenges claims 1, 2, 4–8, and 12, of which claim 1 is independent and is reproduced below.

1. A signal conditioning system, comprising:
a first converter;
a random clock, said random clock configured to decorrelate an input signal provided to said first converter from said random clock so that the average output signal of said first converter is proportional to a first offset signal; and
a first offset sensor connected to sense the first offset signal, and in response to said sensing, to condition said first converter output.

Ex. 1201, 13:61–14:3.

C. Related Proceedings

Petitioner and Patent Owner identify the following related litigation asserting the '750 patent: *Analog Devices, Inc. v. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd.*, C.A. No. 19-cv-02225-RGA (D. Del.). Pet. 84; Paper 5, 2. Patent Owner also states that “Petitioner[] filed petitions for *Inter Partes* Review of U.S. Patent No. 10,250,250 (Case No. IPR2020-01210), U.S. Patent No. 8,487,659 (Case No. IPR2020-01219), U.S. Patent No. 7,012,463 (Case No. IPR2020-01336), U.S. Patent No. 7,286,075 (Case No. IPR2020-01559), U.S. Patent No. 7,719,452 (Case No. IPR2020-01561), and U.S. Patent No. 6,900,750 (Case Nos. IPR2020-01483, IPR2020-01484, and the present case), which are also at issue in the above litigation.” Paper 5, 2.

D. References

Petitioner relies on the following references:

1. “Jamal” (A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration, IEEE Journal of Solid-State Circuits, vol. 37, no. 12, pp. 1618–27, Dec. 2002) (Ex. 1205);

2. “Ferragina” (Gain and offset mismatch calibration in multi-path sigma-delta modulators, Proceedings of the 2003 International Symposium on Circuits and Systems, 2000) (Ex. 1207).
3. “Elbornsson” (Analysis of Mismatch Effects in Randomly Interleaved A/D Converter Systems, Report no.: LiTH-ISO-R-2496, Linkoping University Electronic Press, March 3, 2003.) (Ex. 1204);
4. “Eklund” (U.S. Patent No. 6,392,575 B1, issued May 21, 2002) (Ex. 1206);

E. Asserted Challenges to Patentability

Petitioner asserts that claims 1, 2, 4–8, and 12 are unpatentable on the following challenges:

Ground	Claims Challenged	35 U.S.C. §	References/Basis
1	1, 2, 4–6	102	Jamal
2	7, 8	103	Jamal, Ferragina
3	12	103	Elbornsson and Jamal
4	12	103	Eklund and Jamal

Petitioner also relies on testimony from Dr. Douglas Holberg (Ex. 1202, “Holberg Decl.”).

II. ANALYSIS

A. *Legal Principles*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (To anticipate a patent claim under 35 U.S.C. § 102, “a single prior art reference must expressly or inherently disclose each claim limitation.”). Moreover, “[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008). This is not an *ipsissimis verbis* test, however—identical terminology is not required. *See In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he

dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference.”). Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of obviousness or nonobviousness, i.e., secondary considerations. See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated

reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Furthermore, Petitioner does not satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. Petitioner asserts a person of ordinary skill in the art (“POSITA”) at the time of the invention “would have at least a Master’s Degree in Electrical Engineering or equivalent field, including studies in designing data converters, and two to five years of relevant experience; or a Ph.D. degree in Electrical Engineering or equivalent field.” Pet. 34 (citing Ex. 1202 ¶¶ 17–18). Patent Owner does not address the level of ordinary skill in the art in its Response. *See generally* PO Resp.

For purposes of this decision, we adopt Petitioner’s formulation because it is consistent with the ’750 patent and the asserted prior art.

C. Claim Construction

We interpret claims in the same manner used in a civil action under 35 U.S.C. § 282(b) “including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. §42.100(b) effective

November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Patent Owner contends that “random clock,” “offset sensing circuit,” and “sensing” a gain or offset signal need to be construed. PO Resp. 13–17. Petitioner contends that no construction of any term is necessary. Reply 2–5. The contentions of the parties were addressed in our Final Written Decision for IPR2020-01483, which was mailed on the same day as this Decision. We decline to construe these terms for the reasons given in that Final Written Decision.

D. Asserted Anticipation Over Jamal

1. Overview of Jamal (Ex. 1205)

Jamal discloses a time-interleaved ADC that uses digital-background calibration to overcome offset, gain, and sample-time errors between channels. Ex. 1205, 7.¹ Figure 1 of Jamal is reproduced below.

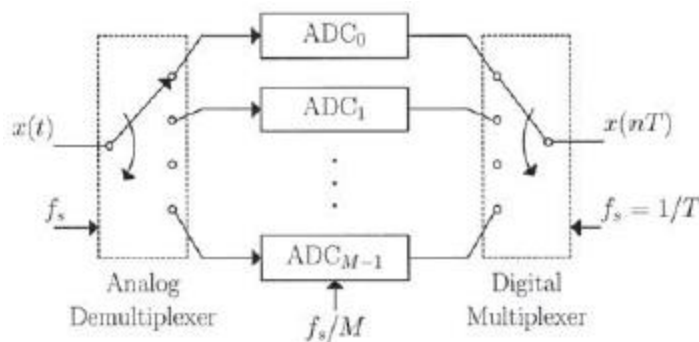
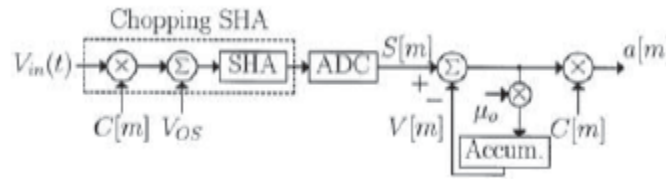


Figure 1 above shows a block diagram of a time-interleaved ADC including M ADCs in parallel, an analog demultiplexer at the input, and a digital multiplexer at the output. Ex. 1205, 7. During operation, the analog

¹ We cite to the page numbers inserted by Petitioner at the bottom of each page of Exhibit 1205.

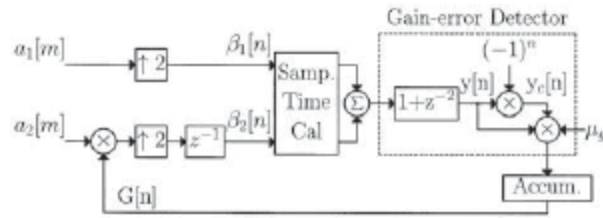
demultiplexer selects each channel in turn to process the analog input signal. *Id.* The digital multiplexer selects the digital output of the selected channel to form a high-speed ADC, where the overall sampling rate increases by a factor of M. *Id.* The performance of the interleaved ADCs, however, is sensitive to mismatches among the channels. *Id.*

Figure 3 of Jamal shows a block diagram of a signal channel that uses chopper-based offset calibration to correct the offset at the output of each ADC and is reproduced below. *Id.* at 8.



As shown in Figure 3 above, a chopping SHA (sample and hold amplifier) multiplies the analog input signal $V_{in}(t)$ by a pseudorandom binary signal $C[m]$, where m is a discrete time index. *Id.* $C[m]$ is white, has zero mean, and is uncorrelated with the input signal. *Id.* Together with V_{os} , the chopped analog signal is sampled and digitized by the ADC, producing signal $S[m]$. *Id.* The accumulator produces a variable offset $V[m]$ that is subtracted from the output $S[m]$ of the ADC, and to result is multiplied again by $C[m]$ to produce the channel output $a[m]$. *Id.* The combination of the accumulator and the summer forms a feedback loop that forces the average of the accumulator input to be zero, which results in canceling the offset of the channel. *Id.*

Jamal also discloses correcting gain mismatch between ADC channels using a gain calibration method shown in Figure 5, which is reproduced below. *Id.* at 8–9.



As shown in Figure 5 above, a gain-error detector and an accumulator produce a gain correction signal $G[n]$ based on signals $a_1[m]$ and $a_2[m]$ that represent the outputs of two ADC channels after offset calibration. *Id.* Gain correction signal $G[n]$ adjusts to be the ratio of G_1 to G_2 , which are the gains of two interleaved ADC channels, respectively. *Id.* The gain mismatch is corrected by multiplying the offset calibrated output signal $a_2[m]$ by gain correction signal $G[n]$, which makes the gain of each channel equal to G_1 . *Id.*

2. Analysis

Petitioner contends claims 1, 2, and 4–6 are anticipated by Jamal. Pet. 34–45. The preamble of claim 1 recites “[a] signal conditioning system.” Petitioner contends, to the extent the preamble is limiting, Figure 3 of Jamal describes this limitation in disclosing an ADC system that conditions an analog input signal to provide a digital output signal. Pet. 34–35 (citing Ex. 1205, 7–8; Ex. 1202 ¶ 123).

Claim 1 recites “a first converter.” Petitioner contends Jamal describes this limitation in disclosing an interleaved ADC system that includes a plurality of ADCs, where each ADC corresponds to the claimed “converter.” Pet. 35–36 (citing Ex. 1205, 7–8, Figs. 1, 3; Ex. 1202 ¶ 125).

Claim 1 recites “a random clock.” Petitioner contends Jamal describes this limitation in disclosing a pseudorandom binary signal $C[m]$. Pet. 36–37 (citing Ex. 1205, 8, Fig. 3; Ex. 1202 ¶¶ 127–129).

Claim 1 recites “said random clock configured to decorrelate an input signal provided to said first converter from said random clock so that the average output signal of said first converter is proportional to a first offset signal.” Petitioner contends Jamal describes this limitation in disclosing that the pseudorandom binary signal $C[m]$ is multiplied by the analog input signal $V_{in}(t)$, so that the resulting dc offset in output signal $S[m]$ is attributable to offsets present in the ADC and SHA. Pet. 38–39 (citing Ex. 1205, 7–8, Fig. 3; Ex. 1202 ¶¶ 132–134).

Claim 1 recites “a first offset sensor connected to sense the first offset signal, and in response to said sensing, to condition said first converter output.” Petitioner contends Jamal describes this limitation in disclosing an accumulator and a summer at the output of each ADC to estimate and correct the offset present at the output. Pet. 39–41 (citing Ex. 1205, 8, Fig. 3; Ex. 1202 ¶¶ 135–37).

Patent Owner contends that the chopping SHA shown in Figure 3 of Jamal is the only structure that operates on both the input signal provided to the converter and the signal $C[m]$, which Petitioner alleges corresponds to the claimed random clock. PO Resp. 22–23. Patent Owner contends that Jamal discloses that $C[m]$ “is uncorrelated with the input signal.” *Id.* at 24 (quoting Ex. 2205, 8). Patent Owner contends that applying the signal $C[m]$ to the input signal provided to the converter cannot decorrelate the input signal from the alleged random clock, because the alleged random clock is already decorrelated. Reply 9.

Petitioner contends that Patent Owner’s expert, Dr. Raychowdhury, testifies that Jamal discloses decorrelating the input from the random chopping sequence. Reply 6 (quoting Ex. 2206 ¶ 64). Petitioner also contends that Patent Owner’s infringement contentions in the district court

litigation contradict the positions taken in the PO Response. *Id.* at 7. In particular, Petitioner contends that Patent Owner's infringement contentions assert that the claimed "'random clock' can be satisfied by a 1-bit pseudo-random bit sequence." Pet. 36; Reply 7. Petitioner contends that Jamal meets all of the limitations of claim 1 because of the admission of Patent Owner's expert, and because of Patent Owner's infringement contentions. *Id.* at 9.

Dr. Raychowdhury testifies that, in Jamal's technique, "the input is de-correlated from the pseudo random chopping sequence." Ex. 2206 ¶ 64. Then, inexplicably, Dr. Raychowdhury testifies that "Jamal is unambiguous that ' $C[m]$ is white, has zero mean, and *is uncorrelated with the input signal.*'" *Id.* at ¶ 69. Patent Owner does not explain nor even address Dr. Raychowdhury's inconsistent testimony. Given the inconsistent positions taken by Patent Owner's expert, and the lack of explanation from Patent Owner, we give no weight to Dr. Raychowdhury's testimony.

Patent Owner contends that "Petitioner's reliance on one page of preliminary infringement contentions that have both already been supplemented and have not yet gone final is of no relevance." PO Sur-Reply 8. We disagree with Patent Owner and find that the preliminary infringement contentions are relevant at least because the '750 patent is asserted against Petitioner in the underlying litigation, the basis for which Patent Owner has initially alleged in the preliminary infringement contentions. The infringement contentions are also relevant because, under 35 U.S.C. §315(b), Petitioner may not have the luxury of waiting for Patent Owner's final infringement contentions to initiate this proceeding. However, neither Petitioner nor Dr. Holberg has explained why either the preliminary infringement contentions or Dr. Raychowdhury's inconsistent

testimony outweigh Jamal's disclosure that $C[m]$ is uncorrelated with the input signal.

Even were we to accept Petitioner's contention, that a "random clock" can be satisfied by a 1-bit pseudo-random bit sequence," (Pet. 36), Jamal discloses that the alleged random clock $C[m]$ "is uncorrelated with the input signal." Ex. 1205, 8. A chopping SHA multiplies the input signal and the uncorrelated random signal $C[m]$, then provides a chopped analog signal to the ADC converter. *Id.* Petitioner has not persuasively shown that chopping an input signal with an uncorrelated random signal, then providing the chopped signal to a converter as disclosed by Jamal, describes "said random clock configured to decorrelate an input signal provided to said first converter from said random clock" as recited in claim 1. We find that claim 1 is not unpatentable based on Jamal. Because claims 2 and 4–6 depend from claim 1, we find that these claims are also not unpatentable based on Jamal.

E. Asserted Obviousness over Jamal and Ferragina

1. Overview of Ferragina (Ex. 1207)

Ferragina discloses correcting offset mismatch in time interleaved ADCs. Ex. 1207, 6.² Ferragina discloses that "[t]he difference between the digital outputs of the path under calibration and the reference path is integrated over the calibration time slot NT_{CK} ." *Id.* at 7. "The result is a digital word proportional to the difference between the offsets of the two paths." *Id.* Thus, when the offset "is added to the output of the path under calibration, its overall offset becomes equal to the offset of the reference

² We cite to the page numbers inserted by Petitioner at the bottom of each page of Exhibit 1207.

path.” *Id.* at 8. According to Ferragina, “This procedure is repeated for the M paths” so that “all the M paths have the same overall offset of the reference path, thus avoiding spurious tones.” *Id.*

2. *Analysis*

Petitioner contends claims 7 and 8 are unpatentable as obvious over Elbornsson, Jamal, and Ferragina. Pet. 45–50. Claim 7 depends from claim 6, which depends from independent claim 1. Claim 8 depends from claim 6, which depends from claim 1. Petitioner does not contend that Ferragina teaches “said random clock configured to decorrelate an input signal provided to said first converter from said random clock” as recited in independent claim 1. Because the combination of Jamal and Ferragina does not teach “said random clock configured to decorrelate an input signal provided to said first converter from said random clock” as recited in claim 1, we find that claims 7 and 8 are not unpatentable over Jamal and Ferragina.

F. Asserted Obviousness over Elbornsson and Jamal

1. *Overview of Elbornsson (Ex. 1204)*

Elbornsson discloses a time interleaved ADC system to increase the sampling rate of the system. Ex. 1204, 3.³ Elbornsson discloses that a drawback of such a system is that the ADCs are not identical, due to errors in the manufacturing process, which means that time, gain, and offset mismatch errors are introduced into the system. *Id.* Elbornsson discloses decreasing the impact of mismatch errors by randomizing the order in which the ADCs are used. *Id.* Figure 3 of Elbornsson is reproduced below.

³ We cite to the page numbers inserted by Petitioner at the bottom of each page of Exhibit 1204.

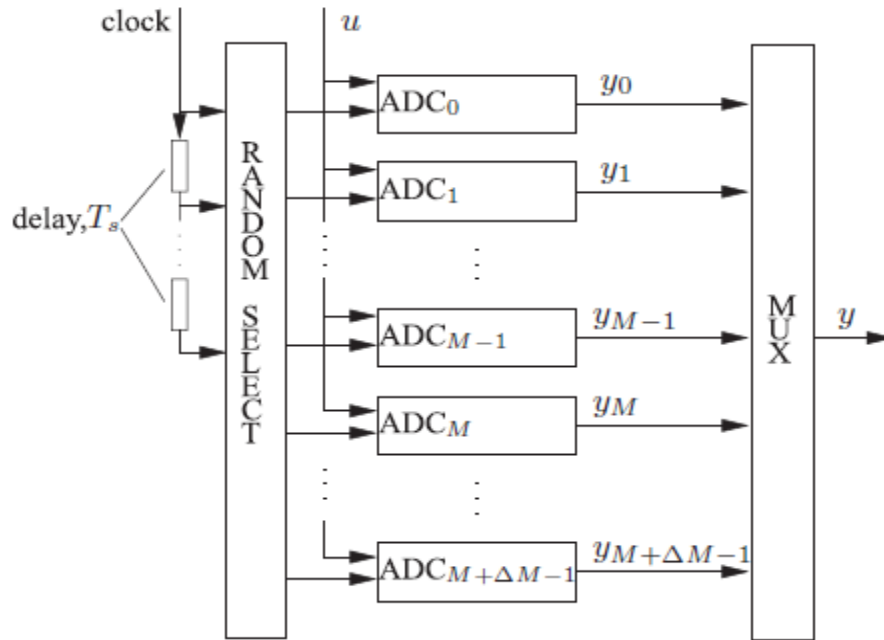


Figure 3 above shows a randomly interleaved ADC system including $M + \Delta M$ parallel ADC units having outputs coupled to a multiplexer.

Ex. 1204, 3–4. As shown in Figure 3, input signal u is connected to all ADCs. *Id.* at 3. Each ADC works with a sampling interval of MT_s , where M is the number of ADCs in the array and T_s is the sampling interval. *Id.* The i th ADC gives an output signal y_i . The output signals are multiplexed to form one output signal y . *Id.* The clock signal is delayed by delay blocks, each having a delay of T_s such that the clock signal to the i th ADC is delayed with iT_s , to give an overall sampling interval of T_s . *Id.* The impact of distortion is decreased by randomizing the selection of which ADC is used at each time instance. *Id.*

Elbornsson further discloses correcting the output signal from offset errors by subtracting an offset value of a given ADC from the output, or subsequence, of the ADC to yield an offset corrected output. *Id.* at 12. In order to correct the gain of each subsequence, Elbornsson discloses dividing

the offset corrected subsequence by the ratio of the average amplitude of the *i*th ADC to the average amplitude of all ADCs. *Id.*

2. *Analysis*

Petitioner contends that claim 12 is unpatentable over Elbornsson and Jamal. Pet. 50–66. Claim 12 depends from independent claim 10. The preamble of claim 10 recites “[a]n integrated circuit that converts between an analog signal and a corresponding digital code with a system sampling rate f_s .” Petitioner contends, to the extent the preamble is limiting, the combination of Elbornsson and Jamal teaches this limitation because “Elbornsson suggests implementing the ADC, random selection, and mismatch correction algorithms using an integrated circuit by mentioning non-idealities caused by a ‘manufacturing process,’” and Jamal discloses implementing time interleaved ADCs and an offset calibration system on an integrated circuit. Pet. 51–52 (citing Ex. 1204, 4, Fig. 3; Ex. 1205, 7–8, 13, Fig. 12).

Petitioner contends that implementing Elbornsson’s ADC system on an integrated circuit as disclosed by Jamal is the combination of familiar elements according to known methods that does no more than yield predictable results, uses a known technique to improve similar devices in the same way, and applies a known technique to a known device ready for improvement to yield predictable results. Pet. 53 (citing Ex. 1202 ¶¶ 182–187). Petitioner further contends that a person of ordinary skill in the art would have implemented Elbornsson’s offset and gain correction calibration algorithms on an integrated circuit for the benefit of making the overhead small enough to use the calibration algorithms in products as taught by Jamal. Pet. 53–54 (citing Ex. 1205, 13; Ex. 1202 ¶¶ 188–192).

Claim 10 recites “a plurality of converter circuits clocked by a random clock.” Petitioner contends Elbornsson discloses this limitation because Elbornsson discloses a plurality of converter circuits, each of which is randomly clocked by a random select block. Pet. 54–55 (citing Ex. 1204, 3–4, Fig. 3; Ex. 1202 ¶¶ 250–254).

Claim 10 recites “at least one converter circuit in said plurality of converter circuits sampling the analog signal at least every $1/f_s$ seconds.” Petitioner contends Elbornsson discloses this limitation because Elbornsson discloses an overall sampling interval of T_s . Pet. 55 (citing Ex. 1204, 3; Ex. 1202 ¶ 258). Dr. Holberg testifies that the sampling interval T_s is the reciprocal of the sampling rate f_s . Ex. 1202 ¶ 258. Dr. Holberg testifies that in order to support an overall sampling interval of $T_s = 1/f_s$ seconds, at least one ADC would need to sample the analog signal every $1/f_s$ seconds. *Id.*

Claim 10 recites “an offset sensing circuit configured to sense signal offsets and/or signal offset differentials between the outputs of said plurality of converter circuits.” Petitioner contends Elbornsson discloses estimating offset errors present at the output of each ADC. Pet. 56 (citing Ex. 1204, 4, 12; Ex. 1202 ¶¶ 259–264). Petitioner contends Jamal discloses an offset sensing circuit configured to sense signal offsets at the output of each ADC. Pet. 56–57 (citing Ex. 1205, 8, Fig. 3).

Petitioner contends that using Jamal’s offset correction in Elbornsson’s ADC system is the substitution of Jamal’s known plurality of offset correction circuits for Elbornsson’s known single correction circuit that yields the predictable benefits of correcting the offset for each channel and reducing the calculation needed to detect and correct the offset. Pet. 57–62 (citing Ex. 1202 ¶¶ 202–232).

Claim 12 recites “the sampling is provided by a sampling circuit clocked by said random clock to decorrelate the analog input signal from a random clock signal provided by said random clock.” Petitioner contends Jamal teaches this limitation in disclosing that the pseudorandom binary signal $C[m]$ is multiplied by the analog input signal $V_{in}(t)$, so that the resulting dc offset in output signal $S[m]$ is attributable to offsets present in the ADC and SHA, where the SHA is a bottom phase SHA that uses conventional non-overlapping clocks with two primary phases along with two extra phases to reduce the sample-to-hold transition error. Pet. 62–66 (citing Ex. 1205, 7–8, Figs. 3, 10).

Patent Owner contends that Petitioner has not shown that Elbornsson was published prior to the critical date of the ’750 patent, which is April 16, 2003. PO Resp. 49–61; PO Sur-Reply 17–21. Patent Owner contends that Petitioner provides no credible reason explaining why a person of ordinary skill would be motivated to modify Elbornsson’s system to add aspects of Jamal’s system. PO Resp. 62–66; PO Sur-Reply 21–24. Patent Owner contends that the proposed combination would render the combination unsatisfactory for its intended purpose, and would change Jamal’s principle of operation. PO Resp. 66–69; PO Sur-Reply 24–25. Patent Owner contends that Jamal expressly criticizes systems like Elbornsson’s which use extra sub-ADCs. PO Resp. 69–70. Patent Owner contends that Petitioner’s expectation of success is conclusory. PO Resp. 70–72; PO Sur-Reply 25.

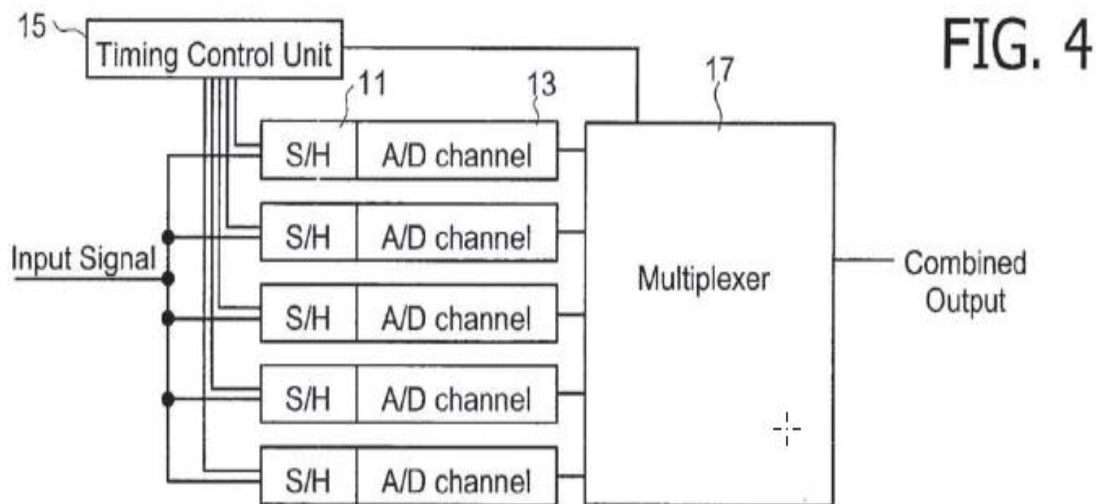
We addressed Patent Owner’s contentions in our Final Written Decision for IPR2020-01483, which was mailed the same day as this Decision. We disagree with Patent Owner for the reasons given in that Final Written Decision. We are persuaded that Elbornsson and Jamal teach all of the limitations of claim 12, and that a person of ordinary skill would have

combined the teachings of the references to achieve the integrated circuit recited in the claim and would have had a reasonable expectation of success in doing so. Dr. Holberg's testimony provides sufficient evidence of reasons that a person of ordinary skill would have used the teachings of Jamal within the interleaved ADC system of Elbornsson, and would have had a reasonable expectation of success in doing so. Petitioner has proven by a preponderance of the evidence that claim 12 would have been obvious over Elbornsson and Jamal.

G. Asserted Obviousness Over Eklund and Jamal

1. Overview of Eklund (Ex. 1206)

Eklund discloses a parallel analog-to-digital converter having random conversion sequencing. Ex. 1206, code (54). Figure 4 of Eklund shows a block diagram of a parallel ADC converter and is reproduced below. *Id.* at 3:13–14.



As shown in Figure 4 above, input analog signal V_s is sampled by sample and hold circuits 11, as controlled by clock signals from timing control unit 15. *Id.* at 3:30–35. The timing control unit can use a random number generator to control which circuit receives the clock signal. *Id.*

at 4:20–34. The clock signals are generated at a uniform rate to sample the analog input signal at periodically occurring times. *Id.* at 3:36–37. A/D channel 13 connected to a corresponding sample and hold circuit compares the sampled value to reference values, and delivers an output to multiplexer 17. *Id.* at 38–45.

2. *Analysis*

Petitioner contends claim 12 is unpatentable over Eklund and Jamal. Pet. 66–84. Claim 12 depends from claim 10. The preamble of claim 10 recites “[a]n integrated circuit that converts between an analog signal and a corresponding digital code with a system sampling rate f_s .” Petitioner contends, to the extent the preamble is limiting, the combination of Elbornsson and Jamal teaches this limitation because “Elbornsson suggests implementing the ADC, random selection, and mismatch correction algorithms using an integrated circuit by mentioning non-idealities caused by a ‘manufacturing process,’” and Jamal discloses implementing time interleaved ADCs and an offset calibration system on an integrated circuit. Pet. 51–52 (citing Ex. 1206, Figs. 1, 4, 1:11–15, 3:25–46; Ex. 1205, pp. 7–8, 13, Fig. 12).

Petitioner contends that implementing Eklund’s ADC system on an integrated circuit as disclosed by Jamal is the combination of familiar elements according to known methods that does no more than yield predictable results, uses a known technique to improve similar devices in the same way, and applies a known technique to a known device ready for improvement to yield predictable results. Pet. 69–70 (citing Ex. 1202 ¶¶ 279–289). Petitioner further contends that a person of ordinary skill in the art would have implemented Eklund’s offset and gain correction calibration algorithms on an integrated circuit for the benefit of making the

overhead small enough to use the calibration algorithms in products as taught by Jamal. Pet. 70–71 (citing Ex. 1205, p. 13; Ex. 1202 ¶¶ 290–294).

Claim 10 recites “a plurality of converter circuits clocked by a random clock.” Petitioner contends Elbornsson discloses this limitation because Elbornsson discloses a plurality of converter circuits, each of which is randomly clocked by a random clock. Pet. 71–73 (citing Ex. 1206, Figs. 4, 5, 3:29–36, 3:63–4:9).

Claim 10 recites “at least one converter circuit in said plurality of converter circuits sampling the analog signal at least every $1/f_s$ seconds.” Petitioner contends Eklund discloses this limitation because Eklund discloses at least one converter circuit that samples the analog signal at least every $1/f_s$ seconds. Pet. 73–74 (citing Ex. 1206, 3:25–4:5; Ex. 1202 ¶¶ 343–46).

Claim 10 recites “an offset sensing circuit configured to sense signal offsets and/or signal offset differentials between the outputs of said plurality of converter circuits.” Petitioner contends Jamal discloses an offset sensing circuit configured to sense signal offsets at the output of each ADC. Pet. 74–75 (citing Ex. 1205, 8, Fig. 3).

Petitioner contends that using Jamal’s offset correction circuit in Eklund’s interleaved ADC system is the combination of familiar elements according to known methods that yields the predictable benefit of reducing gain and offset mismatch in an interleaved ADC system, resulting in an improved SNDR. Pet. 75–80 (citing Ex. 1202 ¶¶ 295–325).

Claim 12 recites “the sampling is provided by a sampling circuit clocked by said random clock to decorrelate the analog input signal from a random clock signal provided by a random clock.”

Patent Owner contends that Petitioner does not explain why a person of ordinary skill would be motivated to modify Eklund's system to include aspects of Jamal's circuitry. PO Resp. 30–36; PO Sur-Reply 9–14. Patent Owner contends that the proposed combination would render the prior art unsatisfactory for its intended purpose and would change Jamal's principle of operation. PO Resp. 36–38; PO Sur-Reply 14–16. Patent Owner contends that Jamal expressly criticizes systems like Eklund which use extra sub-ADCs. PO Resp. 38–41; PO Sur-Reply 17.

We addressed Patent Owner's contentions in our Final Written Decision for IPR2020-01484, which was mailed the same day as this Decision. We disagree with Patent Owner for the reasons given in that Final Written Decision. We are persuaded that Eklund and Jamal teach all of the limitations of claim 12, and that a person of ordinary skill would have combined the teachings of the references to achieve the integrated circuit recited in the claim and would have had a reasonable expectation of success in doing so. Dr. Holberg's testimony provides sufficient evidence and persuasive reasoning explaining why a person of ordinary skill would have used the teachings of Jamal within the interleaved ADC system of Eklund, and would have had a reasonable expectation of success in doing so. For example, Dr. Holberg testifies that a person of ordinary skill in the art "would have appreciated that an interleaved ADC system could be implemented on an integrated circuit, as taught by Jamal, without changing the function of the interleaved ADC system." Ex. 1202 ¶ 284 (citing Ex. 1205, Section V, 1624–1626). By using an improved interleaved ADC system such as that taught by Jamal, Dr Holberg explains further that a "POSITA would have understood that this improvement could be applied to Eklund's interleaved ADC system in the same manner as it is applied to

Jamal’s interleaved ADC system, namely by implementing ADC circuitry on [a] chip.” *Id.* ¶ 286 (citing Ex. 1205, 1624). To support his testimony, Dr. Holberg relies on express teachings in Jamal, describing improvements where a “prototype consists of the two interleaved ADC channels but does not include the digital calibration circuits for simplicity . . . however, the area and power dissipation for the calibration circuit would scale to about 0.9 mm and 40 mW, making the overhead small enough to consider using these techniques in products.” *Id.* ¶ 282 (quoting Ex. 1205, 1624).

Considering all the evidence and arguments presented by the parties, we determine that Petitioner has proven by a preponderance of the evidence that claim 12 would have been obvious over Eklund and Jamal.

III. CONCLUSION

As summarized in the table below, the Petition and supporting evidence has not shown by a preponderance of the evidence that claims 1, 2, and 4–8, of the '750 patent are unpatentable, and has shown that claim 12 is unpatentable.⁴

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 4–6	102	Jamal		1, 2, 4–6
7, 8	103	Jamal, Ferragina		7, 8
12	103	Elbornsson, Jamal	12	
12	103	Eklund, Jamal	12	
Overall Outcome			12	1, 2, 4–8

⁴ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

Accordingly, it is:

ORDERED that claims 1, 2, and 4–8 of the '750 patent are not unpatentable;

FURTHER ORDERED that claim 12 of the '750 patent is unpatentable; and

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01564
Patent 6,900,750 B1

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