

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,  
Petitioner,

v.

ARBOR GLOBAL STRATEGIES, LLC,  
Patent Owner.

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IPR2020-01567<sup>1</sup>  
Patent 7,126,214 B2

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Before KARL D. EASTHOM, BARBARA A. BENOIT, and  
SHARON FENICK, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining All Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

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<sup>1</sup> Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00735 and has been joined as a party to IPR2020-01567.

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–6 and 26–31 (the “challenged claims”) of U.S. Patent No. 7,126,214 B2 (Ex. 1001, “the ’214 patent”). Pet. 1. Petitioner filed a Declaration of Paul Franzon, Ph.D. (Ex. 1002) with its Petition. Arbor Global Strategies LLC (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). We determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims, and on March 5, 2021, we instituted this proceeding as to all challenged claims and all grounds of unpatentability. Paper 13 (“Institution Decision” or “Inst. Dec.”).

After institution, Taiwan Semiconductor Manufacturing Co. Ltd. (“TSM”) filed a Petition seeking *inter partes* review of the claims challenged in this proceeding and a Motion for Joinder. IPR2021-00735, Papers 1, 3, 5.<sup>2</sup> We instituted an *inter partes* review in IPR2021-00735 and joined TSM as a party to this proceeding. Paper 20.

Subsequently, Patent Owner filed a Patent Owner Response (Paper 19, “PO Resp.”) and a declaration of Shukri Sourì, Ph.D. in support thereof (Ex. 2011); Petitioner filed a Reply (Paper 23, “Pet. Reply”) and a supplemental declaration of Dr. Franzon in support thereof (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 27, “PO Sur-reply”). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 33 (“Tr.”).

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<sup>2</sup> The petition in IPR2021-00735 (Paper 1) filed on April 5, 2021 was replaced by a corrected petition (Paper 5), which was accepted by the Board (Paper 7).

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

## I. BACKGROUND

### *A. Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies itself (Pet. 48) and TSM identifies itself and TSMC North America (IPR2021-00735, Paper 5, 48). Patent Owner identifies Arbor Global Strategies LLC. Papers 4, 1; 6, 1.

### *B. Related Proceedings*

The parties identify *Arbor Global Strategies LLC v. Xilinx, Inc.*, 1:19-cv-1986-MN (D. Del.) (filed October 18, 2019) as a related proceeding. *See* Pet. 48; Papers 4, 1; 6, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in three related patents, respectively IPR2020-01568 challenging U.S. Patent No. 7,282,951 (“the ’951 patent”), IPR2020-01570 challenging U.S. Patent No. RE42035, and IPR2020-01571 challenging U.S. the 6,781,226 patent. *See, e.g.*, Pet. 48. These three patents also have been challenged by a different petitioner in IPR2020-01020, IPR2020-01021 (“IPR-1021”), and IPR2020-01022. The joined party here (TSM) also was joined as a party to each of those proceedings.

### *C. The ’214 patent*

The ’214 patent describes a stack of integrated circuit (“IC”) die elements including a field programmable gate array (FPGA) on a die, a

memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. Ex. 1001, code (57), Fig. 4. According to the '214 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” Ex. 1001, code (57), Fig. 4.

Figure 4 follows:

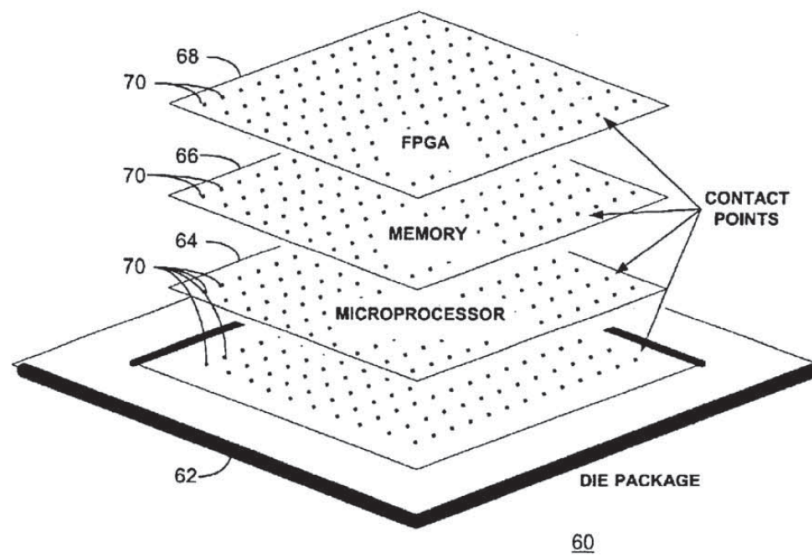


**Fig. 4**

Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using contact holes 70. Ex. 1001, 4:59–5:2.

The '214 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” See Ex. 1001, 1:23–39. Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA) making the processor faster than

one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See* Ex. 1001, 1:23–39. A “reconfigurable processor” provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See* Ex. 1001, 1:23–39.

#### *D. Illustrative Claim*

The Petition challenges claims 1–6 and 26–31, of which claims 1, 2, 26, and 27 are independent claims. Each of the challenged claims are directed toward a programmable array module. *See, e.g.*, Ex. 1001, 7:56 (independent claim 1), 8:2 (independent claim 2), 9:41 (independent claim 26), 9:52. Claim 1, reproduced below with bracketed numbering added for reference, illustrates the challenged claims at issue:

1. A programmable array module comprising:
  - [1.1] at least a first integrated circuit functional element including a field programmable gate array; and
  - [1.2] at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element
  - [1.3] wherein said field programmable gate array is programmable as a processing element, and
  - [1.4] wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.

Ex. 1001, 7:56–67.

Among the differences recited by the independent claims, independent claims 2 and 27 recite “said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout

the surfaces of said functional elements.” Ex. 1001, 8:1–15, 9:58–61. Independent claims 26 and 27 recite “wherein said memory array is functional to accelerate external memory references to said processing element.” Ex. 1001, 9:49–51, 10:2–4.

*E. The Asserted Grounds*

Petitioner challenges claims 1–6 and 26–31 of the ’214 patent on the following grounds (Pet. 1):

| Claims Challenged          | 35 U.S.C.<br>§   | References                                                             |
|----------------------------|------------------|------------------------------------------------------------------------|
| 1, 2, 4, 6, 26, 27, 29, 31 | 103 <sup>3</sup> | Zavracky <sup>4</sup> , Chiricescu <sup>5</sup> , Akasaka <sup>6</sup> |
| 3, 28                      | 103              | Zavracky, Chiricescu, Akasaka, Satoh <sup>7</sup>                      |

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<sup>3</sup> The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of institution, the ’214 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

<sup>4</sup> Zavracky, US 5,656,548, issued Aug. 12, 1997 (Ex. 1003).

<sup>5</sup> Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98 (Ex. 1004).

<sup>6</sup> Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Issue 12, pp. 1703–14, Dec. 1986, ISSN 0018-9219 (Ex. 1005).

<sup>7</sup> Satoh, PCT App. Pub. No. WO00/62339, published Oct. 19, 2000. (Ex. 1008 (English translation)).

| Claims Challenged | 35 U.S.C.<br>§ | References                                               |
|-------------------|----------------|----------------------------------------------------------|
| 5, 30             | 103            | Zavracky, Chiricescu,<br>Akasaka, Alexander <sup>8</sup> |

Petitioner contends that each of the asserted references is prior art to each of the challenged claims. Pet. 1–3.

## II. ANALYSIS

Petitioner challenges claims 1–6 and 26–31 as obvious based on the grounds listed above. Patent Owner disagrees.

### *A. Legal Standards*

To prevail in challenging Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e) (2012); 37 C.F.R. § 42.1(d) (2017). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied on).

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<sup>8</sup> Michael J. Alexander et al., *Three-Dimensional Field-Programmable Gate Arrays*, Proceedings of Eighth International Application Specific Integrated Circuits Conference, Sept. 1995 (Ex. 1009).

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.<sup>9</sup> See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

To demonstrate obviousness, “there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418. More specifically, Petitioner must demonstrate by a preponderance of evidence that “a skilled artisan would have had reason to combine the teaching of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success from doing so.” *PAR Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1193 (Fed. Cir. 2014).

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<sup>9</sup> No argument or evidence regarding secondary considerations has been presented in this proceeding.

*B. Level of Ordinary Skill in the Art*

The parties dispute the level of ordinary skill in the art. The level of ordinary skill in the art is “a prism or lens through which . . . the Board views the prior art and claimed invention” to prevent hindsight bias. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). In determining the level of ordinary skill, various factors may be considered, including the “types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovation are made; the sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation and citation omitted). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm’t, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Relying on the declaration testimony of Dr. Franzon, Petitioner contends that

[a] person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’214 patent would have been a person with a Bachelor’s Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication. Ex. 1002 ¶¶ 58–60.

Pet. 7 (citing Ex. 1002 ¶¶ 58–60).

Patent Owner asserts that

[a] person of ordinary skill in the art (“POSITA”) around December 5, 2001 (the earliest effective filing date of the ’214 Patent) would have had a Bachelor’s degree in Electrical Engineering or a related field, and either (1) two or more years

of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field. Sourl Decl., ¶ 25.

PO Resp. 8–9 (citing Ex. 2011 ¶ 25).

We adopt Petitioner’s proposed level of ordinary skill in the art as we did in the Institution Decision, which comports with the teachings of the ’214 patent and the asserted prior art. *See* Inst. Dec. 7. Patent Owner’s proposed level largely overlaps with Petitioner’s proposed level while lacking some specificity found in Petitioner’s proposed level. Even if we adopted Patent Owner’s proposed level, the outcome would remain the same. *See* Pet. Reply 1 (indicating Dr. Franzon confirmed his opinions under Patent Owner’s proposed level of ordinary skill).

### *C. Claim Construction*

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, which is the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

In its Petition, Petitioner did not provide an express construction for any claim term. Pet. 13. Nor did Patent Owner in either its Preliminary Response or its Response to the Petition. Prelim. Resp. 5; PO Resp. 9 (quoting 37 C.F.R. § 42.100(b)). In our Institution Decision, we agreed that no terms require explicit construction. Inst. Dec. 11–12 (citing Pet. 13; Prelim. Resp. 4, 5).

In that decision, we also noted and addressed the claim construction issue raised by Patent Owner in its Preliminary Response based on similar terms we construed in instituting trial in IPR-1021. Inst. Dec. 8–11. Specifically, Patent Owner argued the proper scope of the claim terms “said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element” recited in independent claims 1 and 2 and “said memory array is functional to accelerate external memory references to said processing element” recited in independent claims 26 and 27 (collectively, “the functional to accelerate” limitations). Inst. Dec. 8–11. We did not agree with Patent Owner’s arguments and noted that the instituted trial would afford both parties an opportunity for further briefing the issue. Inst. Dec. 10–11.

During trial, the parties have disputed the scope of the “the functional to accelerate” limitations in the context of the purported teachings of the prior art and in their respective Reply and Sur-reply. *See, e.g.*, PO Resp. 19, Pet. Reply 2–3; PO Sur-reply 1–2. Patent Owner contends that the plain language of the challenged claims requires “that a memory array is responsible for the claimed acceleration of data references.” PO Sur-reply 1. Each of the challenged independent claims recites “said memory array is functional to accelerate” either “reconfiguration of said field programmable

gate array as a processing element” (claims 1 and 2) or “external memory references to said processing element” (claims 26 and 27). Ex. 1001, 7:56–67 (claim 1), 8:1–15 (claim 2), 9:41–51 (claim 26), 10:2–4 (claim 27).

Patent Owner further contends that the structure within the memory array responsible for accelerating is the wide configuration data port disclosed in the ’214 patent. PO Resp. 19 (“Rather, as the claims themselves require, it is a structure provided *within the memory array* (i.e. the wide configuration data port disclosed in the ’214 Patent) that is responsible for accelerating the programmable array’s accelerated memory references.” (citing Ex. 2011 ¶ 53)); PO Sur-reply 2 (repeats statement that the wide configuration data port is the structure provided *within the memory array* that is responsible for the claimed acceleration (quoting PO Resp. 18–19)). Thus, Patent Owner equates (by using “i.e.”) the requisite structure within the memory array to be the wide configuration data port disclosed in the ’214 patent.

The challenged claims recite a function of the memory array and that that the memory array structurally is “stacked with and electrically coupled to” the FPGA. Ex. 1001, 7:59–60 (claim 1); *see also* Ex. 1001, 7:56–8:30 (claims 1, 2), 9:41–10:21 (claims 26, 27). None of the claims recite a wide configuration data port or any structure *within* the memory array.

For support, Patent Owner relies on Dr. Sourì’s declaration testimony. PO Resp. 19 (citing Ex. 2011 ¶ 53 (concluding that “it is the structure provided *within the memory array* (i.e. the wide configuration data port disclosed in the ’214 Patent) that is responsible for accelerating the programmable array’s accelerated external memory references”)). Prior to this conclusion, at the cited paragraph, Dr. Sourì quotes a passage from the

'214 patent specification, but that passage describes nothing about a memory array, and Dr. Souri provides no explanation for how he reaches this conclusory position. *See* Ex. 2011 ¶ 53 (quoting Ex. 1001, 5:16–26).

When explaining that position “[i]n more detail,” Dr. Souri describes a wide configuration data port as interconnecting the two elements of a memory die and a programmable array die. Ex. 2011 ¶ 54 (describing the inventors as solving the problem of “unacceptably long reconfiguration times” “*by stacking a memory die with a programmable array die*” and “*by interconnecting those two elements with a ‘wide configuration data port’ that employs through-silicon contacts, with the potential for even further acceleration where the memory die is ‘tri-ported.’*” (citing Ex. 1001, 5:16–26) (emphasis added here)). As such, Dr. Souri describes the wide configuration data port as *interconnecting a memory die and a programmable array die*. Although Dr. Souri describes the wide configuration data port as interconnecting two dies, Dr. Souri does not describe the wide configuration data port as being *within the memory array*. Because Dr. Souri does not adequately explain how a wide configuration data port *interconnecting a memory die* with another element shows a wide configuration data port *within a memory array*, we give little weight to Dr. Souri’s testimony that the claims require a wide configuration data port *within* the memory array.

The weight we accord Dr. Souri’s testimony in this regard is further supported by Patent Owner’s expert Krishnendu Chakrabarty, Ph.D. who indicates the very wide configuration data port shown in Figure 5 of the ’214

patent connects the memory die and FPGA die.<sup>10</sup> Ex. 1075, 157:23–158:7; Ex. 1075, 156:7–10<sup>11</sup>; *see* Ex. 1075, 163:8–21 (describing a data port as “just an interface to send data from one place to another” and a configuration data port as “just a data port used for configuration”); *see also* Pet. Reply 9 (quoting 1075, 157:23–158:3, 163:8–163:21). Patent Owner argues its own prior expert’s testimony contradicts the ’214 patent description of “the wide configuration data port *with buffer cells*.” PO Sur-reply 8 (citing Pet. Reply 9; Ex. 1001, 5:27–36) (emphasis added). For the reasons explained below, we do not agree that the ’214 patent requires a wide configuration data port *to include buffer cells* and so do not agree with Patent Owner that Dr. Chakrabarty’s description of a wide configuration data port contradicts the ’214 patent.

Furthermore, the disclosure of a wide configuration data port in Figure 5 of the ’214 patent does not support Patent Owner’s position that the claims require such a structure *within* the memory array. The ’214 patent depicts a “VERY WIDE CONFIGURATION DATA PORT 82” as a “black box” in Figure 5 and is not clear on its face how the wide configuration data port 82 in Figure 5 relates structurally to a memory die or memory array. Ex. 1001, 5:27–37, Fig. 5. Additionally, Figure 5 of the ’214 patent includes structures (specifically, buffer cells) described as preferably being within the

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<sup>10</sup> Dr. Chakrabarty is Patent Owner’s expert in the IPR2020-01020, IPR2020-01021, and IPR2020-01022 that challenge other patents of Patent Owner that have a substantially similar written description with regard to the cited portions of the ’214 patent. *See* IPR2020-01020, Ex. 1001, Figs. 4–5; IPR2020-01021, Ex. 1001, Figs. 4–5; IPR2020-01022, Ex. 1001, Figs. 4–5.

<sup>11</sup> “Q: So in this system [referencing Fig. 4], the configuration data port has wires that connect the memory die to the FPGA die. Right? A: Yes.”

memory die and structures (specifically logic cells) as being part of the FPGA. Thus, Figure 5 of the '214 patent does not depict the wide configuration data port 82 as being *within* a memory array.

Specifically, Figure 5 follows:

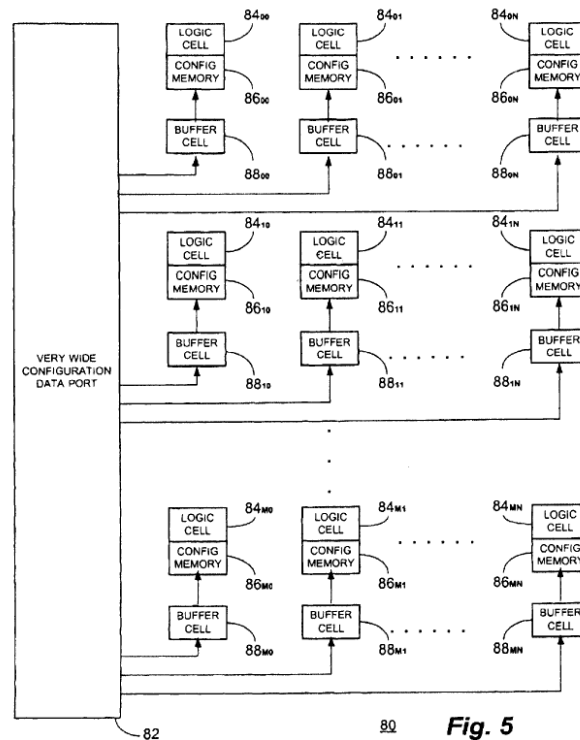


Figure 5 shows a very wide configuration data port 82 on the left side of the figure that is connected to each buffer cell depicted to the right of very wide configuration data port 82. *See* Ex. 1001, Fig. 5, 5:33–37. In turn, each buffer cell is connected to an associated configuration memory cell 86, which is adjacent to a logic cell 84. *See* Ex. 1001, Fig. 5, 5:33–37. The '214 patent indicates that “[t]he buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4)” but is silent as to the wide configuration data port’s structural relationship to the memory die. Figure 5, however, depicts very wide configuration data port 82 as being separate from the buffer cells. Moreover, the '214 patent indicates that “the FPGA 68 compris[es] the logic

cells 84,” which are depicted in Figure 5 as being separate from the very wide configuration data port 82. Ex. 1001, 5:38.

Therefore, the '214 patent in Figure 5 and its corresponding description do not describe the wide configuration data port as being within the memory array. Ex. 1001, Fig. 5, 5:27–47. To the extent the claims implicate any portion of a wide configuration data port, it is the numerous via connections associated with that port connected to a memory die that supports a “memory array [] functional to accelerate” data references. This is consistent with the testimony of Patent Owner’s experts Dr. Souri and Dr. Chakrabarty as outlined above.

Moreover, the '214 patent further indicates that Figure 5 is a “functional block diagram of the configuration cells” through which the FPGA 70 shown in Figure 4 is updated “in one clock cycle by updating all of the configuration cells in parallel.”<sup>12</sup> Ex. 1001, 5:27–33. Notably, the reconfigurable processor module 60 depicted in Figure 4 comprises “a die package 62 to which is coupled a microprocessor die 64, memory die 66 and FPGA die 68, all of which have a number of corresponding contact points,

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<sup>12</sup> The '214 patent specification also states that “[f]urther disclosed herein is an FPGA module that uses stacking techniques to combine it with a memory die for the purpose of accelerating FPGA reconfiguration.” Ex. 1001, 2:61–63. This, and other disclosures, indicate that reconfiguration may occur by using the significant number of vias of the stacking technique (i.e., without necessarily requiring any other structure of Figure 5’s wide configuration data port (whatever it is)). *See id.* at 5:41–47 (“Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory (“RAM” than can be offered within the FPGA die 68 itself.”)).

or holes 70 formed throughout the area of the package 62 and the various die 64, 66, and 68.” Ex. 1001, 4:64–5:2. Thus, even in the embodiment describing the wide configuration data port 82 as part of Figure 4’s reconfigurable processor module 60 that includes elements outside of memory die 66, the ’214 patent does not indicate the wide configuration data port 82 is within a memory array. A wide configuration data port is not otherwise described in the ’214 patent.

For these reasons, we find Figure 5’s depiction of the wide configuration data port 82 does not support Patent Owner’s position that a structure *within* the memory array is responsible for the recited acceleration.

In its Sur-reply, Patent Owner contends that the ’214 patent “describes that the memory array is functional to accelerate when it describes a wide configuration data port and ‘buffer cells 88 . . . a portion of memory die 66’ (a necessary part of the wide configuration data port) that is responsible for the acceleration of reconfiguration data to the field programmable gate array (‘FPGA’)[sic].” PO Sur-reply 1–2 (citing Ex. 1001, 5:32–41 (discussing Fig. 5)). The Patent Owner appears to be contending that the buffer cells 88 depicted in Figure 5 both (i) are a portion of memory die 66 and (ii) are a necessary part of the wide configuration data port. *See also* PO Resp. 21 (indicating the ’214 patent “discloses utilizing a portion of the memory array as a wide configuration data port including buffer cells” (citing Ex. 1001, 5:33–38)); Tr. 53:18–19 (Patent Owner confirming its position that “buffer cells are part of the wide configuration data port.”).

For the reasons discussed above, we do not agree that Figure 5 depicts the buffer cells as part of the wide configuration data port. The ’214 patent expressly describes the central purpose of the buffer cells: “*they can be*

*loaded while the FPGA 68 comprising the logic cells are in operation,”* which “then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration cells 84 updated in parallel.” Ex. 1001, 5:39–43 (emphasis added). None of the challenged claims, however, recite buffer cells or require that the recited FPGA be reconfigured while in operation.

Additionally, Patent Owner’s edited quotation omits the qualification that “[t]he buffer cells are *preferably* a portion of the memory die 66” shown in Figure 4, which further undermines Patent Owner’s position. Ex. 1001, 5:36–37. Additionally, the buffer cells are only “preferably a portion of the memory die 66” that enables loading the buffer cells while the logic cells are in operation. Ex. 1001, 5:36–39 (“The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68 comprising logic cells 84 are in operation.”). None of the challenged claims require loading the FPGA while it is in operation, which further undermines Patent Owner’s position.

In sum, the ’214 patent does not support Patent Owner’s contentions regarding the wide configuration data port.<sup>13</sup> Additionally, Patent Owner’s expert, Dr. Souri, describes a wide configuration data port as *interconnecting* “the two elements of a memory die and a programmable array die” rather than *being within* the memory array. Ex. 2011 ¶ 54. Moreover, Patent Owner appears elsewhere to describe the wide configuration data port as the

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<sup>13</sup> Moreover, during the Oral Hearing, Patent Owner’s counsel allowed for buffer cells being on the FPGA. Specifically, Patent Owner’s counsel argued that “when the buffer cells are on the FPGA, it then raises the question, okay, well, what’s on the memory array, right. And my answer would be probably more buffer cells.” Tr. 54:21–24.

“die-area interconnection arrangement with buffer cells,” which further supports that the wide configuration data port is not a structure provided within the memory array. PO Sur-reply 2 (“the novel die-area interconnection arrangement with buffer cells (i.e., wide configuration data port) allows the parallel loading of data from the memory die to the programmable array that is responsible for the claimed acceleration”).

Furthermore, the '214 patent consistently identifies acceleration with stacking techniques that include contacts throughout the stacked dies, without requiring other structure. For example, the abstract of the '214 patent describes a processor module “constructed by stacking one or more thinned microprocessor, memory and/or . . . FPGA die elements and interconnecting the same utilizing contacts that traverse the thickness of the die.” Ex. 1001, code (57). The abstract indicates that this processor module “allows for significant acceleration of the sharing of data between the microprocessor and the FPGA element. . . .” Ex. 1001, code (57). Notably, this description of “significant acceleration” does not include a wide configuration data port or buffer cells.

Additionally, the '214 patent similarly describes stacking techniques as accelerating the sharing of data between the microprocessor and the FPGA and accelerating external memory references, without referring to a wide configuration data port or buffer cells. *See* Ex. 1001, 2:64–66 (describing “a processor module with a reconfigurable capability that may include, for example, a microprocessor, memory and FPGA die stacked in a single block for the purpose of accelerating the sharing of data between the microprocessor and FPGA”), 2:64–66 (indicating “the FPGA module may employ stacking techniques to combine it with a memory die for the purpose

of accelerating external memory references”). The ’214 patent indicates that “[b]ecause the various die 64, 66 and 68 (FIG. 4) have very short electrical paths between them, the signal levels can be reduced while at the same time the interconnect clock speeds can be increased.” Ex. 1001, 5:50–53 (emphasis added). Similarly, “there is an added benefit of . . . increased operational bandwidth.” Ex. 1001, 5:48–50. Notably, the descriptions of shorter electrical paths, increased speed and bandwidth are due to the stacking techniques and are made within the context of Figure 4 without mention of Figure 5’s wide configuration data port and buffer cell embodiment. As noted above, even reconfiguration may occur without the specific wide configuration data port embodiment of Figure 5, for example, “[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68.” Ex. 1001, 5:41–45.

For these reasons, we conclude that the claims do not require a wide configuration data port (with or without buffer cells) *within a memory array* under the ordinary and customary meaning or otherwise.

*D. Asserted Obviousness of Claims 1, 2, 4, 6, 26, 27, 29, and 31*

Petitioner contends the subject matter of claims 1, 2, 4, 6, 26, 27, 29, and 31 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 1, 14–38. Patent Owner disputes Petitioner’s contentions. PO Resp. 18–39.

*1. Summaries of Zavracky, Chiricescu, and Akasaka*

*a. Disclosure of Zavracky*

Zavracky describes “a multi-layered structure” including a “microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure.” Ex. 1003, code (57). Zavracky’s “invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing.” *Id.* at 2:5–10. Zavracky includes numerous types of stacked elements, including “programmable logic devices” stacked with “memory” and “microprocessors.” *See id.* at 5:19–23.

Zavracky’s Figure 12 follows:

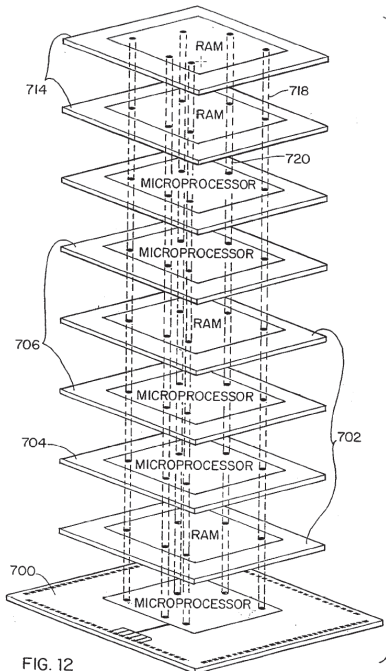


Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements

wherein “buses run vertically through the stack by the use of inter-layer connectors.” Ex. 1003, 12:24–26.

*b. Disclosure of Chiricescu*

Chiricescu describes a three-dimensional chip, comprising an FPGA, memory and routing layers. Ex. 1004, 232. Chiricescu’s FPGA includes a “layer of on-chip random access memory . . . to store configuration information.” *Id.* Chiricescu describes and cites the published patent application that corresponds to Zavracky as follows:

At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip [3].

See Ex. 1004,232, 235 (citing “[3] P. Zavracky, M. Zavracky, D-P Vu, and B. Dingle, ‘*Three Dimensional Processor using Transferred Thin Film Circuits*,’ US Patent Application # 08-531-177, allowed January 8, 1997”).<sup>14</sup>

Chiricescu describes “[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information.” Ex. 1004, 232. Chiricescu also describes using memory on-chip to “significantly improve[] the reconfiguration time,” explaining as follows:

The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

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<sup>14</sup> Zavracky lists the same four inventors and “Appl. No. 531,177,” which corresponds to the application number cited by Chiricescu.

*Id.* at 234.

Figure 2 of Chiricescu follows:

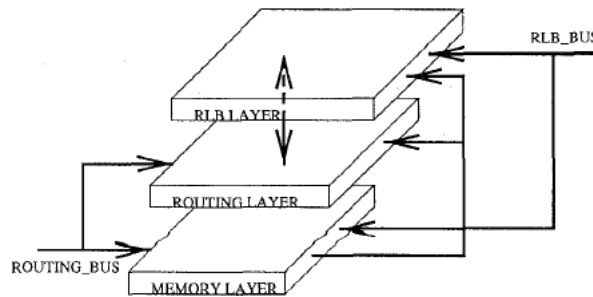


Figure 2. The layers of our 3-D FPGA architecture.

Figure 2 illustrates three layers in the 3D-FPGA architecture, with the RLB layer including routing and logic blocks in a “sea-of-gates FPGA architecture,” a routing layer, and the memory layer (to program the FPGA). *See* Ex. 1004, 232–33.

*c. Disclosure of Akasaka*

Akasaka generally describes trends in three-dimensional integrated stacked active layers. Ex. 1005, 1703.<sup>15</sup> Akasaka states that “tens of thousands of via holes” allow for parallel processing in stacked 3-D chips, and the “via holes in 3-D ICs” decrease the interconnection length between IC die elements so that “the signal processing speed of the system will be greatly improved.” Ex. 1005, 1705. Akasaka further explains that “high-speed performance is associated with shorter interconnection delay time and parallel processing” so that “twice the operating speed is possible in the best case of 3-D ICs.” Ex. 1005, 1705.

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<sup>15</sup> Petitioner refers to pages in Ex. 1005 using the page numbers in the original article (e.g., 1703–1714) rather than the page numbers of the exhibit itself (e.g., 1–23). For convenience we follow Petitioner’s practice of citing the page numbers of the original article.

Also, Akasaka discloses that “input and output circuits . . . consume high electrical power.” Ex. 1005, 1705. However, “a 10-layer 3-D IC needs only one set of I/O circuits,” so “power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs.” Ex. 1005, 1705.

Figure 4 of Akasaka follows:

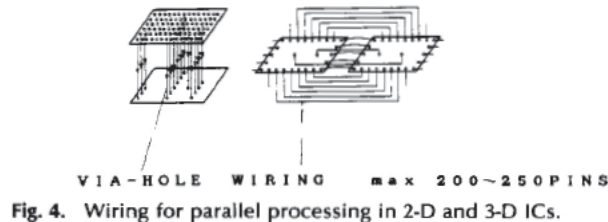


Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

## 2. *Petitioner’s Combination of Zavracky, Chiricescu, and Akasaka*

Before proceeding through a detailed analysis of Petitioner’s and Patent Owner’s respective arguments and evidence, we provide some general analysis regarding the limitations of the independent claims to provide context for our detailed analysis.

### a. *General Contentions Regarding Independent Claim Limitations*

In the main, Petitioner relies on Zavracky’s disclosure of a stack of functional circuit elements, including microprocessor and memory elements through which “buses run vertically through the stack by the use of inter-layer connectors.” Ex. 1003, 12:24–26. Petitioner points to Zavracky’s Figures 12 and 13 as disclosing a PLD (programmable logic device) and memory array in the stack as the recited first and second integrated circuit functional elements and the inter-layer connections (described as “via holes” or “contact holes”) as the electrical coupling between the elements. Pet. 23–

28 (citing, e.g., Ex. 1003, 9:45–45. 12:28–38, 2:1-7, 2:2–6, 5:19–23, 12:12–38, 6:48–50; 5:21–23, 12:33–36, Figs. 12, 13).

With regard to the recited FPGA, Petitioner provides evidence that one of ordinary skill in the art would understand that the PLD 802 at the bottom layer of the stack shown in Figure 13 was a field programmable gate array (FPGA) because a PLD was a type of FPGA. Pet. 24 (citing Ex. 1035, 1:29–30 (stating “a field programmable gate array (FPGA) 100, which is one type of PLD”); Ex. 1037, 1:13–22 (indicating “[o]ne type of PLD, the field programmable gate array (FPGA); Ex. 1038, Abstract (indicating a “programmable logic device (PLD), such as a field programmable gate array (FPGA)”). Petitioner also provides evidence that Zavracky’s programmable logic array (also called programmable logic device) 802 is programmable to provide a user-defined communication protocol and, as such, functions as a processing element, as required by the claims. Pet. 28 (citing Ex. 1002 ¶ 302 (citing Ex. 1003, 12:28–38; Ex. 1057, 57; Ex. 1040, 319)).

Petitioner relies on Chiricescu in its combination of Zavracky, Chiricescu, and Akasaka for teaching a memory layer to which configuration data from “off-chip memory” is loaded and from which Chiricescu’s FPGA can be reconfigured with that reconfiguration data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex. 1002 ¶¶ 304–07). Petitioner contends that Chiricescu’s memory layer accelerates reconfiguration of Chiricescu’s FPGA because reconfiguration data that has already been loaded into the memory array is used to reconfigure the FPGA. Pet. 30. In this way, as Petitioner indicates, Chiricescu addresses the “main bottleneck in the implementation of a high performance configurable computer machine

[which] is the high configuration time of an FPGA.” Ex. 1004, 232; *see* Pet. 29–30 (quoting ex. 1004, 232; citing Ex. 1002 ¶ 304–07).

As Petitioner indicates, Chiricescu describes “[t]he architecture of a 3-dimensional FPGA for reconfigurable computing machines” and this architecture “is based on a novel 3-D circuit technology developed at Northeastern University,” referring to Zavracky. Ex. 1004, 232 (Abstract), 235 n.3; Pet. Reply 13. Chiricescu specifically notes “[a]t Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip” and cites Zavracky for this technology. Ex. 1004, 232, 235 n.3.

Petitioner relies on Chiricescu to bolster Petitioner’s position relying on Zavracky for teaching or suggesting a programmable FPGA. Specifically, Petitioner relies on Chiricescu’s disclosure that one of its “key features” is “quickly reconfigur[ing]” its FPGA as a processing element to implement “arbitrary logic.” Petitioner provides evidence in the form of credible testimony by Dr. Franzon that Chiricescu shows reconfiguring an FPGA to perform multiplication. Pet. 29 (citing Ex. 1002 ¶ 303 (describing Ex. 1004, 234 (“FPGA is reconfigured from performing  $A \times B$  to  $A \times C$  or vice versa”) as providing an example of “the multiplication of a 4-bit variable”)).

Independent claim 2 additionally requires that the number of contact points (that electrically couple the first and second integrated circuit functional elements) be “distributed throughout the surfaces of said functional elements.” For this limitation, Petitioner relies on Zavracky’s express teaching that “openings or via holes” used for inter-layer

connections “can be placed anywhere on the die” of various functional elements, such that the connections “are not limited to placement on the outer periphery.” Pet. 32 (quoting Ex. 1003, 6:43–47, 13:43–46, 14:56–63). Petitioner bolsters its position by further relying on Akasaka’s disclosure of electrical coupling active layers in 3-D integrated circuits through “via holes” as shown in Akasaka’s Figure 4 and Akasaka’s statement that “[s]everal thousands or several tens of thousands of via holes are present in these devices.” Pet. 32 (quoting Ex. 1005, 1705).

In addition to contesting Petitioner’s reasons to combine the references, Patent Owner contests the “memory array functional to accelerate” limitations in each independent claim. Patent Owner throughout its briefing combines specific contentions with Petitioner’s contentions regarding “the memory array functional to accelerate” limitations with Patent Owner’s overly narrow interpretation—that the claims require a wide configuration data port as Patent Owner interprets Figure 5 of the ’214 patent to be and/or that the claims require buffer cells to be present in the wide configuration data port. For the reasons discussed previously in Section II.C (Claim Construction), we do not agree with Patent Owner’s position and so do not agree with Patent Owner’s many arguments that incorporate Patent Owner’s improperly narrow reading of the claims.

Many of Patent Owner’s arguments also apply to a misunderstanding of Petitioner’s combination. For example, Patent Owner seems unduly focus on Chiricescu’s data transfer when loading configuration data *into the memory cells*, whereas Petitioner’s combination relies on acceleration of reconfiguring the FPGA using configuration data that *has been* loaded into Chiricescu’s memory layer. Patent Owner’s arguments such as these that do

not address Petitioner's combination do not undermine Petitioner's combination.

Patent Owner also at times asserts that Dr. Franzon "admitted" something during his deposition testimony. As described below with respect to specific instances, we do not agree with Patent Owner's characterization where Patent Owner's arguments overgeneralize Dr. Franzon's testimony and do not sufficiently take into consideration the context of Dr. Franzon's testimony. For example, Patent Owner characterized Dr. Franzon's testimony discussing a prior art reference (Trimberger)<sup>16</sup> as "unequivocally stat[ing] that Petitioner's proposed combination was not feasible" and "admitting Chiricescu's 'RLB BUS' that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the '214 Patent." PO Sur-reply 14 (citing Ex. 2012, 71:19–72:1; PO Resp. 29); PO Sur-reply 19–20 (citing Ex. 2012, 80:10–22). We address Patent Owner's challenges to Dr. Franzon's testimony in detail below.

We now turn to addressing Petitioner's contentions and Patent Owner's arguments in detail.

*b. Petitioner's Reasons to Combine Zavracky, Chiricescu, and Akasaka*

In contending the subject matter of claims 1, 2, 4, 6, 26, 27, 29, and 31 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka, Petitioner provides reasons that one of ordinary skill in the art would have "integrate[d] the disclosures of Zavracky (including a stacked interconnected programmable 3-D module), Chiricescu (including

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<sup>16</sup> Ex. 1006 (Trimberger) has not been asserted in any of Petitioner's grounds in this proceeding.

accelerated FPGA reconfiguration using stacked memory), and Akasaka (including thousands of distributed interconnections).” Pet. 18; *see* Pet. 18–19 (citing Ex. 1002 ¶¶ 221–28 (citing Ex. 1004, 234; Ex. 1003, 5:65–66; Ex. 1020, 2; Ex. 1055 [0014]; Ex. 1040, 317)); Pet. 18–22 (discussing integrating Zavracky with Chiricescu and integrating Akasaka with Zavracky and Chiricescu). Petitioner also includes reasons one of ordinary skill in the art would have had a reasonable expectation of success. *See* Pet. 18–22; Pet. 20 (“With these understandings, [one of ordinary skill in the art] would have had a reasonable expectation of success in achieving the Zavracky-Chiricescu combination.”); Pet. 20–21 (One of ordinary skill in the art “would have expected success in the combination [] by knowing of successful similar prior art designs.”).

i) “[F]olding in” Chiricescu’s teachings (including using stacked memory to reconfigure the FPGA) with Zavracky’s 3D stacks

Relying on Dr. Franzon’s testimony, Petitioner contends that one of ordinary skill in the art would have “been encouraged to fold in Chiricescu’s teachings (including using stacked memory to reconfigure the FPGA) with Zavracky’s 3D stacks, understanding that it would lead to ‘significant[] improvement in the reconfiguration time.’” Pet. 18–19 (citing Ex. 1002 ¶ 212); Ex. 1002 ¶ 212 (quoting Ex. 1004, 234 (“The elimination of loading configuration data on an as needed basis from memory off-chip significant improves the reconfiguration time for an on-going application.”), ¶ 217 (testifying one of ordinary skill in the art “would readily recognize (because a cache is a building block of computer devices, and used in almost every processor on Earth) the ability to accelerate external memory references by ‘eliminat[ing] loading configuration data on an as needed basis’ would, as

Chiricescu teaches, ‘significant improves the reconfiguration time for an on-going application.’”). Petitioner points out that “Chiricescu, for example, explicitly references and uses the interconnections of Zavracky, as detailed in § VII.A.2” as another reason one of ordinary skill in the art would have folded in Chiricescu’s teaching with Zavracky’s 3D stacks. Pet. 18 (noting the explicit citation to and description of Zavracky in Chiricescu); Ex. 1002 ¶ 218 (explaining that (i) Chiricescu and the Zavracky inventors were in the same research group at a university and (ii) “Chiricescu describes and cites the Zavracky patent application in his paper on the first page” (citing Ex. 1004, 232)).

Based on Dr. Franzon’s declaration testimony, Petitioner also asserts that one of ordinary skill would have enhanced and expanded Zavracky’s programmable logic device within its co-stacked microprocessors and memories to include image and signal processing tasks as Chiricescu suggests by teaching the use of FPGAs to implement arbitrary logic functions. Pet. 19 (citing Ex. 1002 ¶¶ 229–30; Ex. 1005, 1705; Ex. 1003, 12:25–30; Ex. 1004, 232; Ex. 1058, 41; Ex. 1048); Ex. 1002 ¶ 229 (Dr. Franzon’s testifying that image and signal processing were recognized as good applications for 3-D stacked chips that required parallel computation, such as signal processing citing various references for support (including Ex. 1005, 1705; Ex. 1048; Ex. 1003, 12:25–30; Ex. 1004, 232; Ex. 1058, 41)).

Relying on Dr. Franzon’s declaration testimony, Petitioner contends that one of ordinary skill in the art would have had a reasonable expectation of success in making this combination because one of ordinary skill in the art “would have viewed Chiricescu with Zavracky as a routine

modification.” Pet. 20 (Ex. 1002 ¶¶ 231–32). Dr. Franzon’s opinion that the combination was a routine modification is supported by Dr. Franzon’s credible explanation that “Chiricescu would have actually just be[en] providing what Zavracky is generally describing when Zavracky states that in Figure 13, its programmable logic device ‘can be programmed to provide for user-defined communication protocol[s].’” Ex. 1002 ¶ 231.

Again relying on Dr. Franzon’s declaration testimony, Petitioner also contends that one of ordinary skill in the art “would have been familiar with other prior art processor modules including other microprocessor-FPGA-memory combinations.” Pet. 20 (Ex. 1002 ¶¶ 231–32 (citing Ex. 1026)). Dr. Franzon’s well-reasoned testimony is supported by evidence in the form of a reference “that performs exactly that stack” that was described in Dr. Franzon’s declaration testimony regarding background art known to one of ordinary skill in the art. Ex. 1002 ¶ 232 (citing Ex. 1026; referring to Ex. 1002 ¶¶ 125–28).

ii) Applying Akasaka’s Thousands of Distributed Contact Points

Relying on Dr. Franzon’s declaration testimony, Petitioner also contends that it was “a predictable advantage and also suggested by Akasaka itself that applying Akasaka’s distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity.” Pet. 20 (citing Ex. 1002 ¶ 233; Ex. 1005, 1705). Petitioner adds that “Zavracky and Chiricescu . . . invited such a combination.” Pet. 20 (citing Ex. 1003, 6:43–47 (“connections . . . can be placed anywhere on the die”); Ex. 1004, 232 (similar); Ex. 1020, 9). Petitioner further relies on Dr. Franzon’s testimony as follows:

[One of ordinary skill in the art] knew of the need for replicated “common data memory” in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence. Ex. 1002 ¶ 236 (citing Ex. 1034, 466–469; Ex. 1005, 1713 & Fig. 25). That structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky. Ex. 1002 ¶ 237. [One of ordinary skill in the art] thus would have been motivated to seek out Akasaka’s distributed contact points in order to build a “common data memory.” The POSITA’s background knowledge, including prior art successes, would have suggested success in this combination. *Id.* (citing Ex. 1005, Ex. 1021).

Pet. 21.

In his declaration testimony cited by Petitioner, Dr. Franzon further explains that the common data memory “still obtain[s] the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on a microprocessor, and cheaper than an ASIC).” Ex. 1002 ¶ 237. Dr. Franzon also explains that “the POSITA would have known that the more densely connected communication structure of Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack,” including multi-processor cache coherence. Ex. 1002 ¶ 236 (citing Ex. 1713, Fig. 25; Ex. 1034, 466–469).

Relying on Dr. Franzon’s declaration testimony, Petitioner contends that one of ordinary skill in the art would have had an expectation of success in making this combination because one of ordinary skill in the art “would have known many references teaching stacked functional-element dies with thousands of distributed connections, including” depicted stacks (e.g., Figure 4 in Exhibit 1020, Figure 9 in Exhibit 1028, and Figure 1(a) in Ex. 1021). Pet. 21 (referring to Pet. 8–10).

*c. Patent Owner's Contentions*

Patent Owner contends that Petitioner fails to provide the required articulated reasoning to support a conclusion of obviousness. PO Resp. 2–3, 23–39; PO Sur-reply 10–14.

(i) Alleged Misrepresentation of Chiricescu

First, Patent Owner contends that “Petitioner misrepresents Chiricescu to allege motivation to combine Zavracky and Chiricescu.” PO Resp. 24–25 (Section VI.A.3(a)). Patent Owner specifically asserts that Chiricescu does not employ Zavracky’s principles, does not utilize Zavracky’s principles to improve reconfiguration time, and “does not employ Zavracky’s die-area vertical interconnections to connect a memory die to an FPGA, and no die-area vertical is involved whatsoever in reconfiguring Chiricescu’s FPGA.” PO Resp. 24 (citing Pet. 18–19, Ex. 1004, 232 (Exhibit page 1), 234 (Exhibit page 3); Ex. 2011 ¶ 61<sup>17</sup>).

The record does not support this line of argument. Chiricescu’s Abstract indicates the paper describes “[t]he architecture of a 3-dimensional FPGA for reconfigurable computing machines” and “is based on a novel 3-D circuit technology developed at Northeastern University.” Ex. 1004, 232 (Abstract); *see* Pet. Reply 13. Chiricescu specifically notes “[a]t Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal

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<sup>17</sup> Dr. Sourì’s declaration testimony cited by Patent Owner (Ex. 2011 ¶ 61) is a single-sentence conclusion that provides no more reasoning than that included in the Patent Owner Response to the Petition (Paper 19).

interconnections (i.e., interlayer vias) placed anywhere on the chip” and citing Zavracky for this technology. Ex. 1004, 232, 235 n.3.

Moreover, Patent Owner unduly focuses on Chiricescu’s use of ‘on-chip’ memory to mitigate the time it takes to transfer configuration data from ‘off-chip’” and contends that Petitioner’s combination does not “mak[e] any use of Zavracky’s die-area vertical interconnections to transfer configuration data from the ‘on-chip’ memory into the FPGA.” PO Resp. 24 (citing Ex. 1004, 232, 234). Patent Owner also argues that “[n]either Zavracky nor Chiricescu even contemplate using die-area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 1, 2, 26, and 27.” PO Resp. 24 (citing Ex. 2011 ¶ 62); Ex. 2011 ¶ 62 (Dr. Sourì’s conclusory testimony that contains no more reasoning than in the Patent Owner’s Response).

The record does not support this line of argument. First, Petitioner’s combination focuses on Chiricescu for “using stacked memory to reconfigure the FPGA” (Pet. 18–19 (citing Ex. 1004, 232)). For example, Chiricescu discloses using 3-D layered FPGAs with interlayer vias and describes 3-D hierarchical interconnections between logic blocks as a feature. *See* Chiricescu, 232 (“Our architecture utilizes an extremely flexible 3-D hierarchical connection scheme in which the interconnections between logic blocks do not affect the use of logic resources. Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.”).

As discussed above, Zavracky’s Figure 13 shows that Zavracky contemplates moving data on vertical buses between RAM memory 808 (and RAM memory on processor layer 806) and programmable array 802

(Ex. 1003, 12:29–39), and Chiricescu’s Figure 2 shows that Chiricescu contemplates moving data on “vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip” (based on Chiricescu’s characterization of Zavracky) between memory layer and the “sea of gates FPGA” RLB layer (Ex. 1004, 232); *see also* Ex. 1004, 232 § 1 (“Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.”).

Also, Petitioner shows persuasively one of ordinary skill in the art would have recognized that speed improvement emanates partly from shorter interconnection distances and/or parallel processing using a larger number of vias (as compared to connections on the same plane). *See* Reply 6 (arguing Zavracky’s “approach **accelerates** communication between the dies in the chip by way of ‘**smaller delays** and **higher speed** circuit performance’” (emphasis by Petitioner (quoting Ex. 1003, 3:4–14)), and arguing that “Zavracky’s short interior ‘inter-layer connectors’ to stacked ‘random access memory . . . results in reduced memory access time, **increasing the speed** of the entire system.’ (emphasis by Petitioner (quoting Ex. 1003, 11:63–12:2)).

Nor do we agree with Patent Owner’s contention that, “because Chiricescu discloses that the configuration data is stored in on-chip memory, the approach of Zavracky-Chiricescu would result in a structure in which data is removed from the microprocessor cache and placed in the FPGA’s on-chip memory, making it **much harder** for the microprocessor to access memory given that the same type of slow front side bus distinguished in the ’214 Patent would be required for the microprocessor to access the FPGA’s on-chip memory, [which would] result in significantly **decreased** processing

speeds . . . , thus not leading to an improvement in the reconfiguration time.” PO Resp. 24–25 (citing Ex. 2011 ¶ 63) (emphasis in PO Resp.); Ex. 2011 ¶ 63 (Dr. Sourì’s testimony contains no additional reasoning than that in the Patent Owner’s Response). Petitioner’s combination “folding in” Chiricescu’s teaching does not require configuration data to be stored in on-chip memory, and so Patent Owner’s contentions do not address Petitioner’s combination.

Moreover, neither Petitioner nor Dr. Sourì sufficiently consider Petitioner’s more general showing, based on Dr. Franzon’s declaration testimony, that one of ordinary skill in the art “would have recognized that the more densely connected communication structure of Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack.” Pet. 21 (citing Ex. 1002 ¶ 236 (citing Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25)).

On balance, we find Dr. Franzon’s testimony in this regard more credible than Dr. Sourì’s testimony. Dr. Franzon’s testimony is based on specific descriptions of references consistent with his opinion, whereas Dr. Sourì’s testimony does not provide evidentiary support.

For these reasons, we do not agree with Patent Owner’s position that Petitioner “misrepresents Chiricescu” and so does not provide articulated reasoning to support a conclusion of obviousness.

(ii) Motivation Alleged to Be Untethered to Claims

Second, Patent Owner also contends that Petitioner’s alleged motivation to combine Zavracky and Chiricescu “is untethered to the challenged claims.”<sup>18</sup> PO Resp. 25–26 (Section VI.A.3(b)). Patent Owner

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<sup>18</sup> We understand Patent Owner’s “untethered” argument to challenge Petitioner’s showing as to why “a skilled artisan would have had reason to

specifically argues that Petitioner does not provide motivation to combine Zavracky and Chiricescu “to reach a memory array functional to accelerate an external memory reference[] or accelerate the reconfiguration of a programmable array, as claimed.” PO Resp. 25–26 (citing Ex. 2011 ¶ 64).

The record does not support this line of argument. Petitioner tethers its argued reasons to combine to accelerating external memory references and reconfiguration of a programmable array. For example, Petitioner asserted that one of ordinary skill would have combined “Chiricescu’s teachings (including using stacked memory to reconfigure the FPGA) with Zavracky’s 3D stacks, understanding that it would lead to ‘significant[] improvement in reconfiguration time.’” Pet. 18 (citing Ex. 1002 ¶¶ 221–28 (citing Ex. 1004, 234; Ex. 1003, 5:65–660; Ex. 1020, 2; Ex. 1055 [0014]; Ex. 1040, 317)); Pet. Reply 14 (citing Pet. 18). Similarly, Chiricescu’s technology that acts like cache memory for reconfiguration data results in accelerated access to external memory references (Pet. 30) likewise is tethered to the claimed acceleration provided by Chiricescu’s technology to reconfigure the FPGA. Pet. 18–19; *see* Pet. Reply 14–15.

In addition, Petitioner discusses in the context of the programmability of an FPGA recited in each of the challenged claims. As such, and in contrast to Patent Owner’s assertion that “Petitioner fails to articulate any reason that Chiricescu’s alleged teaching of performing ‘arbitrary logic functions’ is related to the claimed invention,” (PO Resp. 26), Petitioner tethers the description one of Chiricescu’s “‘key features’ is that its FPGA can be ‘quickly reconfigured’ to implement ‘arbitrary logic’” to the recited

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combine the teaching of the prior art references to achieve the claimed invention.” *PAR Pharm.*, 773 F.3d at 1193.

limitation that “said field programmable gate array is programmable as a processing element.” Pet. 28–29. Thus, Petitioner’s position that one of ordinary skill in the art “would have taken Chiricescu’s suggestion of a FPGA to perform ‘arbitrary logic functions’” as a reason to combine the references is tethered to claim language. *See* Pet. 19.

(iii) Alleged Major Modifications

Third, Patent Owner contends that Petitioner’s alleged motivation to combine Zavracky and Chiricescu “requires major modifications.” PO Resp. 26–29 (Section VI.A.3(c)). Patent Owner argues that Chiricescu’s narrow data port, the lack “of the type of wide configuration data port responsible for the accelerating features of the challenged claims,” “or to arrange a microprocessor and programmable array such that the two components share data” would necessitate major modifications beyond the level of ordinary skill and neither Zavracky or Chiricescu discloses a structure—“a memory array that achieves the claimed acceleration (i.e. utilizing a portion of the wide configuration data port)” in the ’214 patent—to address the problem of reducing the amount of time to move data from a memory die to the programmable array. PO Resp. 28 (citing Ex. 2011 ¶ 68). Dr. Souri explains that the major modification to configure a stacked module to meet the acceleration limitations of the claims requires a “wide configuration data port between the memory and the FPGA” and that such a modification would alter Chiricescu’s principle operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB Bus and its ‘routing layer,’ which Chiricescu declares ‘is of critical importance since it is used for the implementation of the

interconnection of the non-neighboring RLBs.” Ex. 2011 ¶ 67 (citing Ex. 1004, 233 (page 2 of exhibit); *see* PO Resp. 27.

As discussed previously (in Section II.C), however, the ’214 patent in Figure 5 does not support Patent Owner’s contentions that the claims require such a structure *within* the memory array. *See, e.g.*, PO Resp. 19. The ’214 patent describes the vertical contacts distributed throughout the surface (“vias”) to allow multiple short paths for data transfer between the memory and processing element. As Petitioner also persuasively argues, no “‘modifications’ are required to Chiricescu at all because the Petition’s combination involves ‘fold[ing] in Chiricescu’s teachings (including using stacked memory to reconfigure[] the FPGA) with Zavracky’s 3D stacks.” Pet. Reply 15 (quoting Pet. 17–18).

Moreover, even if employing Chiricescu’s FPGA structure also suggests implementing its routing layer on a separate layer, Chiricescu does not describe its routing layer as a narrow port, contrary to Patent Owner’s arguments. Pet. Reply 15–16 (noting that Dr. Franzon did not admit Chiricescu includes a narrow port and citing Dr. Franzon’s testimony that on-chip area-wide connections in 3D stacks were well-known (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68; Ex. 1020)); *see also* Ex. 1004, 232, Fig. 2 (depicting connections between the memory layer, routing layer, and RLB layer (a “sea-of-gates FGPA structure”) with connections that are distinct from the RLB bus); Ex. 1004, 232 (noting that “routing congestion will also be improved by the separation of layers,” further suggesting that the routing layer is not part of a narrow port). In addition, Petitioner indicates that “Chiricescu describes ‘vertical metal interconnections (i.e., interlayer vias),’ and **‘three separate layers with metal interconnects**

**between them.”** Pet. Reply 13 (citing Ex. 1004, 232). Ciricescu’s “architecture is based on technology developed by Zavracky at Northeastern University.” Pet. Reply 13 (quoting Ex. 1004, 232). And Ciricescu states that Zavracky’s architecture provides “3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) *placed anywhere* on the chip.” Ex. 1004, 232 (emphasis added). For these reasons, the record does not support a conclusion that Chiricescu’s principle of operation does not require a narrow port, contrary to Patent Owner’s arguments.

(iv) Akasaka and Common Data Memory

Fourth, Patent Owner further contends that “Akasaka exacerbates the problems with Petitioner’s obviousness combination.” PO Resp. 29–33 (Section VI.A.3(d)). According to Patent Owner, “Akasaka’s only relevant disclosure is the ‘common data memory’ concept involved in the Petition, which does not disclose data shared between any processors” but “discloses that each processor in the stack accesses only the memory *in its own layer*.” PO Resp. 30 (citing Ex. 1005, 11, Fig. 11; Ex. 2011 ¶ 71).

The record does not support this line of argument. Petitioner’s combination relies on Akasaka for teaching “thousands of distributed interconnections.” Pet. 18; *see also* Pet. 17–18 (overview of Akasaka). Petitioner uses Akasaka’s common data layer to provide a reason that one of ordinary skill in the art would have used Akasaka’s “thousands of distributed interconnections” in Petitioner’s combination of Zavracky-Chiricescu that includes Zavracky’s three-dimensional circuits electrically connected by via holes. Pet. 21; *see, e.g.*, Pet. 26–27 (citing Ex. 1003, 14:51–63, Figs. 12–13).

More specifically, relying on Dr. Franzon’s declaration testimony, Petitioner contends that one of ordinary skill in the art would have known

“of the need for replicated ‘common data memory’ in stacked designs, including as taught in Akasaka, to enable, e.g., multiprocessor cache coherence.” Pet. 21 (citing Ex. 1002 ¶ 236 (citing Ex. 1034, 466–69; Ex. 1005, 1713, Fig. 25)).

Dr. Franzon explains that particular technique (“Write Broadcast”) ensures multi-processor cache coherency by “broadcast[ing] the new data over the bus [so that] all copies are updated with the new value.” Ex. 1002 ¶ 236 (citing Ex. 1034, 466–69 (computer architecture text book)).

Dr. Franzon relates this known technique for ensuring multi-processor cache coherency to keeping replicated ‘common data memory’ in stacked designs consistent. Dr. Franzon points to Akasaka’s Figure 25 as illustrating such a broadcast technique to keep the memory data in each independent layer consistent. Ex. 1002 ¶ 236 (discussing Ex. 1005, Fig. 25, 1713).

Dr. Franzon further explains that Akasaka’s Figure 25 structure implementing the broadcast technique “would be difficult in the design to accomplish with just a limited number of interconnections between dies n Zavracky and certainly would be improved by Akasaka’s distributed connections teaching.” Ex. 1002 ¶ 237. This explanation supports Dr. Franzon’s opinion that one of ordinary skill in the art “would have been motivated to seek out Akasaka’s distributed contact points in order to build a ‘common data memory,’ as taught in Akasaka, while still obtaining the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on the microprocessor, and cheaper than an ASIC.” Ex. 1002 ¶ 237.

As such, Dr. Franzon’s explanation of broadcast techniques to enable ‘common data memory’ consistency provides a reason that one of ordinary

skill in the art would include Akasaka's thousands of distributed interconnections (not just the smaller number taught by Zavracky) in Petitioner's combination of Zavracky, Chiricescu, and Akasaka. We do not understand Petitioner's position to require bodily incorporation of Akasaka's Figure 25 into Petitioner's Zavracky-Chiricescu combination, as Patent Owner seems to suggest. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012). "What matters in the § 103 nonobviousness determination is whether a person of ordinary skill in the art, having all the teachings of the references before him, is able to produce the structure defined by the claim." *Orthopedic Equip. Co., Inc. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983). Rather, we understand Petitioner's position to be that one of ordinary skill in the art would included Akasaka's thousands of distributed interconnections, motivated in part by Akasaka's Figure 25 illustration of keeping a common data memory consistent by parallel transfer of data.

Furthermore, Petitioner relies on Dr. Franzon's testimony that accomplishing the "common data memory" desirable for "multi-processor cache coherence" "would be more difficult to accomplish with a limited number of interconnections as in Zavracky." Pet. 21 (citing Ex. 1002 ¶ 237).

For these reasons, we do not agree with Patent Owner's arguments that "Akasaka exacerbates the problems with Petitioner's obviousness combination." PO Resp. 29–33.

Moreover, Petitioner provides a second independent reason that one of ordinary skill in the art would have had to apply Akasaka's distributed contact points in the 3D stacks of Zavracky or Chiricescu. Petitioner points to advantages "suggested by Akasaka" that using Akasaka's distributed contact points "would increase bandwidth and processing speed through better parallelism and increased connectivity in the stack of Zavracky. Pet. 20 (citing Ex. 1002 ¶ 233 (quoting Ex. 1005, 1705); *see also* Pet. 17–18 (describing Akasaka's benefits). Petitioner relies on Dr. Franzon's declaration testimony that one of ordinary skill in the art would have recognized these benefits and "would have sought out Akasaka's connectivity to improve Zavracky's stacks in applications requiring parallel processing," such as image processing. Pet. 20 (citing Ex. 1002 ¶¶ 233, 235; Ex. 1005, 1705, citing Ex. 1003, 6:43–47; Ex. 1004, 232, Ex. 1020, 9). We find Dr. Franzon's testimony in this regard to provide persuasive explanation and analysis that relies on quotations of specific passages that support his testimony. *See* Ex. 1002 ¶ 233 (explaining two reasons one of ordinary skill in the art would have combined Akasaka's distributed contact points with Petitioner's combination of Zavracky-Chiricescu: "increased parallelism (e.g., the ability . . . to move and process data simultaneously) and increased connectivity (e.g., the ability to access various parts of the chip directly"); quoting Ex. 1005, 1705 (Akasaka identifying benefits); reproducing Ex. 1005, Fig. 4 (titled "Wiring for parallel processing in 2-D and 3-D ICs and depicting "via-hole wiring").

(v) Alleged Lack of Reasonable Expectation of Success

Fifth, Patent Owner contends that "Petitioner fails to demonstrate how [one of ordinary skill in the art] would have integrated Akasaka's thousands

of via interconnects with Zavracky-Chiricescu's design and circuitry with a reasonable expectation of success." PO Resp. 33 (Section VI.A.3(e)).

Regarding Patent Owner's arguments, first, we do not agree with Patent Owner's characterization of Dr. Franzon and Petitioner's analysis that one of ordinary skill in the art "would have understood the references *could be* combined" and, as such, fail to provide the requisite articulate reason to support a conclusion of obviousness. PO Resp. 36. Rather, Petitioner and Dr. Franzon provides specific reasons why one of ordinary skill in the art *would have* combined the references in the manner proposed by Petitioner. *See* Pet. 18–22 (repeatedly stating "would have been motivated"; "would have been encouraged to"; "would have taken"; "would have recognized"); *see also* Pet. Reply 17 (Petitioner indicating that it did not make a "could be combined" argument).

Turning back to Patent Owner's assertion that Petitioner fails to demonstrate that one of ordinary skill in the art would have a reasonable expectation of success to integrate Akasaka's thousands of via interconnects with Petitioner's combination of Zavracky-Chiricescu (PO Resp. 33–34) and Patent Owner's contention that Petitioner "failed to 'account for a single one of [the alleged] problems' related to TSV (through-silicon vias) interconnections." Petitioner characterizes these issues as "at most normal engineering issues, not problems preventing a combination." Pet. Reply 17 (alteration in Reply). We note, as discussed above, that Petitioner relies on Dr. Franzon's testimony that accomplishing the "common data memory" desirable for "multi-processor cache coherence" "would be more difficult to accomplish with a limited number of interconnections as in Zavracky" than

in using Akasaka's thousands of via interconnects. Pet. 21 (citing Ex. 1002 ¶ 237).

Furthermore, Petitioner relies on Dr. Franzon's testimony that one of ordinary skill in the art's "background knowledge, including prior art successes, would have suggested success in this combination." Pet. 21 (citing Ex. 1002 ¶ 237 (citing Ex. 1005, Ex. 1021, 18)). In addition to Akasaka's description, Dr. Franzon identifies a 1998 IEEE article that, according to Dr. Franzon, describes a "large number of interconnects to SRAMs and DRAMs. Ex. 1002 ¶ 237 (citing Ex. 1021, 18 as "describing the large number of interconnects to SRAMs and DRAMs"). We credit Dr. Franzon's testimony based on additional evidence of what one of ordinary skill in the art would understand. We also note that generally it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse."). Here the level of ordinary skill is a Bachelor's Degree in Electrical Engineering, with at least two years of industry experience. This further supports that one of ordinary skill in the art would have an expectation of success based on prior art successes of implementing a large number of interconnects to connect well-known circuits together such as FPGAs, microprocessor, and memories.

Additionally, many of Patent Owner's arguments seem to suggest bodily incorporation is required and must be explained for Petitioner to prevail. For example, Patent Owner asserts "Petitioner and Dr. Franzon's analysis wholly fails to provide any explanation whatsoever as to how

Akasaka's thousands of via interconnections would be laid out, connected to, and operate with the various functional blocks of Zavracky-Chiricescu 3-D device circuitry, and therefore necessarily would work." PO Resp. 38.

In another example, Patent Owner asserts that

[a]t the time of the invention, a POSITA was aware of numerous TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ("HDL") algorithms, which must be considered. Souri Decl., ¶ 78; Ex. 2014 at 85, 87, 89.

Petitioner's combination does not account for a single one of these problems, let alone demonstrate that they could have been solved by a POSITA at the time of the invention with a reasonable expectation of success.

PO Resp. 37.

To the extent that Patent Owner supports its position with a suggestion that bodily incorporation is required, we do not agree with such arguments by Patent Owner. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012). "What matters in the § 103 nonobviousness determination is whether a person of ordinary skill in the art, having all the teachings of the references before him, is able to produce the structure defined by the claim."

Nor do we agree with Patent Owner's characterization of Dr. Franzon's testimony as "unequivocally stat[ing] that Petitioner's proposed combination was not feasible." PO Sur-reply 14 (citing Ex. 2012, 71:19–72:1; PO Resp. 29). Rather, Dr. Franzon's testimony indicated that *off-chip access* to a wide configuration data port 100,000 bits wide was not feasible. He testified

one of ordinary skill in the art “would understand that you have an off-chip access to this wide configuration data port. That off-chip access can’t be, for example, 100,000 bits wide. For practical reasons you can’t have that number of IO. And this is both in the case of Trimberger and [the challenged patent], memory going from the external to the module.

Ex. 2012, 71:19–72:1.

This testimony relates to the previous discussion about using narrow ports to load configuration information, as in Chiricescu, and does not address the feasibility of using such pre-loaded configuration information to reconfigure a FPGA or accelerate external references to memory, both of which happen in the stack using the short vias that connect the layers in the stack. Here again, Patent Owner conflates the loading of the stack with configuration information with the claimed elements—including the memory array functional to accelerate reconfiguration of a FPGA as a processing element (independent claims 1 and 2) or the memory array functional to accelerate external memory references to said processing element (independent claims 26 and 27).

### *3. Independent Claims 1, 2, 26, and 27*

Turning to the independent claims 1, 2, 26, and 27, Petitioner presents various arguments and evidences regarding the prior art purported teaching or suggesting the claimed elements. *See, e.g.*, Pet. 22–33, 36–38.

#### *a. Undisputed Limitations of Independent Claims 1, 2, 26, and 27*

Claim 1 recites “[a] programmable array module comprising” various elements. Petitioner contends that one of ordinary skill in the art would have understood Zavracky to be describing a programmable array module from Zavracky’s disclosure of (i) “a common module body to perform a combined

function,” (ii) a module based on “programmable logic array 802,” and (iii) its invention as relating to “the structure [of] vertically stacked and interconnected circuit elements for. . . programmable computing.” *See* Pet. 22 (relying on Ex. 1003, 9:42–45, 12:28–38, 2:1–7, Fig. 13; citing Ex. 1002 ¶¶ 282–86). Petitioner further argues that the combination of Zavracky and Chiricescu’s “system where the focus of the 3D module is on a FPGA and a memory designed to accelerate external references . . . to the FPGA” “provid[es] a programmable array module,” relying on FPGA as a programmable array. Pet. 22–23 (citing Ex. 1004, 234).

Petitioner contends that Zavracky discloses “at least a first integrated circuit functional element including a field programmable gate array” (limitation [1.1]). Pet. 23–26. Petitioner relies on Zavracky’s Figure 12 as disclosing “layers that comprise integrated circuit functional elements” that perform specific functions, including being a memory or microprocessor. Pet. 23 (citing Ex. 1003, 2:2–6, 5:19–23, Fig. 12). Petitioner further relies on Zavracky’s Figure 13 as disclosing an integrated circuit element that functions as a programmable logic device. Pet. 23.

For the recited “field programmable gate array” (FPGA), Petitioner relies on Zavracky’s express disclosure of a programmable logic device (PLD). Pet. 24 (citing Ex. 1003, 5:21–23, Fig. 13). Petitioner cites Dr. Franzon’s testimony that one of ordinary skill in the art “would have known that a FPGA is an exemplary PLD” and provides evidence to support its contention. Pet. 24 (quoting Ex. 1002 ¶ 293). Petitioner relies on declaration testimony of Dr. Franzon that, as Petitioner notes, identifies citations to specific passages of prior art references to support his testimony. Pet. 24 (citing Ex. 1002 ¶ 293; quoting Ex. 1035, 1:29–30 (“a field

programmable gate array (FPGA) 100, which is one type of PLD”); Ex. 1036, 4:1–9 (“Thus, in a programmable logic device, such as a field programmable gate array (FPGA). . .”); Ex. 1037, 1:13–22; Ex. 1038, Abstract)).

Additionally, Petitioner cites “Zavracky’s description of a PLD for a ‘user-defined’ communication protocol, Ex. 1003, 12:33–36” and Dr. Franzon’s testimony that this description would have “suggested to [one of ordinary skill in the art] that a FPGA was [a] type of PLD since the ‘user’ would be ‘defining’ that protocol later in the field.” Pet. 25 (quoting Ex. 1002 ¶ 294 (citing Ex. 1040; Ex. 1051). Petitioner also relies on Dr. Franzon’s testimony that one of ordinary skill in the art “would have been motivated to use a FPGA because a field programmable array was recognized as the correct programmable logic device for such a ‘user-defined’ network device.” Pet. 25 (citing Ex. 1002 ¶ 294). Dr. Franzon’s testimony is supported by summary of two papers that describe FPGAs used in that context. *See* Ex. 1002 ¶ 294 (describing Ex. 1040 (using a FPGA-based firewall); Ex. 1051 (describing using an FPGA to create an “adaptable digital network processor))).

Petitioner also contends that “the combination of Zavracky and Chiricescu teaches or suggests ‘a first integrated circuit functional element including a field programmable gate array.’” Pet. 25 (citing Ex. 1002 ¶ 296; Ex. 1004, 232). “Chiricescu literally describes Zavracky as teaching technology ‘to build 3-D layered **FPGAs** which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.” Pet. 25 (citing Ex. 1004, 232) (emphasis in Petition); *see* Ex. 1004, 235 n.3 (citing Ex. 1003). Petitioner contends that “the Zavracky-Chiricescu combination

yields a modified version of Zavracky's 3D chip stack where Zavracky's 'PLD' layer is implemented as Chiricescu's" FPGA layer. Pet. 25–26 (citing Pet. VII.A.2 (summary of Chiricescu); *see also* Pet. 16 (describing Chiricescu having an FPGA layer")).

Regarding "at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element" (limitation [1.2]), Petitioner again relies on Zavracky's Figures 12 and 13 as disclosing stacked integrated circuit functional elements. Pet. 26. Petitioner indicates that Zavracky describes Figure 12 as having a "random access memory array." Pet. 26 (citing Ex. 1003, Fig. 12, 12:15–28); Ex. 1003, 12:14–15 ("FIG. 12 presents a stacked microprocessor and random access memory array . . .").

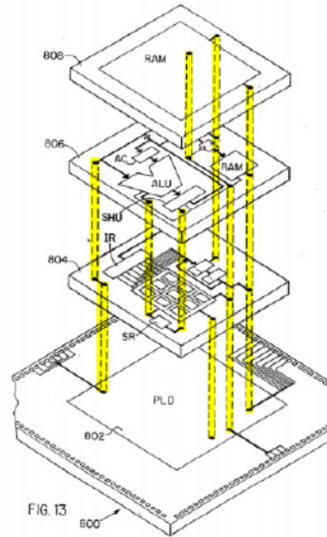
Petitioner quotes Zavracky's teaching of vertically stacked and interconnected circuit element layers that are electrically coupled:

One significant aspect in the formation of three-dimensional circuits involves interconnecting the layered devices. . . . Via holes are formed through the upper contact areas to gain access to the lower contact areas. . . . Electrical contact between the upper and lower devices is made by filling the via holes 1022 with an electrically conductive material . . . [.]

Pet. 27 (quoting Ex. 1003, 14:51–63; citing Ex. 1003, 2:18–22, 2:27–35, 10:8–21, 10:61–65, Fig. 6).

Petitioner also contends that Zavracky's PLD (on which Petitioner relies as teaching or suggesting the FPGA of the first integrated circuit functional element) is vertically stacked with and electrically coupled to Zavracky's memory array, such as shown in Figures 12 and 13. Pet. 27–28 (Ex. 1003, Fig. 12 (annotated), Fig. 13 (annotated)). Petitioner's annotated

version of Zavracky's Figure 13 depicts stacked functional elements and the coupled contact points relied upon by Petitioner:



Pet. 27–28. Zavracky's Figure 13 above as annotated by Petitioner depicts (highlighted) inter-layer via connections in programmable logic array 802, which “can be programmed to provide for user-defined communication protocol between the microprocessor and any off-chip resources.” Ex. 1003, 12:29–37.

Regarding limitation [1.3]—“wherein said field programmable gate array is programmable as a processing element,” Petitioner relies on Zavracky's disclosure that its “programmable logic array 802” “can be programmed to provide for user-defined communication protocol” and its analysis regarding limitation [1.1] that Zavracky's PLD would teach or suggest the recited FPGA. Pet. 28. For support, Petitioner relies on declaration testimony of Dr. Franzon that one of ordinary skill in the art would have understood Zavracky's programmable logic array to be

operating as a processing element. Pet. 28 (summarizing Ex. 1002 ¶ 302). Petitioner, in its citation, notes that Dr. Franzon’s declaration testimony relies on evidence to support its conclusion. Pet. 28 (“Ex. 1002 ¶ 302 (citing Ex. 1040)”). Petitioner also asserts that Chiricescu discloses a FPGA that can be quickly reconfigured to implement arbitrary logic. Pet. 29 (citing Ex. 1004, 233–234).

In its combination of Zavracky, Chiricescu, and Akasaka, Petitioner identifies with particularity “Chiricescu’s FPGA and memory” with respect to claim 1’s acceleration limitation [1.4]—“wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.” Pet. 29–30. According to Petitioner, Chiricescu’s solution to the problem of high configuration time of a FPGA is a memory layer storing configuration information to avoid going “off-chip” to load FPGA reconfiguration data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex. 1002 ¶¶ 304–07). Petitioner asserts Chiricescu teaches that the FPGA-reconfiguration is accelerated by the data already having been loaded into the memory array. Pet. 30 (Ex. 1004, 234; Ex. 1002 ¶¶ 304–07).

To support its contention, Petitioner relies on passages from Chiricescu and four paragraphs of Dr. Franzon’s declaration testimony, which provides reasoning with citations to Chiricescu and to a 1999 reference that predates the earliest filing date claimed by the ’214 patent (Ex. 1057).<sup>19</sup> In his declaration testimony cited by Petitioner, Dr. Franzon further explains his conclusion that “Chiricescu’s ‘cache’ memory . . . is

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<sup>19</sup> In Ex. 1002 ¶ 304 Dr. Franzon quotes Pierre Marchal, *Field-Programmable Gate Arrays*, ACM, Communications of the ACM, Vol. 42, No. 4 (April 1999) (Ex. 1057).

functional to accelerate reconfiguration of said FPGA as a processing element,” as required by claim 1’s acceleration limitation. Ex. 1002 ¶ 307; Pet. 29 (citing Ex. 1002 ¶¶ 304–09); Pet. 30 (citing same). On this basis, Dr. Franzon expressly concludes that Chiricescu’s memory is functional to accelerate as recited in claim 1.

Independent claim 2 includes the same limitations as recited in independent claim 1. *Compare* Ex. 1001, 7:56–65, *with id.* at 8:1–15. For those limitations, Petitioner relies on its arguments made with respect to independent claim 1. Pet. 30–31 (Petitioner’s contentions regarding claim 2 referencing analysis regarding same limitations in claim 1).

Independent claim 2 additionally recites “said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements.” Ex. 1001, 8:7–10. For this limitation, Petitioner relies on its combination of Zavracky, Chiricescu, and Akasaka. Pet. 31. In its combination for this limitation, Petitioner identifies Akasaka’s description of electrical coupling of active layers through via holes and asserts Akasaka’s 3D IC (shown in Akasaka’s Figure 4) is similar to Figure 4 and corresponding the description in the ’214 patent. Pet. 31–32 (citing Ex. 1001, 4:63–5:1, 5:7–11, 5:16–26, Fig. 4; Ex. 1005, 1705, 1707; Ex. 1002 ¶¶ 327–32).

The record supports Petitioner’s position. We find Akasaka’s active circuit layers connected electrically through via holes teach or suggest the recited “integrated circuit functional elements that are coupled by a number of contact points distributed throughout the surfaces of said functional elements.” Akasaka’s active layers in its 3D-IC are integrated circuit

functional elements. (Ex. 1005, 1705 (“Each layer or set of several active layers can have its own function”)).

Akasaka describes “exchang[ing] signals between upper and lower circuit layers through via holes in 3-D ICs” and further specifics that “[e]ach active layer is connected electrically via holes, and signals can be transferred between the layers.” Ex. 1005, 1705, 1707; Fig. 4 (showing via-hole connections between two active layers in a 3-D integrated circuit). Akasaka indicates “[s]everal thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or vice versa) through them.” Ex. 1005, 1705. That Akasaka uses the term “holes” rather than the recited “contact points.” The ’214 patent, however, describes “contact points” shown in its Figure 4 also as via holes. Ex. 1001, 4:63–5:1 (describing Fig. 4 as depicting a stack of dies including “microprocessor die 64, memory die 66, and FPGA die 68, all of which have a number of corresponding contact points, or holes 70”); *see* Ex. 1002 ¶ 327 (Dr. Franzon testifying that the ’214 patent “describes ‘contact points’ as ‘holes’ or through-silicon contacts” (quoting Ex. 1001, 4:63–5:1, 5:7–8, 5:16–17 for support)).<sup>20</sup>

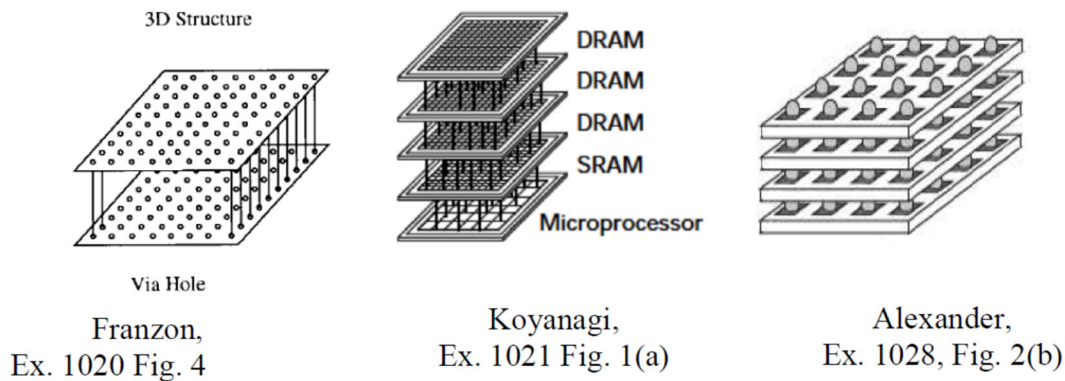
Regarding the requirement that the contact points be “distributed throughout the surfaces of said functional element,” we agree with Petitioner that the combination of Zavracky and Akasaka would have taught or suggested this feature. *See* Pet. 32–33 (citing Ex. 1003, 6:43–47, 13:43–47,

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<sup>20</sup> Dr. Franzon testimony cites to the ’035 patent specification and notes that equivalent disclosures exist in the other challenged patents. Ex. 1002 ¶ 327. The ’214 patent includes the portions cited by Dr. Franzon at the citations noted above.

14:52–63; Ex. 1005, 1705; Ex. 1002 ¶ 332). More specifically, this feature is at least suggested by Zavracky’s teaching of 3D stack elements where “openings or via holes” providing inter-layer connections “can be placed anywhere” and “are not limited to placement on the outer periphery” and Akasaka’s teaching of “tens of thousands of via holes.” Ex. 1003, 6:43–47, 13:43–47, 14:52–63; Ex. 1005, 1705; *see* Pet. 32 (citing Ex. 1003, 6:43–47, 13:43–47, 14:52–63; Ex. 1005, 1705); *see also* Ex. 1005, Fig. 4 (showing three sets of via holes in active layers, including the center set of via holes placed away from two of the edges of the active layers); Ex. 1002 ¶ 331 (Dr. Franzon describing Akasaka as “teaching that ‘tens of thousands of via holes’ can be distributed throughout the surface of the stacked elements (as shown in Akasaka’s Figure 4)”).

We credit Dr. Franzon’s testimony in this regard because it is consistent with the descriptions in Zavracky and Akasaka as noted above. Furthermore, Dr. Franzon provides additional citations to prior art references to support his opinion that structures of “stacked [integrated circuit] elements with contact points (e.g., via holes) distributed across the surfaces of elements” were “ubiquitous in the prior art” and that one of ordinary skill in the art “would have been well acquainted with such structures.” Ex. 1002 ¶ 332 (citing Ex. 1020, 9–10 (“‘through hole vias’ provide ‘array of contacts [that] are used to provide vertical interconnections’”), Fig. 4; Ex. 1021, Figs. 4, 17 (“more than  $10^5$  interconnections per chip”); Ex. 1028, Fig. 9, 1 (“‘10,000’ vias with enlarged diagram to show structure”)). For example, Dr. Franzon included three figures reprinted below:



Each of the three figures show stacked layers with via holes distributed across the element layers. See Ex. 1020, Fig. 4; Ex. 1021, Fig. 1(a); Ex. 1028, Fig. 2(b).

For these reasons, we find that Petitioner’s combination of Zavracky, Chiricescu, and Akasaka teaches or suggests “said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements,” as recited in claim 2.

Independent claims 26 and 27 each recite many of the limitations also recited in independent claims 1 and 2. For example, like claim 2, independent claim 27 recites “said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements.”

Independent claims 26 and 27, however, “wherein said memory array is functional to accelerate *external memory references to said processing element*,” rather than reciting “functional to accelerate *reconfiguration of said field programmable gate array as a processing element*.”

Petitioner relies on its arguments made with respect to independent claims 1 and 2 for the claim limitations recited in independent claims 26 and

27. Pet. 36–37 (Petitioner’s contentions regarding claims 26 and 27 referencing analysis regarding limitations in claims 1 or 2).

*b. Disputed Limitations in Independent Claims 1, 2, 26 and 27*

A central issue in this proceeding is whether Petitioner’s combination of Zavracky, Chiricescu, and Akasaka teaches or suggests “the functional to accelerate” limitations recited in the independent claims.

(i) Petitioner’s Contentions

For these limitations, in its combination of Zavracky, Chiricescu, and Akasaka, Petitioner identifies with particularity “Chiricescu’s FPGA and memory” used to address the problem of “the high configuration time of an FPGA.” Pet. 29–30. To address this problem caused by having to load configuration data from off-chip memory, Chiricescu uses a “memory layer” in which “random access memory is provided to store configuration information” to avoid going “off-chip” to load FPGA reconfiguration data. Pet. 29–30 (citing Ex. 1004, 232, 234; Ex.1002 ¶¶ 304–07). In addition to the numerous short vias of the combination providing acceleration, Petitioner also asserts Chiricescu teaches that the FPGA-reconfiguration is accelerated by the data already having been loaded into the memory array. Pet. 30 (citing Ex. 1004, 234; Ex. 1002 ¶¶ 304–07).

To support its contention, Petitioner relies on passages from Chiricescu and four paragraphs of Dr. Franzon’s declaration testimony, which provides reasoning with citations to Chiricescu and to a 1999 reference that predates the earliest filing date claimed by the ’214 patent (Ex. 1057). In his declaration testimony cited by Petitioner, Dr. Franzon further explains his conclusion that “Chiricescu’s ‘cache’ memory . . . is

functional to accelerate reconfiguration of said FPGA as a processing element,” as required by claim 1’s “functional to accelerate” limitation. Ex. 1002 ¶ 307; Pet. 29 (citing Ex. 1002 ¶¶ 304–09); Pet. 30 (citing same). Thus, Dr. Franzon expressly concludes that Chiricescu’s memory is functional to accelerate as required in claim 1.

As noted previously, Petitioner’s combination “fold[s] in Chiricescu’s teachings (including using stacked memory to reconfigure a FPGA) with Zavracky’s 3D stacks” to lead to significant improvement in reconfiguration time, among other reasons. Pet. 18–19. Thus, as noted above, Chiricescu’s stacked memory to reconfigure a FPGA accelerates FPGA reconfiguration because the needed data is already stored in Chiricescu’s stacked memory.

Petitioner relies on this analysis for the same limitation in independent claim 2 and for “said memory array is functional to accelerate external memory references to said processing element,” as recited in independent claims 26 and 27. Petitioner adds in the context of claims 26 and 27 that the relevant analysis is “discussing acceleration of FPGA reconfiguration through acceleration of external memory references.” Pet. 37 (claim 26), 38 (claim 27).

(ii) Patent Owner’s Contentions

Patent Owner contends that Zavracky, Chiricescu, and Akasaka alone or as combined by Petitioner fail to teach or suggest “wherein said memory array is functional to accelerate *external memory references to said processing element*” recited in claims 26 and 27 and fail to teach or suggest “wherein said memory array is functional to accelerate *reconfiguration of said field programmable gate array as a processing element*,” as recited in claims 1 and 2. PO Resp. 18–22 (claims 26 and 27), 22–23 (claims 1 and 2).

Patent Owner first presents contentions regarding claims 26 and 27 (which Patent Owner argues together). *See PO Resp.* 18–22; PO Sur-reply 2–10. Patent Owner then addresses claims 1 and 2 (which Patent Owner groups together), like Petitioner does, by indicating the arguments addressing claims 26 and 27 also show claims 1 and 2 to be patentable. PO Resp. 22–23; PO Sur-reply 10.

According to Patent Owner, Petitioner’s combination fails because the claims require “structure ***provided within the memory array*** (*i.e.* the wide configuration data port disclosed in the ’214 Patent) that is responsible for accelerating the programmable array’s accelerated external memory references. PO Resp. 18–19 (citing Ex. 2011 ¶¶ 53–54); PO Sur-reply 3 (indicating Petitioner’s proposed combination does not “include a wide configuration data port as the claimed invention requires”). For the reasons explained previously (Section II.C), we do not agree with Patent Owner.

Patent Owner correctly notes that the ’214 patent “provides accelerated memory references due to its technique of stacking a programmable array with a memory die using through-silicon vias (TSVs).” PO Resp. 18–19 (quoting Ex. 1001, 5:16–26). Patent Owner then contends “Chiricescu’s ‘RLB BUS’ that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the ’214 Patent” and “loads the configuration data ‘in a byte serial fashion and must configure the cells sequentially.’” PO Resp. 19–20 (citing Ex. 2012, 80:12–17; Ex. 1001, 4:51–58; Ex. 2011 ¶ 55). For these reasons, Patent Owner asserts, that “Chiricescu fails to disclose any technique for accelerating external memory references over the baseline of a narrow configuration data port that loads data ‘in a byte serial fashion.’” PO Resp. 20.

Contrary to Patent Owner's arguments, Petitioner persuasively argues and as summarized above, the Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka to teach the "functional to accelerate clause." *See* Pet. Reply 4–7; Pet. 29–30. Patent Owner's arguments unduly focus on Chiricescu alone without sufficiently considering Petitioner's combination of Zavracky, Chiricescu, and Akasaka. *See* Pet. Reply 10–11 (citing Pet. 14–30; Ex. 2012, 29:15–32:15).

Petitioner also persuasively shows that Patent Owner "misrepresents Dr. Franzon's testimony" regarding an alleged narrow port in Chiricescu. *See* Pet. Reply 11 (addressing PO Resp. 19–20). As Petitioner persuasively argues,

Dr. Franzon's cited testimony: (1) has nothing to do with Chiricescu; (2) was given in response to a question about Trimberger; and (3) was discussing the connection to "an off-chip memory" (80:11). Ex. 2012, 80:10–22.

Pet. Reply 11.

Dr. Franzon's cited deposition testimony supports Petitioner. Specifically, Dr. Franzon's cited deposition testimony refers to Trimberger in the context of "off-chip memory that loads in through the data port," and Dr. Franzon testifies that one of ordinary skill in the art "would interpret figure 5 as [including an undepicted] similar narrow structure on the left of the very wide configuration data port" to load data from an external source." *See* Ex. 2012, 80:3–22. In other words, Dr. Franzon's testimony does not describe Chiricescu's stacked memory layer as using a narrow port to transfer reconfiguration data to the RLB (with FPGA gates) layer from this "on-chip" memory within the 3D stack, as Patent Owner alleges. *See* Ex. 1004, Fig. 2.

As Petitioner also argues, Patent Owner’s “‘narrow data port’ arguments are contrary to Chiricescu’s teachings” and do not address the combined teachings of Chiricescu, Zavracky, and Akasaka. Pet. Reply 11 (citing PO Resp. 19–20). Petitioner notes that Zavracky describes “interconnects as being ‘placed anywhere on the chip’ without restriction.” Pet. Reply 11 (emphasis added) (quoting Ex. 1004, 232). In addition, Petitioner notes that Chiricescu “discloses ‘three separate layers with metal interconnects [including a “memory layer”] between them.’” Pet. Reply 11 (quoting Ex. 1004, 232) (bracketed text added by Petitioner) (emphasis omitted).

In other words, by placing vias anywhere throughout the different dies as Chiricescu and the combined teachings suggest, the combined teachings distinguish over a narrow data port, where Petitioner provides well-known reasons for employing wide data ports, such as allowing for increased bandwidth and parallelism. *See* Pet. 18–20; Ex. 1001, 5:16–21 (describing “through-die array contacts 70 . . . routed up and down the stack in three dimensions” as “not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die,” so that by placing contacts throughout, “cells that may be accessed within a specified time period is increased”) (emphasis added).

As Petitioner also persuasively argues, even if the claims require a wide configuration data port, according to Patent Owner’s expert in the IPR2020-01020, IPR2020-01021, and IPR2020-01022, a “configuration data port . . . is . . . just a data port used for configuration . . . And data port is just an interface to send data from one place to another.” Reply 9 (quoting

Ex.1075, 163:8–163:21). “And ‘the reason it’s a very wide configuration data port is because it has a lot of connections through these TSVs between the memory die and the FPGA die.’” Pet. Reply 9 (quoting Ex. 1075, 157:23–158:3 (Dr. Chakrabarty agreeing with this statement)).

In other words, under Petitioner’s persuasive showing, even if the challenged claims require a wide configuration data port, the combined teachings meet the claims for the reasons noted. Pet. Reply 9 (“The Zavracky, Chiricescu, and Akasaka Combination provides the ‘memory . . . accelerate’ limitations even under [Patent Owner’s] flawed construction” that the wide configuration data port is responsible for accelerating.). Petitioner persuasively shows that the Zavracky-Chiricescu-Akasaka 3D module uses numerous vias throughout the dies to transfer data between the dies—i.e., acting as a wide configuration data port functional to accelerate all manner of data and signals in parallel. *See, e.g.*, Pet. 17 (showing that Akasaka teaches that “‘tens of thousands of via holes’ permit parallel processing” by utilizing the many interconnections; as a result of this parallel processing, “the signal processing speed of the system will be greatly improved”; and due to “shorter interconnection delay time and parallel processing” made possible from the area-wide interconnects, the processing of data between layers is accelerated such that “twice the operating speed is possible in the best case of 3-D ICs” (quoting Ex. 1005, 1705)), 20 (arguing that “it was a predictable advantage and also suggested by Akasaka itself that applying Akasaka’s distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity” (citing Ex. 1002 ¶ 233 (quoting Ex. 1005, 1705))). Petitioner also shows that

“[i]t was well known that ‘interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,’ and that ‘wide buses are very desirable’ and were made possible by 3-D stacking.” Pet. 12.

Therefore, Petitioner shows that the numerous via connections between the memory die and FPGA connect to the memory array to render the “memory array functional to accelerate memory references to the processing element,” as claim 1 requires. *See, e.g.*, Pet. 20–21 (showing that Akasaka’s numerous connections would have motivated a POSITA to replicate common data memory, and “increase bandwidth and processing speed through better parallelism and increased connectivity”).

Additionally, Patent Owner argues that, because Dr. Franzon did not provide a baseline against which to measure acceleration, Petitioner has not demonstrated “the combination of references ‘accelerates external memory references to said processing element’ over the baseline of the relatively narrow configuration port distinguished in the ’214 Patent (and taught in Chiricescu).” PO Resp. 20–21 (citing Ex. 2012, 25:21–26:23; Ex. 1001, 1:50–55, 4:27–32; Ex. 2011 ¶ 56). Petitioner also persuasively addresses Patent Owner’s argument that the claims require acceleration over a “baseline.” *See* PO Resp. 20–21; Reply 11–12. Petitioner points to Dr. Franzon’s testimony “that the Zavracky-Chiricescu-Akasaka combination provides acceleration compared to the baseline of other prior art with different structural characteristics.” Pet. Reply 11–12 (citing Ex. 1002 ¶¶ 212, 215–17, 304–05; Ex. 2012, 29:15–33:15, 28:9–21).

Petitioner also persuasively addresses Patent Owner’s argument that “external memory references . . . are not data, but are instructions directed to

a particular place memory [sic] address in memory.” PO Resp. 12 (including [sic] annotation). Petitioner quotes Dr. Franzon’s declaration testimony:

Chiricescu is teaching to use that memory as a “cache”... By doing so, the FPGA’s external memory references... will be accelerated because [they] will “hit” in the “cache” and be returned from the on-chip memory without having to go off-chip. Chiricescu is thus teaching to the POSITA to accelerate memory lookups....

Pet. Reply 12 (block quoting Ex. 1002 ¶¶ 215–16; citing Ex. 2012, 42:9–14, 48:6–50:1).

In response to Petitioner’s Reply, Patent Owner contends that Dr. Franzon testified that external memory references could be located on an off-chip memory die stacked with the programmable array die and, therefore, Dr. Franzon testified that it is the “off-chip memory on the second integrated die element [that] is functional to ‘accelerate external memory references to the processing element.’” PO Sur-reply 7 (block quoting Ex. 2012, 42:21–43:3). Patent Owner concludes that Petitioner’s combination of Zavracky, Chiricescu, and Akasaka “does not teach or suggest the claimed structure under any construction” because Petitioner’s combination of Zavracky, Chiricescu, and Akasaka “does not satisfy a ‘memory array [is] functional to accelerate external memory references to said processing element’” and does not “include a wide configuration data port as the claimed invention requires.” PO Sur-reply 3. Patent Owner, however, misinterprets Dr. Franzon’s testimony that concerned the plain and ordinary meaning of “external memory references” as indicating what element (i.e., off-chip memory) would be performing an external memory

reference. *See* Ex. 2012, 4215–44:45.<sup>21</sup> For this reason, we do not agree with Patent Owner’s characterization of Dr. Franzon’s deposition testimony.

Patent Owner also argues, in response to Petitioner’s Reply, that “[t]he entire point of Chiricescu is that it achieves accelerated FPGA configuration by storing configuration data ‘on-chip’ so that it does not need to load configuration data from off-chip.” Sur-reply 4-5. Patent Owner also argues that “all off-chip connections are carried out through a typical narrow configuration data port, that suffers the same problems as the prior art distinguished in the ’214 Patent.” PO Sur-reply 5. Patent Owner then argues that “moving Chiricescu’s cache memory off-chip (i.e., into Zavracky’s 3D stacked memory die) eliminates the benefit gained from moving the memory on-chip, [so] a POSITA would not have contradicted Chiricescu’s fundamental teachings to arrive at Petitioner’s proposed combination.” PO Sur-reply 5.

We do not agree with Patent Owner’s position. Patent Owner does not sufficiently address Chiricescu’s memory and FPGA layers that are short “interlayer vias” “placed anywhere on the chip” within the same 3D stack and, thus, is not off-chip. As Petitioner notes, Dr. Franzon described “routine use of on-chip area-wide connections in 3D stacks, including his prior work.” Reply 17–18 (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶ 65; Ex. 1020; *see also* Ex. 1004, Fig. 2, 232 § 1 (describing “on chip random access

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<sup>21</sup> Ex. 2012, 42:15–43:3 (discussing meaning of “external memory reference” before a break), 43:13:44:3 (characterizing topic before the break as “discussing the plain and ordinary memory of the term ‘external memory references’”), 44:4–4 (questioning “what element would be performing this type of memory reference”).

memory . . . provided to store configuration memory”—i.e., the memory layer of Figure 2).

Patent Owner contends that “the movement of *Chiricescu*’s on-chip cache memory to *Zavracky*’s off-chip memory would throttle” speed gains. Sur-reply 5. We do not agree with Patent Owner. In the context of *Chiricescu*’s teachings and Petitioner’s showing, *Zavracky* includes memory in a stack of chips connected by numerous short vias as Petitioner shows and as discussed above. *See, e.g.*, Pet. 14–16, 23–28. Patent Owner’s attempt to conflate *Zavracky*’s modified stack of chips as “off-chip” such that “all off-chip connections are carried out through a typical narrow configuration data port” is not supported. *See* Sur-reply 5. *Chiricescu* describes loading configuration data from “memory off-chip” as “significantly” and distinctly slower (Ex. 1004, 234) than loading it from an “on-chip random access memory layer” (*see* Ex. 1004, 232) within the stacked layers of the disclosed 3D FPGA. *See* Ex. 1004, 234, 232, Fig. 2. As Petitioner persuasively shows throughout its briefing, *Zavracky*’s stack of chips connected by numerous vias, as modified by *Akasaka*’s and *Chiricescu*’s teachings, operates just like *Chiricescu*’s “on-chip” circuit layers in a single chip connected by numerous vias in terms of speed and acceleration. *See* Pet. Reply 6 (“*Zavracky*’s short interior ‘inter-layer connectors’ to stacked ‘random access memory . . . results in reduced memory access time, increasing the speed of the entire system,’” and “*Chiricescu* also teaches the acceleration advantages and ‘significantly improve[d FPGA] reconfiguration time’ achieved by its interconnected layers, including a memory layer configured as a cache for fast access to ‘configuration data... from memory off-chip.’” (quoting Ex. 1003, 11:63–12:2; Ex. 1004, 232)), 7 (noting

Akasaka's "acceleration advantages" based on "teaching, e.g., that '[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing' and that 'shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems.'" (quoting Ex. 1005, 1705)). In other words, as Petitioner shows, in addition to "stacking techniques," "[t]he Zavracky-Chiricescu-Akasaka Combination also discloses the other ways that the '214 patent even arguably implies increases speed—i.e., through caching, the use of short electrical paths, or significantly increased number of connections." Pet. Reply 8 (citing Pet. 14–30).

Patent Owner agrees that "Chiricescu says . . . [that] "[t]he elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application." Sur-reply 4 (quoting Ex. 1004, 234). Patent Owner argues, however, that "Petitioner concocts its hypothetical structure based on its demonstrably false claim that Chiricescu's improved FPGA reconfiguration time is 'achieved by its interconnected layers, including a memory layer configured as a cache for fast access to "configuration data . . . from memory off-chip.'" Sur-reply 4 (quoting Reply 6 (quoting Ex. 1004, 234)). Patent Owner contends that "Chiricescu says just the opposite." PO Sur-reply 4 (citing Ex. 1004, 234).

Contrary to Patent Owner's argument, Petitioner argues that Chiricescu improves FPGA reconfiguration time because Chiricescu's cache pre-stores and holds configuration data on-chip that it obtains from an external source (i.e., off-chip memory)—so that the FPGA need *not* access

that external (off-chip memory) source to load the FPGA through a typical narrow configuration data port during FPGA reconfiguration. *See* Pet. Reply 6 (describing acceleration “achieved by its interconnected layers, including a memory layer configured as a cache for fast access to ‘configuration data . . . from memory off-chip’” (quoting Ex. 1004, 232); Ex. 1004, 234 (“The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.”)).

Patent Owner additionally contends that Petitioner’s combination would improperly alter Chiricescu’s principle of operation. PO Resp. 27–28 (arguing Petitioner’s combination “would improperly alter Chiricescu’s principle of operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB bus and its ‘routing layer’”). As Petitioner notes, Patent Owner’s argument is based on a misunderstanding of Petitioner’s combination that does not modify Chiricescu but rather “folds in Chiricescu teaching with Zavracky’s 3D stacks.” Pet. Reply 15 (addressing Patent Owner’s principle of operation argument); *see* Pet. 18–19 (“The POSITA would have been encouraged to fold in Chiricescu’s teachings (including stacked memory to reconfigure the FPGA) with Zavracky’s 3D stacks, understanding it would lead to ‘significant[] improvement in the reconfiguration time.’”). In response to Petitioner’s Reply, Patent Owner indicates Chiricescu addresses “the problem of ‘loading configuration data on an as needed basis from memory off-chip’ was to move that memory on-chip.” PO Sur-reply 5.

We do not agree with Patent Owner that Petitioner’s combination alters Chiricescu’s principle of operation because, as discussed throughout

this decision, Petitioner’s combination relies on Zavracky’s stack of chips connected by numerous vias (as modified by Akasaka’s and Chiricescu’s teachings) that operate in terms of speed and acceleration like Chiricescu’s “on-chip” circuit layers in a single chip connected by numerous vias. *See, e.g.,* Pet. 18–22; Pet. Reply 5–6.

Patent Owner further contends that Dr. Franzon “concedes that Akasaka’s thousands of connections would not and could not be used in Petitioner’s hypothetical structure such that the ‘memory array [is] functional to accelerate external memory references to said processing element.” PO Sur-reply 5–6 (citing Ex. 2012, 80:10–17).

We do not agree with Patent Owner’s characterization of Dr. Franzon’s testimony. First, the cited portion of Dr. Franzon’s testimony did not address “Akasaka’s thousands of connections” as Patent Owner contends. Rather, Dr. Franzon’s testimony was made in the context of the implicit similarity of the structure of another reference and in the context of loading data from an external source—Trimberger (Ex. 1006)—and undepicted narrow port implicit “on the left of” Figure 5 of the challenged patent.<sup>22</sup> Ex. 2012, 80:3–6 (Dr. Franzon testifying, “So if there’s 100,000 memory circuits in Trimberger, it can’t reload all those memory contents within one clock cycle [from an external source]. The same would be true of ’226 [patent]. The structure in figure 5 of ’226 [patent] does not show anything on the left of the very wide configuration data port.”); 80:15–22 (Dr. Franzon testifying, “you wouldn’t have thousands of bits wide access

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<sup>22</sup> Dr. Franzon’s testimony concerned his declaration testimony (Ex. 1002) concerning four patents, one of which was the ’214 patent. Ex. 2012, 4:14–5:13, 8:4–8. The ’214 patent also includes Figure 5 of the ’226 patent.

[from an external source] to the DRAM in a normal memory structure in this time frame. So there would be a similar narrow structure—[one of ordinary skill in the art] would interpret figure 5 as a similar (undepicted) narrow structure *on the left of the very wide configuration data port*” (emphasis added)).

Second, Patent Owner’s arguments do not undermine Petitioner’s combination of Zavracky, Chiricescu, and Akasaka having multiple vertical vias in the stacked memory chip structure of Zavracky, as modified by the teachings of Chiricescu and Akasaka, to accommodate the memory array operating as a cache memory to accelerate the loading of the reconfiguration data. *See* Pet. 18–22, 28–32. Petitioner notes, for example, that Akasaka suggests “that applying Akasaka’s distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity.” Pet. 18 (citing 1002 ¶ 233 (quoting Ex. 1005, 1705)).

Patent Owner also responds to Petitioner’s Reply by asserting that “Dr. Franzon admits that it is the structure of the wide configuration data port, including buffer cells, that allows for the acceleration of external memory references to the programmable array.” PO Sur-reply 6 (citing Ex. 2012, 77:5–15, 42:21–43:3). Patent Owner characterizes that testimony as indicating “it is a new and improved configuration (not discussed in any of Petitioner’s myriad of references) that allows for the memory array to be functional to accelerate external memory references to the processing element of the programmable array.” PO Sur-reply 6–7.

Here, too, we do not agree with Patent Owner’s characterization of Dr. Franzon’s cited testimony. First, Dr. Franzon does not characterize the

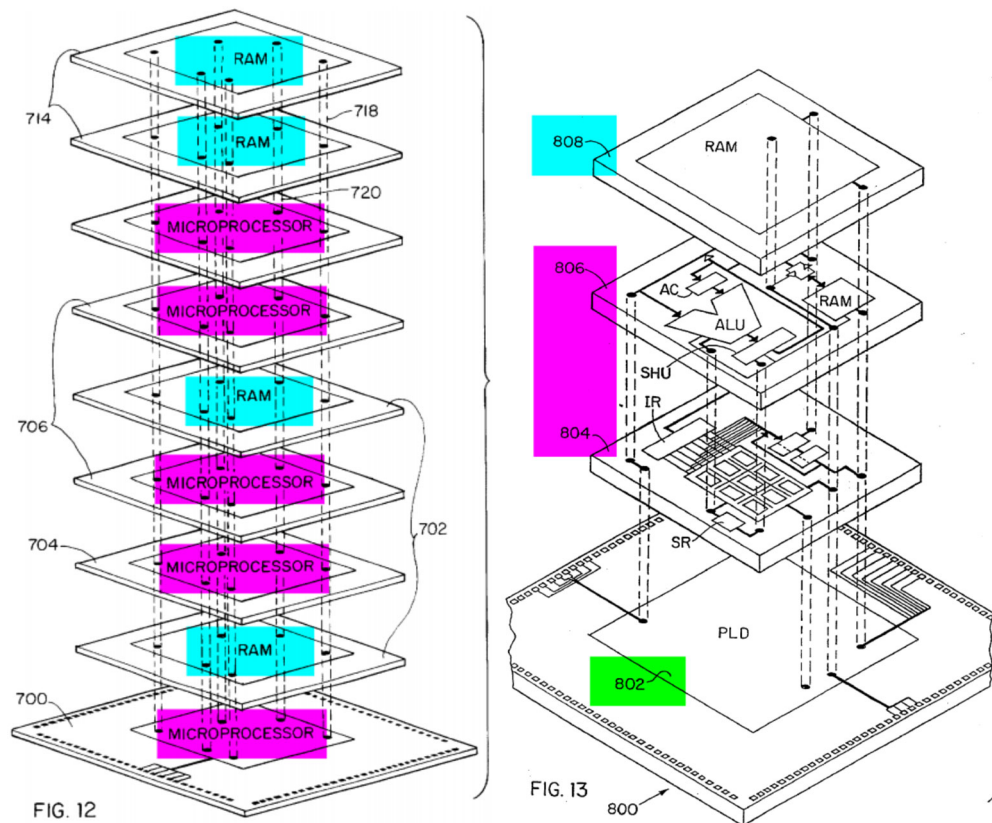
structure of the wide configuration data port as including buffer cells. Rather, Dr. Franzon indicates the “exemplary wide configuration data port 82 depicted in figure 5 [of the challenged patent] shows a direct path to every buffer cell.” Ex. 2012, 77:7–10. As discussed previously, Figure 5 depicts the wide configuration data port as a “black box” and that depiction does not include the buffer cells as part of the “black box” wide configuration data port 82. *See* Section II.C (Claim Construction) above. Second, Dr. Franzon’s testimony at page 77 describes how the wide configuration data port shown in Figure 5 of the challenged patent is able to “store a configuration in the buffer cell and upload it to the logic cell in one clock cycle” and that the same structure is shown in Trimberger. Ex. 2012, 77:5–15. Rather than describing the wide configuration data port of Figure 5 of the challenged patent as “a new and improved configuration (not discussed in any of Petitioner’s myriad of references” (as Patent Owner alleges), Dr. Franzon states that it is the “same structure” as shown in a prior art reference (Trimberger, Ex. 1006). Third, Dr. Franzon’s cited testimony on pages 42–43 opines that the recited external memory reference is located in off-chip memory. Patent Owner does not sufficiently explain how the *location* of external memory references relates to allowing for the memory array to be functional to accelerate those references.

#### *4. Dependent Claims 4, 6, 29, and 31*

Petitioner presents evidence that dependent claims 4, 6, 29, and 31 would have been obvious over Zavracky, Chiricescu, and Akasaka. Pet. 34–36, 38. Patent Owner does not present separate arguments for limitations additionally cited by these dependent claims.

Claim 4 depends from independent claim 2 and additionally recites “further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements” for which Petitioner partly relies on Zavracky’s Figures 12 and 13. Pet. 34–35. Claim 29, depends from independent claim 27, and additionally recites the same limitation as recited in claim 4. Petitioner’s argument regarding dependent claim 29 partly relies on Petitioner’s argument for claim 4. Pet. 38.

For the recited third integrated circuit functional element, Petitioner identifies the microprocessors shown in Zavracky’s Figures 12 (microprocessors on their own) and 13 (a multi-layer microprocessor). Pet. 34. Petitioner’s annotated Figures 12 and 13 are depicted below:



Zavracky's Figure 12 "presents a stacked microprocessor and memory array." Ex. 1003, 12:14–15, Fig. 12. Zavracky describes first microprocessor layer 700 that "shares random access memory 702 on the second layer, [with] another microprocessor 704 located above the random access memory." Ex. 1003, 12:17–20. Zavracky describes "address 720, and data 718 buses [that] run vertically through the stack by the use of inter-layer connectors." Ex. 1003, 12:25–27. Zavracky's Figure 13 depicts "programmable logic array 802 . . . fabricated upon the first layer 800. The second 804 and third 806 layers comprise a multi-layer microprocessor, with random access memory on the fourth layer 808." Ex. 1003, 12: 31–34. Notably, Zavracky indicates programmable logic array 802 "can be formed in any of the layers of a multilayer structure as described elsewhere herein." ex. 1003, 12:37–39.

Claim 6 depends directly from claim 4 and indirectly from independent claim 2. Claim 6 additionally recites "said third integrated circuit functional element includes an I/O controller" for which Petitioner partly relies on Zavracky's controller depicted in Figure 13. Pet. 35–36. Claim 31, depends from independent claim 29, and additionally recites the same limitation as recited in claim 4. Petitioner's argument regarding dependent claim 31 partly relies on Petitioner's argument for claim 6. Pet. 38.

Petitioner identifies controller depicted on multi-layer microprocessor 804 in Figure 13 and also shown and labeled as "CONTROLLER" in Figure 11. Pet. 35. Based on Zavracky's express descriptions of the "controller," Petitioner persuasively argues, with support of Dr. Franzon's testimony, that one of ordinary skill in the art "would have understood

Zavracky as describing an I/O controller, which arbitrates the inputs and outputs to a shared communication bus.” Pet. 35–36 (quoting Ex. 1003, 5:54–60, 5:49–52, Ex. 1002 ¶¶ 324–25). We find Dr. Franzon’s testimony in this regard as credible because he provides persuasive explanation and analysis with comparisons between specific passages of a prior art reference (Ex. 1052) and Zavracky’s description. Ex. 1002 ¶¶ 324–25 (citing Ex. 1052, Abstract, 4:65–5:1; Ex. 1003, 5:54–60, 5:49–52 among others).

### *5. Summary*

After a full review of the record, including Patent Owner’s Response and Sur-reply and evidence, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, and Akasaka would have rendered obvious claims 1, 2, 4, 6, 26, 27, 29, and 31.

### *E. Asserted Obviousness of Claims 3 and 28*

Petitioner contends claims 3 and 28 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Satoh. *See* Pet. 1, 38–42.

#### *1. Disclosure of Satoh*

Satoh discloses a semiconductor integrated circuit incorporating a variable logic circuit and specifically a Field Programmable Gate Array (FPGA). Ex. 1008, 46.<sup>23</sup> Satoh also describes testing a semiconductor integrated circuit “incorporating a variable logic circuit (FPGA) for outputting a signal indicating whether or not a circuit is normal and forming

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<sup>23</sup> We cite to the page numbers in the header of Sato, as is Petitioner’s practice.

a given logic [and] a memory circuit capable of reading and writing data.” Ex. 1008, 46. Satoh states that “the variable logic circuit (FPGA) performs a self-test, a memory test circuit is built for testing the memory in accordance with a specified algorithm with only the basic logic cells exclusive of defective parts by using information indicating the defective parts obtained by the self-test, and the memory circuit is tested.” Ex. 1008, 46.

Satoh also describes “configuring in the variable logic circuit a memory tester circuit that generates a specified test signal and an expected value signal based on a specified algorithm using only normal basic logic cells, supplies the test signal to the memory circuit, compares the output signal obtained as a result from the memory circuit with the expected value signal.” Ex. 1008, 49.

## *2. Claims 3 and 28*

Claim 3 depends from independent claim 2, and claim 28 depends from independent claim 27. Claims 3 and 28 each further recite “wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element.”

### *a. Petitioner’s Combination*

For claims 3 and 28, Petitioner relies on a combination of Zavracky, Chiricescu, Akasaka, and Satoh. Pet. 38–39. Petitioner contends that in the Zavracky-Chiricescu-Akasaka-Satoh combination, “the test signal is sent through the contact points between the FPGA of the first IC die element and the memory of the second IC die element, which is how those elements are stacked and electrically coupled.” Pet. 41–42 (citing Ex. 1002 ¶¶ 357–59).

Regarding the requisite reason to combine the references, Petitioner relies on Dr. Franzon's declaration testimony that "[i]t was well-known to test stacked modules in order to avoid the expense and waste of silicon by creating 'dead' chips, and improve yield." Pet. 40 (citing Ex. 1002 ¶ 241; indicating Ex. 1002 ¶ 241 further cites Ex. 1009; Ex. 1043). Petitioner indicates that "Satoh specifically praised the use of an FPGA to test 'memory circuits' for 'improving yield and productivity of the semiconductor integrated circuit.'" Pet. 40 (quoting Ex. 1008, 47:23–27).

Additionally, Petitioner further relies on Dr. Franzon's testimony for other reasons one of ordinary skill in the art would have combined Satoh's testing functionality with the 3D chip of Zavracky-Chiricescu-Akasaka:

Recognizing the need to test the 3D stack of the Zavracky-Chiricescu-Akasaka Combination, the POSITA would have sought out Satoh's teaching of using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity. Ex. 1002 ¶242. Moreover, (4) a FPGA is reusable: after being configured for testing in manufacture, the FPGA would then be reconfigured for its normal "in the field" purpose. *Id.* (citing Ex. 1045 ("Another advantage . . . is that after testing is complete, the reconfigurable logic (FPGA 28) can be reconfigured for post-testing adapter card functions."); Ex. 1046).

Pet. 40.

Petitioner also relies on Dr. Franzon's declaration testimony in asserting that one of ordinary skill in the art would have had a reasonable expectation of success:

It was well known to use a FPGA to test circuitry with 2-D chips as taught by Satoh. Ex. 1002 ¶241 (citing Ex. 1043). The POSITA would have recognized Satoh's teaching would readily

apply to the 3-D chip elements in the Zavracky-Chiricescu-Akasaka Combination. This includes because such a combination would have been a routine use of an FPGA, whose testing ability was not dependent on structure. Ex. 1002 ¶¶242–43. The result of this combination would have been predictable, by known FPGA testing to the 3D stack according to known methods to yield a predictable result. Ex. 1002 ¶244.

Pet. 41.

*b. Patent Owner's Contentions*

Patent Owner relies on the same unavailing arguments it advances with respect to the challenged claims addressed above. *See* PO Resp. 39 (“Because Petitioner does not contend that Satoh cures any of the deficiencies of the combination of Zavracky, Chiricescu, and Akasaka, as discussed above with respect to Ground 1, its reliance on the same rationales for Ground 3 also fail.”).

Patent Owner also argues that “Petitioner’s contention that [one of ordinary skill in the art] would be motivated to make the combination because it was well-known to test stacked die and Satoh tested memory elements on the same semiconductor chip (*see* Petition at 40) is divorced from the claimed invention.” PO Resp. 39–40. Patent Owner contends that “Petitioner’s generic rationale for using FPGAs for testing is wanting in particularity as to why a POSITA would combine the references as recited in the Challenged Claim.” PO Resp. 40. Patent Owner contends that Petitioner’s rationale fails “as it lacks sufficient explanation of how or why [one of ordinary skill in the art] would have been motivated to use Satoh’s FPGA for testing with the hypothetical 3-D structure of Zavracky-Chiricescu-Akasaka ‘in the way the claimed invention does.’” PO Resp. 40. (quoting *ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d

1312, 1328 (Fed. Cir. 2012)). Patent Owner contends that “[w]hether the use of Satoh’s FPGA is beneficial for testing does not sufficiently explain why a POSITA would have combined the references to yield the claimed invention.” PO Resp. 40–41.

*c. Analysis*

Petitioner provides specific reasons related to specific recitations in the claims as outlined above, including tying Satoh’s testing of a memory array using FPGA testing circuitry to the similar claim elements in claims 3 and 28. Petitioner’s arguments are supported by citations to Satoh and Dr. Franzon’s declaration testimony that in this regard provides persuasive explanation consistent with specific descriptions of relevant references cited for support. Pet. 40–41 (citing Ex. 1008, 47:23–27; Ex. 1002 ¶¶ 241–44); *see* Ex. 1002 ¶ 241 (citing Ex. 1020, 12; Ex. 1009, 254; 1043, [36], Ex. 1008, 47:23–27), ¶ 241 (citing Ex. 1045, Ex. 1046), ¶ 243 (citing Ex. 1021, Abstract; Ex. 1003, Abstract, 2:9–13, 3:58–67; Ex. 1008, 3); ¶ 244 (citing Ex. 1043).

For example, Petitioner identifies using Satoh’s FPGA test circuitry and memory testing teachings to avoid “dead chips”—a specific “beneficial” reason—and ties these teachings specifically to FPGA contact points in the Zavracky-Chiricescu-Akasaka” stack to test memory in that stack. *See* Pet. Reply 19–20 (reiterating five reasons supplied in the Petition, including, for example, “(1) the known problem of the need to test stacked modules to avoid the expense and waste of silicon by creating ‘dead’ chips” (citing Ex. 1002 ¶ 241 (citing Ex. 1009; Ex. 1020; Ex. 1043); Pet. 41–42 (explaining that “[i]n the Zavracky-Chiricescu-Akasaka-Satoh Combination, the test signal is sent through the contact points between the FPGA of the

first IC die element and the memory of the second IC die element, which is how those elements are stacked and electrically coupled” (citing Ex. 1008, 49:32–37; Ex. 1002 ¶¶ 357–59)).

In other words, Petitioner persuasively shows a reasonable expectation of success with specific reasons to combine, all supported by the record, including beneficial testing to avoid dead chips and maintain reliable memory to reconfigure the 3D stack’s FPGA post-manufacture, thereby showing how to apply the teachings to the claimed 3D stack as suggested by Zavracky, Chiricescu, and Akasaka. Specifically, claims 3 and 28 each recites “wherein said contact points are further functional to provide test stimulus from said [FPGA] to said at least second integrated circuit die element.” Petitioner persuasively applies Satoh’s teachings to these contact points in order to avoid dead chips.

Patent Owner advances an argument in its Sur-reply that “[t]he references Petitioner and Dr. Franzon cite do not disclose testing of 3D stacked processor[s] but instead disclose that individual die[s] are tested independently and prior to any 3D packaging.” Sur-reply 15. This argument is not relevant to a claim limitation at issue here. Neither claim 3 nor claim 28 recite packaging, and neither precludes “provid[ing] test stimulus from said field programmable gate array to said at least second integrated circuit die element” prior to any packaging.

Patent Owner cites to a single paragraph of Dr. Sourì’s declaration that is conclusory. PO Resp. (citing Ex. 2011 ¶ 83); Ex. 2011 ¶ 83 (Dr. Sourì testifying without citation to references or explanation). We give little weight to Dr. Sourì’s conclusory and unsupported testimony.

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Satoh would have rendered obvious claims 3 and 28.

*F. Asserted Obviousness of Claims 5 and 30*

Petitioner contends claims 5 and 30 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Alexander. Pet. 42–45.

*1. Disclosure of Alexander*

Alexander describes “stacking together a number of 2D FPGA bare dies” to form a 3D FPGA. Ex. 1009, 1.<sup>24</sup> Alexander explains that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” Ex. 1009, 1.

Alexander’s Figure 2 follows:

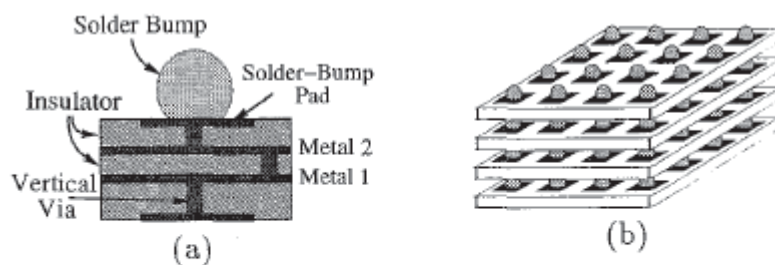


Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.

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<sup>24</sup> We cite, as Petitioner does, to the exhibit page numbers (rather than to the original page numbers).

Figure 2(a) shows vertical vias traversing a chip with a solder pad and solder bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1009, 1.

Alexander explains that stacking dies to form a 3D FPGA results in a chip with a “significantly smaller physical space,” lower “power consumption,” and greater “resource utilization” and “versatility” as compared to conventional layouts. Ex. 1009, 1.

## *2. Claims 5 and 30*

Claim 5 depends indirectly from independent claim 2, and claim 30 depends indirectly from independent claim 27. Claims 5 and 30 each further recite “wherein said third integrated circuit functional element includes another field programmable gate array.”

### *a. Petitioner’s Combination*

For claims 5 and 30, Petitioner relies on a combination of Zavracky, Chiricescu, Akasaka, and Alexander. Pet. 42–45. In reciting “wherein said third integrated circuit functional element includes another field programmable gate array,” claims 5 and 30 each essentially adds another FPGA to claim 27 as addressed above, requiring at least three stacked integrated circuit die elements: a memory array stacked with “another” FPGA (i.e., a total of two FPGAs), with the “integrated circuit functional elements,” which “include[]” the memory array and two FPGAs, electrically coupled together by “a number of contact points distributed through the surfaces of said functional elements,” “wherein said memory array is functional to accelerate external memory references to said processing element [one of the FPGAs]” (as recited in independent claim 2) or

“wherein said memory array is functional to accelerate external memory references to said processing element” (as recited in independent claim 27).

Petitioner relies on Alexander as disclosing “multiple stacked FPGA functional elements in different layers of a 3D package.” Pet. 44 (citing Ex. 1009, 1–3, Fig. 2; Ex. 1002 ¶ 321). As such, Petitioner contends that the combination of Zavracky, Chiricescu, Akasaka, and Alexander provides the additional FPGA as required by claims 5 and 30.

Regarding the requisite reason to combine, Petitioner contends as follows:

[One of ordinary skill in the art] would have known (as Zavracky notes) that multiprocessor systems were needed for “parallel processing applications,” for example, “signal processing applications.” Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, [one of ordinary skill in the art] would have appreciated Alexander’s teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). *Id.* [One of ordinary skill in the art] would have sought out Alexander’s multiple stacked FPGAs to enhance the Zavracky-Chiricescu-Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 43.

Additionally, Petitioner asserts one of ordinary skill in the art “would have had a reasonable expectation of success in integrating Alexander into that existing combination.” Pet. 43. More specifically, Petitioner contends that Alexander’s similar structure—having multiple stacked FPGAs, as similar to multiple processors stacked with multiple memories of the Zavracky-Chiricescu-Akasaka combination—evidences a reasonable expectation of success of stacking FPGAs with memories, “with multiple

functional elements stacked and vertically interconnected including using thousands of contact point vias (holes).” Pet. 43–44. Petitioner also asserts that “[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result.” Pet. 44 (citing Ex. 1002 ¶¶ 260–61).

*b. Patent Owner’s Contentions*

Patent Owner responds that “Petitioner’s only rationale for the combination of all four references . . . merely identifies a generalized benefit without sufficiently linking it to the features of the claimed invention,” and so “Petitioner fails to adequately explain how or why Alexander’s multiple FPGA dies can and would be combined with Zavracky-Chiricescu-Akasaka to reach the” limitation recited in claims 5 and 30. PO Resp. 42. More specifically, Patent Owner contends that “[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a POSITA would have been motivated to combine Alexander with Zavracky-Chiricescu-Akasaka to reach a 3-D processor module having ‘a third integrated circuit die element [that] includes another field programmable gate array.’” PO Resp. 42–43 (citing Ex. 2011 ¶ 84).

Patent Owner also argues that Petitioner’s “conclusory rationale is further discredited by Petitioner’s suggestions elsewhere in the Petition that Chiricescu discloses a FPGA application that enhances Zavracky.” PO Resp. 43 (citing Pet. 19). More specifically, Patent Owner argues that the Petition elsewhere suggest that a “POSITA would have taken Chiricescu’s suggestion of a FPGA to perform ‘arbitrary logic functions,’ . . . as a cue to

enhance and expand upon the packet processing task performed by the programmable logic device in Zavracky, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors and memories as taught in Zavracky.” PO Resp. 43 (quoting Pet. 19). Patent Owner argues that “there is no reason . . . to combine Alexander with Zavracky-Chiricescu-Akasaka,” because “Petitioner acknowledges that, Chiricescu, like Alexander, offers FPGAs to enhance parallel processing image and signal tasks of Zavracky’s microprocessor.” PO Resp. 43 (citing Ex. 2011 ¶ 85).

Patent Owner also contends that Petitioner fails to explain how the combination would be made with a reasonable expectation of success. PO Resp. 43–45. Patent Owner contends that “[n]either Petitioner nor Dr. Franzon provide any analysis of” Alexander’s “acknowledgment that ‘[t]he 3D FPGA model gives rise to a number of new challenges,’ including heat dissipation and heat stress (collectively, ‘thermal issues’).” PO Resp. 44; PO Sur-reply 17–18.

In response to Petitioner’s Reply, Patent Owner more specifically contends that Petitioner does not sufficiently explain why or how one of ordinary skill in the art would have combined Alexander’s 3D FPGA into the Zavracky-Chiricescu-Akasaka combination when the combination “already includes Chiricescu’s FPGA on the first integrated die element and that Alexander’s 3D FPGA architecture is disparate from Chiricescu’s.” PO Sur-reply 16 (reproducing Chiricescu’s Fig. 2 “depicting a separate memory, routing, and RLB layers in the FPGA” and Alexander’s Fig. 2 “depicting stacked 2D FPGA dies using solder bumps”). Patent Owner argues that Petitioner does not sufficiently address using disparate FPGA architecture in

the first and third integrated die elements because Petitioner “fails to explain how the circuitry of Alexander’s 3D FPGA would be laid out, connected to, and operating with the proposed Zavracky-Chiricescu-Akasaka structure, which already includes Chiricescu’s unique FPGA to arrive at the claimed invention.” PO Sur-reply 17.

*c. Analysis*

We determine that Petitioner provides sufficient evidence supporting Petitioner’s asserted reason to combine. Petitioner contended as follows:

[One of ordinary skill in the art] would have known (as Zavracky notes) that multiprocessor systems were needed for “parallel processing applications,” for example, “signal processing applications.” Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, [one of ordinary skill in the art] would have appreciated Alexander’s teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). *Id.* [One of ordinary skill in the art] would have sought out Alexander’s multiple stacked FPGAs to enhance the Zavracky-Chiricescu-Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 43. Petitioner’s evidence includes reasoning provided by Zavracky based on a plain reading of the cited passage. *See, e.g.*, Ex. 1003, 12:13–17 (“This technology is also useful in the microprocessor environment. FIG. 12 presents a stacked microprocessor and random access memory array which is one potential microprocessor embodiment used in parallel processing applications. The first layer 700 is a **microprocessor** which shares random access memory 702 on the second layer, [with] **another microprocessor** 704 located above the random access memory. . . . This configuration lends itself well to use in signal processing applications.” (emphasis added)).

Petitioner's evidence also includes Dr. Franzon's declaration testimony that one of ordinary skill in the art would have used "Alexander's multiple stacked FPGAs to enhance" Petitioner's combination because such stacked FPGA's were preferred because "(1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible)." Pet. 43 (citing Ex. 1002 ¶ 258). We credit Dr. Franzon's testimony that provides well-reasoned explanation and analysis based on quoted passages from a 2000 IEEE article (Ex. 1058) that examined "processors and FPGAs to characterize and compare their computational capabilities" and another reference describing customized parallel hardware. Ex. 1058, 41<sup>25</sup>; Ex. 1051; *see* Ex. 1002 ¶ 258 (quoting Ex. 1058, 43; quoting Ex. 1051, 3:45–67).

In addition, claims 5 and 30 each recite "said third integrated circuit functional element includes another field programmable gate array" (FPGA). Petitioner's arguments and evidence includes Dr. Franzon's testimony that one of ordinary skill in the art would have used "Alexander's multiple stacked FPGAs" because "stacked FPGA's were preferred." Thus, we do not agree with Patent Owner's assertion that "Petitioner's alleged motivation to combine is untethered to the claimed invention." PO Resp. 42–43.

Furthermore, in contrast to Dr. Franzon's well-supported testimony in this regard, Patent Owner's expert, Dr. Souri, in paragraph 84 provides only conclusory statements. For example, Dr. Souri states, without providing explanation or evidence, "[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no

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<sup>25</sup> Citation is to original page numbers of article.

bearing on whether a skilled artisan would have been motivated to combine Alexander with Zavracky-Chiricescu-Akasaka to reach a 3-D processor module having ‘a third integrated circuit functional element [that] includes another field programmable gate array.’” Ex. 2011 ¶ 84. The only citations in paragraph 84 are citations to the claims in the challenged patent and to the Petition’s assertion that Dr. Souri attempts to rebut. Ex. 2011 ¶ 84 (only citing Ex. 1001, claims 5 and 30; Pet. 43). We give little weight to Dr. Souri’s conclusory and unsupported testimony in this regard.

Dr. Souri also testified that “in my opinion there is no reason whatsoever that [one of ordinary skill in the art] would have looked to combine Alexander with Zavracky-Chiricescu-Akasaka” because “Chiricescu, like Alexander, offers FPGAs to enhance parallel processing image and signal tasks of Zavracky’s microprocessor.” Ex. 2011 ¶ 85. As noted above, however, Dr. Franzon provides specific reasons, supported by evidence and uncontroverted in the record, as to why one of ordinary skill in the art “would have viewed Alexander’s teaching of stacked FPGAs as preferable over alternatives” in a multiprocessor system, as Petitioner responds. Pet. Reply 21. Additionally, in Reply, Petitioner cites a patent issued in 1996 that indicates “a stack of 4 FPGA’s, for example, would have the potential of being used to performing a digital task having four times the complexity that a single FPGA could perform” that further supports Dr. Franzon’s that processing tasks were further improved when multiple FPGAs were stacked together. Pet. Reply 22 (quoting Ex. 1027, 2:58–60).

For these reasons, we determine that, Petitioner has provided sufficient evidence of a reason why one of ordinary skill in the art would

have combined Alexander with the Zavracky-Chiricescu-Akasaka combination.

Contrary to Patent Owner’s argument that Petitioner did not describe how to combine the references, Petitioner also indicated in the Petition that “using multiple dies in the stack as taught by Alexander would work in a straightforward manner similar . . . to stacking multiple memories, or multiple microprocessors, as already taught in the Zavracky-Chiricescu-Akasaka Combination.” Pet. Reply 21 (quoting Pet. 44). Petitioner continues in the Petition asserting, “[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result.” Pet. 44 (citing Ex. 1002 ¶¶ 260–61).

The record does not support Patent Owner’s assertions that multiple FPGAs would not work in a straightforward manner and one of ordinary skill in the art would not have had a reasonable expectation of success. *See* PO Resp. 43–44. First, Petitioner’s combination “simply combin[es] the extra FPGA of Alexander with the existing 3-D stack” of the Zavracky, Chiricescu, and Akasaka combination “according to known methods to yield a predictable result.” Pet. 44 (citing Ex. 1002 ¶¶ 260–61). In the words of Dr. Franzon,

the result of this combination would have been predictable, simply combining the extra FPGA of Alexander . . . with the existing 3-D stack according to known methods (the same methods used to attach the other integrated circuit functional elements) to yield a predictable result (two FPGAs in the stack).  
Ex. 1002 ¶ 261. Patent Owner provides no evidence that undermines this persuasive straightforward explanation of how Petitioner proposes to

combine Alexander's FPGA in the Zavracky, Chiricescu, and Akasaka combination.

Turning to Patent Owner's assertion based on Alexander's indication of thermal issue challenges and the need to reduce power consumption to mitigate thermal issues (PO Resp. 44), we agree with Petitioner that one of ordinary skill in the art, in view of Zavracky's teaching of a FPGA with a memory and a microprocessor in Figure 13, "would have understood that combining an FPGA with a memory and another FPGA (as in claims 5 and 30) would **reduce** purported thermal issues, not increase them." Pet. Reply 22 (citing Ex. 1003, 12:29–39, Fig. 13; Ex. 1070 ¶¶ 37–41). Petitioner explains that "FPGAs were more energy-efficient than microprocessors for the same size die, reducing heat." Pet. Reply 22–23 (citing Ex. 1070 ¶¶ 37–41 (citing Ex. 1058, 1082)). We are persuaded by Petitioner's position, which is based on Dr. Franzon's declaration testimony. We credit Dr. Franzon in view of his reasonable explanation and analysis that relies on citations to references that support his testimony. *See* Ex. 1070 ¶¶ 37–41 (citing Ex. 1003, 12:29–39, Fig. 13; Ex. 1058, 43; Ex. 1082).

Petitioner also provides evidence that thermal management was a routine consideration in view of various known ways to address thermal issues. Pet. Reply 23 (citing Ex. 1020, 11 for "describing and citing five 'methods [that] are effective' for thermal management").

For these reasons, we conclude that Petitioner has provided by a preponderance of evidence articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below

that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Alexander would have rendered obvious claims 5 and 30.

*G. Exhibit 1070*

Patent Owner argues that “[p]aragraphs 5–9, 13–41, 59–68, 79–89, and 90–103 from Dr. Franzon’s second declaration (Ex. 1070)” in reply to Patent Owner’s Response are not sufficiently discussed in the Reply. PO Sur-reply 18. Patent Owner contends that “Petitioner provides no substantive discussion of Dr. Franzon’s testimony . . . but instead references Dr. Franzon’s testimony from the abovementioned paragraphs (collectively spanning over roughly 39 pages) based on citation alone or a cursorily parenthetical.” PO Sur-reply 18–19 (identifying Pet. Reply 7, 8, 10, 16, 17, 19, 22, and 23).

Patent Owner contends that “Dr. Franzon’s arguments from his second declaration [Reply Declaration] should not be considered.” PO Sur-reply 19 (citing 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”)); *Gen. Access Sols., Ltd. v. Sprint Spectrum L.P.*, 811 F. App’x 654, 658 (Fed. Cir. 2020) (standing for “upholding the Board’s finding of improper incorporation by reference because, *inter alia*” “‘playing archaeologist with the record’ is precisely what the rule against incorporation by references was intended to prevent”)).

The situation here is different than in *General Access Solutions*, because there, the court noted a problem with identifying a party’s substantive arguments *prior to turning to the declaration at issue*: “To

*identify GAS's substantive arguments*, the Board was forced to turn to a declaration by Struhsaker, *and further to delve into a twenty-nine-page claim chart attached as an exhibit.*" *Gen. Access Sols.*, 811 F. App'x 658 (emphasis added). Here, Patent Owner does not describe or allege any problem with identifying Petitioner's substantive arguments.

In addition, Patent Owner provides a list of Reply Declaration paragraphs and a list of reply pages without identifying with particularity where the identified paragraphs may be found. It appears that not all the paragraphs identified by the Patent Owner are located on any of the identified Reply pages. For example, paragraphs five through nine do not appear to be included in any of the Reply pages identified by Patent Owner. Those paragraphs address the level of ordinary skill in the art. Similarly, Patent Owner identifies paragraphs 59–68 and, of the identified Reply pages, paragraphs 59–66 are referenced on Reply page 19 and paragraphs 65 and 68 are referenced on Reply page 16. Paragraph 67 does not appear to be referenced on any of the Reply pages identified by Patent Owner.

Even setting aside these discrepancies in Patent Owner's Sur-reply, we do not agree with Patent Owner that we should not consider Dr. Franzon's Reply Declaration. Patent Owner makes only general assertions that seem to be based primarily on multiple paragraphs being identified in a citation, which as discussed below we find provide context for Petitioner's arguments. Additionally, Patent Owner does not address the significant overlap in the cited paragraphs with arguments made in the Reply. Moreover, in reaching our decision regarding the patentability of the challenged claims, we exercised judgment as to all the evidence cited by the parties for its relevance, context, and substance, and weighed it accordingly.

We turn now to each page in the Reply identified by Patent Owner as having improperly incorporated arguments. Regarding Reply page 7, Patent Owner identifies paragraphs 79–89 of the Reply Declaration. These paragraphs provide opinions in response to our claim construction discussion in the Institution Decision and those paragraphs are referenced on page 7 of the Reply in the section asserting that Petitioner’s Zavracky, Chiricescu, and Akasaka combination meets the Board’s claim interpretation. Paragraphs 83 and 84 discuss Zavracky’s inter-layer connections, and are substantially similar to Petitioner’s arguments on page 5 of the Reply. Paragraph 85 discusses Chiricescu and is substantially similar to Petitioner’s arguments on page 6 of the Reply. Paragraphs 87 and 88 discuss Akasaka and are substantially similar to Petitioner’s arguments on pages 6 and 7 of the Reply. Notably, the arguments in this section of the Reply (pages 5–7) principally rely on the express disclosures of the references. Petitioner’s reference to paragraphs 79–89 of the Reply Declaration serve to confirm the correctness of Petitioner’s understanding of the plain language of the references presented within this section of the Reply.

Petitioner’s reference on page 8 of the Reply to paragraphs 90–93 of the Reply Declaration follows a similar pattern. Petitioner on page 8 of the Reply asserts that the Zavracky, Chiricescu, and Akasaka combination increases speed in the same five ways as the challenged patent and identifies five citations to the challenged patent, as does paragraph 91 in the Reply Declaration. The additional three cited paragraphs provide additional context—including two conclusions (paragraphs 90 and 93) and discussion of testimony by another Patent Owner expert (paragraph 91), which was not necessary for our decision regarding patentability.

Page 10 of the Reply cites paragraphs 94–103 of the Reply Declaration in asserting the Zavracky, Chiricescu, and Akasaka combination meets “the functional to accelerate” limitations under Patent Owner’s proposed interpretation of what structure the claims require in a wide configuration data port. Pet. Reply 9–10. The Reply Declaration paragraphs 94 and 95 directly address Petitioner’s Reply arguments regarding Patent Owner’s expert testimony, including Dr. Chakrabarty<sup>26</sup> regarding the ordinary and custom meaning of a wide configuration data port. including citing substantially the same portions of the relevant deposition transcript as Petitioner in its Reply. Pet. Reply 9 (quoting Ex. 1075, 157:23–158:3); Ex. 1070 ¶¶ 94–95 (citing Ex. 1075, 163–64, 157–58). Paragraph 103 largely overlaps the discussion of Zavracky and Chiricescu on pages 9–10 of the Reply. Petitioner’s Reply is ambiguous as to what portions of the Reply Declaration are cited because the Reply Declaration presents paragraphs 94, 95, and 103, and then presents paragraphs 96–102, which address claim limitations in the ’226 patent not at issue here. Thus, a reasonable inference is that the Reply citation of 94–103 means the sequential pages that include only paragraphs 94, 95, and 103, which largely mirror Petitioner’s arguments on pages 9 and 10 of the Reply.

On page 16 of the Reply, Petitioner cites two paragraphs of the Reply Declaration (65 and 68) with a clear parenthetical explanation (“Dr. Franzon

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<sup>26</sup> Dr. Chakrabarty was Patent Owner’s expert in IPR2020-01020, IPR2020-01021, and IPR20220-01020. Exhibit 1071 in this proceeding is Dr. Chakrabarty’s deposition in those cases. Petitioner uses Dr. Chakrabarty’s deposition testimony here to undermine Patent Owner’s position regarding a wide configuration data port. Pet. Reply 9; Ex. 1070 ¶¶ 94–95 (citing Ex. 2011 ¶ 55; citing Ex. 1075, 163–64, 157–58).

noting the routine use of on-chip area-wide connections in 3D stacks, including his prior work, Ex. 1020”).

On page 17 of the Reply, Petitioner cites paragraphs 13–28 with a clear parenthetical explanation (“Dr. Franzon rebutting Dr. Souris’s testimony as to each purported issue with citations to evidence.”). This supports the prior sentence asserting the “TSV interconnection issues” identified by Patent Owner were “at most normal engineering issues” by asserting that each issue was rebutted by Dr. Franzon. We understand Petitioner in this context to point to these paragraphs, not for the detailed rebuttals, but for the fact that Dr. Franzon analyzed the issues identified by Dr. Souris. Similarly, in note 7 on page 19 of the Reply, Petitioner identifies paragraphs 59–66 in the parenthetical—“Dr. Franzon rebutting Dr. Souris’s opinions re: same”—as supporting the assertion that Patent Owner “describes Akasaka’s teaching inaccurately.” Again on page 23 of the Reply, in the context of Petitioner’s contention that thermal issues were a routine consideration, paragraphs 29–41 of Dr. Franzon’s Supplemental Declaration are cited with the parenthetical explanation: “Dr. Franzon rebutting Dr. Souris’s ipse dixit with evidence of known ways to address thermal issues.”

On pages 22 of the Reply, Petitioner references paragraphs 37–41 with a parenthetical explanation: “Dr. Franzon noting that use of a second FPGA die would have reduced any purported thermal issues as compared to a similar stack with a microprocessor.” This directly follows and supports Petitioner’s contention: “Given this teaching in Zavracky, [one of ordinary skill in the art] would have understood that combining an FPGA with a

memory and another FPGA (as in claims 5 and 30) would reduce purported thermal issues, not increase them.”

Accordingly, for these reasons, the examination of the citations identified by Patent Owner in full context, reveals that Petitioner’s use of and citation to Dr. Franzon’s testimony is not improper.

### III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.<sup>27</sup> In summary:

| <b>Claims</b>                 | <b>35 U.S.C.<br/>§</b> | <b>References/<br/>Basis</b>                 | <b>Claims<br/>Shown<br/>Unpatent-<br/>able</b> | <b>Claims<br/>Not<br/>shown<br/>Unpatent<br/>-able</b> |
|-------------------------------|------------------------|----------------------------------------------|------------------------------------------------|--------------------------------------------------------|
| 1, 2, 4, 6, 26, 27,<br>29, 31 | 103(a)                 | Zavracky,<br>Chiricescu,<br>Akasaka          | 1, 2, 4, 6, 26,<br>27, 29, 31                  |                                                        |
| 3, 28                         | 103(a)                 | Zavracky,<br>Chiricescu,<br>Akasaka,<br>Sato | 3, 28                                          |                                                        |

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<sup>27</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

| <b>Claims</b>              | <b>35 U.S.C.<br/>§</b> | <b>References/<br/>Basis</b>                      | <b>Claims<br/>Shown<br/>Unpatent-<br/>able</b> | <b>Claims<br/>Not<br/>shown<br/>Unpatent<br/>-able</b> |
|----------------------------|------------------------|---------------------------------------------------|------------------------------------------------|--------------------------------------------------------|
| 5, 30                      | 103(a)                 | Zavracky,<br>Chiricescu,<br>Akasaka,<br>Alexander | 5, 30                                          |                                                        |
| <b>Overall<br/>Outcome</b> |                        |                                                   | 1–6, 26–31                                     |                                                        |

#### IV. ORDER

In consideration of the foregoing, it is hereby  
ORDERED that claims 1–6 and 26–31 of the '214 patent are  
unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision,  
parties to the proceeding seeking judicial review of the Decision must  
comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01567  
Patent 7,126,214 B2

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