

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and
TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC,
Patent Owner.

IPR2020-01571¹
Patent 6,781,226 B2

Before KARL D. EASTHOM, BARBARA A. BENOIT, and
SHARON FENICK, *Administrative Patent Judges*.

FENICK, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00738 and has been joined as a party to IPR2020-01571. *See also* Paper 38 (order dismissing-in-part Taiwan Semiconductor Manufacturing Co. Ltd. as a party with respect to claims 13, 14, 16–23, and 25–30).

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–30 (the “challenged claims”) of U.S. Patent No. 6,781,226 B2 (Ex. 1001, “the ’226 patent”). Petitioner filed a declaration of Dr. Paul Franzon (Ex. 1002) with its Petition. Arbor Global Strategies LLC (“Patent Owner”), filed a Preliminary Response (Paper 7). We determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims and we instituted this proceeding on March 5, 2021, as to all challenged claims and all grounds of unpatentability. Paper 12 (“Dec. on Inst.”).

After institution, Patent Owner filed a Patent Owner Response (Paper 18, “PO Resp.”) and a declaration of Dr. Shukri J. Sourì in support (Ex. 2006); Petitioner filed a Reply (Paper 22, “Pet. Reply”) and a second declaration of Dr. Franzon in support (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 26, “PO Sur-reply”). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 32 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

As the real parties-in-interest, Petitioner identifies only itself. Pet. 69. Taiwan Semiconductor Manufacturing Co. Ltd. identifies itself and TSMC

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North America as real parties-in-interest. *See* IPR2021-00393, Paper 1, 69. Patent Owner identifies only itself as a real party-in-interest. Paper 4, 1.

B. Related Proceedings

The parties identify *Arbor Global Strategies LLC v. Xilinx, Inc.*, No. 19-CV-1986-MN (D. Del.) (filed Oct. 18, 2019) as a related infringement action involving the '226 and three related patents, U.S. Patent No. RE42,035 E (the "'035 patent"), U.S. Patent No. 7,282,951 B2 (the "'951 patent") and U.S. Patent No. 7,126,214 B2 (the "'214 patent"). *See* Pet. 69; Paper 4, 1. Petitioner "contemporaneously fil[ed] [*inter partes* review] petitions challenging claims in each of these patents," namely IPR2020-01567 (challenging the '214 patent), IPR2020-01568 (challenging the '951 patent), and IPR2020-01570 (challenging the '035 patent). Pet. 69.

The parties also identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) ("the Samsung action") as a related infringement action involving the '035, '951, and '226 patents. Pet. 69; Paper 4, 1. Subsequent to the complaint in the Samsung action, Samsung Electronics Co., Ltd. ("Samsung") filed petitions challenging the three patents, and the Board instituted on all challenged claims, in IPR2020-01020, IPR2020-01021, and IPR2020-01022 ("the 1022IPR"). *See* IPR2020-01020, Paper 11 (decision instituting on claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the '035 patent)); IPR2020-01020, Paper 30 (final written decision finding all challenged claims unpatentable); IPR2020-01021, Paper 11 (decision instituting on challenged claims 1, 4, 5, 8, 10, and 13–15 the '951 patent); IPR2020-01021, Paper 30 (final written decision finding all challenged claims unpatentable); IPR2020-01022, Paper 12 (decision instituting on

challenged claims 13, 14, 16–23, and 25–30 of the '226 patent) (Ex. 2004); IPR2020-01022, Paper 34 (final written decision finding all challenged claims unpatentable).

C. The '226 Patent

The '226 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '226 patent, this arrangement “allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost.” *Id.*

Figure 4 follows:

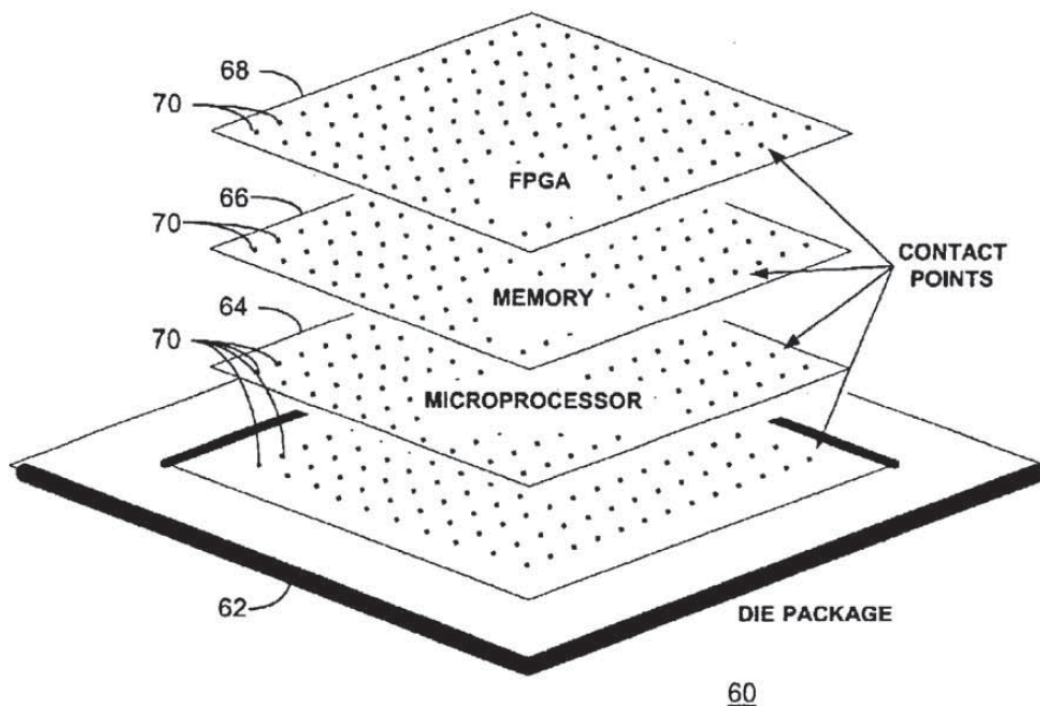


Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 66, memory die 66, and microprocessor die 64, interconnected using contact holes 70. *Id.* at 4:9–33.

The '226 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” *See* Ex. 1001, 1:19–35. Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA), making the processor faster than one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See id.* A “reconfigurable processor” provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See id.*

D. Illustrative Claims 1 and 10

The Petition challenges claims 1–30. Of these claims, 1, 7, 13, and 22 are independent and claims 2–6, 8–12, 14–21, and 23–30 depend from one of the challenged independent claims either directly or indirectly. Claims 1, 7, 13 and 22, reproduced below with bracketed numbering added for reference, illustrate the challenged claims at issue:

1. A processor module comprising:
 - [1.1] at least one field programmable gate array integrated circuit die element including a programmable array; and
 - [1.2] at least one microprocessor integrated circuit die element stacked with and electrically coupled to said programmable array of said at least one field programmable gate array integrated circuit die element,
 - [1.3] such that processing of data shared between the microprocessor and the field programmable gate array is accelerated.

Ex. 1001, 6:16–26.

7. A processor module comprising:

at least one field programmable gate array integrated circuit die element including a programmable array; and

at least one microprocessor integrated circuit die element stacked with and electrically coupled to said programmable array of said at least one field programmable gate array integrated circuit die element,

[7.3] the at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the at least one microprocessor integrated circuit die element during manufacture and prior to completion of the module packaging.

Ex. 1001, 6:45–57, Cert. of Corr.

13. A processor module comprising:

at least a first integrated circuit die element including a programmable array;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[13.4] means for reconfiguring the programmable array within one clock cycle.

Ex. 1001, 7:9–22.

22. A processor module comprising:

at least a first integrated circuit die element including a programmable array and a plurality of configuration logic cells;

at least a second integrated circuit die element including a processor stacked with and electrically coupled to said

programmable array of said first integrated circuit die element;

at least a third integrated circuit die element including a memory stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit die elements respectively; and

[22.4] means for updating the plurality of configuration logic cells within one clock cycle.

Ex. 1001, 8:4–17.

E. The Asserted Grounds

Petitioner challenges claims 1–30 of the '226 patent on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1–6	103 ²	Zavracky, ³ Chiricescu, ⁴ Akasaka ⁵
7–12	103	Zavracky, Chiricescu,

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Petitioner and Patent Owner each use December 5, 2001 in their analysis. Pet. 3, 5; Ex. 1002 ¶¶ 27–29; PO Resp. 10; Ex. 2006 ¶ 25. We assume that the '226 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment) and that the pre-AIA version of § 103 applies.

³ Zavracky et al., US 5,656,548, issued Aug. 12, 1997. Ex. 1003.

⁴ Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98. Ex. 1004.

⁵ Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Iss. 12, pp. 1703–1714, Dec. 1986, ISSN 0018-9219. Ex. 1005.

Claims Challenged	35 U.S.C. §	References
		Akasaka, Satoh ⁶
13–30	103	Zavracky, Chiricescu, Akasaka, Trimberger ⁷

II. ANALYSIS

Petitioner challenges claims 1–30 as obvious based on the grounds listed above. Patent Owner disagrees.

A. Legal Standards

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one

⁶ Satoh, PCT App. Pub. No. WO00/62339, published Oct. 10, 2000. Ex. 1008 (English translation).

⁷ Steve Trimberger, Dean Carberry, Anders Johnson, and Jennifer Wong, *A Time-Multiplexed FPGA*, Proceedings of the 1997 IEEE International Symposium on Field-Programmable Custom Computing Machines, April 1997, ISBN 0-8186-8159-4. Ex. 1006.

of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Franzon, Petitioner contends that [t]he person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’226 patent would have been a person with a Bachelor’s Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication.

Pet. 5 (citing Ex. 1002 ¶¶ 58–60).

Patent Owner asserts that

[a] person of ordinary skill in the art (“POSITA”) around December 5, 2001 (the earliest effective filing date of the ’226 Patent) would have had a Bachelor’s degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 10 (citing Ex. 2006 ¶ 25).

As we did in the Decision on Institution, we adopt Petitioner’s proposed level of ordinary skill in the art, which comports with the teachings of the ’226 patent and the asserted prior art. *See* Dec. on Inst. 21. Patent Owner’s proposed level overlaps substantially with Petitioner’s proposed level. Even if we adopted Patent Owner’s proposed level, the outcome would remain the same.

C. Claim Construction

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under the same standard

applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure.

Phillips v. AWH Corp., 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

“There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner and Patent Owner each agree that both “means for reconfiguring the programmable array within one clock cycle” (limitation 13.4 in claim 13) and “means for updating the plurality of configuration logic cells within one clock cycle” (limitation 22.4 in claim 22) are means-plus-function limitations and should be construed as per 35 U.S.C. § 112, ¶ 6. Pet. 10–13; PO Resp. 11.

Both of these limitations listed above recite “means” and further recite a function, thus creating a presumption that 35 U.S.C. § 112, ¶ 6 applies. *See* 35 U.S.C. § 112, ¶ 6 (“An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.”); *see also Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc in relevant part) (quoting *Personalized Media Commc’ns, LLC v. Int’l Trade Comm’n*, 161 F.3d 696, 703 (Fed. Cir. 1998)) (holding that “use of the word ‘means’ creates a presumption that § 112, ¶ 6 applies”). We agree with the parties

that these limitations are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6. Pet. 11, 13; PO Resp. 11.

Patent Owner additionally argues that we should construe “wide configuration data port,” which appears in challenged claims 14 and 23, and which additionally appears in each party’s proposals for the structure of the means-plus-function limitations described above. Pet. 11–13; PO Resp. 19–25; Pet. Reply 2–6; PO Sur-reply 1–5. Because of this, we begin with this construction and then discuss construction of the means-plus-function terms.

1. “wide configuration data port”

While neither party proposed construction of this term in pre-institution briefing, Patent Owner did propose its construction in its Response, and the parties each briefed the construction before the oral hearing. PO Resp. 14–20; Pet. Reply 3–6; PO Sur-reply 1–5.

a. Patent Owner’s Position

Patent Owner argues that the term “wide configuration data port” should be construed as “a configuration data port that allows the parallel updating of logic cells in a programmable array through use of buffer cells.” PO Resp. 15–19 (citing Ex. 1001, 4:45–59, Fig. 5; Ex. 2006 ¶¶ 32, 40–44); In support of this construction, Patent Owner cites as intrinsic evidence the ’226 patent’s disclosure that the wide configuration data port “is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cells 88.” Ex. 1001, 4:51–54 (quoted at PO Resp. 15). Patent Owner argues that the ’226 patent describes, as background and in contrast to the use of a wide configuration data port, the use of a “relatively narrow” serial data port that accesses configuration memory serially. *Id.* at 17–19 (citing Ex. 1001, 3:63–4:9, Fig. 5; Ex. 2006 ¶¶ 42–44).

Patent Owner contends that the '226 patent disclosure distinguishes the wide configuration data port because it allows the updating of logic cells in parallel through use of buffer cells, which Patent Owner argues is “a key distinguishing feature of the wide configuration data port.” *Id.* at 18–19. Patent Owner argues that its experts “have been consistent that the word ‘wide’ in this term requires a sufficient number, and appropriate arrangement, of connections between the memory die and the programmable array to permit parallel updating of the array.” PO Sur-reply 2 (citing Ex. 2006 ¶ 38; Ex. 1076, 42:3–20).

Patent Owner argues that the buffer cells must be part of a proper construction. Patent Owner contends that “the wide configuration data port 82 achieves single cycle reconfiguration of the programmable array *by loading reconfiguration data into buffer cells 88 in parallel*, even while the programmable array is operational.” PO Resp. 16 (emphasis added). In the Sur-reply, however, Patent Owner contends that it is not the parallel loading of reconfiguration data into buffer cells that allows single cycle reconfiguration, but rather the updating of the logic cells in parallel, using the data in the buffer cells. PO Sur-reply 4–5. Patent Owner further supports its contention that the buffer cells must be included with the die-area connections in the construction of “wide configuration data port” because “Petitioner fails to point to any embodiment in the '226 Patent in which the vertical die-area connections and the buffer cells are not used in conjunction and therefore cannot credibly claim that Arbor’s construction excludes such an embodiment.” *Id.* at 3.

b. Petitioner's Position

Petitioner, in its Reply, argues that the term should have its plain and ordinary meaning. Pet. Reply 3–4. Petitioner argues that the plain and ordinary meaning of a configuration data port is “a port for configuration data, i.e., a connection or place through which configuration data is transferred.” *Id.* (citing Ex. 1002 ¶¶ 96–97; also citing Ex. 1075, 163:8–163:21 (deposition of Patent Owner’s expert Dr. Krishnendu Chakrabarty in the 1022IPR)). Petitioner argues that the ’226 patent shows a configuration data port that is wide because it includes direct connections / paths for configuration data to be loaded, contrasting this with the Figure 3 prior art embodiment of the ’226 patent, which is not “wide.” *Id.* at 3–4 (citing Ex. 1002 ¶¶ 96–97).

With respect to Patent Owner’s proposed construction, Petitioner argues that Arbor’s proposal improperly includes the buffer cells, which are shown and described in the ’226 patent as separate elements from the wide configuration data port. *Id.* at 4 (citing Ex. 1001, 4:50–54, Fig. 5). Petitioner argues that the construction is contradicted by testimony presented by Patent Owner’s expert Dr. Chakrabarty in the 1022IPR, and that Dr. Souris did not read this testimony. *Id.* at 5 (citing Ex. 1076, 73:22–74:7). Petitioner argues Patent Owner’s construction, in its use of the term “allows,” is ill-defined, and that Patent Owner describes elements such as logic cells, configuration memory, and a large number of die-area contacts as required, but that these elements are not included in the proposed construction. *Id.* at 4–5. Lastly, Petitioner argues that Patent Owner incorrectly asserts that the loading of reconfiguration data into buffer cells occurs in one clock cycle, but that it is the updating of the logic cells that

occurs in one clock cycle in the '226 patent. *Id.* at 6 (citing PO Resp. 16; Ex. 1001, 4:55–59; Ex. 1070 ¶ 111).

c. Analysis and Conclusion

We determine that one of ordinary skill in the art would not understand the ordinary and customary meaning of “wide configuration data port” to include buffer cells or configuration memory cells, and construction in accordance with the prosecution history would likewise not require the inclusion of buffer cells or configuration memory cells. We also note that Patent Owner’s proposed construction (“a configuration data port that allows the parallel updating of logic cells in a programmable array through use of buffer cells”) contains some ambiguity in not making clear how buffer cells *allow* parallel updating, and we decline to provide a construction including this ambiguity.

The '226 patent does not make extensive use of the term “wide configuration data port.” With the exception of the claims, which do not provide additional context, the references in the '226 patent are the labelling of element 82 of Figure 5 as “very wide configuration data port” and the paragraph referencing this figure, cited extensively by both parties, in which the specification describes the following:

With reference additionally now to FIG. 5, a corresponding functional block diagram of the configuration cells 80 of the reconfigurable processor module 60 of the preceding figure is shown wherein the FPGA 70 may be totally reconfigured in one clock cycle by updating all of the configuration cells in parallel. As opposed to the conventional implementation of FIG. 3, a wide configuration data port 82 is included to update the various logic cells 84 through an associated configuration memory 86 and buffer cell 88. The buffer cells 88 are preferably a portion of the memory die 66 (FIG. 4). In this manner, they can be loaded while the FPGA 68

comprising the logic cells 84 are in operation. This then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of its configuration logic cells 84 updated in parallel. Other methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory (“RAM”) than can be offered within the FPGA die 68 itself.

Ex. 1001, 4:45–65 (cited or quoted in whole or part at PO Resp. 15–16; Pet. Reply 4, 6; PO Sur-reply 3–5).

Patent Owner, in focusing on this portion of the ’226 patent disclosure, does not adequately explain why buffer cells and configuration memory cells must be included in the proper construction of “wide configuration data port,” and seeks to import a functional description of the use of a wide configuration data port (“that *allows parallel updating* of logic cells in a programmable array through use of buffer cells”) into the claim construction. PO Resp. 15–17; PO Sur-reply 2–4. While the discussion in the ’226 patent describes an example of a wide configuration data port used in a specific way that aligns with Patent Owner’s proposal (Ex. 1001, 4:45–59), other examples of the use of a wide configuration data port are included (*id.* at 4:59–65), and therefore we do not agree that one of ordinary skill would understand this use to be part of the construction of the term.

We agree with Petitioner that the proper construction of the term does not require buffer cells. *See* Pet. Reply 4–6. Rather, we note that the specification of the ’226 patent contrasts loading of data to an FPGA in a byte serial fashion through a narrow port, which “results in [] long reconfiguration times,” with the use of a wide configuration data port, and therefore we determine that one of ordinary skill would understand the wide

configuration data port, in contrast to the byte serial “relatively narrow” port, to include parallel connections between cells in the dies. *See* Ex. 1001, 4:3–9. This additionally is consistent with certain arguments by Patent Owner, for example in the Patent Owner’s Response, which opens with a discussion of the “innovative” processor’s arrangement of die-area contacts, such as through-silicon vias, “into a wide configuration data port” and we find that description more consistent with the proper construction of this term. PO Resp. 1–2; *see also* PO Sur-reply 2–3 (“Arbor’s experts have been consistent that the word ‘wide’ in this term requires a sufficient number, and appropriate arrangement, of connections between the memory die and the programmable array to permit parallel updating of the array.”)

In the Final Written Decision issued in the 1022IPR, we construed “wide configuration data port” to be “a configuration data port connecting in parallel cells on one die element to cells on another die element.” IPR2020-01022, Paper 34 at 13–16 (PTAB Nov. 24, 2021). During the hearing, we referred to that decision, indicated our interest in the Petitioner’s and Patent Owner’s positions on its claim constructions, and the parties discussed our constructions in that proceeding to some degree in their arguments. Tr. 6:1–6, 25:12–30:6, 43:6–23, 61:18–63:10.

The ’226 patent describes updating the logic cells of an FPGA in one clock cycle to reconfigure the FPGA by loading associated configuration memory from buffer cells, preferably located on a different die element. Ex. 1001, 4:45–59. Additionally, the ’226 patent describes that doing this “takes advantage of the significantly increased number of connections to the cache memory die.” *Id.* at 4:59–65. This construction is supported by Petitioner’s expert’s description of the plain and ordinary meaning of “configuration data

port” as “a connection or place through which configuration data is transferred” and that in the prior art wide buses were made possible by 3-D stacking. *See, e.g.*, Ex. 1002 ¶¶ 54, 96–97. This construction additionally is supported by Patent Owner’s expert’s description that “the inventors of the ’226 Patent arranged die-area contacts of the SDH [(stacked die hybrid)] processor, such as through-silicon vias (‘TSVs’), into a wide configuration data port that reconfigures them in a parallel scheme.” Ex. 2006 ¶ 32; *see also* PO Resp. 1–2; PO Sur-reply 4–5 (“the wide configuration data port . . . includes a large number of die-area interconnections (*e.g.*, TSVs) that interconnect stacked chips”); Ex. 1075, 157:23–158:3, 163:8–163:21 (Patent Owner’s expert in the 1022 IPR). The specification supports a construction of the wide configuration data port as a configuration data port that makes connections between die elements in parallel. Ex. 1001, 3:33–37, 4:45–65; *see also id.* at code (57) (“significant acceleration in the sharing of data between the microprocessor and the FPGA element”).

The ’226 patent describes the loading of buffer cells, preferably on the memory die, while the programmable array is in operation, with the configuration logic cells then updated in parallel from the buffer cells through the significantly increased number of connections for reconfiguration in one clock cycle. Ex. 1001, 4:45–59. But none of the challenged claims requires configuring or updating while the programmable array/FPGA is in operation. And the specification shows that the buffer cells are not part of the wide configuration data port. *See id.* at Fig. 5. They are described, rather, as preferably part of the memory die. *Id.* at 4:54–55. We determine that the specification supports a construction that the parallel connection between die elements are between cells on each die element.

This parallel connection implies that cells on one die are connected in parallel to cells on another die, for example, buffer cells or configuration memory cells. *Id.* at 4:50–55, Fig. 5.

For these reasons, we construe “wide configuration data port” as “a configuration data port connecting in parallel cells on one die element to cells on another die element.”

2. *Limitation 13.4 – “means for reconfiguring the programmable array within one clock cycle”*

The first step in construing a means-plus-function claim element is to identify the recited function in the claim element. *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003). The second step is to look to the specification and identify the corresponding structure for that recited function. *Id.*

Petitioner argues that the recited function for limitation [13.4] is “reconfiguring the programmable array within one clock cycle.” Pet. 11. Patent Owner agrees. PO Resp. 11. We also agree. *See Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999) (“[35 U.S.C. § 112, ¶ 6] does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.”)

We next review the ’226 patent to determine the corresponding structure for the identified function. Our preliminary determination in the Decision on Institution was that the correct corresponding structure would be “a wide configuration data port interconnecting a memory and the programmable array using contact points distributed through the first integrated circuit die element and the third integrated circuit die element.” Dec. on Inst. 23–29. In the Final Written Decision in the 1022 IPR, we determined that the correct corresponding structure is “a wide configuration

data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.” IPR2020-01022, Paper 34 at 17–21; *see* Tr. 6:1–6, 25:12–30:6, 43:6–23, 61:18–63:10 (raising and/or discussing constructions from the Final Written Decision in the 1022 IPR).

In the Petition, Petitioner proposed two structures from the ’226 specification as the corresponding structure: “a wide configuration data port [used] to update the various logic cells through an associated configuration memory and buffer cell” and “a stacked FPGA die and memory die interconnected by a wide configuration data port using contact points distributed throughout the dies.” Pet. 11–13. In Reply, Petitioner agrees with our preliminary determination, but in the alternative refers to the two structures discussed in the Petition. Pet. Reply 2.

Patent Owner proposes that the structure is simply a “wide configuration data port,” according to its construction of that term, which includes buffer cells. PO Resp. 11–20; PO Sur-reply 5 (“[T]he buffer cells connected in parallel (using die-area interconnections) with the memory configuration cells allow for FPGA to be totally reconfigured in one clock cycle.”). Patent Owner contends that what allows for the reconfiguration in one clock cycle is “buffer cells connected in parallel . . . with the memory configuration cells” “using die-area connections.” PO Sur-reply 5.

“While corresponding structure need not include all things necessary to enable the claimed invention to work, it must include all structure that actually performs the recited function.” *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). Conversely, structural features that do not actually perform the recited

function do not constitute corresponding structure and thus do not serve as claim limitations. *Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc.*, 145 F.3d 1303, 1308–09, (Fed. Cir. 1998); *see B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997) (“[S]tructure disclosed in the specification is ‘corresponding’ structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.”).

Patent Owner’s arguments regarding buffer cells connected with memory configuration cells using die-area interconnections requires that the buffer cells be located on a different die than the memory configuration cells, but the ’226 patent discloses only that “[t]he buffer cells 88 are preferably a portion of the memory die 66” and not that they always are on the memory die, and also that the significantly increased number of connections to the cache memory die may allow the cache memory die to replace configuration bit storage on the FPGA die. Ex. 1001, 4:50–54, 4:59–63. Thus, we decline to require in the corresponding structure that buffer cells or configuration memory are included on any die element.

Rather, we find that what is disclosed as actually performing the recited function of “reconfiguring the programmable array within one clock cycle” is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.” The support for this is found in the ’226 patent’s comparison of the long reconfiguration times through a narrow port (Ex. 1001, 4:3–9) with the time to reconfigure through a wide configuration data port with a significantly increased number of connections (*id.* at 4:45–65), and the implementation of this in a module that has multiple dies

“which have a number of corresponding contact points, or holes, 70 formed throughout the area of the [die] package” (*id.* at 4:9–20). The use of a wide configuration data port, as per our construction, implicates two die elements. This was reflected in our preliminary claim construction, for which the corresponding structure described “contact points distributed through the first integrated circuit die element and the third integrated circuit die element.” Dec. on Inst. 29. As the function is “reconfiguring the programmable array within one clock cycle,” one of the die elements is the first integrated circuit die element, which includes the programmable array.

We acknowledge that, in the Samsung litigation, the District Court for the Eastern District of Texas has construed this limitation (and limitation 22.4). Ex. 2005.⁸ The District Court construed the function for this limitation identically, and the corresponding structure as “wide configuration data port 82, and contact points formed throughout the area of each die element; and equivalents thereof.” *Id.* at 8–18. The chief distinction between this construction and the one that we adopt is the inclusion of all die elements in the District Court claim construction, rather than only the first die element (including the programmable array) and one additional die element in ours. Our patentability determination here would be the same

⁸ We additionally acknowledge the construction for certain additional limitations in the challenged claims, which the parties do not address construction of, and which we do not herein construe. Ex. 1036, 18–25 (“processor module”), 25–37 (“programmable array”), 38–44 (“stacked with and electrically coupled to”), 44–49 (“contact points distributed throughout the surfaces of said die elements”). However, the patentability determination here would be the same were we to explicitly adopt the construction provided by the District Court for those terms.

were we to adopt the construction provided by the District Court for the corresponding structure of the means-plus-function limitations.

For the reasons discussed above, we determine that, for means-plus-function limitation 13.4 of claim 13, the function is “reconfiguring the programmable array within one clock cycle,” and the corresponding structure is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.”

3. Limitation 22.4 – “means for updating the plurality of configuration logic cells within one clock cycle”

Petitioner and Patent Owner refer back to or recapitulate their arguments with respect to limitation 13.4 in their arguments for the function and structure of means-plus-function claim limitation 22.4. Pet. 13; PO Resp. 11–20; Pet. Reply 2; PO Sur-reply 5. To support arguments regarding this claim term, the parties cite no additional disclosure other than that previously discussed, and we agree that the previously discussed disclosure supports the construction of claim limitation 22.4. Claim 22 differs from claim 13 in several respects, including the inclusion of a plurality of configuration logic cells in the first integrated circuit die element. Limitation 22.4 differs from limitation 13.4 in its statement of function (“updating the plurality of configuration logic cells” rather than “reconfiguring the programmable array”). The configuration logic cells referenced are included in the first integrated circuit die element, and thus here too, the corresponding structure specifies the first integrated circuit die element is included in the description of the structure. Ex. 1001, 8:4–17.

For the reasons presented above, we find that, for means-plus-function limitation 22.4 of claim 22, the function is “updating the plurality of

configuration logic cells within one clock cycle,” and the corresponding structure is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.”

4. Limitation 1.3 – “such that processing of data shared between the microprocessor and the field programmable gate array is accelerated”

While neither party explicitly requests construction of this claim limitation, certain of the arguments presented by the parties relate to their different understandings of this limitation.

Patent Owner presents arguments indicating that it interprets “data shared between the microprocessor and the field programmable gate array” in limitation 1.3 to require more than data being transferred from the microprocessor to the FPGA. PO Resp. 30–36; PO Sur-reply 7–8. Patent Owner argues that a showing by Petitioner that the output data of a microprocessor is sent to the FPGA would not satisfy this limitation, because no data is described as being processed by both the microprocessor and the FPGA. PO Resp. at 31–32 (citing Ex. 2006 ¶ 65); PO Sur-reply 7–8. Patent Owner argues that the ’226 patent explicitly describes memory that is equally accessible by both a microprocessor and an FPGA with equal speed, asserting that this too is required. PO Resp. 34–36 (citing Ex. 1001, 4:34–44; Ex. 2006 ¶ 69); PO Sur-reply 7–8 (citing Ex. 1001, 1:62–2:3, 2:50–54, 4:34–44; Ex. 2006 ¶ 69). Patent Owner’s expert quotes the description of the embodiment in Figures 4 and 5 of the ’226 patent as including a memory “accessible by both the microprocessor 64 and the FPGA 68 with equal speed” and indicates that the “references fail” because they do not provide

data shared between an FPGA and a microprocessor and accessible to each with “anything approximating ‘equal speed.’” Ex. 2006 ¶¶ 69–70.

Petitioner argues that “there is no reasonable argument that data transferred back and forth between the processor and the programmable array is not being shared between them” and that Patent Owner’s arguments improperly exclude direct sharing of data between the microprocessor and the FPGA. Pet. Reply 7–8 (citing Ex. 1001, code (57), 2:50–54; Ex. 1070 ¶¶ 73–74).

We agree with Petitioner that this limitation does not require a memory accessible by both a microprocessor and FPGA with equal speed, or that the same data be processed by both the microprocessor and the FPGA. While Patent Owner is correct that the ’226 patent describes the stacking of a memory die in between a processor die and an FPGA die in the embodiment of Figures 4 and 5, no memory die is claimed or mentioned in claim 1. Additionally, claim 2, which depends from claim 1 and further requires a memory IC die element, requires only that that memory IC die element be connected to one or the other of the FPGA IC die element or the microprocessor IC die element of claim 1. Ex. 1001, 6:27–32. The ’226 patent specification describes one embodiment in which memory on a cache memory die is accessible by a microprocessor and FPGA with equal speed; however, we do not read this requirement into claim 1, which does not require a memory IC die element. *See id.* at 4:34–39.

Additionally, the ’226 patent specification provides no support for Patent Owner’s contention that the same data must be processed by the microprocessor and the FPGA or any description of this occurring. The specification describes “accelerating the sharing of data between the

microprocessor and the FPGA.” Ex. 1001, code (57), 2:50–57. The specification additionally presents instances in which data is transferred from one element to the other and processed/used by the recipient after the transfer, for example, the use of transferred data to reconfigure the FPGA, and the FPGA providing test stimulus for the microprocessor during manufacturing. *Id.* at 4:34–65, 5:5–15. Each of these describes only sharing of data from one die component to another, and not equal accessibility or any mutual processing of the same data.

Therefore, while we do not provide an explicit construction of “such that processing of data shared between the microprocessor and the field programmable gate array is accelerated,” we determine that the correct construction does not require a memory that is equally accessible by the microprocessor and the field programmable gate array, that the correct construction does not require that some data be processed by both the microprocessor and the field programmable gate array, and that the correct construction does not require data to be accessed at equal or approximately equal speed by the microprocessor and the field programmable gate array.

5. No additional constructions

No other terms require explicit construction. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness, Claims 1–6

Petitioner contends the subject matter of claims 1–6 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 14–41. Patent Owner disputes Petitioner’s contentions. PO Resp. 30–44.

1. Zavracky

Zavracky describes “a multi-layered structure” including a “microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure.” Ex. 1003, code (57). Zavracky’s “invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing.” *Id.* at 2:5–10. Zavracky includes numerous types of stacked elements, including “programmable logic devices” (PLDs) stacked with “memory” and “microprocessors.” *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

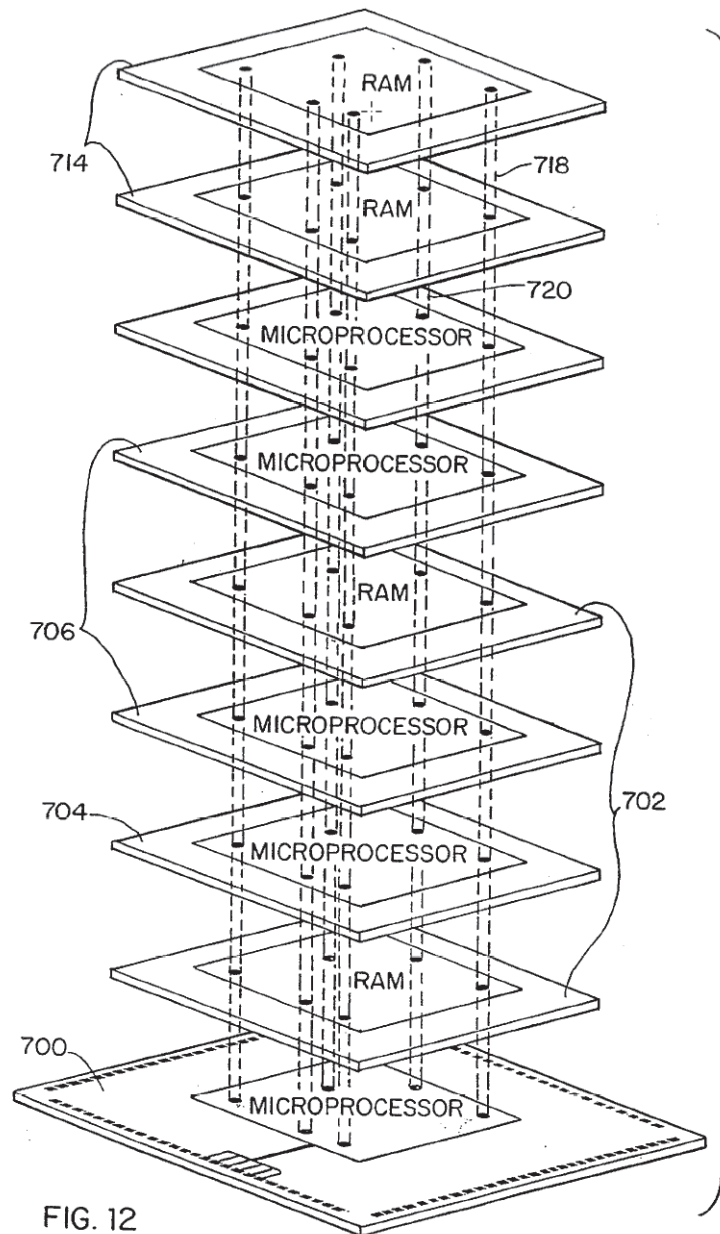


Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein “buses run vertically through the stack by the use of inter-layer connectors.” Ex. 1003, 12:24–26.

2. *Chiricescu*

Chiricescu describes a three-dimensional chip, comprising an FPGA, memory, and routing layers. Ex. 1004, 1. Chiricescu's FPGA includes a "layer of on-chip random access memory . . . to store configuration information." *Id.* Chiricescu describes and cites the published patent application that corresponds to Zavracky as follows:

At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.

See id. at 1, 4 (citing "M. P. Zavracky, Zavracky, D-P Vu and B. Dingle, 'Three Dimensional Processor using Transferred Thin Film Circuits,' US Patent Application # 08-531-177, allowed January 8, 1997").⁹

Chiricescu describes "[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information." Ex. 1004, 1. Chiricescu also describes using memory on-chip to "significantly improve[] the reconfiguration time," explaining as follows:

The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

Id. at 3.

⁹ Zavracky lists the same four inventors and "Appl. No. 531,177," which corresponds to the application number cited by Chiricescu. Ex. 1003, codes (75), (21).

Figure 2 of Chiricescu follows:

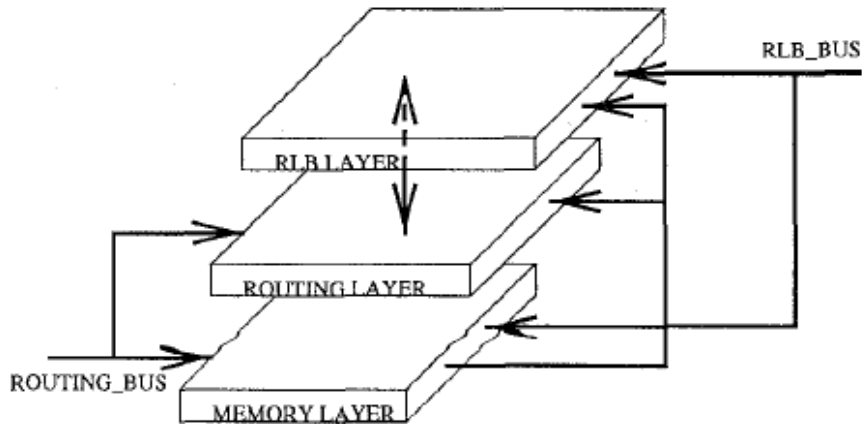


Figure 2. The layers of our 3-D FPGA architecture.

Figure 2 illustrates three layers in the 3D-FPGA architecture, with the RLB layer including routing and logic blocks in in a “sea-of-gates FPGA architecture,” a routing layer, and the aforementioned memory layer (to program the FPGA). *See* Ex. 1004, 1–2.

3. Akasaka

Akasaka, a December 1986 paper published in the Proceedings of the IEEE, generally describes trends in three-dimensional integrated stacked active layers. Ex. 1005, 1. Akasaka states that “tens of thousands of via holes” allow for parallel processing in stacked 3-D chips, and the “via holes in 3-D ICs” decrease the interconnection length between IC die elements so that “the signal processing speed of the system will be greatly improved.” *Id.* at 3. Akasaka further explains that “high-speed performance is associated with shorter interconnection delay time and parallel processing” so that “twice the operating speed is possible in the best case of 3-D ICs.” *Id.*

Also, “input and output circuits . . . consume high electrical power.” Ex. 1005, 3. However, “a 10-layer 3-D IC needs only one set of I/O

circuits,” so “power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs.” *Id.*

Figure 4 of Akasaka follows:



Fig. 4. Wiring for parallel processing in 2-D and 3-D ICs.

Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

4. *Claim 1*

For its arguments that claim 1 is unpatentable, Petitioner relies on a combination of Zavracky, Chiricescu, and Akasaka, “integrat[ing]” Zavracky’s “stacked interconnected programmable 3-D module,” Chiricescu’s “accelerated FPGA reconfiguration using stacked memory,” and Akasaka’s “thousands of distributed interconnections.” Pet. 18.

a. *Combination of Zavracky, Chiricescu, and Akasaka*

With respect to the combination of Zavracky and Chiricescu, Petitioner argues that Chiricescu explicitly references and uses the interconnections of Zavracky. Pet. 18 (citing Ex. 1002 ¶¶ 218–232); *see* Pet. 16 & n.3; *supra* § II.D.2 (noting the explicit citation to and description of Zavracky in Chiricescu). Petitioner further argues that one of ordinary skill would have used Chiricescu’s teachings with Zavracky’s 3-D stacks to achieve improvements in reconfiguration time. *Id.* at 18–19 (citing Ex. 1002 ¶¶ 221–228 (citing Ex. 1004, 2; Ex. 1003, 5:65–66)). Additionally, Petitioner argues that the combination would have been motivated by

Chiricescu's suggestion of using an FPGA for "arbitrary logic functions" to "expand" on the limited task performed by the programmable logic device in Zavracky, to combine prior art elements according to known methods to yield a predictable result, and as a routine modification. Pet. 19–20 (citing Ex. 1003, 2:29–39; Ex. 1004, 1; Ex. 1002 ¶¶ 229–232).

Petitioner argues that the further combination of Akasaka with Zavracky and Chiricescu would have been motivated by a desire to increase bandwidth and processing speed through better parallelism and increased connectivity. Pet. 20 (citing Ex. 1005, 3; Ex. 1002 ¶ 233). Petitioner contends that Zavracky and Chiricescu each teach or suggest that connections could be placed anywhere on the die. *Id.* (quoting Ex. 1003, 6:43–47; citing Ex. 1004, 1). To improve Zavracky's stacks, according to Petitioner, one of ordinary skill would have sought out Akasaka's teachings to increase bandwidth and processing speed and expected success. *Id.* (citing Ex. 1002 ¶ 235). Petitioner also argues that Akasaka's communication structure would have enabled desirable uses of the Zavracky-Chiricescu combination. *Id.* at 20–21 (citing Ex. 1005, 11, Fig. 25; Ex. 1002 ¶¶ 236–237). Petitioner also argues that one of ordinary skill would have been motivated to make a combination with Akasaka, and that such a combination "would have been a logical extension" to the Zavracky-Chiricescu combination, in light of "many references teaching stacked dies with thousands of distributed connections." *Id.* at 21 (citing Ex. 1009; Ex. 1030; Ex. 1021; Ex. 1002 ¶¶ 238–239).

Patent Owner argues that one of ordinary skill in the art would not have combined Zavracky, Chiricescu, and Akasaka as Petitioner argues. PO Resp. 36–44.

Patent Owner argues that, because Chiricescu discloses configuration data stored in on-chip memory, the combination of Chiricescu and Zavracky would result in a structure in which data is removed from the microprocessor's cache to be stored in the FPGA's on-chip memory, which would make the data harder for the microprocessor to access. PO Resp. 37–38. This is based on Patent Owner's argument that Zavracky and Chiricescu both include only a small number of vertical interconnections between the layers. *Id.*; *see id.* at 20 (describing Zavracky as disclosing a small number of vertical interconnections between layers), 26 (describing Chiricescu as having only a small number of interconnects between memory and RLB layers).

Patent Owner additionally argues that the combination of Zavracky and Chiricescu would not have resulted in the acceleration of data shared between a microprocessor and an FPGA. *Id.* at 38–39. Patent Owner calls the motivation to combine “untethered to the accelerating processing claims,” in an argument relating to its interpretation of limitation 1.3, discussed above at Section II.C.4. *Id.* at 38–39 (citing Ex. 2006 ¶ 75 (Dr. Souris's testimony describing the reasons for combining as flawed because “none of the cited references disclose the processing of shared data” or acceleration of such processing)). Lastly, Patent Owner argues that major modifications would need to be made to the combination of Zavracky and Chiricescu to allow for the accelerated processing of shared data, again, relating to Patent Owner's interpretation of limitation 1.3 of claim 1. *Id.* at 38–41.

With respect to the combination of Zavracky, Chiricescu, and Akasaka, Patent Owner argues, again with reference to its interpretation of

limitation 1.3 of claim 1, that Akasaka does not remedy the issues it argues are present with a combination of Zavracky and Chiricescu with respect to accelerating the processing of shared data. *Id.* at 41–42. Citing Figure 25 of Akasaka, Patent Owner argues that Akasaka teaches each processor in a stack only accessing memory in its own layer. *Id.* at 41–42. Again referencing Figure 25 of Akasaka, Patent Owner argues that Petitioner “does not attempt to adequately explain **how** a POSITA would incorporate Akasaka’s common memory data system into the combined Zavracky-Chiricescu system to achieve accelerated processing of data shared between a microprocessor and an FPGA.” *Id.* at 42. Patent Owner argues that Akasaka’s Figure 25 teaches that “each individual processor disclosed in Akasaka only has direct access to its own memory and not any other processor’s memory.” PO Sur-reply 9.

Patent Owner argues that the modification of Zavracky-Chiricescu with Akasaka would require the stacked memory from Chiricescu to be moved to its FPGA layer, which would be contrary to Chiricescu’s principle of operation that moves memory out of the FPGA layer. *Id.* at 43–44.

Patent Owner’s arguments are unavailing. To the extent that they rely on Patent Owner’s construction of limitation 1.3, the arguments fail as we have not adopted this construction. *See supra* § II.C.4. Additionally, Petitioner’s arguments regarding a “common data memory” and citations to Akasaka’s Figure 25 relate to the knowledge of one of ordinary skill for “common data memory” and not to any indication that the specific configuration of Figure 25 would be used in the combination. *See* Pet. 20–21, 30–31. As Petitioner discusses, Zavracky specifically describes a stacked configuration of integrated circuit elements, and connecting bus

lines between an FPGA/PLD element and other integrated circuit elements, including memory and a processor. *See* Pet. 14–15, 23–24 (citing Ex. 1003, 2:5–10, 3:62–4:4, 4:7–9, 5:19–23, 6:43–47, 12:12–38, 14:56–58, Figs. 12, 13). Petitioner shows a number of other stacked dies or layers with multiple via connections – in addition to Akasaka (Ex. 1005, Fig. 4), Petitioner cites Franzon (Ex. 1020, Fig. 4), Koyanagi (Ex. 1021, Fig. 1(a)), and Alexander (Ex. 1028, Fig. 2(g)). *See id.* at 21, 37. As discussed further below, Trimberger (Ex. 1006) also shows parallel loading by “*flash reconfiguring* all [100,000] bits in logic and interconnect array [i.e., an FPGA] . . . simultaneously from one memory plane.” Ex. 1006, 22.¹⁰ Patent Owner concedes Zavracky and Chiricescu each show how to connect layers with a small number of vertical interconnections. PO Resp. 20 (Zavracky), 26 (Chiricescu), 38. Petitioner shows that a large number of vias would have been obvious in view of the combined teachings, to enhance speed, allow parallel processing and data transfer, minimize latency, and maximize bandwidth.

Thus, Petitioner persuasively relies on the knowledge of the artisan of ordinary skill and the combined teachings of Zavracky, Chiricescu, and Akasaka supported by specific reasons and rational underpinning to show how the combination teaches or suggests increasing the number of contact points or via holes for electrically coupling FPGA, memory, and processors together. Petitioner also shows the “why”—to allow for parallel data

¹⁰ Petitioner employs Trimberger to address challenged claims 13–30 as discussed further below (§ II.F), but it is also further evidence of a reasonable expectation of success as it relates to connecting several thousands of bit lines in parallel.

transfers, speed increases, larger bandwidth, etc., all with a reasonable expectation of success.

b. Preamble, Limitation 1.1, and Limitation 1.2

Claim 1's preamble recites "[a] processor module comprising." Petitioner relies on the combined teachings of Zavracky, Chiricescu, and Akasaka, as discussed further below, and provides evidence that Zavracky discloses a processor module, including a programmable array, memory (RAM), and microprocessor as part of a stack of dies forming a 3-D device. *See* Pet. 22 (reproducing Ex. 1003, Figs. 12–13; citing Ex. 1003, 2:1–7, 5:19–23, 9:42–45, 12:12–38, Figs. 12–13; Ex. 1002 ¶¶ 282–288).

Claim 1 recites limitation 1.1, "at least one field programmable gate array integrated circuit die element including a programmable array." Petitioner contends that the combined teachings of Zavracky and Chiricescu render the limitation obvious. Pet. 23–24. Petitioner relies on Zavracky's layers as teaching dies, citing Zavracky's description of interlayer connections as "placed anywhere on the die" and thereby "achieved with a minimal loss of die space." *Id.* (quoting Ex. 1003, 6:43–7:9; citing Ex. 1003 4:63–65, 10:61–65, Figs. 1 (element 140), 6, 7; Ex. 1002 ¶¶ 278–280). Thus, Petitioner argues that Zavracky describes stacked layers of integrated circuit die elements. *Id.* at 24. Petitioner further argues, with reference to PLD 802 in Figure 13 of Zavracky and its described programming to provide a user-defined communication protocol, that one of ordinary skill in the art would have understood that an FPGA was an example of such a programmable logic device. *Id.* at 24–25 (citing Ex. 1003, 5:21–23, 12:33–36, Fig. 13; Ex. 1002 ¶¶ 293–295). Petitioner adds that, Chiricescu describes Zavracky as teaching technology "to build 3-D layered FPGAs"

and thus confirms the understanding of Zavracky as teaching an FPGA. *Id.* at 25 (citing Ex. 1004, 1; Ex. 1002 ¶ 296). Additionally, in a combination of Chiricescu and Zavracky, Petitioner contends that Chiricescu’s “sea-of-gates FPGA” would teach or suggest an FPGA as the PLD layer of Zavracky. *Id.* (citing Ex. 1004, 1, 3).

With respect to the “programmable gate array” of limitation 1.1, Petitioner first refers to its arguments with respect to an FPGA as the PLD, asserting that the FPGA includes a programmable array. *Id.* at 25–26 (citing Ex. 1002 ¶ 288). Next, Petitioner argues that in the combination of Chiricescu and Zavracky, the configurable routing and logic blocks in the FPGA layer teaches a programmable gate array. *Id.* at 26 (citing Ex. 1004, 1; Ex. 1002 ¶ 299).

Petitioner argues that the “microprocessor integrated circuit die element” of limitation 1.2 is taught in Zavracky’s layered multi-processor system (Figure 12) or multi-layer microprocessor (Figure 13), citing the multiple multiprocessors, each on one die element in the Figure 12 embodiment, and the multi-layer microprocessor in the Figure 13 embodiment. Pet. 27–28 (citing Ex. 1003, Fig. 12 (elements 700, 704, 705), Fig. 13 (elements 804, 806); Ex. 1002 ¶¶ 310–312). Limitation 1.2 further requires that this die element be “stacked with an electrically coupled” to the programmable array of the die element from limitation 1.1. Petitioner cites Zavracky’s teaching of vertically stacked and interconnected circuit element layers, electrically coupled to each other. *Id.* at 28 (citing Ex. 1003, 2:7–8, 11:63–12:2, 12:13–39, 14:51–63).

Other than addressing motivation as discussed herein, Patent Owner does not make any specific arguments with respect to these limitations.

c. Limitation 1.3 of Claim 1

With respect to the final limitation 1.3 of claim 1, “such that the processing of data shared between the microprocessor and the field programmable gate array is accelerated,” Petitioner argues that Zavracky’s programmable logic acting as an intermediary to the microprocessor means that data is shared between the microprocessor and programmable logic. Pet. 29 (citing Ex. 1003, 12:28–38; Ex. 1002 ¶ 342). Petitioner further argues that Akasaka’s thousands of via holes would have been used to allow information to be transferred between die layers. *Id.* at 30 (citing Ex. 1005, 3; Ex. 1002 ¶¶ 233–239, 347–348).

To teach or suggest “that processing . . . is accelerated” as per limitation 1.3, Petitioner argues that Zavracky’s approach offers higher speed from “reduction in the length of the busses.” Pet. 30 (quoting Ex. 1003, 3:1–11; citing Ex. 1002 ¶ 346). Petitioner additionally cites Akasaka’s teaching of “thousands of via holes” to permit parallel processing, and that “twice the operating speed is possible in the best case of 3-D ICs.” *Id.* at 17, 31 (quoting Ex. 1005, 3 (emphasis omitted); citing Ex. 1002 ¶ 347). Additionally, Petitioner cites similar teachings of Chiricescu with respect to benefits from a stacked arrangement with vertical interconnects and the background knowledge of one of ordinary skill in the art. *Id.* at 5–10, 17 (citing Ex. 1004, 3; Ex. 1002 ¶ 348).

Patent Owner contends that the Zavracky-Chiricescu-Akasaka combination does not teach or suggest limitation 1.3’s feature of accelerating processing of data. PO Resp. 30–36. Patent Owner argues that Petitioner only describes data being transferred from a microprocessor to an FPGA, and not shared. *Id.* at 31–32. Patent Owner contends that “*data processed*

by *Zavracky*'s microprocessor is not even shared with the FPGA" but rather that "it is the **output** of *Zavracky*'s microprocessor that is sent to the FPGA." *Id.* (citing Ex. 2006 ¶ 65). Patent Owner additionally argues that Akasaka's teachings regarding common memory data does not involve processing of data shared between a microprocessor and an FPGA. *Id.* at 32–33 (citing Ex. 1005, 11, Fig. 25(c); Ex. 2006 ¶¶ 66–67). Patent Owner additionally argues that, because the combination does not teach or suggest the processing of shared data, it also does not teach or suggest accelerating such processing. *Id.* at 34. Lastly, Patent Owner suggests that the combination does not teach or suggest limitation 1.3 of claim 1 because it does not disclose memory accessible to a microprocessor and FPGA with approximately equal speed. *Id.* at 35–36 (citing Ex. 2006 ¶ 70).

Each of these arguments is based on Patent Owner's interpretation of limitation 1.3, which we do not agree with and have addressed above, in Section II.C.4. Considering the record and arguments made, Petitioner has shown that the combination of *Zavracky*, *Chiricescu*, and *Akasaka* teaches both data shared between the FPGA and the microprocessor, and also how a three-dimensional approach as in *Zavracky* (with shorter busses), the distributed contact points and shorter interconnects of *Akasaka*, and the stacked arrangement of *Chiricescu* combine to teach or suggest accelerated processing of data shared between the microprocessor and the FPGA, for example, for reconfiguring the FPGA. *See* Pet. 28–31 (citing Ex. 1003, 3:1–11, 6:1–12, 12:28–38; Ex. 1004, 3; Ex. 1005, 3, 11; Ex. 1002 ¶¶ 342–348).

d. Conclusion – Claim 1

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 1 would have been obvious.

5. *Claims 2–6*

Claim 2 depends from claim 1 and further recites that the processor module further comprises “at least one memory integrated circuit die element stacked with and electrically coupled to” either the field programmable gate array IC die element (of limitation 1.1) or the microprocessor IC die element (limitation 1.2) of claim 1. Ex. 1001, 6:27–31. Petitioner argues that Zavracky’s figures 12 and 13 describe a layer including random access memory. Pet. 32 (citing Ex. 1003, 11:63–65, 12:33–35, Figs. 10, 12, 13). Petitioner further argues that this layer is, in the combination of Zavracky, Chiricescu, and Akasaka, stacked with and electrically coupled to the other die elements as explained with reference to the die elements of claim 1. *Id.* at 32–33 (citing Ex. 1003, 11:63–65, 12:15–28, 12:33–35, Figs. 10, 12; Ex. 1004, 1; Ex. 1002 ¶ 319).

Claim 3 depends from claim 1 and further recites that “said programmable array is configurable as a processing element.” Ex. 1001, 6:32–33. Petitioner argues that Zavracky’s programmable array functions as a processing element. Pet. 34 (citing Ex. 1003, 12:28–38; Ex. 1002 ¶ 302). Petitioner further contends that Chiricescu’s FPGA can be reconfigured as a processing element. *Id.* (citing Ex. 1004, 2, 3; Ex. 1002 ¶ 302).

Claim 4 depends from claim 1 and further recites that “at least one field programmable gate array and said at least one microprocessor integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements.” Ex. 1001, 6:34–38. Claim 5 depends from claim 4 and further requires that “said contact points traverse said die elements through a thickness thereof.” Ex. 1001, 6:39–40. Claim 6 depends from claim 5 and further requires that

“said contact points traverse said die elements through a thickness thereof.” Ex. 1001, 6:41–43. Patent Owner argues that the limitations of claims 4 and 5 are taught by Zavracky’s “openings or via holes” providing inter-layer connections placed anywhere on the die, and Akasaka’s layers connected through via holes. Pet. 36–39 (citing Ex. 1003, 6:43–7, 13:43–46, 14:56–63; 1005, 2–5; Ex. 1002 ¶¶ 313–316, 327–334).

With respect to Claim 6, Petitioner argues that the general knowledge of one of ordinary skill in the art would have been that die elements are thinned to a point at which contact points traverse the thickness of the elements, and that one of ordinary skill would have known to employ this thinning, including because of Zavracky’s suggestion of a need for thin stacks and contact point traversal. *Id.* at 39–41 (citing Ex. 1003, 13:54–57; Ex. 1002 ¶¶ 262–266, 335–341).

Except for arguments with respect to claim 1, addressed above, Patent Owner presents no arguments relating to these dependent claims.

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claims 2–6 would have been obvious.

E. Obviousness, Claims 7–12

Claim 7 largely tracks the limitations recited in claim 1, but additionally includes a limitation, 7.3, that “at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the at least one microprocessor integrated circuit die element during manufacture and prior to completion of the module packaging.” Ex. 1001, 6:44–57. Claims 8, 9, 10, 11, and 12 duplicate the additional limitations of claims 2, 3, 4, 5, 6, 7, and 8, respectively. Petitioner argues

that claims 7–12 are unpatentable in view of a combination of Zavracky, Chiricescu, Akasaka, and Satoh. Pet. 41–46.

1. Satoh

Satoh, titled “Semiconductor Integrated Circuit, Method for Testing the Same, and Method for Manufacturing the Same,” describes using an FPGA to generate test stimuli to test elements on the same chip. Ex. 1008, code (54). Satoh describes a test circuit formed in a portion of the FPGA and used to test a CPU. *See* Ex. 1008, 14, Fig. 7.

2. Claim 7

Petitioner proposes one of ordinary skill would have combined Satoh with Zavracky, Chiricescu, and Akasaka, to teach or suggest the requirements of limitation 7.3, with the other limitations taught as discussed with respect to claim 1. Pet. 42, 44–45 (citing Ex. 1008, 5:16–22, 7:36–8:1, 45:4–36, 47:6–14; Ex. 1002 ¶¶ 350–56). Petitioner argues that one of ordinary skill would have used Satoh’s teachings with respect to using an FPGA to test circuitry to achieve known predictable benefits in testing, chip real estate, and design complexity, and would have had a reasonable expectation of success in the combination. *Id.* at 43–44 (citing Ex. 1002 ¶¶ 241–244). Petitioner argues that Satoh’s teaching of an FPGA providing a test signal and an expected value signal to test a CPU teaches “at least one field programmable gate array integrated circuit die element being configured to provide test stimulus to the at least one microprocessor integrated circuit die element during manufacturing.” *Id.* at 44–45 (citing Ex. 1008, 3:5–8, 5:16–22, 7:36–8:1, 45:4–36, 46:4–36, 47:6–14; Ex. 1002 ¶¶ 350–356). Petitioner further contends that one of ordinary skill would have understood this to occur “prior to completion of the module

packaging,” because Satoh teaches the testing occurs to ensure high yield, and one of ordinary skill would have recognized that testing prior to packaging would avoid the expense and waste of packaging a module that would not be part of the hoped-for yield. *Id.* at 45 (citing Ex. 1008, 2:32–35, 3:22–23; Ex. 1043 (“Mess”); Ex. 1002 ¶¶ 355–356); Pet. Reply 16–17 (citing Ex. 1009; Ex. 1020; Ex. 1043 ¶ 37; Ex. 1002 ¶ 241).

Patent Owner argues that Satoh does not teach or suggest an FPGA used to test the CPU prior to completion of the module packaging. PO Resp. 45–46. Patent Owner contends that Satoh’s teaching is that testing could improve yield by detecting defective parts of the FPGA and avoiding those parts. *Id.* (citing Ex. 1008, 4–5; Ex. 2006 ¶ 83). Dr. Souri testifies that this teaching of Satoh “demonstrates that Satoh describes a process of improving yield by avoiding defective parts of an FPGA when using the FPGA to test other internal circuits, not by ensuring that the testing is conducted ‘prior to packaging being finished,’ as asserted in the Petition.” Ex. 2006 ¶ 83. Thus, Dr. Souri testifies, Satoh teaches a technique to improve yield for integrated circuit dies even if portions of dies are defective. *Id.* ¶ 84.

Patent Owner argues that Satoh does not teach testing a stacked microprocessor, and that this is why Petitioner relies on Mess. PO Resp. 47. Patent Owner contends that Mess, cited by Petitioner, describes testing individual dies prior to stacking. PO Resp. 47–49 (citing Ex. 1043 ¶¶ 6, 36, 38; Ex. 2006 ¶¶ 86–87); PO Sur-reply 16. Patent Owner argues that, while another embodiment of Mess teaches that a stacked die package that passes testing optionally may be encapsulated, because Mess describes the encapsulating layer is optional and the only step left after testing the stacked

die package, Mess does not support Petitioner's arguments with respect to limitation 7.3. PO Resp. 48–49 (citing Ex. 1043 ¶ 46, Fig. 8; Ex. 2006 ¶ 88).

We agree with Petitioner that these arguments do not address the combined teaching of the asserted references, with respect to what one would understand about testing the stacked die package taught by Zavracky, Chiricescu, and Akasaka. Pet. Reply 14. Thus, Patent Owner's argument that Petitioner must rely on Mess to bolster the contentions regarding the teachings of Satoh is rendered moot. Furthermore, given Patent Owner's acknowledgment that Mess teaches a stacked die package being encapsulated only if it passes testing, we agree with Petitioner that this shows, as Petitioner argues, that one of ordinary skill would have recognized that this testing should occur before packaging. *See* Pet. 45. While the encapsulation is optional, Mess teaches that it occurs (if it occurs) only if the stacked die package passes testing. Ex. 1043 ¶ 46; Ex. 2006 ¶ 8.

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 7 would have been obvious.

3. Claims 8–12

Claims 8–12 are argued by Petitioner with respect to the arguments relating to claim 7 and claims 2–6. Pet. 45–46. Patent Owner presents no additional arguments relating to these dependent claims. For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 8–12 would have been obvious.

F. Obviousness, Claims 13–30

Petitioner contends claims 13–30 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. *See* Pet. 46–62. Patent Owner contests the showing with respect to limitations

13.4 and 22.4, and with respect to the combination of art proposed by Patent Owner. PO Resp. 52–73; PO Sur-reply 17–26.

1. Trimberger

Trimberger, titled “A Time-Multiplexed FPGA” (1997), teaches an FPGA with on-chip memory distributed around the chip. Ex. 1006, 1. Trimberger teaches that the memory “can also be read and written by on-chip [FPGA] logic, giving applications access to a single large block of RAM.” *Id.* Trimberger teaches that “the entire configuration of the FPGA can be changed in a single cycle of the memory” and that “[w]hen the device is *flash reconfigured*, all bits in the logic and interconnect array are updated simultaneously from one memory plane.” *Id.* Trimberger teaches 100,000 bit lines that may be involved in reconfiguration. *Id.* at 27.

2. Claim 13

Petitioner contends claims 13 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. *See* Pet. 47–57.

With the exception of limitation 13.4, the Petition relies on the teachings or suggestions of Zavracky, Chiricescu, and Akasaka to teach or suggest the limitations of claim 13, as described with respect to claim 1 or claim 2. Pet. 50–51. We have addressed these in Sections II.D.4 and II.D.5. With respect to limitation 13.4, “means for reconfiguring the programmable array within one clock cycle,” we have concluded that the corresponding structure is “a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element.” *See supra* § II.C.2. We have additionally concluded that a wide configuration port should be construed as “a

configuration data port connecting in parallel cells on one die element to cells on another die element.” *See supra* § II.C.1.

a. Petitioner’s Showing

Our constructions correspond most closely to Petitioner’s arguments with respect to the second structure it proposed for means-plus-function limitation 13.4, “a stacked FPGA die and memory die interconnected by a wide configuration data port using contact points distributed throughout the dies.” *See Pet.* 11–13. Petitioner contends that the combination of Zavracky, Chiricescu, Akasaka, and Trimberger teaches or suggests this second structure, including in the die elements connected by contact points distributed throughout the dies. *Pet.* 56–57 (referencing *id.* at 35–37). Petitioner argues that Akasaka describes that its active layers are interconnected through “several thousands or tens of thousands of via holes” distributed throughout the surfaces of the die elements. *Id.* at 36–37 (citing Ex. 1005, 3, 5; Ex. 1002 ¶¶ 327–332). Petitioner additionally presents Dr. Franzon’s declaration to the effect that this configuration was “ubiquitous” in the prior art. *Id.* at 37 (citing Ex. 1020, Fig. 4; Ex. 1021, Fig. 1(a); Ex. 1028, Fig. 2(b); Ex. 1002 ¶ 332). Petitioner argues that these interconnections and Trimberger’s memory access port teach or suggest the wide configuration data port. *Id.* at 56–57. Petitioner references its discussion of Trimberger with reference to its first proposed structure for 13.4, in which Petitioner argues that Trimberger includes a wide configuration data port in the single access memory access port that “has a direct connection to each of the buffer memory cells around the chip” using “massive connectivity within the chip.” *Id.* at 51–54 (citing Ex. 1006, 22, 26, 27; Ex. 1002 ¶ 367).

Petitioner argues that one of ordinary skill would have combined Trimberger with Zavracky, Chiricescu, and Akasaka to obtain the benefits of the one-cycle FPGA reconfiguration of Trimberger. Pet. 48–49. Petitioner argues that the motivation would have been to address Chiricescu’s stated issue with high configuration time for an FPGA; to prevent data from being dropped during reconfiguration; and to address the delays arising from a shared bus as in Zavracky. *Id.* at 48–49 (citing Ex. 1004, 1; Ex. 1003, 5:55–56; Ex. 1002 ¶¶ 252–254). Petitioner further argues that one of ordinary skill would have expected success in using a memory and area-wide interconnections as in Trimberger for reprogramming an FPGA in one clock cycle, given the state of the art at the time of the invention. *Id.* at 49 (citing Ex. 1020; Ex. 1021; Ex. 1041; Ex. 1047; Ex. 1002 ¶ 256).

b. Patent Owner’s Contentions and Our Analysis

Patent Owner contends that the Petition mapped Trimberger’s “single memory access port” to the wide configuration data port, and that the single memory access port is a narrow port. PO Resp. 53–54; PO Sur-reply 17–19. Patent Owner additionally contends that Petitioner has impermissibly shifted its theory in its Reply. PO Sur-reply 18–19. Patent Owner additionally contends that the Petition’s contentions are deficient because they involve the single memory access port of Trimberger which, Patent Owner argues, is not involved in the reconfiguration of the FPGA. PO Resp. 55–58 (citing Ex. 2006 ¶¶ 96–101). Thus, Patent Owner argues, Petitioner has improperly relied on the functionality from one portion of Trimberger (one-cycle reconfiguration) and the structure from another portion of Trimberger (memory access port). *Id.*

While our final constructions are not identical to those in the Decision on Institution, here and in that Decision we focused on the second corresponding structure proposed by Petitioner, and in Petitioner's arguments relating to that, Petitioner contends that

[t]he wide configuration data port (i.e., the place through which the configuration data is transferred to each of the configuration logic cells in the FPGA) using the contact points, is provided by Zavracky in combination with Chiricescu and Akasaka (and in particular, the “thousands or several tens of thousands of via holes are present in these devices” taught by Akasaka), and Trimberger (for the “memory access port” that connects to the configuration data “memory plane”). As discussed, integration of Trimberger's teachings yields the claimed function of “reconfiguring the programmable array within one clock cycle.”

Pet. 56–57. We consider this argument, which was clearly stated in the Petition, and find it persuasive. Patent Owner's arguments relate to constructions including buffer cells, which we have not adopted, or to the teachings of Trimberger in isolation, rather than in combination with the teachings of the art in combination. The Petition persuasively shows that limitation 13.4 is taught, not by Trimberger's teachings regarding the “single memory access port” that provides access to configuration memory (Pet. 51, 57; Ex. 1006, 26) alone, but rather in combination with the description in Trimberger of instantly switching to a new configuration with bit lines for a memory plane read simultaneously from configuration memory (Pet. 53–55; Ex. 1006, 27) and with Akasaka's teaching of thousands or tens of thousands of via holes (Pet. 56–57; Ex. 1005, 3, 5). This argument, which after considering the record we find persuasive, was present in the Petition. We agree with Petitioner that the combination of Zavracky, Chiricescu, and Akasaka with Trimberger yields a structure corresponding to the claimed

structure (a wide configuration data port and contact points formed throughout the area of the first integrated circuit die element and another integrated circuit die element) and the function of reconfiguring the programmable array within one clock cycle.

We recognize Patent Owner’s argument that “a petitioner cannot rely on one reference for the structure and turn to another reference for the function to demonstrate that the prior art is present in both the function and corresponding structure.” PO Sur-reply 20–21 (citing *Fresenius USA, Inc. v. Baxter Int’l, Inc.*, 582 F.3d 1288, 1299 (Fed. Cir. 2009); *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1361 (Fed. Cir. 2001) (Michel, J. dissenting)). The relevant portion of *Fresenius* involved a dispute regarding whether claims with means-plus-function limitations were shown to be invalid. *Fresenius*, 582 F.3d at 1293–94. Our reviewing court found that there was no evidence of what the correct corresponding structure was for certain means-plus-function limitations, and no comparison of structure in the specification to those present in the prior art. *Id.* at 1299–1300. While the Federal Circuit took the opportunity to stress that, for showing invalidity of a claim with a means-plus-function limitation, both the function and the corresponding structure must be found to be present in the prior art, we do not see any indication in this case relating to Patent Owner’s assertion of impropriety in finding structure and function in an asserted combination based on the combined teachings of references. And Judge Michel, in the *McGinley* dissent, was discussing a single-reference obviousness analysis, thus structure and function would necessarily be in the same reference, and no inference can be made regarding Judge Michel’s opinion regarding

invalidity arguments for means-plus-function claims based on a combination of multiple references. *See McGinley*, 262 F.3d at 1361.

Patent Owner argues that Petitioner “rel[ies] on one reference for the structure and turn[s] to another reference for the function.” PO Sur-reply 20. But this is not the case here. Rather, Petitioner presents the structure in a combination of Zavracky, Chiricescu, Akasaka, and Trimberger and the function from relevant portions of Trimberger, with specific reference to the function attributed by Trimberger to the structure included from Trimberger in the asserted combination. We find no error in such an analysis.

Patent Owner also argues that the references do not teach buffer cells, and that Trimberger’s configuration memory would not correspond to buffer cells as the data is not transiently stored in configuration memory. PO Resp. 59–64. These arguments are moot in view of our constructions, which do not require buffer cells.

Lastly, Patent Owner argues that one of ordinary skill in the art would not have been motivated to combine Zavracky, Chiricescu, Akasaka, and Trimberger. First, Patent Owner reiterates the contentions previously addressed with respect to the combination of Zavracky, Chiricescu, and Akasaka relating to claim 1. PO Resp. 65–66. Patent Owner also argues that, because Trimberger provides on-chip memory, a combination with Zavracky, Chiricescu, and Akasaka would require a change in that combination, with the memory no longer stacked in a separate die with the FPGA and microprocessor dies. *Id.* at 67–69. Patent Owner additionally argues that because of the requirement that Trimberger’s configuration memory must be on the same chip as the FPGA, one of ordinary skill would not have been motivated to or capable of making the combination. These

arguments, however, do not consider what the combination of the art would have suggested to one of ordinary skill or relate to the proposed combination, in which a memory die would be used in place of the on-chip memory of Trimberger. Pet. 47–49, 56–57; *see* Pet. Reply 28. No evidence or rationale cited by Patent Owner shows that the location of Trimberger’s on-chip memory is necessary in some way to Trimberger’s teachings. As detailed above, Petitioner presents a discussion of the use of a separate memory plane and a wide configuration data port and describes the motivation that one of ordinary skill would have had for the combination of Trimberger’s teachings with those of Zavracky, Chiricescu, and Akasaka. Pet. 48–49.

c. Conclusion – Claim 13

Based on the foregoing discussion and a review of the full record, Petitioner persuasively shows that claim 13 would have been obvious.

3. Claims 14–21

Claims 14–21 are argued by Petitioner largely with respect to the arguments relating to claims 1, 4–7, and 13. Pet. 57–60. Patent Owner presents no additional arguments relating to these dependent claims. For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 14–21 would have been obvious.

4. Claims 22–30

Claim 22 is argued by Petitioner with respect to the arguments made relating to claim 13, with the exception of limitation 22.1’s inclusion of “a plurality of configuration logic cells” on the integrated circuit die element that includes a programmable array. For this limitation, Petitioner contends that Trimberger describes an FPGA with a plurality of configurable logic

block configuration cells. Pet. 60–61 (citing Ex. 1006, 26; Ex. 1044; Ex. 1002 ¶¶ 300–301).

Claims 23–30 are argued with respect to arguments presented for claims 6, 14, 15, 16, 17, 18, 19, 20, and 22. Pet. 61–62.

Patent Owner presents no additional arguments relating to claim 22 or dependent claims 23–30.

For the same reasons given with respect to those claims, Petitioner persuasively shows that claims 22–30 would have been obvious.

G. Exhibit 1070

Patent Owner argues that “[p]aragraphs 5–9, 23–28, 42–56, 59–65, 73–74, 76–77, 95–105, and 110–118 from Dr. Franzon’s [Reply D]eclaration (Ex. 1070) addressing Petitioner’s alleged obviousness grounds are not sufficiently discussed in the Reply” at pages 13, 22, and 27–29 of the Reply. Sur-reply 27. Patent Owner contends that the noted paragraphs are “not discussed in the Reply, but instead incorporated by citation or a cursorily parenthetical.” *Id.* Patent Owner further contends that “the Board should not and cannot play archeologist with the record to search for the arguments” and “should not . . . consider[] Dr. Franzon’s arguments.” *Id.* (citing 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”)).

Patent Owner also cites *Gen. Access Sols., Ltd. v. Sprint Spectrum L.P.*, 811 F. App’x 654, 658 (Fed. Cir. 2020) as “upholding the Board’s finding of improper incorporation by reference because, *inter alia*” (Sur-reply 25), “‘playing archaeologist with the record’ is precisely what the rule against incorporation by references was intended to prevent,” (*id.* (quoting *Gen. Access Sols.*, 811 F. App’x at 658, internal citation omitted)). The

situation here is different than in the cited case in which the court noted a problem with identifying a party’s substantive arguments *prior to turning to the declaration at issue*: “*To identify GAS’s substantive arguments, the Board was forced to turn to a declaration by Struhsaker, and further to delve into a twenty-nine-page claim chart attached as an exhibit.*” *Id.* (emphasis added).

Here, Patent Owner does not describe or allege any problem with identifying Petitioner’s substantive arguments. In context, the paragraphs of Dr. Franzon’s Reply Declaration (Ex. 1070) cited by Petitioner properly support Petitioner’s substantive arguments at the pages of the Reply identified by Patent Owner.

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.¹¹ In summary:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent- able
1–6	103	Zavracky, Chiricescu, Akasaka	1–6	

¹¹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent- able
7–12	103	Zavracky, Chiricescu, Akasaka, Satoh	7–12	
13–30	103	Zavracky, Chiricescu, Akasaka, Trimberger	13–30	
Overall Outcome			1–30	

IV. ORDER

In consideration of the foregoing, it is hereby
ORDERED that claims 1–30 of the '226 patent are unpatentable; and
FURTHER ORDERED that because this is a Final Written Decision,
parties to the proceeding seeking judicial review of the Decision must
comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01571
Patent 6,781,226 B2

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