

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

IMPINJ, INC.,
Petitioner,

v.

NXP USA, INC.,
Patent Owner.

IPR2020-01630
Patent 6,680,523 B2

Before MIRIAM L. QUINN, MICHELLE N. WORMMEESTER, and
STACY B. MARGOLIES, *Administrative Patent Judges*.

QUINN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Impinj, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–4 of U.S. Patent No. 6,680,523 B2 (Ex. 1001, “the ’523 patent”). Paper 2 (“Pet.”). NXP USA, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). After considering the merits of the Petition and the arguments against institution by Patent Owner, we instituted *inter partes* review. Paper 12 (“Dec. on Inst.”).

During the trial phase, Patent Owner filed a Response (Paper 20, “PO Resp.”), Petitioner filed a Reply (Paper 22, “Reply”), and Patent Owner filed a Sur-reply (Paper 23, “Sur-reply”). We held oral argument on January 12, 2022, the transcript of which is filed in the record. Paper. 34 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claims 1–4 of the ’523 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018).

A. *Real Parties in Interest*

Petitioner identifies itself as a real party in interest. Pet. 1. Patent Owner identifies the following entities as real parties in interest: NXP B.V., NXP USA, Inc., NXP Semiconductors N.V., and Freescale Semiconductor Holdings V, Inc. Paper 4, 1.

B. *Related Matters*

The parties indicate that the ’523 patent has been asserted in the following proceeding: *NXP USA, Inc. and NXP B.V. v. Impinj, Inc.*, Case No. 1:19-cv-01875-RGA (D. Del.). Pet. 1; Paper 4, 1. At the time Patent

Owner filed its Mandatory Notices, Patent Owner indicated that the district court proceeding had been transferred to the Western District of Washington but had not been assigned yet a civil action number. Paper 4, 1. The district court assigned a civil action number: *NXP USA, Inc., and NXP B.V. v. Impinj, Inc.*, Case No. 2:20-cv-01503-RSM-MAT (W.D. Wash.). See Ex. 1008.

C. The '523 Patent

The '523 patent relates to a semiconductor wafer with process control modules. Ex. 1001, code (54). The '523 patent explains that it is known for semiconductor wafers to have a given number of chips in one of a multitude of adjacent exposure fields and to have process control modules arranged on a given area of the semiconductor wafer. *Id.* at 1:4–11. According to the '523 patent, there are three variants of such known semiconductor wafers. *Id.* at 1:10–47. The first variant consists of placing a process control module in each of the “drop-in areas which contain so-called alignment markers.” *Id.* at 1:12–18. According to the '523 patent, this first variant has a disadvantage in that only a small number of process control modules (i.e., two or three) may be placed on the semiconductor wafer. *Id.* at 1:18–26. The second variant consists of arranging the process control modules in the “dicing paths” extending between the chips. *Id.* at 1:27–31. According to the '523 patent, in this second variant the dicing paths must be wide enough to accommodate the process control modules, which results in a waste of space. *Id.* at 1:31–36. The third variant consists in providing a process control module for each chip, where such a variant is appropriate only for large-area chips. *Id.* at 1:42–47.

The '523 patent explains the invention as providing a semiconductor wafer with a given number of chips situated in one of a multitude of adjacent exposure fields and in which “each process control module takes the place of at least one chip.” *Id.* at 1:63–64. Figure 2, reproduced below, shows an exposure field of the semiconductor wafer. *Id.* at 2:64–65.

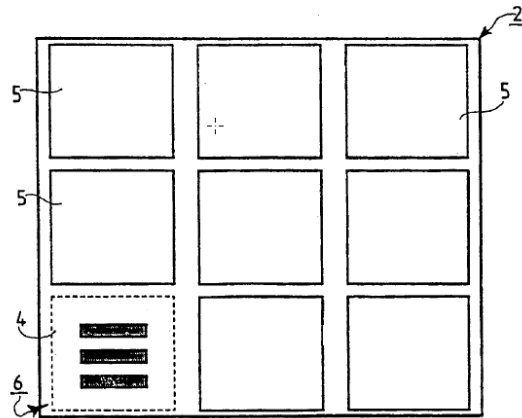


FIG.2

Figure 2 depicts one of a multitude of exposure fields 2 (also referred to as “reticles”). *Id.* at 3:3–6. Figure 2 also shows process control module (“PCM”) 4 provided in exposure field 2 in place of one of a given number of chips 5. *Id.* at 3:13–19. This arrangement is applicable to exposure fields 2 in which a PCM 4 has been provided in place of a chip 5. *Id.* at 3:17–19. The '523 patent explains that “it is not strictly necessary to provide a process control module 4 in each exposure field 2.” *Id.* at 3:19–21, 3:32–34.

D. Illustrative Claim

Of the challenged claims, claim 1 is independent. Each of challenged claims 2–4 depends directly or indirectly from claim 1, which is reproduced below.

1. A semiconductor wafer (1) having a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2),

and having process control modules (4) which are each arranged in a given area on the semiconductor wafer (1), in which the given areas are formed by the exposure fields (2), and in which each process control module (4) takes the place of at least one chip (5).

Ex. 1001, 4:12–20.

E. Evidence

The asserted grounds in this proceeding involve the following prior art references:

- a) *Yamaguchi*: US 6,492,189 B1, filed on October 26, 2000 and issued December 10, 2002, filed as Exhibit 1003; and
- b) *Satya*: US 6,633,174 B1, filed on August 25, 2000 and issued October 14, 2003, filed as Exhibit 1004.¹

Petitioner asserts the following grounds of unpatentability (Pet. 3):

Claims Challenged	35 U.S.C. §	Reference(s)
1–4	102(e) or 103(a)	Yamaguchi
1–4	102(e) or 103(a)	Satya
1–4	103(a)	Yamaguchi, Satya

Petitioner also relies on a first Declaration of Scott E. Thompson, filed as Exhibit 1007 (“Thompson Decl.”) and a Reply Declaration of Scott

¹ Petitioner asserts that Satya should be accorded a priority date of April 18, 2000 because the provisional application (Ex. 1005) to which Satya claims priority provides written description support for the invention claimed in Satya and Petitioner presents a claim chart showing such written description support (Ex. 1006). However, there is no dispute that Satya is prior art under 35 U.S.C. § 102(e). *See* PO Resp. 31–51. Accordingly, we proceed with our analysis with Satya as prior art.

E. Thompson, filed as Exhibit 1011 (“Reply Thompson Decl.”). Patent Owner relies on a declaration of Vivek Subramanian, Ph.D. in support of its Patent Owner Response. Ex. 2002 (“Subramanian Decl.”).

II. DISCUSSION

A. Claim Construction

In an *inter partes* review requested in a petition filed on or after November 13, 2018, we apply the same claim construction standard used in district courts, namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2019).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner proposes that the term “process control module” includes test structures and alignment markers based on two disclosures of the ’523 patent. Pet. 13–14. According to Petitioner, the ’523 patent describes a process control module able to detect or recognize flaws at nearby locations of the semiconductor wafer. *Id.* at 13 (citing Ex. 1001, 1:24–26). Petitioner also proffers the ’523 patent’s description of one variant in which a process control module is “formed by so-called drop-areas which contain so-called alignment markers, which are reference or positioning structures.”

Id. at 14 (citing Ex. 1001 1:13–16). Petitioner supports its claim construction position with testimony of Dr. Thompson, who also relies on the above-cited descriptions in the ’523 patent to conclude that test structures and alignment markers are types of PCMs. *See* Thompson Decl. ¶ 46.

In the preliminary stage of the proceeding, Patent Owner argued that the ’523 patent distinguishes between process control modules and alignment markers. Prelim. Resp. 15–16. In our Decision on Institution we agreed with Patent Owner and determined preliminarily that the recited “process control module” would not encompass alignment markers. Dec. on Inst. 6–7. We stated:

In describing the first variant of the semiconductor wafer, the ’523 patent states that given areas in which a process control module is located “are formed by so-called drop areas which contain so-called alignment markers.” Ex. 1001, 1:12–18. The patent further states that, with this first variant, “these process control modules cannot detect or recognize flaws at locations of the semiconductor wafer which lie comparatively far from these process control modules.” *Id.* at 1:18–26. We understand the ’523 patent disclosure to describe PCMs specifically for detecting and recognizing flaws at locations of the semiconductor wafer, but not to describe what Petitioner alleges—that alignment markers are a type of PCM.

Id.

During the trial phase of the proceeding, Petitioner did not respond to our preliminary determination that the “process control modules” do not encompass alignment markers. *See generally* Reply. Patent Owner, on the

other hand, reiterated its argument that alignment marks² are not process control modules. PO Resp. 16.

We see no reason to deviate from our determination that a “process control module” does not encompass an alignment mark for the same reasons stated above. That is, the specification describes “process control modules” and “alignment markers” distinctly from each other. Ex. 1001, 1:10–26. A specific drop-in area may contain alignment marks and also may have formed therein a “process control module.” *Id.* There is no description or persuasive evidence in the record that these terms (“process control module” and “alignment marks”) are equivalent or that an alignment mark may be used to detect flaws as is described for the process control module. Consequently, we determine that the term “process control module” does not encompass alignment markers.

As for further construction of the claim term, Patent Owner argues that “process control module” should be construed to mean “structure configured to be tested during the wafer fabrication process using optical lithography equipment.” PO Resp. 6–8. Petitioner challenges Patent Owner’s proposed construction as deviating from the plain and ordinary meaning and proposes an ordinary meaning of the term in view of Patent Owner’s arguments. Reply 7, 12.³ Petitioner argues that there is no

² Neither party argues that an alignment mark (in the prior art) and an alignment marker (disclosed in the ’523 patent) differ in any meaningful way, and thus, the terms are used interchangeably in our discussion.

³ We note here Patent Owner’s argument that Petitioner did not provide any claim construction for the term and, therefore, failed to satisfy the burden of proving unpatentability. Sur-reply 1–9. The argument hinges on Patent Owner’s characterization of the Petition as offering “no usable definition” for the term and merely challenging Patent Owner’s proposal. *Id.* We do

indication either in the claims or in the specification of the '523 patent that the process control module would be limited to optical lithography testing. Reply 8–10. Petitioner also argues that the '523 patent nowhere limits the flaw detection performed by the process control modules to detection that occurs only “during the wafer fabrication process.” *Id.* at 10–11. We address each of these issues in turn.

1. Using Optical Lithography Equipment

Patent Owner presents arguments based on the specification of the '523 patent to support the proposition that the recited “process control modules” are tested “using optical lithography equipment.” PO Resp. 6. For instance, the '523 patent describes fabrication using “*drop-in areas*” for positioning the semiconductor wafer, and this disclosure, according to Patent Owner, makes evident the use of “process control modules” in the context of optical lithography fabrication. PO Resp. 6 (citing Ex. 1001, 3:6–10, 1:12–26; Subramanian Decl. ¶ 23). Because the “drop-in areas” are used to align the wafer with the exposure masks, the argument goes, a person of ordinary skill in the art would have understood that the '523 patent is describing “the use of optical lithography equipment.” PO Resp. 7 (citing Subramanian Decl. ¶ 25, which cites Exs. 2004-05). Patent Owner also makes the point that the only embodiment of the '523 patent uses an optical

not agree because Petitioner asserts a claim construction in the Petition and clarifies it further in the Reply. Pet. 13; Reply 12. Nevertheless, Patent Owner was given ample opportunity to explain its claim construction position in light of Petitioner’s contentions regarding the proper meaning of “process control module.” Sur-reply 4 (erroneously asserting that the Board deemed Petitioner’s proposed definition as “wrong and overbroad”); Tr. 26:14–31:22.

lithography system, and, therefore, the '523 patent would be limited to the field of optical lithography. *Id.* at 8 (citing *Phillips v. AWH Corp.*, 414 F.3d 1303, 1315 (Fed. Cir. 2005)).

Patent Owner also argues that the prosecution of the '523 patent provides further support for the proposition that the use optical lithography is “central” to the invention. PO Resp. 8. For example, Patent Owner contends that in response to a rejection over U.S. Patent No. 5,128,737 (Ex. 2003, “van der Have”), the applicant explained the “*present invention*” is to be limited to “process control modules in optical lithography systems.” *Id.* at 8–9 (citing Ex. 1002, 29–34, 37–38). Although the argument presented to the examiner explained the problem with having insufficient number of process control modules, according to Patent Owner, such a problem “existed specifically in the field of optical lithography systems.” *Id.* at 9.

Patent Owner further argues that Petitioner’s expert testimony supports Patent Owner’s contention. Specifically, during cross-examination, Dr. Thompson answered a line of questioning directed to whether the '523 patent supports his opinion that exposure fields and reticles can be used interchangeably: “I’m basing it on the technology he’s using to form integrated circuits. The reticle sets the exposure field. You shine light through the reticle. The pattern on the reticle is the same pattern that goes to the wafer.” PO Resp. 10–11 (citing Ex. 2006, 29:6–11).

Petitioner responds to all the arguments presented by Patent Owner and contends that Patent Owner’s construction does not comport with the plain and ordinary meaning of the term. Reply 3–4 (citing Ex. 1012, 41:17–23, 45:4–11), 7–11. According to Petitioner, the plain and ordinary

meaning of the term, as understood by a person of ordinary skill in the art, is “modules that were placed on a wafer to assist in the process of producing the integrated circuits (‘ICs’) on the wafer” and “test structures used to detect flaws at any point in the wafer fabrication process.” Pet. 13; Reply 12 (citing Reply Thompson Decl. ¶¶ 4–6); Tr. 6:26–7:13. Patent Owner contends that Petitioner’s claim construction position is overly broad because the ’523 patent is an optical lithography patent. Tr. 27:11–28:13.

We are not persuaded by Patent Owner’s arguments that the specification and prosecution history of the ’523 patent support the contention that “process control monitors” are limited to testing in optical lithography systems. Nor are we persuaded that the testimony of Dr. Thompson supports Patent Owner’s contention.

First, the cited statements in the ’523 patent inform us that (1) the process control modules would not be placed in drop-in areas, if the goal is to increase the number of modules on a wafer, because (2) a small number of control modules on a wafer means that they cannot “detect or recognize flaws at locations of the semiconductor wafer which lie comparatively far from these process control modules.” Ex. 1001, 1:12–26. The specification thus describes process control modules that are provided on the wafer in connection with an optical lithography fabrication process that uses exposure masks placed on a wafer, which, when exposed to light, results in the pattern on the reticle transferred on the wafer. *See* Ex. 1001, 5:5–19; Ex. 2006, 29:6–11. However, the ’523 patent describes the fabrication process *of the wafer* on which the process control modules are placed. The disclosure does not demonstrate that the process control modules *detect or recognize flaws using only* optical lithography systems.

We note here that Patent Owner submits the testimony of Dr. Subramanian in support of its arguments concerning optical lithography. Specifically, Dr. Subramanian's testimony mirrors Patent Owner's arguments that the specification of the '523 patent describes optical lithography equipment, but not other types of lithography, such as electron beam lithography. Subramanian Decl. ¶¶ 22–25. The testimony is not persuasive because the specification, at best, explains that the wafer is fabricated using optical lithography, but does not describe in any detail how the process control modules are used for *testing the wafer*. The mention of technology used in optical lithography, with no mention of other technologies, alone is not reason to limit the term “process control modules” to structures that perform flaw detection or testing in the specific field of use that Patent Owner asserts: optical lithography. Accordingly, we find unpersuasive Patent Owner's arguments that the specification of the '523 patent limits the use of the process control modules *for testing*, exclusively, in an optical lithography manufacturing system.

As for the prosecution history argument, we also are not persuaded that the record is sufficient to construe the term as Patent Owner proposes. *See* PO Resp. 8–9 (citing Ex. 1002, 29–34, 37–38). Patent Owner relies on *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343 (Fed. Cir. 2001), to argue that the phrase “present invention” used in connection with the van der Have arguments during prosecution is evidence that the applicant meant to cover only the process control modules in optical lithography systems. The applicant's statements during prosecution focused on van der Have having a single, large IC on one wafer rather than the “*wafer of the present invention which has a multitude of chips, of which chips each one of a given number of chips is situated in one of a multitude of*”

adjacent exposure fields (as defined in claim 1).” Ex. 1002, 38 (italics added, underlining in original); *see also id.* (stating that “[t]he present invention discloses a novel arrangement of process control modules (PCMs) applicable in IC fabrication” and repeating recited claim language concerning the PCMs arranged on a wafer on areas formed by exposure fields). And in explaining a difference in problems solved by van der Have, the applicant focused again on the process control modules located within the “single chip” versus the problems resulting from the desire to have sufficient number of process control modules on a wafer having “a multitude of chips.” *Id.* Thus, if we were to give any weight to the use of the words “present invention” in connection with the statements made in prosecution, we find that the statements at best demonstrate a desire to highlight the location of the process control modules on a wafer having multiple ICs. None of the statements made during prosecution, however, denotes the applicant’s intent to limit *the use* of the process control modules for testing in optical lithography systems. Consequently, we do not agree with Patent Owner’s contention that the prosecution history evidences the applicant’s intent to limit the recited “process control module” to the asserted field of use.

As for Dr. Thompson’s cross-examination, we are unpersuaded that the cited testimony supports Patent Owner’s contentions. Dr. Thompson opined that the ’523 patent describes the technology to form the integrated circuits, using reticles to set the exposure field. Ex. 2006, 29:6–11. This testimony sets forth how the reticle and an exposure field are linked—nothing about how the process control modules are for testing only in optical lithography systems. Accordingly, we are not persuaded that Patent Owner’s argument is supported by Dr. Thompson’s testimony as alleged.

In sum, we are not persuaded the record supports Patent Owner's argument that the claim term "process control module" is a structure configured "to be tested" "using optical lithography equipment."

2. During Wafer Fabrication Process

According to Patent Owner, a "process control module" is a "structure configured to be tested *during the wafer fabrication process* using optical lithography equipment." PO Resp. 6–8 (emphasis added). Petitioner on the other hand argues that a "process control module" is a "test structure" for detecting flaws during (in-line) and after wafer fabrication (end-of-line).

Reply 2, 12 (citing Reply Thompson Decl. ¶¶ 4–6); Tr. 6:26–7:13.

According to Patent Owner, a test structure is not a "process control module" if it performs only "electrical testing" because such a test is performed after fabrication, at the "end-of-line" stage, and, thus, the test structure is not for "process control." *See* Subramanian Decl. ¶ 40; Ex. 1012, 44:13–47:5. The dispute here centers on whether the recited "process control modules" are for testing only "during" fabrication, thus requiring that any alleged testing be performed "in-line." PO Resp. 12, 18; Reply 5. As we discuss below, we are not persuaded that the term "process control module" would have been understood by a person of ordinary skill in the art to be used for only "in-line" testing.

Neither the '523 patent nor the prosecution history, as stated above, describes *how* the process control modules are used for testing—the same goes for disclosing *when* they are used for testing. Patent Owner proffers the testimony of Dr. Subramanian who opines that, according to the '523 patent specification, "the function of the process control modules is to 'detect or recognize flaws' during the semiconductor wafer fabrication

process.” Subramanian Decl. ¶ 26 (citing Ex. 1001, 1:24–25). In the cited portion of the ’523 patent, however, there is no mention of the timing during which the flaw detection occurs. Lines 23–25, of column 1, state that “process control modules cannot detect or recognize flaws at locations of the semiconductor wafer which lie comparatively far from these process control modules.” Ex. 1001, 1:23–25. In other words, the ’523 patent specification does not support Dr. Subramanian’s opinion.

Dr. Subramanian further opines that the van der Have reference arguments during prosecution confirm that the recited “process control modules” are tested during the wafer fabrication process. Subramanian Decl. ¶ 27. For instance, Dr. Subramanian partially quotes a statement made during prosecution in which the applicant stated that, “Here, it shall be pointed out that the processor control modules 6 in Have patent, but not the processor 02, shall be read as the processor control modules in the present invention (see col. 15, lines 8–16).” *Id.* (citing Ex. 1002, 38). According to Dr. Subramanian, the applicant’s statement shows that the applicant equated van der Have’s “process control monitors” with the recited “process control modules.” *Id.* And, thus, according to Dr. Subramanian, van der Have proves that “process control monitors” are used for “in-line” testing—i.e., during wafer fabrication. *Id.* ¶¶ 27, 28

We do not agree that van der Have supports Dr. Subramanian’s opinion. Even assuming that the applicant’s statement carries out the intent of equating the recited “process control modules” to the process control monitor patterns of van der Have,⁴ such patterns are not limited by van der

⁴ Here we find this argument contradicts and renders unpersuasive Patent Owner’s other arguments of record in which emphasis on the word “*module*”

Have to only performing “in-line” testing. The van der Have reference states that, in addition to using them for the purpose of in-line process control, the process control monitor patterns are also used for verification of key steps during these processes, by electrically probing the patterns “both during and after wafer fabrication to perform these verifications as well as to monitor the density of occurrence of electrically fatal defects in representative circuits and patterns which comprise [patterns] 06.”

Ex. 2003, 15:11–16. We understand van der Have to use the process control monitor patterns also for electrical probing after wafer fabrication to verify the defects in the circuits and patterns comprising the process control monitor patterns. *Id.* Thus, the record does not support Patent Owner’s argument that the recited “process control module” is limited to testing “during” “the wafer fabrication process,” to the extent that phrase is meant to include only “in-line” testing.

Patent Owner further argues that the word “process” in the phrase “process control module” refers to semiconductor wafer processing. PO Resp. 12 (citing Subramanian Decl. ¶ 29). And, according to Patent Owner, processing of the wafer is the same as fabrication of the wafer. *Id.* (citing Ex. 2006, 39:2–5). Patent Owner also provides evidence in the form of technical literature in an effort to prove that “process control” is “related to the semiconductor wafer fabrication process.” *Id.* at 13. These arguments attempt to imbue the word “process” with a specific timeframe of fabrication

in process control module would not be coextensive with the function of process control *monitors*. See, e.g., Sur-reply 11 (arguing that a treatise on semiconductor manufacturing proffered by Petitioner is insufficient because the treatise refers to process control *monitors*, not process control *modules*); Tr. 42:7–18.

that limits the testing performed by the modules to those “in-line” of fabrication. We do not agree. Rather, we are persuaded by the testimony of Dr. Thompson who opines that electrical testing of process control modules may be performed in-line and end-of line as that is how integrated circuits are tested. *See* Ex. 2006, 40–42; Reply Thompson Decl. ¶¶ 4–6. In particular, Dr. Thompson opines that process control modules are used for testing electrical characteristics at the “in-line” stage and also at wafer sort, which is considered “end-of-line.” This testimony is supported by a treatise titled “Semiconductor Manufacturing Technology” enclosed in the Reply Declaration of Dr. Thompson as Attachment B. Ex. 1011, Attachment B. This treatise explains wafer testing as the measurement of electrical parameters of integrated circuits and further describes two types of electrical tests done “during wafer fabrication”—(1) in-line parametric test and (2) wafer sort. *Id.* at 27.⁵ Thus, Dr. Thompson’s declaration provides substantiated evidence that electrical testing of the wafer does not exclude end-of-line testing, contrary to Patent Owner’s assertions. Further, Dr. Thompson explains that electrical testing using process control monitors at wafer sort discards low or zero yielding wafers before running expensive functional and parametric tests. *Id.* ¶ 6 (citing Attachment C, page 33 of Ex. 1011).

Accordingly, the evidence of record does not support Patent Owner’s contention that the recited “process control modules” perform only in-line tests. We credit Dr. Thompson’s testimony over Dr. Subramanian’s in this regard and determine that the phrase “process control modules” are simply structures for detecting flaws, and are not limited to those used for in-line

⁵ Pagination refers to the number added by the footer labeling.

testing. Ex. 1001, 1:20–26; 2:33–38 (describing that process control modules located at equal distances from each other results in more reliable “detection of defective or imperfectly fabricated areas of the semiconductor wafer”).

No further claim construction is required to resolve any issues in dispute. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The “person of ordinary skill in the art” is a hypothetical construct, from whose vantage point obviousness is assessed. *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). “This legal construct is akin to the ‘reasonable person’ used as a reference in negligence determinations” and “also presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Petitioner proffers that a person having ordinary skill in the art “would have had at least a bachelor’s degree in Electrical Engineering and 3–4 years

of experience in the production of semiconductor wafers or equivalent industry experience.” Pet. 12 (citing Thompson Decl. ¶ 21). Patent Owner proposes a different level of ordinary skill as follows:

A POSITA at the time of the invention would have had a degree in mechanical engineering, electrical engineering, physics, or a similar discipline, along with at least two years of experience in the design or implementation of semiconductor technology. Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education.

PO Resp. 4. Patent Owner further argues that no argument raised in this proceeding hinges on adopting a particular level of ordinary skill in the art. *Id.* Given the lack of an actual dispute regarding the appropriate level, we adopt Petitioner’s definition of the level of ordinary skill in the art, as it is consistent with the level of skill in the art reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (stating that the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown).

C. Grounds Based on Yamaguchi Alone

Petitioner asserts that claims 1–4 would have been anticipated or rendered obvious by Yamaguchi. Pet. 20–27.

1. Overview of Yamaguchi (Ex. 1003)

Yamaguchi is directed to a process of forming exposed areas on a semiconductor wafer, including a Test Element Group (“TEG”) region. Ex. 1003, Abstr. A semiconductor wafer produced by Yamaguchi’s exposure process is shown in Figure 7, reproduced below. *Id.* at 6:25–27.

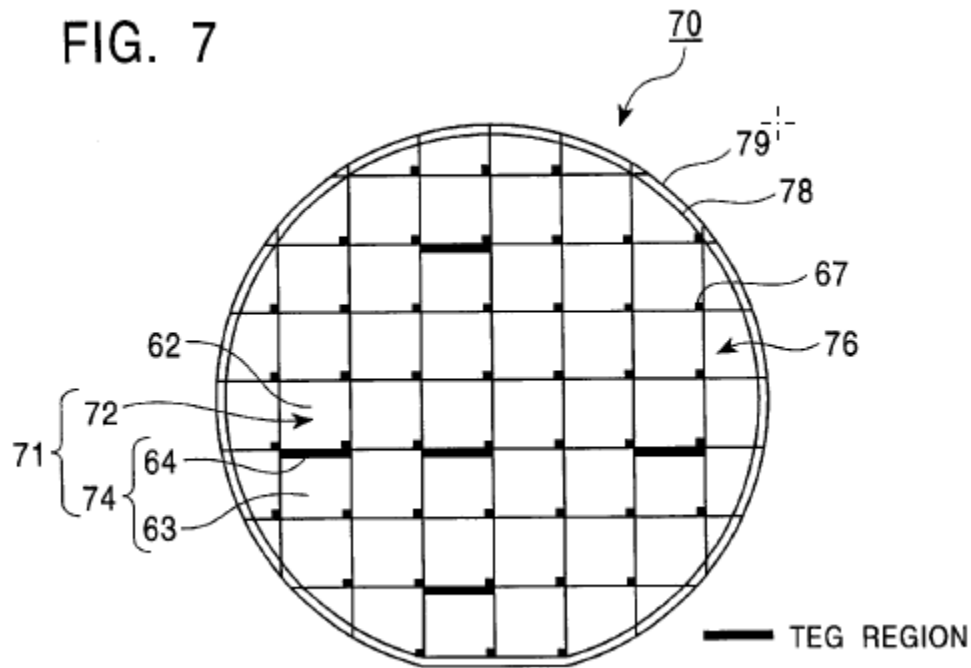


Figure 7 depicts product wafer 70 having TEG regions 64 formed at the tops of second patterned areas 74. *Id.* at 11:43–45. Product wafer 70 further depicts alignment marks 67 that are produced for alignment at the laser trimming step. *Id.* at 11:17–21, 11:55–60. Each patterned area 71 is formed by first exposing pattern area 72 with a reticle that exposes only a device region. *Id.* at 11:1–7. Then patterned region 74 is exposed to include a device region and a TEG region of the reticle at fixed vertical and horizontal pitches that align with pattern area 72. *Id.* at 11:7–12. Because the patterned areas 72 and 74 are arranged vertically and horizontally at fixed pitches, “alignment in the laser-trimming step can be made easily.” *Id.* at 11:9–20.

2. Analysis

After considering the full record, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 4 would

have been obvious over Yamaguchi. We are not persuaded, however, that Petitioner has demonstrated by a preponderance of the evidence that claims 2 and 3 in this ground would have been unpatentable over Yamaguchi.

i. Independent Claim 1

The main issue to resolve in this ground is whether Petitioner has shown that Yamaguchi teaches or suggests the recited “process control modules.” We determine that Petitioner has met its burden in showing all the elements of claim 1 are rendered obvious by Yamaguchi.”

The Petition sets forth, and *we find*, that Yamaguchi teaches the following limitations of claim 1:

a) “A semiconductor wafer (1), having a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2)”: Figure 1 of Yamaguchi showing an exposure field with a consistent number of chips, the given number depending on whether a TEG pattern is also included in the exposure field. Pet. 20–21 (citing Thompson Decl. ¶¶ 73–75, 81; Ex. 1003, 2:8–9, 2:43–54, Fig. 7).

b) “having process control modules (4) which are each arranged in a given area on the semiconductor wafer (1), in which the given areas are formed by the exposure fields (2)”: TEG region 14 of Figure 1 includes a process control module arranged in the TEG pattern region of reticle 10, which is used to generate exposure fields (and the TEG region) on a wafer. Pet. 17, 21, 23–24 (citing Thompson Decl. ¶¶ 73–76, 81; Ex. 1003, 1:40–53, 5:15–19, 5:24–32, 7:17–27, 9:5–20, 10:33–38, 11:43–47, Figs. 1, 3–4, 6C, 7).

Claim 1 further recites that “each process control module (4) takes the place of at least one chip (5).” Petitioner contends that Yamaguchi discloses PCMs in the TEG region and PCMs as alignment marks, both of these features taking the place of at least one device chip in the exposure field. Pet. 24. We analyze this limitation further.

Figure 1 of Yamaguchi showing the TEG region or TEG pattern region is reproduced below.

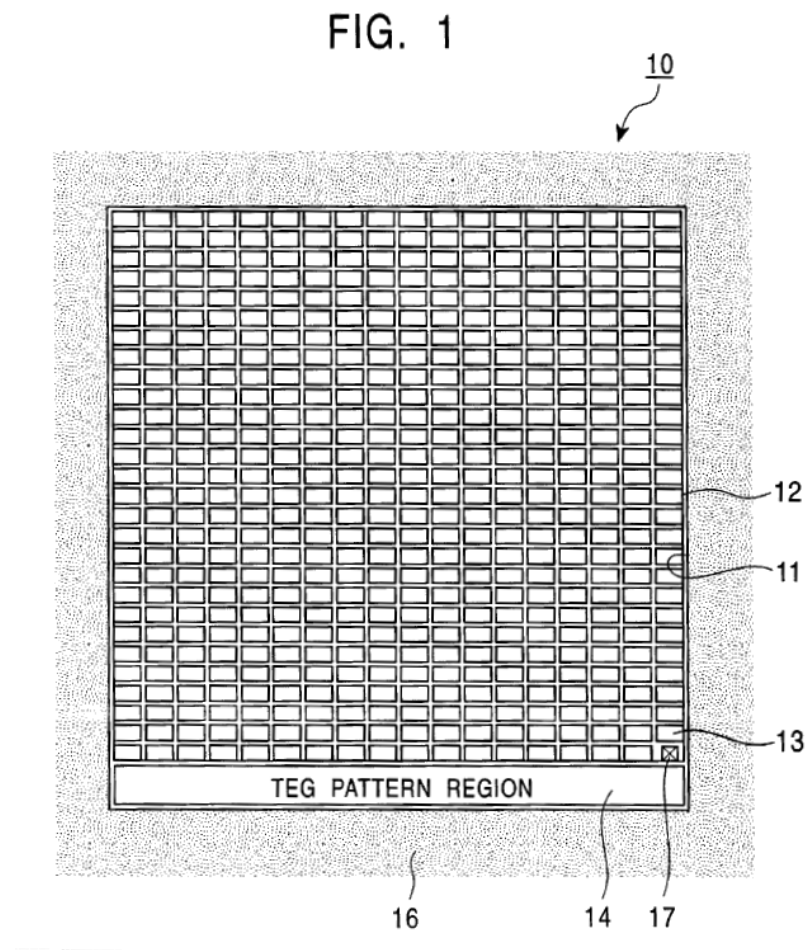


Figure 1 of Yamaguchi shows TEG pattern region 14 on reticle 10. Ex. 1003, 6:41–46. Yamaguchi states that, for this embodiment, the width (or vertical dimension) of “TEG pattern region 14 corresponds to two rows of the semiconductor device chip patterns.” *Id.* at 7:25–28. Petitioner

argues that “the PCMs that compromise [sic] the TEG region . . . each takes the place of at least one device chip in the exposure field.” Pet. 24 (citing Ex. 1003, 2:1–5).

Patent Owner proffers three arguments in response to Petitioner’s challenge as summarized above. Each argument is addressed in turn below.

(1) Yamaguchi’s TEGs are for Electrical Testing, After Wafer Fabrication

First, Patent Owner argues that the TEGs are not process control modules because Yamaguchi uses these “after the wafer fabrication process has been completed and all chip circuitry is in place.” PO Resp. 18 (citing Subramanian Decl. ¶ 40). As stated above with regard to claim construction, however, we determine that the “process control module” is not limited to those used for in-line testing. Yamaguchi plainly describes the TEGs as “test devices for measuring electrical characteristics,” (Ex. 1003, 1:37–38), and as testified to by Dr. Thompson, who we credit in this regard, electrical characteristics are tested both during in-line parametric testing and at wafer sort. Reply 12; Reply Thompson Decl. ¶¶ 4–6. This evidence thus supports our determination that Yamaguchi’s test devices perform the function of the recited “process control modules,” i.e., detecting flaws on a semiconductor wafer. Reply Thompson Decl. ¶ 5 (citing further Attachment B of declaration which states at table 19.2, page 29 of Exhibit 1011, that various test structures are used for “Fault Measurement” and at table 19.3, page 30 of Exhibit 1011, that measuring the test structures during in-line parametric tests, the resulting data is recorded and compared with the expected electrical results).

Now, we understand the Petition to present arguments as to whether a single TEG or the TEG region meets the claim limitation. On the one hand,

Petitioner states that the “test elements in the TEG region of Yamaguchi correspond to the PCMs” in the ’523 patent. Pet. 20 (citing Thompson Decl. ¶¶ 73–76, 81). And Petitioner also argues that some exposure fields include TEG regions, thereby also equating a TEG region with a process control module. *Id.* at 21 (citing Ex. 1003, 2:44–47 and arguing also that Yamaguchi discloses “an exposure field with a consistent number of chips and a *TEG pattern* that replaces one or more chips at the bottom.” (emphasis added)); Reply 14 (arguing that the TEG region is a process control module because it contains a collection of test structures); *see also* Ex. 1012, 82:5–9 (Dr. Subramanian agreeing conceptually that a process control module could encompass multiple test structures as long as the process control module meets the definition of the recited term). Because Yamaguchi’s TEGs (plural) in a TEG region are test devices for measuring electrical characteristics, the TEG region meets the definition of a “process control module” as we have construed the term.

Thus, we find that Yamaguchi’s TEG region meets the definition of “process control module” as it is a structure used for testing electrical characteristics of the wafer.

(2) Yamaguchi’s TEGs do not Take the Place of at Least one Chip

Second, Patent Owner contends that Yamaguchi does not disclose the size of these TEGs and there is no mention of how many TEGs are in the region so that one could establish that a TEG replaces at least one chip. PO Resp. 19–26. Further, according to Patent Owner, Yamaguchi’s TEG region contains multiple TEGs. *Id.* at 20–21 (citing Ex. 1003, 7:18–20). Yamaguchi explains that the vertical dimension of the TEG region corresponds to two rows of semiconductor chip pattern. Ex. 1003, 7:21–28.

Thus, Patent Owner argues, the claim requires that each TEG (not the TEG region as a whole) takes the place of at least one chip, but each TEG does not take the place of one chip. PO Resp. 21.

Petitioner contends that “a TEG pattern [] replaces one or more chips at the bottom” (Pet. 21)⁶ and that the TEG region is a process control module and meets the claim (Reply 14). According to Petitioner, the record contains evidence that a PCM refers to a field or area that can incorporate multiple structures. Reply 14 (citing Ex. 1012 82:5–9) (Dr. Subramanian testifying that a PCM can encompass multiple test structures and meet the requirement of being a process control module). Patent Owner argues that the Petition mapped the entire TEG region to a PCM, not specific test structures within the TEG region—and, therefore, Petitioner cannot now allege that discrete test structures are PCMs. Sur-reply 14–15.

We are not persuaded by Patent Owner’s arguments. The claim requires that “each process control module (4) takes the place of at least one chip (5).” The language does not require that the size of a PCM must be equivalent to the size of one chip. Nor does the claim require a one-for-one correspondence—that one process control module replace one chip. Thus, Patent Owner’s arguments regarding the size of Yamaguchi’s TEGs (or the lack of information thereof) are unpersuasive. If the entire TEG region is a PCM, as it contains several test structures (Reply 14 (citing Ex. 1012 82:5–9)), then Yamaguchi still meets the claim as asserted by Petitioner, because the TEG region “takes the place of at least one chip (5),” as recited in claim 1. The unbounded qualifier “at least one” renders the limitation broad enough such that the TEG region, by taking the space of two rows of

⁶ Citing Ex. 1003, Fig. 1, 2:1–5.

chips, meets the claim language. Ex. 1003, 7:21–28. Accordingly, we need not decide whether a single TEG would meet the limitation.

(3) Yamaguchi's TEG Region is Formed Outside of Device Pattern Region

Third, Patent Owner argues that the TEG region cannot take the place of at least one chip as required by the claim because the TEGs are formed in a different area of the wafer, specific to forming TEGs, but not devices. PO Resp. 26–27. According to Patent Owner, because the TEG region is distinct from the device region, Yamaguchi's TEGs cannot take the place of at least one chip, as chips cannot be formed in the TEG region. *Id.* at 27 (citing Ex. 1003, 6:41–46, 9:5–8; Subramanian Decl. ¶¶ 32–33).

Patent Owner then argues that the different exposure steps of Yamaguchi confirms that device pattern region 12 and TEG region 14 are distinct and separate regions of the reticle, such that when Yamaguchi provides for forming chips, it exposes device pattern region 12 (or a portion thereof), and when Yamaguchi desires to form a TEG region, it exposes reticle 10 in its entirety. *Id.* at 28–29. Thus, according to Patent Owner, Yamaguchi's exposure process ensures that no TEG is located in the area where chips are located and thus cannot take their place. *Id.* at 30 (citing Subramanian Decl. ¶ 38).

Patent Owner's arguments are not persuasive. Yamaguchi discloses a reticle that provides distinct regions in which device chips and TEGs are located. *See, e.g.*, Ex. 1003, 6:41–46. Yamaguchi discloses a process that masks certain portions of the reticle depending on which region (and how much of the region) is going to be exposed. *See id.* at 9:5–10:38. Claim 1, however, is directed to the resulting wafer having process control modules that take the place of at least one chip. As Petitioner argues, and we agree,

the TEG region contains no chips, but by disclosing including a TEG region during one of the exposure steps, Yamaguchi teaches displacing chips that otherwise would have been placed there. *See* Reply 14–15 (citing Ex. 1003, 4:38–39); *see also* Ex. 1003, 4:36–53 (explaining that areas of the semiconductor wafer exposed through the reticle are “exposed areas” and these areas include a device region exposed through the device pattern region “and/or a TEG region exposed through the TEG pattern region on the reticle”). Yamaguchi supports this because, as argued by Patent Owner, Yamaguchi repeatedly projects the device pattern region until it exposes the part of the reticle that includes a TEG region adjacent to a device pattern region. PO Resp. 28–29 (discussing Ex. 1003, 9:21–22, 9:29–30). In other words, but for the intentional exposure of the TEG region during exposure of the full reticle 10 (i.e., both the device region and the TEG region), the area that the TEG region occupies would have been designated to contain two rows of devices. Ex. 1003, Figs. 3–4, 9:5–20 (explaining that device pattern region 2 is projected repeatedly as necessary and the full reticle is projected); 9:21–28 (explaining that the TEG regions are formed when the full reticle is exposed so that the TEG region adjoins a previously exposed area containing only devices); 7:21–28 (describing the TEG region as corresponding to two rows of semiconductor device chip patterns).

Furthermore, as we stated in our Decision on Institution, claim 1 does not recite any specific order or manner of exposing the reticle or certain portions of the reticle to form the exposure fields and placing process control modules on the wafer. The claim further does not preclude forming fields on the semiconductor wafer in more than one step. The claim is plainly directed to a semiconductor wafer with adjacent exposure fields that may or

may not include PCMs; but, if they do include PCMs, these are located in the place of at least one chip. The location of the PCMs recited in the claim contrasts to the '523 patent's description of PCMs located in drop-in areas, dicing paths between chips, or together with the chip in a given area.

Ex. 1001, 1:10–15, 1:27–30, 1:42–47. Thus, the claim language requires the PCMs are located in exposed fields where chips could be placed, but are not because instead PCMs are formed there during fabrication. Yamaguchi's resulting semiconductor wafer shows this, for instance, in Figure 6C, on which Petitioner relies at page 23 of the Petition; Yamaguchi's TEG pattern is formed in an area spanning two rows of chips in some of the exposure fields. *See* Pet. 22 (citing Ex. 1003, Figs. 1, 6C, Fig. 7, 7:17–27, 10:33–38, 11:43–47), *see also* Pet. 21 (relying also on Figure 1 of Yamaguchi because it discloses “an exposure field with a consistent number of chips and a TEG pattern that replaces one or more chips at the bottom”). That Yamaguchi has a specific TEG region and a specific device region in the reticle does not change the fact that the *exposure fields* on the wafer have either TEGs or devices, with the TEGs replacing two rows of devices when a TEG region is formed in place of additional rows of devices on a wafer during an exposure. *See* Pet. 20–21 (“Yamaguchi specifically discloses including TEG regions in some of the exposure fields, thus having two types of exposure fields, some with TEG regions and some without.” (citing Ex. 1003, 2:44–47));

Thompson Decl. ¶ 82; *see also* Ex. 1003, 4:36–53. Petitioner has persuasively shown that Yamaguchi teaches the claim limitation. Thus, we are not persuaded by Patent Owner's arguments that Yamaguchi's TEG region does not take the place of at least one chip as required by claim 1.

(4) Whether Alignment Marks are PCMs

Now we turn to an analysis of Petitioner’s alternative or second mapping to the recited “process control module” that relies on Yamaguchi’s alignment marks. Pet. 23–24. For instance, Figure 1 of Yamaguchi depicts alignment mark 17 in the bottom right corner of device pattern region 12. Ex. 1003, Fig. 1. Petitioner argues that the alignment mark is a PCM located in an exposure field and also takes the place of at least one chip. Pet. 24. Patent Owner argues that Yamaguchi’s alignment marks are not PCMs. PO Resp. 15–17. As a matter of claim construction, discussed above in Section II.A., we agree with Patent Owner that the Specification does not support Petitioner’s assertion that the term “process control module” encompasses an alignment marker. Furthermore, we are persuaded by Patent Owner’s argument that the ’523 patent describes alignment markers or marks distinctly from process control modules and that Yamaguchi describes the alignment marks as positional references for laser trimming. *Id.* 15–16 (citing Ex. 1001, 1:24–25, Subramanian Decl. ¶ 51). More importantly, Petitioner has not shown sufficiently that alignment marks are structures configured to detect a flaw, consistent with the proffered construction of “process control module.” *See* Pet. 22–24 (citing consistently Yamaguchi’s description of the alignment marks as a pattern for laser trimming). Accordingly, we determine, consistent with our preliminary determination in our Decision on Institution, that Yamaguchi’s alignment marks do not meet the “process control module” limitation of claim 1.

(5) Conclusion: Claim 1

We have considered Petitioner’s contentions and evidence and Patent Owner’s arguments and evidence in opposition, and, on the full record

before us, we determine that Petitioner has shown by a preponderance of the evidence that claim 1 is unpatentable as obvious over Yamaguchi.

ii. Claims 2 and 3

Claim 2 depends from claim 1 and further recites that “a process control module (4) is present in each of at least 25% of all the exposure fields (2), and in which the process control modules (4) are situated at equal distances from each other with respect to two mutually perpendicular coordinate directions (7, 8).” For this claim, Petitioner relies exclusively on Yamaguchi’s alignment marks 17 as corresponding to the claimed “process control modules.” Pet. 25–26. As stated above with regard to claim 1, we do not agree with the contention that alignment markers are a type of PCM. *See also* PO Resp. 31. Claim 3 depends from claim 2. Petitioner does not provide any evidence or argument regarding claim 3 beyond the Yamaguchi alignment mark mapping already considered. Accordingly, we determine that Petitioner has not shown by a preponderance of the evidence that claims 2 and 3 are unpatentable as either anticipated by or obvious over Yamaguchi.

iii. Claim 4

Claim 4 depends from claim 1 and further recites that “all the process control modules (4) are each situated at the same location (6) in the respective exposure fields (2).” Petitioner argues that Yamaguchi discloses that the TEG region and alignment marks are in the same position in each exposure field containing them. Pet. 26. For the TEG region, Petitioner argues, and we agree, that although “the TEG region might be at the bottom or the top of the exposure field, depending on the structure, Yamaguchi discloses it as always being in the same place.” *Id.* at 27; Ex. 1003, Figs. 1,

6C, 7. Patent Owner does not argue this dependent claim. *See, e.g.*, PO Resp. 31 (arguing dependent claims 2 and 3, but not claim 4). We are persuaded that Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over Yamaguchi, because the TEG region is in the same place on reticle 10, and, therefore, in their respective exposure fields on the wafer. Ex. 1003, Figs. 1, 6C, 7.

3. Conclusion Regarding Yamaguchi Ground

Based on the foregoing, we determine that Petitioner, for claims 1 and 4, has shown by a preponderance of the evidence unpatentability under obviousness over Yamaguchi.⁷ As to claims 2 and 3, we determine that Petitioner has not demonstrated unpatentability either of anticipation by or obviousness over Yamaguchi by a preponderance of the evidence.

D. Grounds Based on Satya Alone

Petitioner asserts that claims 1–4 are anticipated or would have been obvious over Satya. Pet. 27–35.

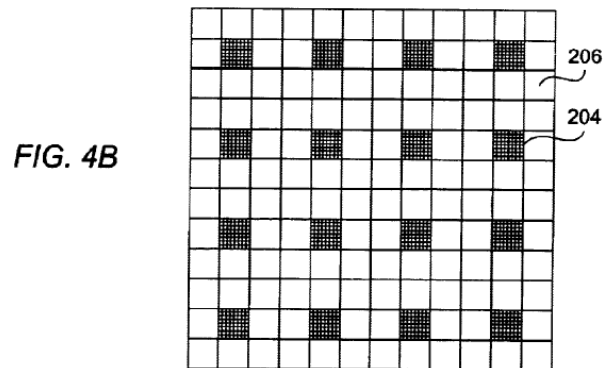
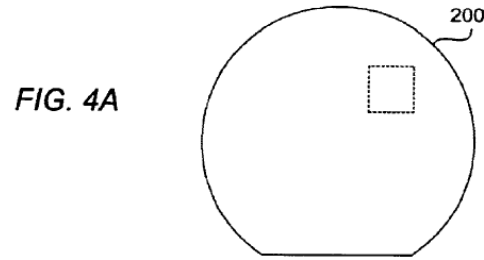
1. Overview of Satya (Ex. 1004)

Satya is directed to defect inspection and analysis of semiconductor integrated circuits. Ex. 1004, 1:21–24. Satya describes that to overcome problems of defective integrated circuits (“ICs”), manufacturers sometimes fabricate semiconductor defect test structures. *Id.* at 1:44–46. “Such defect test structures are often constructed on the same semiconductor substrate as the IC products.” *Id.* at 1:50–52. Satya describes using a scanning electron

⁷ We need not reach whether Yamaguchi anticipates claims 1 and 4 as we determine that Petitioner has shown by a preponderance of the evidence that Yamaguchi renders obvious claims 1 and 4.

microscope (“SEM”) with a continuously moving stage to detect defects in semiconductor devices. *Id.* at 4:24–41. The SEM discharges a beam with charged particles directed at the surface of a substrate for scanning that surface and includes detectors for detecting charged particles emanating from the top and bottom surfaces of the substrate. *Id.* at 2:42–56, 5:10–18. A multi-processor image defect computer is coupled to the charged particle detectors to identify defects on the substrate. *Id.* at 5:18–25. Satya discloses that defects are detected by comparing the obtained images against a standard. *Id.* at 5:36–41. That standard may be an image of another portion of the array, an image from another die of the same substrate, or an image stored in a database. *Id.* at 5:36–66.

Figures 4A and 4B, reproduced below, illustrate a semiconductor wafer prepared for use with the detection method described above. *Id.* at 10:29–32.



Figures 4A and 4B illustrate semiconductor wafer 200 comprising a die array. *Id.* Figure 4B further illustrates that the die array comprises a plurality of test dies 204 and a plurality of actual product dies 206 containing intended integrated circuitry. *Id.* at 10:32–35. Test dies 204 are laid out in an orderly row-column fashion as shown in Figure 4B. *Id.* at 10:63–64. They may occupy a predetermined area on wafer 200 so as to provide a statistically significant data set of test data, yet minimize the inspection cost and avoid adversely affecting the production yield. *Id.* at 10:67–11:4. Test dies 204 allow defect location, defect identification, defect type, and defect density through in-line inspection during the actual manufacturing process of ICs. *Id.* at 10:35–38.

In connection with a specific embodiment, Satya describes parameters for how many test structures may be included in a wafer as follows:

The quantity of test structures of each type in a given portion, or on a test chip, or over an entire wafer, is selected to provide a statistically significant sample of such test structures, so that a statistically significant quantity of defective regions is likely to be found therein. This quantity will vary with the expected yield of the chips on the wafer. For example, in a low yield process (as might be expected to be found in a process that is under development and not yet in production), a relatively small number of test devices might be needed to obtain a reasonable sample size. By contrast, in a high yield process, a larger sample size (and therefore more test structures) may be needed. The quantity of test structures may also be varied depending on the goals of the chip manufacturer. For example, if the chip manufacturer is unwilling to devote much space on the wafer to test structures, the number of such structures could be kept relatively small. If process problems arise, the quantity of test structures present on each wafer could then be increased (to provide the manufacturer with more test data regarding the process) until the nature of the problem has been determined and corrected.

Id. at 11:43–63.

2. Analysis of Grounds

After considering Petitioner’s contentions and Patent Owner’s arguments in opposition, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–4 would have been obvious over Satya.

i. Independent Claim 1

Petitioner asserts that Satya discloses or renders obvious all the limitations of claim 1. For instance, the Petition states, and we agree, that Satya teaches:

- a) “A semiconductor wafer (1) having a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is

situated in one of a multitude of adjacent exposure fields (2)” because of Figure 4B of Satya, which shows a plurality of product dies 206 containing intended ICs and Figure 4B, which shows the die array that “corresponds with the ‘exposure field’ of [the ’523 patent].”

Pet. 28–30 (citing Ex. 1004, 8:43–54, 10:33–35, 10:64–65, 11:43–63, Fig. 4A-4B; Thompson Decl. ¶¶ 70, 95–96, 98); and

b) “having process control modules (4) which are each arranged in a given area on the semiconductor wafer (1), in which the given areas are formed by the exposure fields (2)” because Satya’s die array includes a plurality of test dies 204 on specific portions of the exposure field and each test die has about the same dimensions as the product die. *Id.* at 30–32 (citing Ex. 1004, 11:4–5, Figure 4B; Thompson Decl. ¶¶ 99–100).

The Petition also sets forth that, and we agree, for the limitation “each process control module (4) takes the place of at least one chip,” Satya’s Figure 4B teaches that the PCMs take the place of at least one die. *Id.* at 31–32 (citing Ex. 1004, Fig. 4B; Thompson Decl. ¶ 100). A more detailed explanation of our reasoning follows, presented in the context of our consideration of Patent Owner’s arguments.

Patent Owner presents two main arguments regarding this ground. First, Patent Owner argues that Satya’s test die are not process control modules. PO Resp. 32–39; Sur-reply 17–18. Second, Patent Owner argues that Satya does not disclose “exposure fields.” PO Resp. at 39–51. These arguments are analyzed each in turn.

(1) Satya Does not Teach Process Control Modules

First, Patent Owner contends that the Petition does not explain how Satya's test structures "meet the claimed 'process control module.'" PO Resp. 33–34. Patent Owner contends that the "only explanation" Petitioner provided about Satya's test structures is that they encompass alignment marks. *Id.* at 36 (citing Pet. 28; Thompson Decl. ¶ 94). Patent Owner nevertheless admits that Petitioner cites portions of Satya where it describes that its test structures are "sensitive to defects," but argues that such a functional description is insufficient. *Id.* (citing Ex. 1004, 1:45–50). According to Patent Owner, the functional description does not satisfy the claim construction requirement that the PCMs are "structures." *Id.* at 36–37. We are not persuaded by Patent Owner's argument.

The Petition sets forth, and we agree, that the test structures of Satya are process control modules as they are "structures" fabricated on a wafer and are sensitive to defects that occur in the integrated circuits. Pet. 28; Ex. 1004, 1:44–55. Satya's specific disclosure of these test structures is as broad as the disclosure of process control modules in the '523 patent (i.e., they are both structures that perform a specific function of detecting flaws), and Dr. Thompson opines, who we credit, that at the time of the invention "process control monitors" were also called process control modules and test structures because they are "typically specific structures designed to test for a specific process parameter." Thompson Decl. ¶ 44 (cited in the Petition at 28). This is persuasive support of Petitioner's contention that Satya's test structures are "structures" that detect flaws in accordance with our construction of the term "process control module." *See supra* Section II.A.

Likewise, we do not find persuasive Patent Owner’s argument that Dr. Thompson’s testimony on this point lacks persuasive explanation or evidence as support. PO. Resp. 34–37. Dr. Thompson, however, explains that there are different “types” of process control modules, but all are “test structures that provide process control data.” Thompson Decl. ¶ 44. His testimony on this point uses the word “monitor” and “module” interchangeably in accordance with his experience in the field, which we note shows sufficient qualification to opine reliably on this subject matter and is supported by several textbooks. *Id.* ¶ 44–45. He confirmed the interchangeability of these words during his deposition, and no fact in the record contradicts Dr. Thompson on this point. Ex. 2006, 37:7–18; *see also* Subramanian Decl. ¶¶ 54–60 (lacking any challenge of Dr. Thompson’s understanding regarding the equivalence of Satya’s test structures with process control modules and process control monitors).

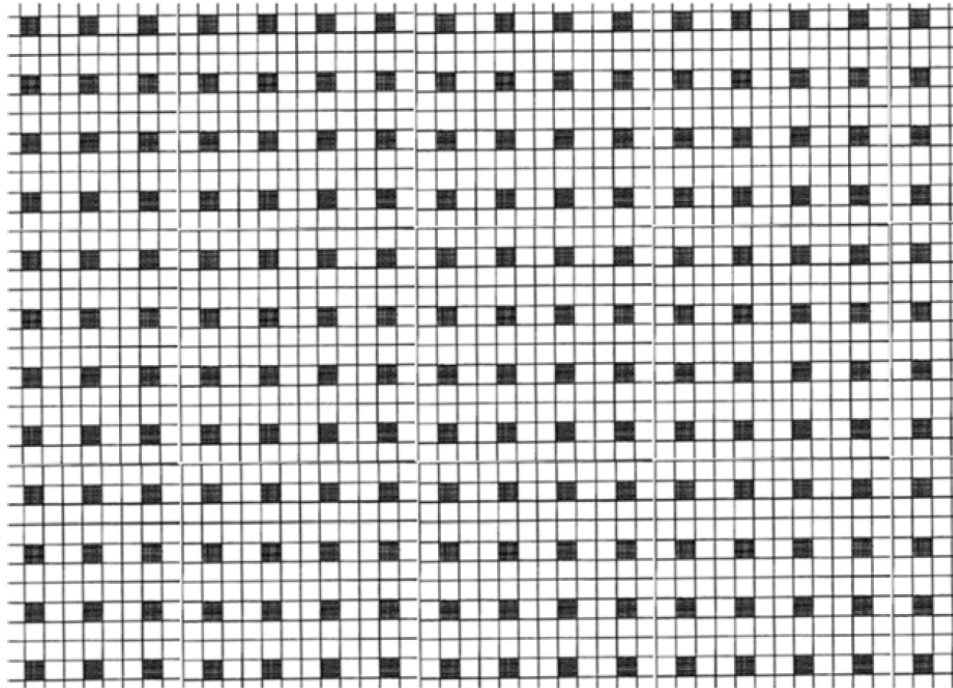
Second, Patent Owner argues that Satya’s test structures are not process control modules because they are not tested with optical lithography equipment. PO Resp. 38–39. This argument relies on Satya’s disclosure of using an electron beam system and on Patent Owner’s proposed claim construction of the term, as stated above in Section II.A. *Id.* (citing Ex. 1004, 6:39–7:7, 14:5–28, 17:24–47, 18:26–48, 20:9–20; Subramanian Decl. ¶ 57). Because we do not adopt Patent Owner’s proposed construction of the term “process control module” to include the limitation of testing with optical lithography equipment, we find Patent Owner’s argument unpersuasive.

In conclusion, we are not persuaded by Patent Owner’s arguments that the Petition failed to prove that Satya’s test structures are test structures for

detecting a flaw in accordance with the meaning of the term “process control module.”

(2) Satya Does Not Disclose “Exposure Fields”

Next, Patent Owner argues that Satya’s disclosures and Figure 4B do not show that “the given areas are formed by the exposure fields” as the claim requires. PO Resp. 39–40. In particular, Patent Owner points out that although Satya’s test dies 204 are arranged on a given area of the semiconductor layer, these test dies are not in areas formed by the exposure fields. *Id.* According to Patent Owner, and relying on the ’523 patent for support, the exposure fields on which the process control modules are formed “need to have a fixed relationship to the geometry of the exposure field—e.g., be in the corner of the exposure field [] or in the center of the exposure field [], or maybe along the side of the exposure field.” *Id.* at 41 (citing Ex. 1001, 3:11–14, 3:26–27, 3:30; Subramanian Decl. ¶¶ 62–65). Patent Owner reasons that the position of the process control modules in the exposure fields accords with an objective of the invention of identifying “very easily, i.e. even with the naked eye,” the individual exposure fields. *Id.* at 40 (citing Ex. 1001, 2:6–26; Subramanian Decl. ¶ 66). According to Patent Owner, if the entire Figure 4B of Satya were equivalent to a *single* exposure field, a wafer section with *multiple* exposure fields would look like the image below, created by Patent Owner to illustrate the point. PO Resp. 44.



The above figure from Patent Owner illustrates the die array shown in Satya’s Figure 4B repeated four times horizontally and three times vertically in a grid pattern. *Id.* The point of this illustration, Patent Owner argues, is to show that the placement of test dies 204 (the black squares in the grid) “would not make it possible to visually identify individual exposure fields.” *Id.* at 43–44. In contrast, the argument goes, the same number of repeated exposure fields disclosed in the ’523 patent would make it easier to identify the exposure fields. *See* PO Resp. 44 (showing a grid pattern that Patent Owner created with the exposure field depicted in Figure 2 of the ’523 patent). The argument is not persuasive.

As Petitioner argues, and we agree, the claim language of claim 1 has no explicit or implicit requirement that the process control modules be placed in any particular position relative to the geometry of the exposure field to facilitate a visual inspection of the exposure field with the naked eye. Petitioner points out persuasively that even Dr. Subramanian agrees that the

claim does not require the alleged benefit. Reply 19 (citing Ex. 1012, 111:13–15). We decline, therefore, to read into claim 1 the need to satisfy the alleged benefit of a visual inspection. Furthermore, the size of the exposure fields so as to make them large enough for visual identification is also not claimed.

And Petitioner makes an obvious “design choice” argument with support from Dr. Thompson, which is not substantively challenged and we find persuasive. Reply 19 (citing Thompson Decl. ¶¶ 96–97); *see* Pet. 29 (citing Ex. 1004, 11:43–63 and arguing that the number of PCMs on an array is simply a design choice). For instance, Dr. Thompson opines that Satya describes the varying number of test structures on the die array and how these test structures are selected and located on the die array, such as to provide “a statistically significant sample of such test structures, so that a statistically significant quantity of defective regions is likely to be found therein.” Thompson Decl. ¶¶ 96–97 (quoting Ex. 1004, 8:43–43, 11:43–63). So, Petitioner’s argument goes, and we agree, a person of ordinary skill in the art—reading Satya’s explanation of selecting the number of test dies and their location to accomplish a statistically significant analysis of the devices on the wafer—would have designed the given areas formed by exposure fields to accomplish such a goal. *Id.*; *see* Ex. 1004, 11:55–56 (“The quantity of test structures may also be varied depending on the goals of the chip manufacturer.”); *see also* Ex. 1004, 10:63–11:8 (explaining that test dies 204 are laid out in an orderly row-column layout that “can be also used as a map to evaluate final test data and to locate certain types of defects occurring on various locations on the wafer during the manufacturing process.”). Based on Dr. Thompson’s testimony, Petitioner persuasively shows that Satya

teaches the layout of the die array, vis-à-vis number and placement of test structures on the die array, to be arranged in a grid pattern that makes it easier to identify the defect location on the wafer and to obtain statistically significant data sets to evaluate such defects.

Patent Owner challenges Petitioner's position in general as giving no meaning to the words "given areas" recited in claim 1. Sur-reply 17–18. According to Patent Owner, mere design choice does not explain what meaning the "given areas" would have and that the visual identification provides that explanation. *Id.* Again, the argument is unpersuasive because there is no evidence in the '523 patent or otherwise that the words "given areas" in the challenged claims means that the resulting wafer must be suitable for a visual inspection of the exposure fields. Patent Owner's argument is also unpersuasive because the '523 patent does not support Patent Owner's contention that a visual (naked eye) inspection is the only benefit of arranging process control modules in a given area formed by exposure field. The '523 patent describes a further, non-manual (or visual) inspection of the exposure fields by disclosing that inspection of the wafer may be further performed during the automatic processing of the chips and additionally using a pick-and-place device to position devices and avoid removing the wrong chip. Ex. 1001, 2:13–26. Again, none of these so-called "benefits" is claimed by the language of claim 1. Nevertheless, the potential other beneficial uses (*id.*) of process control modules arranged in given areas of an exposure field lead us to disagree with Patent Owner's contention that we must reject Petitioner's contention regarding Satya because the die array, if repeated on a wafer as many times as Patent Owner alleges, would not be useful for visual inspection.

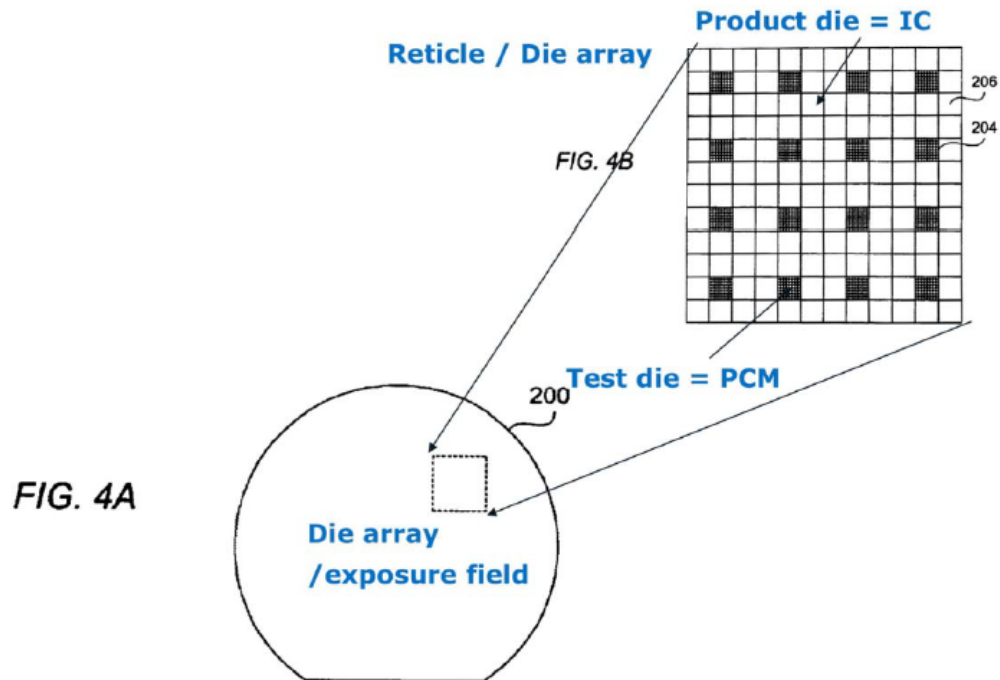
As a final argument, Patent Owner contends that Satya's die array is not an exposure field. PO Resp. 45. According to Patent Owner, Figure 4B is not described as a "single" exposure field, and a person of ordinary skill in the art would not understand such a figure to depict a single exposure field. *Id.* (citing Subramanian Decl. ¶ 70). Furthermore, Patent Owner argues, the manner in which Satya describes "reticles"—succinctly, in one paragraph, and unconnected to the description of Figure 4B—would not have informed a person of ordinary skill in the art that Satya's die array is a single exposure field. *Id.* at 45–47 (citing Ex. 1004, 8:43–61, 10:32–35, Fig. 4B; Subramanian Decl. ¶¶ 71–72). Furthermore, Patent Owner asserts that a person of ordinary skill in the art would not have interpreted Satya's Figure 4B as the die array 202. *Id.* at 47 (citing Subramanian Decl. ¶ 74). Patent Owner then provides possible configurations of a die array, because Figure 4B could be a subset of die array 202 or die array 202 may be a subset of Figure 4B. *Id.* According to Dr. Subramanian, to the extent a person of ordinary skill would have linked Satya's discussion of reticles to Figure 4B, a person of ordinary skill "could reasonably conclude that the test die of Figure 4B were each in their own exposure field, or at least that there were multiple fields in Figure 4B—either of these conclusions contradict[ing] the premise of Petitioner's contention." Subramanian Decl. ¶ 35.

All of these arguments amount to the contention that Satya fails to explain sufficiently that a die array would be an exposure field (or a reticle) and that any possible configuration of the die array, under Patent Owner's characterization of Satya, would not meet claim 1. PO Resp. 49–50. And that even if the test structures (or test die) were arranged in a given area of the wafer, Satya does not disclose that those areas are formed by the

exposure fields or that the chips are situated in adjacent exposure fields (reticles). *Id.* at 50–51. None of these arguments is persuasive.

We credit Dr. Thompson’s testimony over the testimony of Dr. Subramanian that explains that an exposure field is also called a die array. Thompson Decl. ¶ 40. Dr. Thompson explains that the full pattern on the wafer results from a die array pattern that is reproduced or stepped across the wafer. *Id.* Dr. Thompson supports his testimony with a technical dictionary definition from the field of semiconductor manufacturing technology. *Id.* ¶ 41. According to Dr. Thompson, who cites factual support for this opinion, a stepper transfers a full die array pattern onto a wafer in a sequence of exposures of the die array. *Id.* (citing textbook on semiconductor manufacturing). This testimony is unrebutted. *See* Subramanian Decl. ¶¶ 70–79 (omitting any discussion of the understanding of a person of skill in the art concerning the equivalence or overlap of the terms die array, reticle, and exposure fields in the relevant art); *see also* Dec. on Inst. 20 (noting our reliance on Dr. Thompson’s testimony regarding the “die array” definition and how it supports Petitioner’s contentions); Ex. 2006, 32:15–35:11.

Dr. Thompson applies the above-stated understanding to Satya and testifies that Figure 4B of Satya shows a die array, which is an exposure field. Thompson Decl. ¶ 96. Satya’s Figures 4A-4B, reproduced below with annotations, show how Satya’s die array is an exposure field.



Figures 4A and 4B above include annotations added by Petitioner to show that plurality of test dies 204 (black squares) and product dies 206 are arranged in a grid pattern forming a die array or reticle, which is then exposed on wafer 200, as shown in Figure 4A. *Id.*; see also Ex. 1004, 10:29–38; Reply Thompson Decl. ¶ 9. Petitioner persuasively shows that a person of ordinary skill in the art would have understood Figure 4A as showing a die array as an exposure field because it would not make commercial sense otherwise. Reply Thompson Decl. ¶ 9; Reply 18. And according to testimony elicited during cross-examination of Dr. Thompson, wafers at the time of Satya’s disclosure were eight inches in diameter, with exposure fields about one-inch square. Reply Thompson Decl. ¶ 9; Ex. 2006, 98:6–99:9 (testifying regarding Figure 4A of Satya and the square box Dr. Thompson has annotated as a die array). Thus, Satya describes to a person of ordinary skill in the art that the die array shown in Figure 4B is a reticle or exposure field that is stepped on a wafer until a full die array

pattern is exposed on the wafer. *See* Ex. 2006, 99:14–101:24; Reply 18. We credit the testimony of Dr. Thompson as the most credible and consistent with the disclosures of Satya.

In contrast, Patent Owner relies on Dr. Subramanian’s testimony that Satya fails to *expressly* state that the die array shown in Figures 4A and 4B is a reticle or exposure field. Sur-reply 45. Specifically, Dr. Subramanian opines that Satya *does not state* that the die array depicted in Figure 4B is a single exposure field. Subramanian Decl. ¶ 70. This testimony is not persuasive because it focuses only on whether something is expressly stated in Satya, and not on what it teaches to a person of ordinary skill in the art. A reference is prior art not just for what it states but also for the details that a person of ordinary skill in the art would infer from its teachings. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418, 421 (2007) (“A person of ordinary skill in the art is also a person of ordinary creativity, not an automaton” and we should take into account “the inferences and creative steps that a person of ordinary skill in the art would employ.”).

We are also not persuaded by Dr. Subramanian’s testimony that Satya’s discussion of “reticles” does not inform other disclosures of die arrays, such as the disclosure of the embodiment in Figure 4B. Subramanian Decl. ¶ 71. As already discussed, there is persuasive evidence that the “reticle” of Satya is a die array or exposure field. *See* Thompson Decl. ¶¶ 40–41, 96; Reply Thompson Decl. ¶ 9.

Also, as we discussed in our Decision on Institution at pages 20–21, the discussion of reticles in Satya also supports Petitioner’s contention that Satya’s die array is a single exposure field. Ex. 1004, 8:43–61; *see also* Pet. 28–29 (citing Ex. 1004, 8:43–54). Satya explains that multiple reticles may

be used to manufacture wafers in a lot. *Id.* at 8:43–48. For instance, Satya discloses that some of the wafers would be patterned with reticles having large areas devoted to test structures, while the remaining wafers of the lot would be patterned with reticles having relatively fewer test structures. *Id.* at 8:48–53. Satya also explains that for a *given wafer*, one *reticle* with a large area for test structures may be used for a *fraction of that wafer*, and the *remaining fraction* may be patterned with the *reticle* having fewer test structures. *Id.* Thus, a resulting wafer may have exposure fields of varying density of test structures. That discussion provides context for Satya’s further disclosure of the “orderly layout” shown in Figure 4B, where test structures may occupy a “predetermined area on the wafer 200,” or may take up the entire wafer, and that “the wafer could be comprised entirely of test dies.” *Id.* at 10:63–11:8. That is, given that Satya’s reticles are used to provide a variety of arrangements and amounts of test structures on wafers, we conclude that Satya’s discussion of the die arrays having distinct layouts and amounts of test structures is consistent with the notion that Satya’s die array of Figure 4B is a single exposure field and the wafer of Figure 4A includes multiple exposure fields. Accordingly, Patent Owner’s argument and Dr. Subramanian’s testimony that a person of ordinary skill would not have understood Figure 4B to teach an exposure field or reticle is unpersuasive. PO Resp. 45–50; Subramanian Decl. ¶¶ 70–76.

(3) Conclusion as to Claim 1

Therefore, following from the above analysis, and crediting Dr. Thompson’s testimony as discussed previously, we find that Satya teaches a reticle or exposure field in the form of a die array (shown in Figure 4B) that may be configured with test structures and chips arranged thereon as needed

to obtain statistically significant defect analysis. *See* Ex. 1004, 8:43–48, 10:63–11:8, 11:43–63; Thompson Decl. ¶¶ 96–97. We also find that Satya teaches, consistent with Petitioner’s argument and evidence, that the test structures are arranged in given areas formed by exposure fields because those test structures are placed in a specific square in the grid of the die array (“reticle”), where each square is of the same dimension as the integrated circuits arranged adjacent the test structures. *See* Pet. 30–31; Thompson Decl. ¶¶ 98–99; Ex. 1004, Fig. 4B, 10:33–35, 10:64–65, 11:4–5; Reply 18–19. Thus, Satya’s wafer (such as the one depicted in Figure 4A) teaches the limitations of claim 1 requiring a multitude of chips, where a given number of chips is situated in one of a multitude of adjacent exposure fields (Satya’s reticle or die array) and where given areas (formed by the exposure fields or reticles) of the wafer has process control module arranged thereon.

And finally, supported by Satya’s Figure 4B and the testimony of Dr. Thompson, which we credit in this regard, a person of ordinary skill in the art would have understood that Satya’s test structures replace at least one chip on the exposure field or die array shown in Figure 4B. Pet. 31; Thompson Decl. ¶ 100; Ex. 1004, Fig. 4B. As shown in Petitioner’s annotated Figure 4B, reproduced below, a comparison of this figure and Figure 2 of the ’523 patent illustrates this last point.

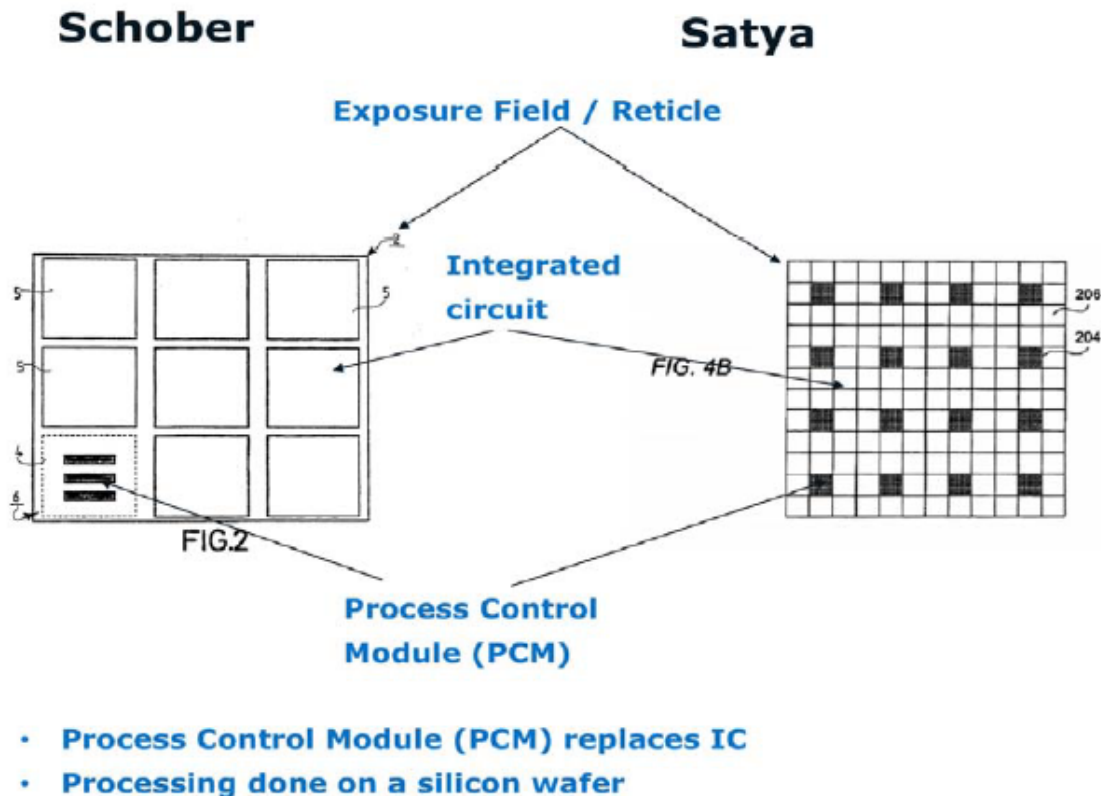


Figure 4B of Satya is compared with Figure 2 of the '523 patent, with annotations showing that the exposure field 2 of the '523 patent corresponds to the die array of Satya, each chip 5 of the '523 patent corresponds to the integrated circuit of Satya (white squares), and each process control module 5 of the '523 patent corresponds to Satya's test structures or test die 204 (black squares in the die array). *See Thompson Decl.* ¶ 100. Thus, each test structure replaces a chip because the die array can have any number of test structures and if placed in any given location on the die array, it replaces an integrated circuit that otherwise would be placed there.

Accordingly, Satya teaches all the limitations of claim 1 of the '523 patent.

ii. Claims 2 and 3

Claim 2 depends from claim 1 and further recites “a process control module (4) is present in each one of at least 25% of all the exposure fields (2), and in which the process control modules (4) are situated at equal distances from each other with respect to two mutually perpendicular coordinate directions (7, 8).” Petitioner asserts that Satya discloses that the reticle can be stepped over the entire wafer and that the number of test dies in a given exposure field is a “design choice” subject to variation. Pet. 32–33 (citing Ex. 1004, Fig. 4B, 10:29–38, 8:48–53. Petitioner further asserts that if Satya’s die array or reticle, which contains PCMs as claimed, were stepped over the entire wafer, every field would contain a PCM. *Id.* at 33 (citing Thompson Decl. ¶¶ 34–41, 101, 102). Furthermore, according to Petitioner, Satya teaches that a wafer may be composed entirely of test structures (or PCMs) for testing a new process. *Id.* (citing Ex. 1004, 11:7–8).

Patent Owner argues for the dependent claims (claims 2, 3, and 4) that Petitioner cannot show Satya teaches the further recited limitations because Satya does not teach “where the exposure fields are in relation to the wafer and on where the test dies are in relation to the exposure fields.” PO Resp. 51.

Patent Owner’s arguments are unpersuasive for the same reason we explained with respect to claim 1. Particularly we explained that Satya’s die array teaches an exposure field and that Figures 4A and 4B teach that a die array relates to the wafer, where multiple die arrays are exposed on the wafer resulting in a full die array pattern. *See* Ex. 2006, 99:14–101:24; Reply 18; *See also* Ex. 1004, 8:43–48, 10:63–11:8, 11:43–63; Thompson

Decl. ¶¶ 96–97. We also explained above how the evidence of record shows that the test structures or test dies in Satya are arranged in the grid of die array according to the design parameters for detecting defects. *See* Ex. 1004, 8:43–48, 10:63–11:8, 11:43–63; Thompson Decl. ¶¶ 96–97.

We determine that Petitioner has shown that, because Satya’s test dies would be present in 100% of all the patterned arrays, the claimed PCMs would be present in at least 25% of all the exposure fields and the depicted PCMs in Figure 4B would be situated at equal distances from each other as recited in claim 2. Thompson Decl. ¶ 101 (testifying that Satya’s reticle shown in Figure 4B, stepped over the entire wafer, results in a wafer in which every field would contain a process control module and meeting the limitation that they are situated at equal distances from each other).

Claim 3 depends from claim 2 and further recites that “a process control module (4) is present in each exposure field (2).” Petitioner again relies on the die array shown in Figure 4B and the reticle being stepped across the entire wafer, ensuring that each exposure field in the wafer would include PCMs. *Id.* at 34; Thompson Decl. ¶ 101. We are persuaded by Petitioner’s argument and evidence regarding claim 3.

Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 2 and 3 would have been obvious over Satya.

iii. Claim 4

Claim 4 depends from claim 1 and further recites “all the process control modules (4) are each situated at the same location (6) in the respective exposure fields (2).” Petitioner relies on the die array shown in Figure 4B, described as the “orderly layout” discussed above. *Id.* at 35.

According to Petitioner, “[t]his ‘orderly layout’ and repetition of the same structure across the wafer ensures that the test die would be situated at the same location in each of the exposure fields (die arrays, 202).” *Id.*

We addressed Patent Owner’s argument concerning the dependent claims above with respect to claims 2 and 3. We are persuaded by Petitioner’s argument and evidence concerning this claim.

We determine that Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over Satya.

3. Conclusion Regarding Satya Grounds

Having reviewed Petitioner’s information and Patent Owner’s arguments and evidence in opposition, we determine that Petitioner has shown by a preponderance of the evidence that claims 1 through 4 would have been obvious over Satya.⁸

E. Additional Obviousness Ground

Petitioner asserts that claims 1–4 would have been obvious over Yamaguchi and Satya. Pet. 36–39. Patent Owner challenges this ground as lacking explanation of how and why a person of ordinary skill in the art would have combined the various elements of Yamaguchi and Satya. Prelim. Resp. 22–23.

We have determined that claims 1 through 4 have been shown to be unpatentable by a preponderance of the evidence based on Satya alone. We therefore do not reach this ground.

⁸ We need not reach whether Satya anticipates claims 1 through 4 as we have already determined that Petitioner has shown by a preponderance of the evidence that Satya renders obvious claims 1 through 4.

III. CONCLUSION

We have addressed each challenged claim of the '523 patent and determine that Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.⁹ Consistent with 35 U.S.C. § 318, this Final Written Decision therefore disposes of all patent claims challenged by Petitioner. *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, Nos. 2019-1594, -1604, -1605, 2020 WL 2071962, at *4 (Fed. Cir. Apr. 30, 2020) (non-precedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding”).

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–4	102 ¹⁰	Yamaguchi		2, 3
1–4	103	Yamaguchi	1, 4	2, 3
1–4	102 ¹¹	Satya		
1–4	103	Satya	1–4	
1–4	103 ¹²	Yamaguchi, Satya		
Overall Outcome			1–4	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–4 of the '523 patent have been proven to be unpatentable; and

FURTHER ORDERED because this is a Final Written Decision, parties to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

¹⁰ We do not reach whether Yamaguchi also anticipates claims 1 and 4 because we have determined those claims are unpatentable as obvious over Yamaguchi.

¹¹ We do not reach this ground because we have found claims 1–4 unpatentable for obviousness over Satya.

¹² We do not reach this ground.

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