

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

FRAUNHOFER GESELLSCHAFT ZUR FÖRDERUNG DER
ANGEWANDTEN FORSCHUNG EV,
Patent Owner.

IPR2020-01669
Patent 6,548,391 B1

Before JEFFREY S. SMITH, MICHELLE N. WORMMEESTER, and
GARTH D. BAER, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background and Summary*

Petitioner filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–4, 6–8, and 11–13 of U.S. Patent No. 6,548,391 B1 (Ex. 1001, “the ’391 patent”). Patent Owner filed a Response. Paper 17 (“PO Resp.”). Petitioner filed a Reply. Paper 27 (“Reply”). Patent Owner filed a Sur-Reply. Paper 28 (“PO Sur-Reply”). A hearing was held on January 27, 2022.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claims 1–4, 6–8, and 11–13 are unpatentable.

B. *Related Matters*

The parties indicate that the ’391 patent is the subject of *Semiconductor Connections LLC v. Taiwan Semiconductor Company Limited et al.*, Case No. 6:20-cv-109 (W.D. Tex.), and Petitioner filed another petition challenging claims 1–4, 6, 7, and 11–13 of the ’391 patent in Case IPR2020-01670. *See* Pet. 90; Paper 5, 2–3.

C. *The ’391 Patent*

The ’391 patent relates to a method of producing a three-dimensional integrated circuit. Ex. 1001, 1:8–9. The method connects a first semiconductor substrate and a second semiconductor substrate in such a way that an electrical connection and a mechanical connection between the two substrates are established exclusively with first and second lands. Ex. 1001, code (57), 4:15–19, 4:41–45. Figures 2a and 2b illustrate an example of how the two substrates are joined, and are reproduced below. Ex. 1001, 6:25–26.

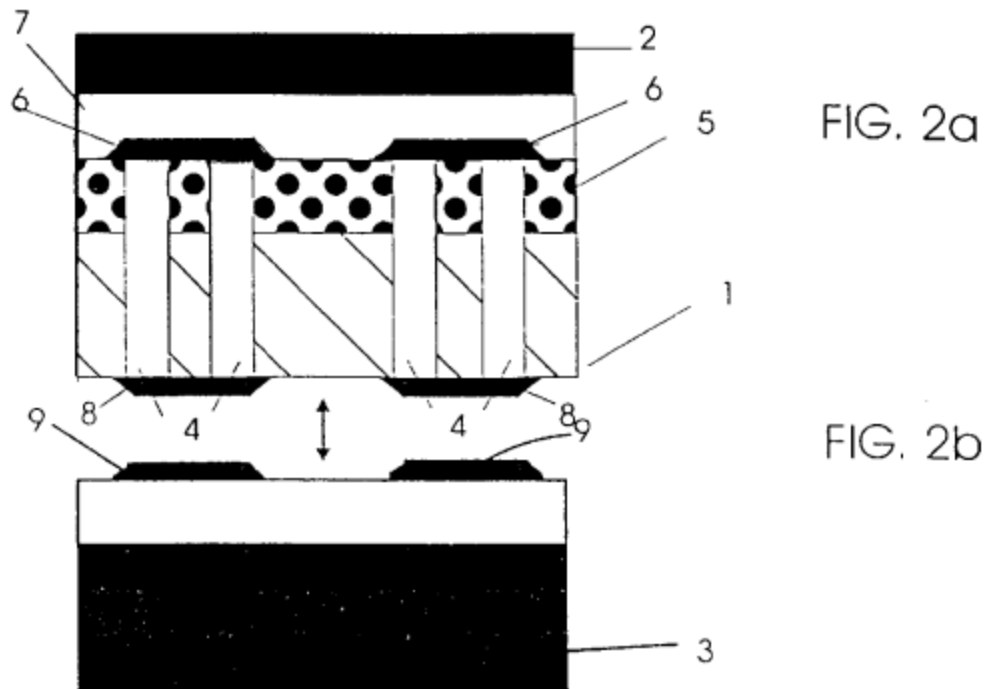


Figure 2a above shows via holes 4 formed in upper substrate 2. Ex. 1001, 6:37–42. An insulating layer such as silicon dioxide lines the surface of the via holes, and the via holes are filled with an electrically conductive material. Ex. 1001, 6:42–46. Via holes 4 connect first lands 8 to electrically active regions. Ex. 1001, 6:56–67. Figure 2b above shows lower substrate 3 with second lands 9 arranged in a mirror inverted mode of arrangement relative to first lands 8, so that when the upper substrate is aligned with and placed on the lower substrate, lands 8 and 9 touch each other. Ex. 1001, 7:1–7. A suitable bonding method, such as a process based on the solid-liquid interdiffusion of two metals, forms a eutectic alloy that mechanically and electrically connects the upper and lower substrates. Ex. 1001, 5:20–65, 7:12–25. As a result, it is not necessary to apply any separate layer for mechanically connecting the upper and lower substrates. Ex. 1001, 5:30–32.

D. Illustrative Claim

Challenged claim 1 of the '391 patent recites:

1. A method of connecting two semiconductor components comprising the steps of

providing in a first main surface of a first semiconductor substrate first component structures including first contact areas;

forming in said first semiconductor substrate via holes filled with electrically conductive material and electrically insulated from said first semiconductor substrate, said via holes extending down to a second main surface of the first semiconductor substrate and being connected in an electrically conductive manner to said first contact areas via an electrically conductive connection material;

forming on the second main surface of the first semiconductor substrate first lands which are connected in an electrically conductive manner to the first contact areas via the electrically conductive material in the via holes;

providing a second semiconductor substrate having second component structures including second contact areas;

forming second lands which are connected in an electrically conductive manner to the second contact areas;

connecting the first and the second semiconductor substrate in such a way that an electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands.

E. Evidence

Petitioner relies on the following prior art:

U.S. Patent No. 6,002,177, issued Dec. 14, 1999 (Ex. 1007, "Gaynes");

U.S. Patent No. 5,424,245, issued Jun. 13, 1995 (Ex. 1008, "Gurtler");

U.S. Patent No. 5,270,261, issued Dec. 14, 1993 (Ex. 1009, "Bertin");

EP 0559366 B1, published Sept. 8, 1993 (Ex. 1010,

“EP366”).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–4, 6–8, and 11–13 of the ’391 patent are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–4, 6, 8, 12, 13	103(a)	Gaynes
1–4, 6, 8, 12, 13	103(a)	Gaynes, Gurtler
7	103(a)	Gaynes, Bertin
7	103(a)	Gaynes, Gurtler, Bertin
11	103(a)	Gaynes, EP366
11	103(a)	Gaynes, Gurtler, EP366

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of obviousness or nonobviousness, i.e., secondary considerations.¹ See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Furthermore, Petitioner does not satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art at the time of invention would “possess a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the

¹The parties do not provide any objective evidence of nonobviousness.

equivalent; and at least three years of experience in design and manufacture of advanced packaging and interconnection techniques for semiconductors.” Pet. 19–20 (citing Ex. 1003 ¶ 37). Patent Owner does not dispute Petitioner’s proposed definition. *See generally* PO Resp. Based on the record presented, including our review of the ’391 patent and the types of problems and solutions described in the ’391 patent and cited prior art, we agree with Petitioner’s proposed definition of the level of ordinary skill in the art and apply it for purposes of this Decision. *See, e.g.*, Ex. 1001, 1:29–3:55 (describing in the “Background of Invention” section of the ’391 patent various methods of producing a three-dimensional integrated circuit by stacking individual integrated circuits.).

C. Claim Interpretation

We interpret the challenged claims

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). “In determining the meaning of [a] disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006). Claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to

this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner and Patent Owner dispute the interpretation of two claim terms. Pet. 15–19; PO Resp. 10–14. The Texas district court provided constructions for the disputed terms, which were affirmed by the Federal Circuit. *See* Ex. 1052; Ex. 1058.

1. “An Electrically Conductive as well as a Mechanically Stable Connection Between the Two Substrates Is Established Exclusively via the First and the Second Lands”

Petitioner argues that “an electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands” in claim 1 should be given its plain meaning. Pet. 17–19. Petitioner contends that the specification’s disclosure that, because of the electrically conductive and mechanical stable connection, “it is not necessary to apply any separate layer . . . for mechanically connecting the upper and lower substrate,” confirms that the claims use the plain meaning. *Id.* at 17–18.

Patent Owner contends that this term should mean that the electrically conductive and mechanically stable connection is “via the appropriate connection of the first and second lands.” PO Resp. 12–13 (citing Ex. 2001 ¶¶ 44–47). According to Patent Owner, the connection between the lands “must be created appropriately to provide a ‘mechanically stable’ connection.” *Id.* at 13. Patent Owner contends that this construction captures both the “electrically conductive” and “mechanically stable” properties recited in the claim. *Id.* at 13–14. Patent Owner contends that

“the appropriate connection” is supported by the specification’s disclosure of a suitable bonding method. *Id.* at 12; PO Sur-Reply 4–6. Patent Owner contends that “created” is supported by the specification’s disclosure of forming a eutectic alloy. PO Resp. 13.

We do not agree with Patent Owner, that construction of this term means the connection is created appropriately using a suitable bonding method to form a eutectic alloy. Although the specification discloses such embodiments, we do not read these embodiments into the claims. The Federal Circuit has held that “it is improper to read limitations from a preferred embodiment described in the specification – even if it is the only embodiment – into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.” *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1327 (Fed. Cir. 2012); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) (“[C]laims may embrace different subject matter than is illustrated in the specific embodiments in the specification.”).

We agree with the district court, that the proper construction of the “connection” that is “established exclusively via the first and the second lands,” as read in light of the specification, is the “plain and ordinary meaning where plain and ordinary meaning excludes use of any other mechanical support between the two substrates.” Ex. 1052; *see* Ex. 1028; Ex. 1029 (defining “exclusive” as “excluding all but what is specified”); Ex. 1001, 5:26–32 (It “is not necessary to apply any separate layer . . . for mechanically connecting the upper and lower substrate.”). We adopt the district court’s construction, which was affirmed by the Federal Circuit. Ex. 1058.

2. “*Component Structures Including . . . Contact Areas*”

Petitioner contends that “component structures including . . . contact areas” should be given its plain meaning consistent with the specification. Pet. 15–16. The district court entered a construction of this term as the plain and ordinary meaning. Ex. 1052. We do not provide an explicit construction for “component structures including . . . contact areas” because doing so is not necessary for our analysis, nor does our final determination turn on the meaning of this term in this *inter partes* review.

3. *Other Terms*

We conclude that no other terms require express construction at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy,’ we need not construe [a particular claim limitation] . . . where the construction is not ‘material to the . . . dispute.’” (citation omitted)).

D. *Obviousness Ground based on Gaynes*

Petitioner contends that claims 1–4, 6, 8, 12, and 13 are unpatentable over Gaynes under 35 U.S.C. § 103(a), citing the declaration testimony of Wilmer Bottoms, Ph.D., as support. Pet. 20–73 (citing Ex. 1003). We are persuaded that Petitioner has shown, by a preponderance of evidence, that claims 1–4, 6, 8, 12, and 13 are unpatentable over Gaynes for the reasons explained below.

1. *Gaynes*

Gaynes discloses stacking integrated circuits, such as memory chips, by drilling holes in individual chips, filling the holes with conductive material, applying conductive structures to the surfaces of the chips, and using the conductive structures to connect the chips mechanically and

of the metals, the metals form a solution of eutectic alloy. *Id.* at 9:59–64.
The alloy solidifies over region 63, forming a connection. *Id.* at 9:64–10:1.

2. *Claim 1*

a) Petitioner's Mapping of Gaynes

The preamble of independent claim 1 recites a “method of connecting two semiconductor components.” Petitioner contends that the preamble is not limiting, but, to the extent it is limiting, Gaynes teaches the preamble in disclosing a method for enabling chip circuits to be stacked one upon the other and allowing inter-chip connectivity. Pet. 25–28; Ex. 1007, 4:21–29, Fig. 6. Patent Owner does not dispute the preamble.

Claim 1 recites “providing in a first main surface of a first semiconductor substrate first component structures including first contact areas.” Petitioner contends that Gaynes teaches a plurality of stacked chips, where each chip includes a semiconductor substrate with transistors, connections, and other electrical components formed on the chip. Pet. 29–32; Ex. 1007, 6:65–7:2, Fig. 6. Patent Owner does not dispute this limitation.

Claim 1 recites “forming in said first semiconductor substrate via holes filled with electrically conductive material and electrically insulated from said first semiconductor substrate.” Petitioner contends that Gaynes teaches “forming in said first semiconductor substrate via holes filled with electrically conductive material” in disclosing drilling holes in the substrate, and filling each hole with a conductive material such as a metal or conductive paste or both. Pet. 33–36; Ex. 1007, 7:42–46, Fig. 6. Petitioner contends that Gaynes teaches electrically insulating the via holes from the first substrate in disclosing an insulating layer such as silicon dioxide located

between the conductive material and the chip. Pet. 36–38; Ex. 1007, Figs. 15, 22.

Petitioner contends that although Figures 3, 6, and 7 of Gaynes disclose conductive material within the hole, and Figures 15 and 22 show an insulating layer coating the hole, a person of ordinary skill would have understood that the vias shown in Figures 3, 6, and 7 use an insulating layer such as the silicon dioxide layer shown in Figures 15 and 22 for electrical insulation between the conductor in the via hole and the semiconductor substrate to prevent leakage current into the substrate. Pet. 36–37.

Petitioner also contends that, should the disclosure related to Figures 3, 6, and 7 be considered a different embodiment than the disclosure related to Figures 15 and 22, a person of ordinary skill in the art would have used the silicon dioxide insulating technique of Figures 15 and 22 to insulate the holes shown in Figures 3, 6, and 7, for the benefits of avoiding short-circuits and preventing leakage. Pet. 38–39; *see Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) (“Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.”).

Claim 1 recites “said via holes extending down to a second main surface of the first semiconductor substrate and being connected in an electrically conductive manner to said first contact areas via an electrically conductive connection material.” Petitioner contends that Gaynes discloses via holes filled with electrically conducting material and extending through the substrate to a second main surface. Pet. 39–41; Ex. 1007, 8:20–50, Fig. 6. Patent Owner does not dispute this limitation.

Claim 1 recites “forming on the second main surface of the first semiconductor substrate first lands which are connected in an electrically

conductive manner to the first contact areas via the electrically conductive material in the via holes.” Petitioner contends that Gaynes discloses a process to combine a layer of a first metal such as lead placed at the vias on facing sides of chips to be connected, and a layer of a second metal such as tin, to form a eutectic alloy that connects the stacked chips in an electrically conductive manner. Pet. 42–43; Ex. 1007, 9:53–10:1, Fig. 6. Patent Owner does not dispute this limitation.

Claim 1 recites “providing a second semiconductor substrate having second component structures including second contact areas.” Petitioner contends that Gaynes discloses a plurality of chips, where each chip has a layout of circuit components, occupies a particular vertical layer within a stack, and has a metallized via through hole that connects the components of the chip to a contact area with another chip. Pet. 43–45; Ex. 1007, 6:65–7:2. Patent Owner does not dispute this limitation.

Claim 1 recites “forming second lands which are connected in an electrically conductive manner to the second contact areas.” Petitioner contends that Gaynes discloses placing layers of metals at the vias on facing sides of stacked chips, to form an electrical connection between the stacked chips. Pet. 45–47; Ex. 1007, 9:53–10:12, 10:23–50, Fig. 6. Patent Owner does not dispute this limitation.

Claim 1 recites “connecting the first and the second semiconductor substrate in such a way that an electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands.” Petitioner contends Gaynes discloses conductive structures to join chips such that chip layers may be mechanically and electrically connected in very high density stacks. Pet. 49; Ex. 1007, 9:53–10:1. Petitioner contends that the conductive structures are

joined using a transient liquid phase process that forms a eutectic alloy that is mechanically stable and electrically conductive. Pet. 50; Ex. 1007, 9:30–46. Petitioner contends that the electrically conductive and mechanically stable connection is established exclusively via the first and the second lands, because the eutectic alloy connections are sufficient on their own to provide mechanical stability, without additional non-land materials. Pet. 50–56; Ex. 1007, 4:37, 9:41; Ex. 1006, 36; Ex. 1020, 1:48–2:7.

b) Patent Owner's Arguments

Patent Owner contends that Gaynes does not teach the claimed “electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands,” because Gaynes does not teach the “appropriate connection” as disclosed in the specification of the '391 patent. PO Resp. 18. Patent Owner's contention is based on a claim construction that is incorrect, as we explained above. Patent Owner does not persuasively explain Gaynes fails to teach this limitation as properly construed.

Even under Patent Owner's incorrect construction, we find that Gaynes teaches this limitation. Patent Owner contends that the specification of the '391 patent describes a mechanically stable connection that exists through a eutectic alloy bonding of copper and tin in the appropriate proportions and formed in accordance to the process of solid-liquid interdiffusion (SLID) of the two metals. PO Resp. 18. Patent Owner contends that Gaynes discloses making a connection using a standard soldering method between lead and tin metals. PO Resp. 21, 25. According to Patent Owner, “TLP (transient liquid phase) is described in Gaynes as being a liquid phase, but this does not mean that in the end there is an intermetallic compound formed as described by the '391 Patent. TLP

simply means that one metal dissolves in another, and there is a slight change in the melting point.” *Id.* at 25; *see* PO Sur-Reply 11–15.

Petitioner contends that the method of Gaynes is not a standard soldering method, but rather, a transient liquid phase method, which is the same as the SLID method disclosed in the ’391 patent, because both methods include solid-liquid interdiffusion that forms a eutectic alloy. Reply 11–12. We agree with Petitioner. Patent Owner’s expert, Dr. Garrou, testifies that “everybody agrees that TLP . . . is synonymous with SLID.” Ex. 1055, 106:14–17. Gaynes discloses:

Referring now to FIG. 6, a TLP connection made between vias is shown The preform or deposit includes a layer of a first metal such as lead and one or both preforms or deposits include a further layer 62 or 62' of at least a second alloying metal such as tin. As the temperature is raised toward the melting point of the lower melting point metal, the metals will form a solution of eutectic alloy.

Ex. 1007, 9:53–63. Although Patent Owner is correct in contending that Gaynes discloses using lead and tin, we disagree that Gaynes uses a standard soldering method. Rather, Gaynes discloses using lead and tin in a TLP process, which is an SLID process, to form a eutectic alloy. Gaynes further discloses using other combinations of metals, including copper and tin, to form a TLP alloy system. *Id.* at 7:56–8:2. Thus, even under Patent Owner’s construction that requires an appropriate connection, Gaynes teaches the appropriate connection.

Patent Owner contends that the soldering disclosed by Gaynes does not provide for a mechanically stable bond. PO Resp. 21, 25 (citing Ex. 2001 ¶¶ 58–63); PO Sur-Reply 15. We disagree. As discussed above, Patent Owner’s expert, Dr. Garrou, testifies that TLP and SLID are synonymous. Gaynes discloses using the TLP process to form a eutectic

alloy that makes a particularly reliable connection. Ex. 1007, 9:30–10:4. Petitioner’s expert, Dr. Bottoms, testifies that “[t]he use of TLP joints as the means of providing electrical and mechanical connections between chips in a stack was well-known . . . at the time.” Ex. 1003 ¶ 89. Dr. Bottoms testifies that “TLP connections, like those in Gaynes, . . . provide[] for improved mechanical strength of the bonding.” *Id.* (citing Ex. 1020, 1:48–66, 2:3–8); *see* Ex. 1007, 4:37, 9:41. We credit the testimony of Dr. Bottoms and his supporting evidence in finding that the TLP connection of Gaynes provides for a mechanically stable bond.

Patent Owner contends that Figure 6 of Gaynes teaches the use of lead and tin preform in contact with aluminum metallization. PO Resp. 22. Patent Owner contends that one cannot solder lead to an aluminum surface as shown in Figure 6 without treatment to convert the surface to another metal which is solderable, because lead is immiscible with usual metallization metals such as aluminum. *Id.* at 23. Patent Owner concludes that what Gaynes discusses is not the type of bond required by the ’391 patent, it is merely a lead tin solder joint on a non-solderable aluminum surface. *Id.*

Petitioner contends that Patent Owner “ignores that the claimed ‘mechanically stable’ connection is ‘exclusively established’ by the lands and shifts the focus to the connection between the land and the via hole.” Reply 15 (emphasis omitted). We agree with Petitioner. The Petition does not rely on the connection between lead and aluminum shown in Figure 6 to teach the claimed “electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands.” Rather, the Petition maps first layer 61 of lead deposited on metallization 33 and/or electrically conductive aluminum in the

via holes as shown in Figure 6 of Gaynes to the claimed “forming on the second main surface of the first semiconductor substrate first lands which are connected in an electrically conductive manner to the first contact areas via the electrically conductive material in the via holes.” Pet. 41–43.

Petitioner contends that the scope of “forming on the second main surface of the first semiconductor substrate first lands which are connected in an electrically conductive manner to the first contact areas via the electrically conductive material in the via holes,” read in light of the specification, does not require using “miscible” metals for the claimed first lands and electrically conductive material in the via holes. Reply 15 (citing Ex. 1001, 5:61–65, 6:45–47; Ex. 1056, 43, 44, 48, 49). We agree with Petitioner. The specification of the ’391 patent discloses that “[e]xamples for combinations of metals which can be used for electrical and mechanical connections according to the present invention are copper and tin or gold and titanium for the respective front and back contacts.” Ex. 1001, 5:61–65. The specification discloses that “the via holes are filled with an electrically conductive material, e.g. copper or tungsten.” *Id.* at 6:45–47. We agree with Petitioner, that the specification’s disclosed via material, tungsten, is immiscible with the specification’s disclosed land materials, copper, tin, and gold. Ex. 1056, 43 (“A large number of metals exist which fail to react with tungsten, like . . . copper, . . . gold . . . [and] tin.”), 44, 48 (“Group 11 (Cu, Ag, Au). These metals do not react with tungsten, and no binary compounds are formed. The solubility of tungsten in the molten metals is negligible.” (emphasis omitted)), 49 (“Tin and lead do not react with tungsten and do not form compounds, while the solubility of tungsten in the respective metal is negligible.”). Patent Owner’s contention that lead is immiscible with aluminum, and that what Gaynes discusses is therefore not the type of bond

required by the '391 patent, is not commensurate with the scope of the claim as read in light of the specification.

Patent Owner contends that Gaynes teaches away from the irreversible bond process described in the '391 patent because it describes stopping the reaction as soon as there is melting. PO Resp. 24 (citing Ex. 1007, 10:15–22; Ex. 2001 ¶¶ 61–63); PO Sur-Reply 15–16. Patent Owner contends that following these instructions, Gaynes would only form a standard solder bond, not an electrically conductive and mechanically reliable bond as claimed. PO Resp. 24. Petitioner contends that Gaynes teaches that all available amounts of the second metal, or lower-melting point metal, is dissolved during the TLP process, and the resulting connections are particularly reliable. Reply 16 (citing Ex. 1007, 9:59–10:2). Petitioner contends that the sentence cited by Patent Owner does not teach away, but rather describes how to control process temperature and time, such that all available amounts of the second metal is dissolved. *Id.*

We agree with Petitioner. Gaynes discloses:

Referring now to FIG. 6, a TLP connection made between vias is shown [T]he metals will form a solution of eutectic alloy having a reduced melting point over a region corresponding in volume to the amount of solute metal until all available amounts of the second metal is dissolved. As further amounts of the first metal enter the solution, however, the composition of the alloy changes and the melting point of the alloy rises; causing the alloy to solidify over region 63, forming a connection. Connections formed in this way are particularly reliable since, if temperature is properly controlled, the process is self-limiting and only occurs where alloying can take place. The volume of material in the liquid phase is limited to a small volume region at the interface of the different metals and displacement of material, if it occurs at all, is extremely small.

Ex. 1007, 9:53–10:7. Gaynes further discloses:

The TLP processes and metallurgical effects are identical in each of these types of connections and the description thereof need not be repeated. It should be noted, however, that the melting point of the lower melting point metal is preferably not exceeded sufficiently or for a period of time sufficient to allow liquefaction of significantly greater amounts thereof than is necessary to form the connection. Therefore, even if metallized through holes are not filled, the preform or deposit does not deform to allow material to be displaced into the vias or through holes.

Id. at 10:12–22. Thus, Gaynes discloses forming a eutectic alloy that makes a TLP connection, and that such connections are particularly reliable if temperature is properly controlled, so that the process occurs only where alloying can take place. Gaynes discloses properly controlling temperature by not exceeding the melting point of the second metal for a time sufficient to allow greater amounts thereof than is necessary to form the connection. We agree with Petitioner, that Gaynes discloses a TLP process that forms a eutectic alloy to make particularly reliable connections, by properly controlling temperature, so that the process occurs only where alloying can take place, thus preventing excessive amounts of the second metal from liquifying and deforming the preform or deposit.

Patent Owner contends that the gold/tin connection of Figure 22 of Gaynes would not create a mechanically stable connection as claimed. PO Resp. 25; PO Sur-Reply 16–18. Petitioner contends that Dr. Garrou testifies that the '391 patent discloses gold and tin as one of the metal combinations that form a mechanically stable connection. Reply 17 (citing Ex. 1055, 79:4–80:25). Petitioner contends that Dr. Garrou testifies that gold and tin are used to form SLID bonds, and that Figure 22 of Gaynes shows an SLID bond between gold and tin. *Id.* (citing Ex. 1055, 83:10–17, 104:6–105:20,

128:7–23). Petitioner contends that Dr. Garrou testifies that when forming SLID bonds, it is beneficial to have more of the high temperature material. *Id.* (citing Ex. 2001 ¶ 56). Petitioner contends that this is exactly what Figure 22 of Gaynes shows, more of the high temperature metal, which is gold. We agree with Petitioner and Dr. Garrou. We credit Dr. Garrou’s testimony in determining that the gold and tin connection shown in Figure 22 of Gaynes creates a mechanically stable connection as claimed.

Patent Owner contends that Petitioner mischaracterizes statements made during prosecution of the corresponding foreign application. PO Resp. 25. Patent Owner contends that during the foreign prosecution, the applicant correctly noted that prior art solder methods, such as those shown by a prior art reference issued to Finnila, were distinct from the claimed mechanical connection. *Id.* at 26; *see* Ex. 1005, 98, 115, 223. Patent Owner also contends that the background section of the ’391 patent distinguishes the claimed mechanical connection over connections formed by prior art soldering methods. *Id.* at 27–28 (citing Ex. 1001, 2:22–27, 3:40–55). The prior art soldering methods discussed in the prosecution history and the background section of the ’391 patent do not disclose a connection formed by a TLP process that makes a eutectic alloy as disclosed by Gaynes. As discussed above, we find that the TLP connection of Gaynes provides for a mechanically stable bond.

Patent Owner contends that Gaynes does not teach “forming in said first semiconductor substrate via holes filled with electrically conductive material and electrically insulated from said first semiconductor substrate” as claimed. PO Resp. 29. Patent Owner argues that Gaynes does not teach an electrically insulated structure as claimed. *Id.* Patent Owner contends that the description of Figures 3–7 of Gaynes is silent on the topic of

insulation, which results in a “teaching away” from the use of including an insulation layer. *Id.* at 31–32. Patent Owner contends that the silicon dioxide layer lining the sidewall of the hole shown in Figure 22 of Gaynes is likely not used as electrical insulation, but rather to increase the adhesion of the metallization to the sidewall of the hole. *Id.* at 34; PO Sur-Reply 20. Patent Owner contends that Figure 15 of Gaynes is an alternative structure where a wire is inserted in a silicon through hole, but has “nothing to do with metallized holes through the silicon substrate or connection via the patented process.” PO Resp. 35; PO Sur-Reply 19. Patent Owner also contends that there is no motivation provided in Gaynes to apply electrical insulation as recited in the claims of the ’391 patent. PO Resp. 35.

Petitioner contends that Gaynes discloses using a silicon dioxide layer between the via and the substrate. Reply 19 (citing Ex. 1003 ¶¶ 63–70). Petitioner contends that using silicon dioxide for insulating vias was well-known. Reply 19–20 (citing Ex. 1055, 41:9–43:2). Petitioner contends that the Gaynes is silent about describing silicon dioxide as insulation because such insulation in through vias was so well-known, and that the silence of Gaynes about such a well-known process is not “teaching away.” *Id.* at 19–21 (citing *Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1364 (Fed. Cir. 2006); *Allergan, Inc. v. Apotex Inc.*, 754 F.3d 952, 964 (Fed. Cir. 2014)).

We agree with Petitioner, that Gaynes explicitly discloses silicon dioxide, that it was well-known to use silicon dioxide for insulating vias, and that a person of ordinary skill in the art would have used silicon dioxide as an insulation layer between the via metallization and the substrate as shown in Figures 15 and 22 of Gaynes. Dr. Bottoms testifies that the silicon dioxide shown in Figures 15 and 22 of Gaynes is an insulating layer located

between the conductive via material in the hole and the semiconductor substrate. Ex. 1003 ¶ 63. Dr. Bottoms testifies that it was well known that without an electrical insulator between the conductor in the via hole and the semiconductor substrate, there will be leakage current which compromises the performance of components such as transistors located within the substrate. Ex. 1003 ¶¶ 64–66. Dr. Bottoms testifies that a person of ordinary skill would have known that an insulating layer such as silicon dioxide would insulate the conductive material in the vias of Gaynes from the substrate. Ex. 1003 ¶¶ 67–69. Dr. Bottoms testifies that to apply the insulating layer, a person of ordinary skill would do no more than add a known process step of thermal oxidation, and that a person of ordinary skill would have done so to avoid short circuiting the conductive vias and to prevent leakage. Ex. 1003 ¶ 70 (citing Ex. 1016, 182–183; Ex. 1017, 248; Ex. 1011, 3:39–47, 5:43–54, 5:75–6:9; Ex. 1009, 4:4–33). Further, Dr. Garrou testifies that an undergraduate would understand that silicon dioxide is an insulator. Ex. 1055, 41:9–42:5. Dr. Garrou testifies that insulators are used to keep the device from shorting out, and that this is taught at the undergraduate level. *Id.* at 42:22–43:3.

We rely on the testimony of Dr. Bottoms and Dr. Garrou in determining that a person of ordinary skill would have used the known insulation technique of adding a layer of silicon dioxide with the known process of creating a conductive via in a semiconductor substrate for the predictable benefits of preventing leakage and avoiding short circuits. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”). “Combining two embodiments disclosed” in Gaynes by lining a hole with silicon dioxide as

shown in Figure 22, then filling the hole with conductive material as shown in Figure 6, “does not require a leap of inventiveness.” *Boston Scientific Scimed, Inc.*, 554 F.3d at 991.

c) Conclusion

For the reasons set forth by Petitioner and explained above, we are persuaded that Gaynes teaches all of the recitations of claim 1, and that a person of ordinary skill would have combined the teachings of Gaynes to achieve the method of connecting two semiconductor components recited in the claim and would have had a reasonable expectation of success in doing so. Dr. Bottom’s testimony provides sufficient evidence of reasons that a person of ordinary skill would have used the silicon dioxide teachings of Gaynes to electrically insulate the electrically conductive material in the via holes from the semiconductor substrate, and would have had a reasonable expectation of success in doing so. Petitioner has proven by a preponderance of the evidence that claim 1 would have been obvious over Gaynes.

3. Claims 2–4, 6, 8, 12, and 13

Claim 2 depends from claim 1 and recites “wherein the contact areas are heavily doped connecting areas.” Ex. 1001, 8:3–4. Petitioner contends that Gaynes teaches this limitation in disclosing that connections to vias can be formed using highly conductive doped semiconductor material as an alternative to metallization, and that a person of ordinary skill would have understood that such doped regions are “heavily doped” as claimed. Pet. 59–61 (citing Ex. 1007, 7:58–59, 14:59–63, 14:65–15:3; Ex. 1003 ¶¶ 97–99).

Claim 3 depends from claim 1 and recites “wherein the contact areas are metallization planes.” Ex. 1001, 8:5–6. Petitioner contends that Gaynes

teaches this limitation in disclosing metallization on both surfaces of the first and second substrates, and that a person of ordinary skill would have understood that metallization 33 (flanges) and patterned metallization connections 71–74 are each “metallization planes” within the meaning of the claim. Pet. 61–63 (citing Ex. 1007, 8:14–19, 10:23–50, Figs. 6, 7; Ex. 1003 ¶ 100).

Claim 4 depends from claim 3 and recites “wherein the contact areas are metallization planes arranged on the first main surface.” Ex. 1001, 8:7–9. Petitioner contends that Gaynes teaches this limitation in disclosing that its contact areas are metallization planes arranged on the top surface of the upper substrate. Pet. 64–65 (citing Ex. 1007, 10:23–29, Fig. 6; Ex. 1003 ¶¶ 49–56, 79–81, 100–101).

Claim 6 depends from claim 1 and recites “wherein the electrically conductive connection material is applied via an additional metallization sequence.” Ex. 1001, 8:14–16. Petitioner contends that Gaynes teaches this limitation in disclosing that different metals or layered combinations or alloys can be used for through hole deposit 32 and surface deposit 33, and that a person of ordinary skill would understand that when different metals or layered combinations are used, a separate metallization sequence is required. Pet. 66–67 (citing Ex. 1007, 7:44–49, 8:31–33, Figs. 3, 6; Ex. 1003 ¶¶ 71–74, 102–104).

Claim 8 depends from claim 1 and recites “wherein the first and the second semiconductor substrate are first subjected to identical processing steps and are then joined in a mirror-inverted mode of arrangement.” Ex. 1001, 8:23–26. Petitioner contends that Gaynes teaches this limitation in disclosing that each of its stacked chips are subjected to identical processing steps, and “that the vertical interconnection points on a chip

surface will be a mirror image of corresponding vertical interconnection points on the adjoining chip surface.” Pet. 67–70 (emphasis omitted) (citing Ex. 1007, 6:27–29, 6:65–7:10, 9:54–69, Fig. 6; Ex. 1003 ¶¶ 105–108).

Claim 12 depends from claim 1 and recites “wherein an electrically conductive connection is established by placing the second main surface of the first semiconductor substrate onto the surface of the second semiconductor substrate in an aligned mode of arrangement, with a simultaneous increase in temperature and application of force.” Ex. 1001, 8:23–26. Petitioner contends that Gaynes teaches “placing the second main surface of the first semiconductor substrate onto the surface of the second semiconductor substrate in an aligned mode” in disclosing “that the vertical interconnection points on a chip surface will be a mirror image of corresponding vertical interconnection points on the adjoining chip surface.” Pet. 70–71 (emphasis omitted) (citing Ex. 1007, 7:2–10, Fig. 6; Ex. 1003 ¶¶ 106–111). Petitioner contends that Gaynes teaches “an electrically conductive connection is established . . . with a simultaneous increase in temperature and application of force” in disclosing a TLP technique performed by depositing a layer of a first metal such as lead, a second alloying metal such as tin, and raising the temperature toward the melting point of the lower melting point metal to form a solution of eutectic alloy, and that a person of ordinary skill would have known that forming a TLP connection requires both a simultaneous increase in temperature and application of force. Pet. 72–73 (citing Ex. 1007, 4:31–36, 8:37–38, 9:54–62; Ex. 1020, 1:46–57, 2:23–27; Ex. 1003 ¶¶ 110–112).

The preamble of independent claim 13 recites a “method of connecting a plurality of semiconductor components, wherein a method of connecting two semiconductor components is repeated iteratively.”

Ex. 1001, 8:48–50. Petitioner contends that the preamble is not limiting, but, to the extent it is limiting, Gaynes teaches the preamble in disclosing a method for enabling chip circuits to be stacked one upon the other and allowing inter-chip connectivity. Pet. 25–28; Ex. 1007, 4:21–29, Fig. 6. Petitioner contends that Gaynes teaches that a third substrate is similarly connected to the combined structure as illustrated in Figure 7, such that the connecting “is repeated iteratively.” Pet. 28 (citing Ex. 1007, Fig. 7; Ex. 1003 ¶¶ 45–48).

Claim 13 recites “providing in a first main surface of a first semiconductor substrate first component structures including first contact areas.” Ex. 1001, 8:54–56. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 29–32.

Claim 13 recites “forming in said first semiconductor substrate via holes filled with electrically conductive material and electrically insulated from said first semiconductor substrate.” Ex. 1001, 8:57–59. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 32–39.

Claim 13 recites “said via holes extending down to a second main surface of the first semiconductor substrate and being connected in an electrically conductive manner to said first contact areas via an electrically conductive connection material.” Ex. 1001, 8:61–65. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 39–41.

Claim 13 recites “forming on the second main surface of the first semiconductor substrate first lands which are connected in an electrically conductive manner to the first contact areas via the electrically conductive

material in the via holes.” Ex. 1001, 8:66–9:2. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 41–43.

Claim 13 recites “providing a second semiconductor substrate having second component structures including second contact areas.” Ex. 1001, 9:3–5. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 43–45.

Claim 13 recites “forming second lands which are connected in an electrically conductive manner to the second contact areas.” Ex. 1001, 9:6–7. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 45–47.

Claim 13 recites “connecting the first and the second semiconductor substrate in such a way that an electrically conductive as well as a mechanically stable connection between the two substrates is established exclusively via the first and the second lands.” Ex. 1001, 9:9–10:3. Petitioner contends that Gaynes teaches this limitation for the reasons given in Petitioner’s analysis of claim 1. Pet. 47–56.

Claim 13 recites “wherein the respective n th semiconductor component plays the part of the first semiconductor component, and the stack of $(n-1)$ combined semiconductor components plays the part of the second semiconductor component.” Ex. 1001, 10:4–8. Petitioner contends that Gaynes teaches this limitation in disclosing that chip 30A shown in Figure 7 includes an n th semiconductor component that can be added on top of previously stacked chips 30B and 30C, with their stack of $(n-1)$ semiconductor components. Pet. 56–58 (citing Ex. 1007, 6:25–28, 6:65–7:7, 10:8–12, Fig. 7; Ex. 1003 ¶¶ 93–95).

Patent Owner does not argue separately claims 2–4, 6, 8, 12, and 13,

but instead relies on arguments presented for claim 1, with which we disagree as discussed in our analysis of claim 1. Petitioner's analysis for claims 2–4, 6, 8, 12, and 13, supported by the testimony of Dr. Bottoms, which we credit, is persuasive that claims 2–4, 6, 8, 12, and 13 would have been obvious over Gaynes. Based on the complete record, we determine that Petitioner has proven by a preponderance of the evidence that claims 2–4, 6, 8, 12, and 13 are unpatentable as obvious over Gaynes.

E. Obviousness Ground Based on Gaynes and Gurtler

Petitioner contends that claims 1–4, 6, 8, 12, and 13 are unpatentable over Gaynes and Gurtler under 35 U.S.C. § 103(a), citing the declaration testimony of Wilmer Bottoms, Ph.D., as support. Pet. 73–76 (citing Ex. 1003). We are persuaded that Petitioner has shown, by a preponderance of evidence, that claims 1–4, 6, 8, 12, and 13 are unpatentable over Gaynes and Gurtler for the reasons explained below.

1. Gurtler

Gurtler discloses a method of forming vias through a two-sided substrate. Ex. 1008, code (54). Active circuit elements of an integrated circuit substrate are interconnected with through-substrate vias. *Id.* at code (57). The vias are formed from a plurality of holes through the substrate. *Id.* A dielectric layer is deposited through the holes, and a conductive layer is deposited through the holes to form the vias. *Id.* The dielectric layer leaves the vias isolated from the substrate. *Id.*; *see id.* at 3:14–17. The substrate is joined to a second substrate having through-substrate vias, and the active circuit elements are interconnected by the vias. *Id.* The dielectric layer is formed using thermal oxidation of the silicon. *Id.* at 4:26–32, 6:8–13, 6:64–66.

2. Claims 1–4, 6, 8, 12, and 13

Petitioner relies on the combination of Gaynes and Gurtler to teach “forming in said first semiconductor substrate via holes filled with electrically conductive material and electrically insulated from said first semiconductor substrate,” as recited in independent claims 1 and 13, and relies on Gaynes to teach the remaining recitations of claims 1–4, 6, 8, 12, and 13. Pet. 73–76. In particular, Petitioner relies on Gurtler to teach that a dielectric layer, such as the layer of silicon dioxide shown in Figures 15 and 22 of Gaynes, electrically isolates the conducting vias and the substrate, and can be formed using thermal oxidation or low-pressure CVD processes of Gurtler. Pet. 74–75. Petitioner contends that a person of ordinary skill would have applied the insulating layer of Gurtler to the conductive vias of Gaynes for the benefit of preventing short circuits. Pet. 76.

Patent Owner contends that there is no motivation to combine Gaynes and Gurtler for the purpose of adding electrical insulation within the connection method of Gaynes. PO Resp. 37–38. Patent Owner contends that Gaynes does not disclose insulation, therefore, a person of ordinary skill would not look to Gurtler to solve a problem that Gaynes deliberately chooses to create. *Id.* Patent Owner also presents arguments similar to those presented for ground 1, namely, that the prior art does not teach both an electrically conductive and mechanically stable connection, with which we disagree as discussed above.

Petitioner contends that the Petition, supported by Dr. Bottoms, provides a reason to combine, namely, that the insulating silicon dioxide layer in Figures 15 and 22 of Gaynes can be formed using well-known processes, such as the thermal oxidation and low-pressure CVD processes of Gurtler, for which a skilled artisan would have a reasonable expectation of

success. Reply 22 (citing Pet. 75; Ex. 1003 ¶ 114; Ex. 1007, 4:1–6; Ex. 1008, 1:23–26). Petitioner contends that applying the insulating layer in Gurtler to the metallized vias in Gaynes yields the benefit of preventing the well-known problem of short circuits between the conductive vias and semiconductor substrate, to obtain an operable device. Reply 22 (citing Pet. 76).

We agree with Petitioner and Dr. Bottoms, that adding the known insulation technique of Gurtler to the known process of creating a conductive via in a semiconductor substrate as taught by Gaynes is the combination of familiar elements according to known methods that yields the predictable result of an electrically isolated via. *See KSR Int’l Co.*, 550 U.S. at 416. We agree with Petitioner and Dr. Bottoms, that a person of ordinary skill in the art would have combined the known insulation technique of Gurtler with the known process of creating a conductive via as taught by Gaynes for the benefit of preventing short circuits.

For the reasons set forth by Petitioner and explained above, we are persuaded that the combination of Gaynes and Gurtler teaches all of the limitations of claim 1, and that a person of ordinary skill would have combined the insulation teachings of Gurtler to the method of connecting two semiconductor components as taught by Gaynes to produce the claimed invention. Dr. Bottom’s testimony provides sufficient evidence of reasons that a person of ordinary skill would have used the silicon dioxide teachings of Gurtler to electrically insulate the electrically conductive material in the via holes of Gaynes from the semiconductor substrate, and would have had a reasonable expectation of success in doing so. Petitioner has proven by a preponderance of the evidence that claim 1 would have been obvious over Gaynes and Gurtler. Patent Owner does not argue separately claims 2–4, 6,

8, 12, and 13, but instead relies on arguments presented for claim 1, with which we disagree. Petitioner's analysis and evidence for claims 2–4, 6, 8, 12, and 13, supported by the testimony of Dr. Bottoms, which we credit, establishes by a preponderance of the evidence that claims 2–4, 6, 8, 12, and 13 would have been obvious over Gaynes and Gurtler.

F. Obviousness Grounds based on Gaynes and Bertin or Gaynes, Gertler, and Bertin

Petitioner contends that claim 7 is unpatentable over Gaynes and Bertin, and also over Gaynes, Gurtler, and Bertin under 35 U.S.C. § 103(a), citing the declaration testimony of Wilmer Bottoms, Ph.D., as support. Pet. 77–83 (citing Ex. 1003). We are persuaded that Petitioner has shown, by a preponderance of evidence, that claim 7 is unpatentable over Gaynes and Bertin, and also over Gaynes, Gurtler, and Bertin for the reasons explained below.

1. Bertin

Bertin discloses a method of fabricating a three-dimensional multichip package having a densely stacked array of semiconductor chips interconnected by metallized trenches. Ex. 1009, code (57). The method includes affixing an integrated circuit to a carrier to expose a surface of its substrate, and thinning the substrate until exposing the metallized trenches. *Id.* Bertin discloses that the method eliminates most excess silicon in the substrate and produces a significantly denser electronic package than that of previous stacking techniques. *Id.* at 38–46.

2. Claim 7

Petitioner relies on Gaynes alone (as explained in ground 1) or Gaynes and Gurtler (as explained in ground 2) to teach all recitations of claim 1. Pet. 20–56, 73–76. Claim 7 depends from claim 1 and recites

“after the formation of the via holes, the first main surface of the first semiconductor substrate is connected to an auxiliary substrate and is then thinned from the side of the first semiconductor substrate located opposite said first main surface.” Petitioner contends that Bertin teaches this limitation in disclosing forming trenches corresponding to via holes in a substrate, filling the trenches with metal, flipping the substrate, bonding the integrated circuit to a carrier, and thinning the substrate until exposing the trenches. Pet. 77–81. Petitioner contends that a person of ordinary skill would have used Bertin’s method of thinning in the process of making chip stacks taught by Gaynes for the benefit of improving density. Pet. 82.

Patent Owner contends that the combination of Gaynes, Gurtler, and Bertin does not teach a connection type that provides both an electrically conductive and a mechanically stable connection between the first and second lands. PO Resp. 38–39. We disagree with Patent Owner for the reasons given in our analysis of ground 1 above. Petitioner has proven by a preponderance of the evidence that claim 7 would have been obvious over Gaynes and Bertin, and also over Gaynes, Gurtler, and Bertin.

G. Obviousness Grounds based on Gaynes and EP366 or Gaynes, Gurtler, and EP366

Petitioner contends that claim 11 unpatentable over Gaynes and EP366, and also over Gaynes, EP366, and Gurtler under 35 U.S.C. § 103(a), citing the declaration testimony of Wilmer Bottoms, Ph.D., as support. Pet. 83–87 (citing Ex. 1003). We are persuaded that Petitioner has shown, by a preponderance of evidence, that claim 11 is unpatentable over Gaynes and EP366, and also over Gaynes, Gurtler, and EP366 for the reasons explained below.

1. EP366

EP366 discloses method for making a stacked three-dimensional multiple chip semiconductor device. Ex. 1010, code (54). EP366 discloses that dummy solder bumps can be used for mechanical support of the lower chip carrier without affecting any of the electrical characteristics of the stacked three-dimensional chip. *Id.* at 7:27–32.

2. Claim 11

Petitioner relies on Gaynes alone (as explained in ground 1) or Gaynes and Gurtler (as explained in ground 2) to teach all recitations of claim 1. Pet. 20–56, 73–76. Claim 11 depends from claim 1 and recites “not all the first and second lands are connected in an electrically conductive manner to respective ones of the first and second contact areas.” Petitioner contends EP366 teaches dummy solder bumps used for mechanical support without affecting electrical characteristics of the chip, and that a person of ordinary skill in the art would have included such dummy bumps in the device of Gaynes for the benefits of preventing warping due to thermal expansion and improving heat dissipation. Pet. 83–86.

Patent Owner contends that the combination of Gaynes, Gurtler, and EP366 does not teach a connection type that provides both an electrically conductive and a mechanically stable connection between the first and second lands. PO Resp. 40. We disagree with Patent Owner for the reasons given in our analysis of ground 1 above. Petitioner has proven by a preponderance of the evidence that claim 11 would have been obvious over Gaynes and EP366, and also over Gaynes, Gurtler, and EP366.

III. CONCLUSION

As summarized in the table below, the Petition and supporting evidence has shown by a preponderance of the evidence that claims 1–4, 6–8, and 11–13 of the '391 patent are unpatentable.²

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–4, 6, 8, 12, 13	103	Gaynes	1–4, 6, 8, 12, 13	
1–4, 6, 8, 12, 13	103	Gaynes, Gurtler	1–4, 6, 8, 12, 13	
7	103	Gaynes, Bertin	7	
7	103	Gaynes, Gurtler, Bertin	7	
11	103	Gaynes, EP366	11	
11	103	Gaynes, Gurtler, EP366	11	
Overall Outcome			1–4, 6–8, 11–13	

² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

It is hereby:

ORDERED that claims 1–4, 6–8, and 11–13 of the '391 patent are unpatentable; and

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01669
Patent 6,548,391 B1

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