

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

FLASH-CONTROL, LLC,
Patent Owner.

IPR2020-01709
Patent 9,257,184 B2

Before JON. M. JURGOVAN, KARA L. SZPONDOWSKI, and
JULIA HEANEY, *Administrative Patent Judges*.

SZPONDOWSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We instituted an *inter partes* review of claims 1–6 and 8–16 of U.S. Patent No. 9,257,184 B2 (Ex. 1001, “the ’184 patent”), in response to a Petition (Paper 1, “Pet.”) filed by Micron Technology, Inc. (“Petitioner”). Paper 8 (“Dec.”). During the trial, Flash-Control, LLC (“Patent Owner”) filed a Response to the Petition (Paper 12, “PO Resp.”), Petitioner filed a Reply (Paper 14, “Reply”), and Patent Owner filed a Sur-reply (Paper 15, “Sur-reply”).

An oral hearing was held on February 8, 2022, and a copy of the transcript was entered into the record. Paper 25 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the complete record, Petitioner has shown, by a preponderance of the evidence, that claims 1–6 and 8–16 of the ’184 patent are unpatentable.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies Micron Technology, Inc. as the sole real party in interest. Pet. 3. Patent Owner identifies Flash-Control, LLC as the sole real party in interest. Paper 3, 2.

B. *Related Matters*

The parties identify the following litigation as related matters:

Flash-Control, LLC v. Micron Technology, Inc., Case No. 6:20-cv-00361 (W.D. Tex.) (asserting the ’814 patent, U.S. Patent No. 9,792,219 (“the ’219 patent”), U.S. Patent No. 8,531,880 (“the ’880 patent”), and U.S. Patent No. 8,817,537 (“the ’537 patent”));

Flash-Control, LLC v. Intel Corp., Case No. 6:20-cv-00360 (W.D. Tex.) (asserting the '184 patent and the '219 patent);

Flash-Control, LLC v. Intel Corp., Case No. 1:19-cv-01107 (W.D. Tex.) (asserting the '880 patent and the '537 patent);

Si-Flash Drives, LLC v. Kingston Tech. Co., Inc., Case No. 8:16-cv-02004 (C.D. Cal.) (asserting U.S. Patent No. 7,855,916 (“the '916 patent”) and U.S. Patent No. 8,194,452 (“the '452 patent”)); and

Si-Flash Drives, LLC v. Adata Tech. (U.S.A.) Co., Ltd., Case No. 8:16-cv-02005 (C.D. Cal.) (asserting the '916 patent and the '452 patent).
Pet. 4; Paper 3, 2.

The parties also identify the following related *inter partes* review proceedings:

Micron Technology, Inc. v. Flash-Control, LLC, IPR2020-01710, which was filed concurrently and challenges the '219 patent;

Adata Tech. (USA) Co., Ltd. et al. v. Si-Flash Drives, LLC et al., IPR2018-00194 (PTAB), challenging the '452 patent; and

Adata Tech. (USA) Co., Ltd. et al. v. Si-Flash Drives, LLC et al., IPR2018-00193 (PTAB), challenging the '916 patent. Pet. 4–5; Paper 3, 2.

C. The '184 Patent (Ex. 1001)

The '184 patent is titled “Nonvolatile Memory Systems with Embedded Fast Read and Write Memories” and generally describes a “nonvolatile memory system . . . with novel architecture coupling nonvolatile storage memory with random access volatile memory” with “[n]ew commands . . . to enhance the read and write performance of the

memory system.” Ex. 1001, codes (54), (57).¹ The ’184 patent explains that “the ‘page buffered architecture’ of today’s NAND flash memory does not lend itself to true, fast, read, and write memory access,” and is “slow compared to volatile memory systems built with SRAMS and DRAMs.” *Id.* at 1:44–45, 1:54–56.

Accordingly, the ’184 patent “focuses on ways to modify the already existing ‘buffers’ in an optimal manner to enhance the random access performance of nonvolatile IC, subsystem, and system.” *Id.* at 1:59–61. The ’184 patent describes a preferred embodiment where the volatile random access memory provides “independent accessible access (read, write etc) at a fine grain level of a bit, or byte.” *Id.* at 1:62–66. “This invention provides every page of each NVM block as an independently accessible random access memory to perform load/store operations, as well as a coupled memory to the assigned NVM block.” *Id.* at 2:20–24. “[The p]age for each block is typically 1 to 2 kilobytes and each bit is independently addressable in a random manner, as well as accessed in a random manner.” *Id.* at 2:26–28. The preferred embodiment includes “New commands with these inventions: Read page as SRAM/RAM, Write Page as SRAM/RAM, Read/Modify/W Write page as SRAM/RAM, Read byte out of a page, etc; Write byte out of a page etc.” *Id.* at 4:24–28.

Figure 9, reproduced below, “shows how the invention of this patent distinguishes itself from today’s nonvolatile memory.” *Id.* at 2:57–58.

¹ Throughout this Decision, we may refer to nonvolatile memory as “NVM,” and volatile memory as “VM.”

NONVOLATILE MEMORY SYSTEMS

- THERE MAY BE OTHER WAYS TO PREVENT 'WRITING INTO FLASH' - YET, LOAD THE 'PAGE' FOR SUBSEQUENT DATA ACCESSES OF ALL KINDS, WITHOUT DISTURBING THE PAGE, TO WHICH THE FLASH BLOCK/SECTOR/BANK BELONGS

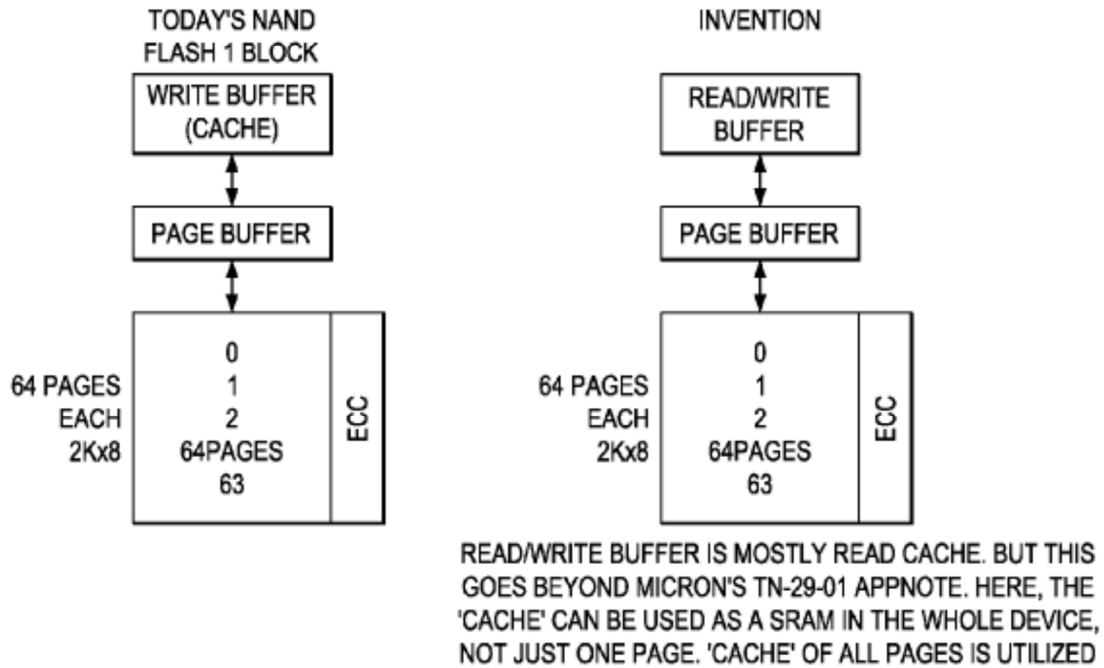


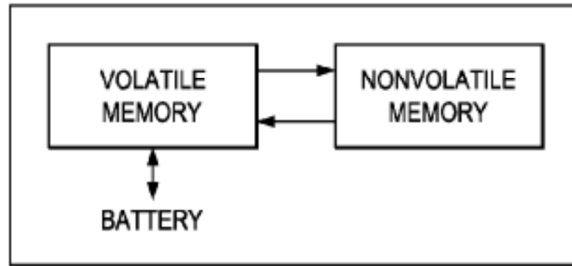
FIG. 9

Figure 9 depicts “Today’s NAND Flash 1 Block,” which includes Write Buffer (Cache), and Page Buffer 64 pages each 2Kx8. Figure 9 also depicts the invention, which includes Read/Write Buffer, and Page Buffer, and 64 pages each 2Kx8. Figure 9 describes that “Read/Write Buffer is mostly read cache . . . [and] the ‘cache’ can be used as SRAM in the whole device, not just one page. ‘Cache’ of all pages is utilized.”

Figure 12, reproduced below, shows a high level architecture of the nonvolatile memory system of the invention.

NONVOLATILE MEMORY SYSTEMS

NONVOLATILE MEMORY MODULE WITH VOLATILE MEMORY



- VOLATILE MEMORY CAN BE DRAM, SRAM OR COMBINATION
- NONVOLATILE MEMORY CAN BE ANY KIND OF FLASH, MAGRAM, FeRAM, CNT ETC.
- READ/WRITE CAN BE THROUGH VM(VOLATILE MEMORY) WHICH ACTS AS A CACHE BUFFER (BOTH DATA AND ADDRESS, COULD BE COMMAND AS WELL)

FIG. 12

Figure 12 depicts nonvolatile and volatile memory, where “volatile memory can be DRAM, SRAM or combination” and nonvolatile memory can be “any kind of flash, MagRAM, FeRAM, CNT, etc.” *Id.* at 2:65–67. Figure 12 further describes that “Read/write can be through VM (volatile memory) which acts as a cache buffer (both data and address, could be command as well).”

D. Illustrative Claims

Petitioner challenges claims 1–6 and 8–16 of the ’184 patent. Pet. 1. Claims 2–6 and 8–16 depend from claim 1. Ex. 1001, 5:22–6:30. Claim 1, reproduced below with brackets noting Petitioner’s identifiers, is illustrative of the subject matter of the challenged claims:

1. [1.PRE] A nonvolatile memory system comprising:

[1.A] a nonvolatile memory for storage of digital information in addressable locations arranged in multiple blocks for access,

[1.B] wherein reading any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location;^[2]

[1.C] a volatile random access memory for read and write operations; and

[1.D] wherein the coupled volatile random access memory and nonvolatile memory for storage are controlled by one or more controllers, the one or more controllers controlling the volatile and nonvolatile memories to:

[1.E] perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location, wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory,

[1.F] perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory,

[1.G] perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein, and

[1.H] write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read.

² Consistent with the nomenclature used by the parties, this limitation will be referred to in this Decision as “limitation 1.B,” or “the requirement limitation.”

Id. at 4:56–5:21.

E. Evidence

Petitioner relies on the following references (*see* Pet. 7).

Reference	Exhibit	Patent/Printed Publication
Lee	1007	US Patent Application Publication No. 2006/0053246 A1 to Lee, published March 9, 2006
Tsunoda	1008	US Patent Application Publication No. 2003/0028733 A1 to Tsunoda et al., published February 6, 2003
Kolokowsky	1009	US Patent No. 7,853,749 B2 to Kolokowsky, issued December 14, 2010
Li	1010	US Patent No. 7,254,059 B2 to Li et al., issued August 7, 2007
Miura	1011	US Patent Application Publication No. 2006/0041711 A1 to Miura et al., published February 23, 2006

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–6 and 8–16 are unpatentable based on the following grounds (Pet. 7–8):

Claim(s) Challenged	35 U.S.C. § ³	Reference(s)/Basis ⁴
1–3, 9–16	103	Lee

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the ’184 patent issued was filed before this date, the pre-AIA version of § 103 applies.

⁴ In each of Petitioner’s grounds, Petitioner separately references the knowledge of a person of ordinary skill in the art. When analyzing whether claims would have been obvious and whether it would have been obvious to modify prior art, it is always from the perspective of an ordinarily skilled

Claim(s) Challenged	35 U.S.C. §³	Reference(s)/Basis⁴
1–3, 5, 6, 9, 11–16	103	Tsunoda, Kolokowsky
4	103	Lee and Li
8	103	Lee and Miura
4	103	Tsunoda, Kolokowsky, Li
8	103	Tsunoda, Kolokowsky, Miura

In addition, Petitioner relies on the Declarations of John Levy, Ph.D. (Exs. 1003, 1035). Patent Owner relies on the Declarations of Dr. Nader Bagherzadeh (Exs. 2001, 2004). Deposition transcripts have been entered into the record for Dr. Levy (Ex. 2005) and Dr. Bagherzadeh (Ex. 1034).

III. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art;

artisan and one must consider knowledge generally available to one of ordinary skill in the art. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (one considers “the background knowledge possessed by a person having ordinary skill in the art”). The “knowledge of a person of ordinary skill in the art” is, therefore, always a consideration and is not a separate basis in an obviousness challenge. Therefore, we do not separately analyze the “knowledge of a person of ordinary skill in the art” and consider obviousness over the cited prior art from the perspective of the ordinarily skilled artisan.

(2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine “must be supported by a ‘reasoned explanation’”).

B. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art at the time of the invention

would have had at least a bachelor’s degree in computer engineering, electrical engineering, computer science, or a similar discipline, along with 2 years of experience in the design, operation, or control of semiconductor memory devices. A more advanced degree can substitute for work experience. This POSA would be aware of and generally knowledgeable about the structure and operation of different types of memories.

Pet. 17 (citing Ex. 1003 ¶¶ 43–47). Patent Owner does not dispute Petitioner’s characterization of a person of ordinary skill in the art. PO Resp. 9.

We find that Petitioner’s proposal is consistent with the level of ordinary skill in the art reflected by the prior art of record, and, therefore, adopt Petitioner’s proposed level of ordinary skill in the art for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b) (2020). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

“It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004). “Attending to this principle, a claim

construction analysis must begin and remain centered on the claim language itself, for that is the language the patentee has chosen to ‘particularly point[] out and distinctly claim[] the subject matter which the patentee regards as his invention.’” *Id.* at 1116 (citing *Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001)). “[A] court looks to those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean. Those sources include the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Id.* “The written description provides a context for the claims, and is appropriately resorted to ‘for the purpose of better understanding the meaning of a claim.’” *Id.* (citing *White v. Dunbar*, 119 U.S. 47, 51 (1886)).

1. “any portion of the stored retrieved digital information can be accessed from the volatile random access memory” (Claim 1, limitation 1.E)

Petitioner asserts that this limitation should be interpreted to mean “the stored retrieved digital information can be accessed at the addressable bit and/or a byte level.” Pet. 14. Petitioner argues that (1) claim 1 recites “any portion or all of the stored digital information,” which illustrates that “any portion” must be less than the entire portion; (2) during prosecution, “Applicant distinguished the prior art by arguing that its alleged invention provides granular access of the volatile memory (‘page buffer’)”; and (3) the Specification describes access at “a fine grain level of a bit, or a byte.” *Id.* at 13–15. Petitioner also provides supporting testimony from Dr. Levy. Ex. 1003 ¶¶ 91–100.

In our Institution Decision, we discerned that the issue was whether “any portion” should be construed to at least include accessibility at the bit and/or byte level. Dec. 12–13. We determined that it should. Therefore, based upon the disclosure in the Specification, we construed this limitation to include access of the stored retrieved digital information at the bit or byte level. *Id.* at 13.

Patent Owner “accepts the Board’s construction.” PO Resp. 18. Petitioner does not further address the construction of this term. *See generally* Reply. Accordingly, we maintain the same construction that we adopted in our Institution Decision.

2. “reading of **any portion** of the digital information in a given block from an associated addressable location” (Claim 1, first part of limitation 1.B)

Petitioner asserts that this limitation should be interpreted to mean when “‘any portion of the digital information in a given block,’ *i.e.*, a sector or a page, from the nonvolatile information is read and modified, it is written back to the same logical address but to a different physical address.” Pet. 16. In support, Petitioner argues that this limitation “refers to reading data in the nonvolatile memory (‘information in a given block’) at its logical flash address (‘an associated addressable location’).” *Id.* According to Petitioner, the ’184 patent supports that it was “not changing the standard page-level access to the flash memory array itself.” *Id.* (citing Ex. 1001, 1:59–2:6, 3:34–45, 3:10–11, 4:21–29). Petitioner also provides testimony from Dr. Levy, including that “the smallest accessible unit for a read or write [in non-volatile memory] is a page.” *See id.* at 16 (citing Ex. 1003 ¶¶ 101–103).

In our Institution Decision, we discerned that “any portion” should not be limited to “a sector or a page” because there was no dispute that the

smallest unit for a read or write in non-volatile memory is a page. Dec. 14. Aside from that, we determined no need to deviate from the plain and ordinary meaning of the limitation.

Neither party further addresses the “any portion” aspect to construction of this term. *See generally* PO Resp., Reply, Sur-reply. Accordingly, we maintain the same construction of “any portion” that we adopted in our Institution Decision.

3. *“reading of any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location” (Claim 1, limitation 1.B or “the requirement limitation”)*

In the Preliminary Response, Patent Owner advanced a proposed construction of limitation 1.B. Paper 7, 12–14. We declined to adopt Patent Owner’s proposed construction in our Institution Decision. Dec. 14–17.

Patent Owner asserts that it “has evaluated the Board’s comments and has revised its proposed construction” to “clarif[y] that the claim requires a read/modify/write operation involving both non-volatile and volatile memory.” PO Resp. 20–21; *see* Sur-reply 4. Patent Owner provides the following chart, comparing the claim language to its proposed construction:

Claim Language	Patent Owner’s Construction
wherein <i>reading of any portion</i> of the digital information in a given block from an associated addressable location and <i>modification thereof for storage back in the memory in the same addressable location requires</i>	wherein the system is configured to perform a read/modify/write operation that involves the consecutive steps of <i>reading any portion</i> of the digital information (i.e., the information accessible at a bit or byte level) in a given block

writing of the modified digital information into a new physical location mapped to the same associated addressable location (limitation 1.B)	from an associated addressable location of a non-volatile memory, modifying the read information in volatile memory , and writing the modified information back to the non-volatile memory into a new physical location mapped to the same associated addressable location.
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PO Resp. 21 (emphasis added by Patent Owner).

Patent Owner contends that the intrinsic record supports this construction, including the claim language and the Specification of the '184 patent. PO Resp. 22–24. Patent Owner also argues that a person of ordinary skill in the art would understand Patent Owner's read/write/modify operation as an "atomic operation," which means there is no "gap" between the three distinct steps. *Id.* at 24–26. Finally, Patent Owner argues that Dr. Levy (Petitioner's declarant) incorrectly interprets this limitation as "not involving an atomic read/modify/write operation with both non-volatile and volatile memory." *Id.* at 26; *see also id.* at 27–31.

Petitioner contends that no express construction of this limitation is necessary. Reply 5. Petitioner contends that Patent Owner is (1) attempting to rewrite limitation 1.B from reciting a single requirement into a three-step process; (2) interjecting extraneous limitations into limitation 1.B namely, a "read/modify/write operation" in which the steps of the operation occur without intervening steps ("atomic"); and (3) ignoring the claim language, specification, file history, and extrinsic evidence. Reply 1, 4.

The parties agree that this issue is dispositive. PO Resp. 1 ("The correct construction of the claims in this proceeding is dispositive"); Sur-

reply 1 (“The proper claim construction is dispositive”). At the hearing, Petitioner’s counsel stated that “[t]he references do not disclose a command called Read/Modify/Write that would read from nonvolatile memory modify write back a single command.” Tr. 7:3–5; *see also* Tr. 7:14–16 (“it is true that the prior art does not disclose something called a Read/Modify/Write operation”). Patent Owner’s counsel stated that “we didn’t make any arguments except for the claim construction argument,” and further stated that “if you do not adopt our claim construction I think the Board can review the record and, you know, make its determination based on the Institution Decision.” Tr. 44:8–10, 12–15. We address the parties’ arguments below.

We decline to adopt Patent Owner’s proposed construction, as it departs from the plain language of limitation 1.B in a manner that, in effect, impermissibly rewrites the claim. *See Nike Inc. v. Wolverine World Wide, Inc.*, 43 F.3d 644, 647 (Fed.Cir.1994) (rejecting the patentee’s proposed claim construction that would, “in effect, rewrite its patent claims to suit its needs in this litigation”); *K–2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) (“Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee.”); Reply 5, 7–8. Petitioner provides the following comparison of limitation 1.B with Patent Owner’s proposed construction, which makes the extent of the departure apparent:

wherein ***[the system is configured to perform a read/modify/write operation that involves the consecutive steps of] reading any portion of the digital information [(i.e., the information accessible at a bit or byte level)]***⁵ in a given

⁵ We construed “any portion” in limitation 1.B in Section III.C.2 above, as not limited to “a sector or a page.” We construed “any portion” in limitation 1.E in Section III.C.1 above, as including accessibility at the bit or byte

block from an associated addressable location *[of a non-volatile memory]* and ~~modification thereof for storage back in the memory in the same addressable location requires~~ *[modifying the read information in volatile memory, and]* writing of the modified digital information *[back to the non-volatile memory]* into a new physical location mapped to the same associated addressable location.

Reply 5–6 (noting that “***bolded*** indicates PO’s proposed additional language and strike-through indicates PO’s deletion of claim language”). As Petitioner points out, and we agree, Patent Owner “[c]hanges the limitation from reciting a requirement to reciting a three-step process,” “[r]ewrites the claim to recite ‘modifying the read information in volatile memory,’ even though [limitation 1.B] does not recite actually modifying the data . . . and does not relate to the VM,” and “[i]nterjects ‘a read/modify/write operation that involves the consecutive steps[,]’ . . . even though the limitation says nothing about such an operation.” See Reply 8.

Although Patent Owner contends that the claim “expressly requires the read/modify/write operation,” (PO Resp. 22 (citing Ex. 2004 ¶ 50)), limitation 1.B does not recite a “read /modify/write operation,” much less a “read/write modify operation that involves . . .[three] consecutive steps.” See PO Resp. 21 (Patent Owner’s proposed construction). Patent Owner argues that the proposed construction “does not rewrite the claim [because] the

level. Patent Owner appears to improperly rely on the construction of “any portion” from limitation 1.E, rather than the construction of “any portion” in limitation 1.B in its proposed construction of limitation 1.B. See Reply 23; Sur-reply 3 (“Patent Owner has accepted the Board’s construction which is ‘accessible at a bit/byte level’”). This provides another reason why we cannot adopt Patent Owner’s proposed construction.

language of claim 1 supports that it already includes the read/modify/write operation.” Sur-reply 5; *see also id.* at 6. But whether the scope of the claim *includes* a read/modify/write operation (*see* Sur-reply 4–5) is beside the point; Patent Owner is attempting to narrow limitation 1.B to *require* a read/modify/write operation.⁶ In other words, we disagree with Patent Owner that “[t]he scope of claim 1 is unchanged by the clarification that the steps performed in claim 1 are the steps of an atomic read/modify/write.” Sur-reply 13.

Patent Owner does not provide persuasive argument explaining why limitation 1.B *requires* a “read/modify/write operation.” *See, e.g.*, Reply 9, 12. Rather, much of Patent Owner’s arguments simply assume that it does. *See, e.g.*, PO Resp. 21 (“the proposed construction clarifies that the read/write/modify operation involves both non-volatile and volatile memory”); Sur-reply 5–7. Dr. Bagherzadeh’s testifies that “this claim requires a read/modify/write operation involving both non-volatile and volatile memory.” Ex. 2004 ¶ 31 (cited at Sur-reply 5, 8, 11). But this testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *see also Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997) (nothing requires a fact finder to credit the inadequately explained testimony of an expert). According to Patent Owner, limitation 1.B “describes the capability wherein the memory system can command the

⁶ Claim 1 uses the transitional term “comprising,” “which is well understood in patent law to mean ‘including but not limited to.’” *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009); *see* Reply 13.

performance of a ‘*read/modify/write*’ operation resulting in information being sequentially (1) *read out of nonvolatile memory so that it may be modified*, (2) *modification* thereof, and (3) *writing back* of the modified information back to nonvolatile memory.” PO Resp. 14. We note that, aside from the argued “performance of a ‘read/modify/write’ operation resulting in information being sequentially,” the foregoing description from Patent Owner aligns much more closely with the claim language of limitation 1.B than Patent Owner’s proposed construction.

The crux of Patent Owner’s argument is that the “read/modify/write operation” is an “atomic operation,” which “means that there is no ‘gap’ between the three distinct steps that are included in a read/modify/write operation that allows for intermediate or unrelated actions to occur.” See PO Resp. 24.⁷ This is reflected in Patent Owner’s proposed construction, which recites (in part) “wherein *[the system is configured to perform a read/modify/write operation that involves the consecutive steps of]*.” Patent Owner, therefore, contends that limitation 1.B recites three steps (reading, modifying, and writing) that are “performed in order and without interruption,” and provides several reasons why intermediate and unrelated actions would be excluded during an atomic operation. Sur-reply 5–7; PO Resp. 24–25 (citing Ex. 2004 ¶¶ 51–52); see *id.* at 25 (citing Ex. 2004 ¶ 53) (“a read/modify/write operation must maintain its sequential integrity without any interference from outside sources (other processors, interrupts,

⁷ Patent Owner contends that “[a]n operation acting on shared memory is ‘atomic’ if it completes in a single step. (Ex. 2004 at ¶ 55)[.] This is a term of art in this field that a POSA would have understood. (Ex. 2004 at ¶ 55).” PO Resp. 29 n. 2.

and exceptions); otherwise, during the read/modify/write operation there could be unintended consequences that would jeopardize the proper operation of the processor and the program execution.”).

On the other hand, Petitioner contends that the plain and ordinary meaning of this claim language is clear: (1) if information in the NVM at a logical address is read and modified (“wherein reading of any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location”), (2) there is a requirement (“requires”) that (3) the information is written back to the same logical address but to a different physical address in the NVM (“writing of the modified digital information into a new physical location mapped to the same associated addressable location”).

Reply 6 (citing Pet. 9–10; Ex. 1035 ¶¶ 13–16); *see also id.* at 10. To that end, Petitioner argues that the claim language does not specify or suggest that the “operations” it actually recites occur without intervening steps. Reply 13 (citing Ex. 1035 ¶¶ 21–22).

There appears to be no dispute that a read/modify/write operation (or command) requires that the read, modify, and write occur as a unitary operation with no intervening operations. *See, e.g.*, Ex. 2005, 96:19–97:12 (Dr. Levy testifying that “the general meaning of a read-modify-write or operation of one requires that the read and the modification and the write occur as the unitary operation where no other operation can occur during that – during the interval, whereas there’s no such specification here in Claim 1”); Ex. 2004 ¶ 33 (Dr. Bagherzaderh testifying that “read/modify/write refers to a memory system operation wherein the following steps occur, i.e., data is read from a specified address in memory,

the read-out data is modified, and the modified data is written back to the original address in memory . . . [e]ach of these steps is p[er]formed sequentially without interruption.”). Therefore, central to the dispute is whether it is appropriate to construe limitation 1.B as requiring such a read/modify/write operation.

We find that it is not. We find persuasive Petitioner’s arguments that limitations 1.C, 1.E, 1.F, and 1.G refer to “read operations” and “write operations,” whereas limitation 1.B does not refer to an “operation.” *See* Reply 12; *see Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007) (when “the specification . . . suggests that the patentees knew how to” use a particular term to restrict claim coverage, use of different term in the claims must have meaning). We note the difference in language used in limitation 1.H (“writ[ing] the digital information stored . . .”), as opposed to that used in limitations 1.E, 1.F, and 1.G (“perform a [read or write] operation”). Ex. 1001, 5:5–17. Similar to limitations 1.E, 1.F, and 1.G, Patent Owner’s proposed construction of limitation 1.B includes the language “the system is configured to *perform* a read/modify/write operation . . .” *See* PO Resp. 21. The language advanced by Patent Owner also changes the recited “modification,” which was passive, to an active “perform . . . modifying the read information,” similar to the language in limitations 1.E, 1.F, and 1.G.

Nor do we find that the Specification supports Patent Owner’s position. The Specification is devoid of any description of a “read/write/modify operation” as advanced by Patent Owner in its proposed construction. Patent Owner argues that “[t]he specification also discloses that allowing for the *performance of a read/modify/write operation*

involving nonvolatile memory, using coupled volatile memory, *is an important aspect of the invention,*” (PO Resp. 22, emphasis added) but Patent Owner lacks support for such an assertion. For example, we note that Dr. Bagherzadeh testifies that “[t]he ’184 patent is directed to novel systems and method coupling VM and NVM to improve performance by, *inter alia*, enhancing the random access performance of NVM systems allowing access at a more flexible and granular level than prior memory systems.” Ex. 2004 ¶ 42. This testimony is supported by the Specification, and says nothing about the “importance” of “performance of a read/modify/write operation involving nonvolatile memory using coupled volatile memory.” See Ex. 1001, Abstr., 1:59–66.

Patent Owner relies on the “new commands” described in the Abstract and the Brief Summary of the Invention. PO Resp. 23 (citing Ex. 1001, abstr., 2:10–20). The pertinent Summary section of the ’184 patent states:

The preferred embodiment ***adds new commands*** to be executed in the Command Register ***of the NVM (nonvolatile memory)***. In other embodiments, these commands can be shared between the NVM IC and memory controller. ***Prior art NVM IC's have limited commands*** like (1) read page in flash; (2) erase block in flash; (3) program page in flash, etc. ***With this invention, new additional commands are executed:*** (4) read page in the SRAM of the block only; (5) ***read new page from*** the nonvolatile memory (NVM) block; (6) ***write page into SRAM of the block, but, not program into the NVM block until such a command is additionally given.***

PO Resp. 23 (quoting Ex. 1001, 2:10–20) (emphases added by Patent Owner). According to Patent Owner, this passage supports that “[i]ncluded among these new commands are an instruction to read a new page from the nonvolatile memory (NVM) block and write (e.g., modify) the page into the

portion of volatile memory (SRAM) coupled to the nonvolatile memory (NVM block) but not program (write) this page back into the NVM block unless this additional instruction is given.” *Id.* We note that this portion of the Specification does not mention a new read/modify/write operation (or command). At most, this portion of the Specification describes three “new additional commands,” (4), (5), and (6). *See* Reply 17–18 (arguing that the “allegedly new commands” identified in the Specification refer to “singular operations that read or write to the VM,” and “not a singular read/modify/write command or operation.”); Ex. 1035 ¶¶ 27–28.

The Specification provides additional description of the new commands: “[*n*ew commands with these inventions: Read page as SRAM/RAM, Write page as SRAM/RAM, **Read/Modify/W Write** [*sic*] **page** as SRAM/RAM, Read byte out of a page, etc; Write byte out of a page etc.” Ex. 1001, 4:24–28 (cited at PO Resp. 24, emphasis added by Patent Owner). We note that this is the only place in the Specification where a “read/modify/write” command is described, and this is the full extent of the description. As Petitioner points out, this “refers to writing the data ‘as SRAM/RAM,’ not writing the data to NVM,” “which [limitation 1.B] clearly states.” Reply 19 (Ex. 1035 ¶ 31). Petitioner’s expert, Dr. Levy, testifies that “on the face of it[,] it’s clearly associated with SRAM or RAM; in other words, volatile memory.” Ex. 2005, 102:4–6; *see also* Ex. 1035 ¶ 31. Patent Owner contends this is “wrong” because (1) “the modifier ‘as SRAM/RAM’ [is used] to indicate **how** the operation will be performed, i.e., **as though** it were being performed in volatile memory”; and (2) “Dr. Levy admits that claim 1’s recited step of writing the data back to the same location in volatile memory indicates there is a modification.” PO Resp.

27–28. We are not persuaded by these arguments as they do not address the language in limitation 1.B, or explain how this disclosure supports Patent Owner’s proposed construction of limitation 1.B. *See* PO Resp. 24, 27–28. Dr. Levy’s testimony as to this disclosure is un rebutted, and, given the dearth of any further description of this command in the Specification, we find credible Dr. Levy’s testimony that “‘Read/Modify/W Write page as SRAM/RAM’ not only say[s] nothing about updating the NVM, ‘Read/Modify/W Write page as SRAM/RAM’ also says nothing about a requirement that the update be to a different physical address.” Ex. 1035 ¶ 31.

Patent Owner also relies on column 4, lines 40–43 of the Specification, which states “To write to a page or pseudo page, WRITE command and immediate PRO[]GRAM SUSPEND to invalidate writing to the NVM. The data should be in page/pseudo page.” PO Resp. 31. According to Patent Owner, because “the write command requires preventing other programs from writing to that location in NVM,” [t]his indicates that read, modification, and write occur as a unitary operation and the claim indicates a read/modify/write operation.” *Id.* The Specification does not further describe the PROGRAM SUSPEND operation. Dr. Levy provides testimony that is un rebutted, explaining why a “suspend” is different from a read/modify/write operation. *See* Ex. 1035 ¶¶ 33–34. We find Dr. Levy’s testimony persuasive as to this point.

Moreover, given the plain language of limitation 1.B, particularly in light of its disparity from the language in limitations 1.E, 1.F, and 1.G (reciting “perform a [read/write] operation”), we do not find persuasive Patent Owner’s argument that “a person of ordinary skill in the art would,

therefore, only have understood that the claimed steps in limitation 1.B are not atomic if there was a clear statement in the record indicating otherwise.” PO Resp. 25–26 (citing Ex. 2004 ¶ 54). Patent Owner stresses that “the ’184 patent characterize[s] a read/modify/write command in nonvolatile memory coupled with volatile memory as ‘new,’”⁸ and argues that Dr. Levy “admitted that he had never before seen a read/modify/write command performed using nonvolatile memory,” and that in “his experience and understanding, [a read/modify/write operation] *only occurs in volatile memory.*” PO Resp. 26–27 (referring to Ex. 2005, 98:15–18, 101:8–15). But this argument only undermines Patent Owner’s argument that a person of ordinary skill in the art would require a clear statement in the record that limitation 1.B does not require a read/modify/write operation.

Patent Owner equates limitation 1.B with limitations 1.D–1.H. *See* Sur-reply 6–7 (“[t]he steps of the claim are intended to be performed in order and without interruption as they describe both by the ‘wherein clause’ under NVM, (Ex. 1001 at 4:58–65 [limitation 1.B]), and the wherein clause found at (Ex. 1001 at 5:1–22 [limitations 1.D–1.H]); Sur-reply 2–3 (stating that limitation 1.B “describes the interaction between the NVM and the VM” and “[t]his interaction is later described, in part, and in more detail, by [limitation 1.F]”); *see also* Tr. 34:16–35:7. At the hearing, referring to limitation 1.G, Patent Owner’s counsel stated “[t]hat is the modification that they refer to and that’s occurring in the volatile memory.” Tr. 35:2–3. Patent Owner’s counsel further stated “I think that you can view limitations [1.E] through [1.H] as providing an additional level of detail about how the

⁸ We disagree with this argument for reasons stated above.

systems are configured to operate and I think that it does match up with limitation [1.B].” Tr. 37:23–38:1. Petitioner, on the other hand, contends that limitations 1.E to 1.H do not correspond to a read/modify/write operation. Reply 14. For example, Petitioner contends that limitation 1.F “involves reading data out of VM . . . [which] is not part of a read/modify/write operation.” *Id.* at 15.

Patent Owner’s position on this point also undermines its argument that the read/modify/write operation is a three-step process, in that limitations 1.E–1H describe four steps. *See, e.g.*, Sur-reply 5–7, 9. Patent Owner argues that “there is nothing improper about including sub-steps at a more granular level,” but does not further persuasively address the conflict in its own position that limitation 1.B recites an “atomic” three-step operation, that bars any intermediate steps, while limitations 1.E–1.H recite four steps. Sur-reply 5. Nor does Patent Owner delineate a “sub-step at a more granular level” versus a “step.”

In conclusion, and for the foregoing reasons, Patent Owner’s proposed construction departs too extensively from the language of limitation 1.B, and we decline to adopt it. In particular, we find that limitation 1.B does not require a read/modify/write operation that involves the consecutive steps. Aside from the construction of “any portion,” discussed above in III.C.1, we agree with Petitioner that no express construction of limitation 1.B is necessary for purposes of this Decision.

4. “*on the fly*” (*Claim 15*)

Petitioner contends that this term should be construed to mean “doing a task or process as needed without suspending or disturbing normal operations.” Pet. 16 (citing Ex. 1012). In support of its argument, Petitioner

cites to the Microsoft Computer Dictionary (5th ed. 2002), and argues that a previous panel of the Board adopted this construction for this term in a related IPR. *Id.* at 16–17 (citing Ex. 1012; Ex. 1013, 5–9). Patent Owner did not address this term in its Preliminary Response. *See generally* Paper 7.

In our Institution Decision, we adopted Petitioner’s proposed construction of “on the fly.” Dec. 17. The parties have not further addressed the construction of this term. *See generally* PO Resp., Reply, Sur-reply. Accordingly, we maintain the same construction that we adopted in our Institution Decision.

*D. Ground 1: Obviousness Based on Lee*⁹

Petitioner contends claims 1–3 and 9–16 would have been obvious over Lee. Pet. 22–42. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–3 and 9–16 are unpatentable over Lee.

1. Lee (Ex. 1007)

Lee is titled “Systems and Methods for Providing Nonvolatile Memory Management in Wireless Phones” and relates “to methods and systems for accessing and managing nonvolatile memory, such as in a wireless phone.” Ex. 1007, code (54), ¶ 4. Lee describes, *inter alia*, “a memory system containing a high-density Flash memory, RAM memory, and a control circuit that, under the control of one or multiple processors, provides a DMA [direct access memory] function to transfer data among

⁹ As set forth in Section III.C.3, the parties agree that claim construction of limitation 1.B is dispositive of this proceeding. However, in the interest of completeness and providing a full record, we address Petitioner’s grounds.

memories, displays (e.g., LCD screens), and/or an externally inserted memory card.” *Id.* ¶ 12.

Figure 2, reproduced below, is a block diagram of a wireless phone including a memory system. *Id.* ¶¶ 24, 77.

FIG. 2

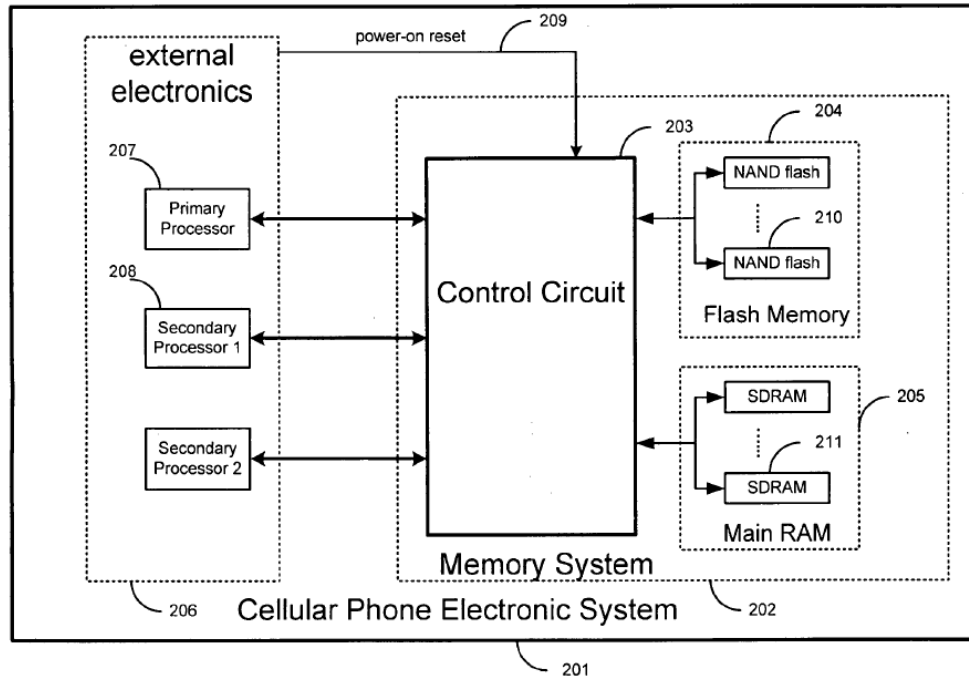


Figure 2 depicts non-volatile Flash Memory 204, volatile random access memory Main RAM 205, and Control Circuit 203. *Id.* ¶ 77. Flash Memory 204 and Main Ram 205 are connected to Control Circuit 203, and Control Circuit 203 “provides control signals to interface with and operate the Flash Memory (204) as well as control signals to interface with and operate the Main RAM (205).” *Id.* ¶ 78. A processor interface configures and activates Control Circuit 203 to perform operations, such as “performing bidirectional DMA transfer between the Flash Memory (204) and the Main RAM (205).” *Id.*

Figure 3, reproduced below, is a block diagram of a first embodiment of a memory system control circuit. *Id.* ¶¶ 25, 83.

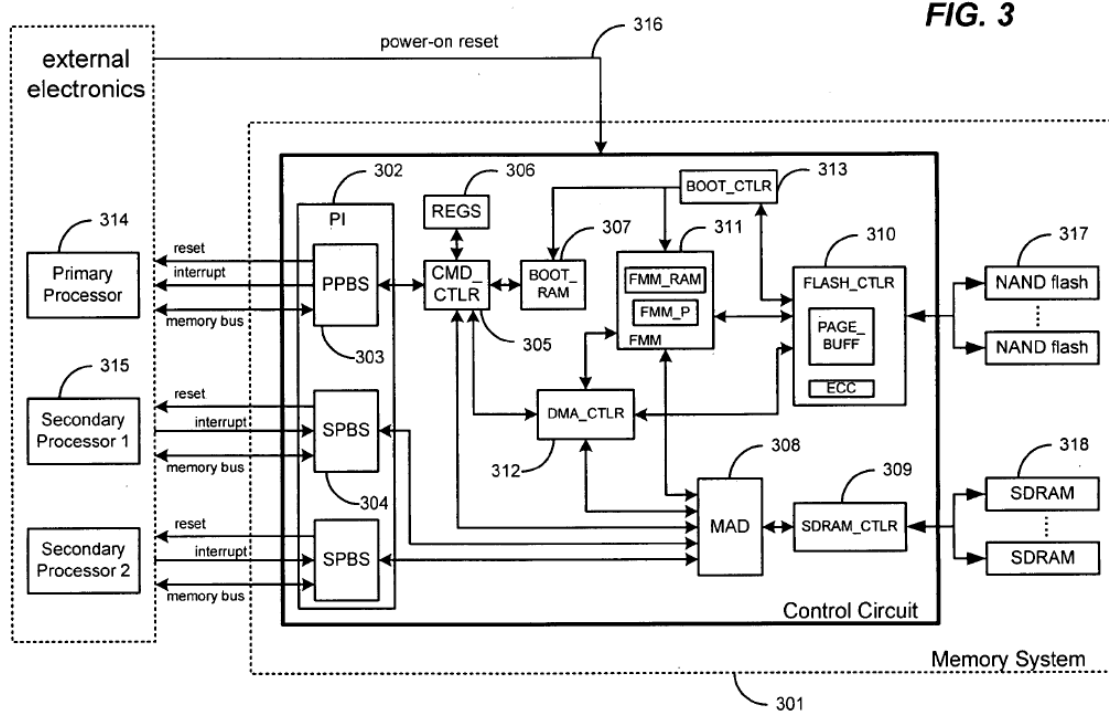


Figure 3 depicts a block diagram of a first embodiment of a memory system control circuit, corresponding to Control Circuit 203 illustrated in Figure 2. *Id.* ¶¶ 25, 83. Figure 3 includes Primary Processor 314 and Primary Processor Bus Slave circuit (“PPBS”) 303, which provides an interface between Primary Processor 314 and the Control Circuit. *Id.* ¶¶ 85, 88. “The PPBS (303) translates the memory bus signals from the Primary Processor (314) into commands, data, and address information and then passes this information to a Command Controller (CMD_CTRL 305), which, in turn, activates the appropriate parts of the Control Circuit to perform the associated operations in the Memory System (301).” *Id.* ¶ 89. For example, “the PPBS (303) translates the memory bus control signals into one of the following exemplary commands: ‘RAM Read,’ ‘RAM Write,’

‘Register Read,’ ‘Register Write,’ ‘Download DMA Transfer’ or ‘Upload DMA Transfer’ and sends the command to the Command Controller (305).” *Id.* ¶ 90. “The data and address signals of the memory bus provide the Command Controller (305) with data and address information associated with the command. The data signals of the memory bus are bidirectional to thereby communicate both write data and read data information.” *Id.* The “Download DMA Transfer” and “Upload DMA Transfer” commands “cause the CMD_CTRL (305) to activate a DMA controller (DMA_CTRL 312) to perform a DMA transfer from NAND Flash memory (317) to SDRAM (318) or from SDRAM (318) to NAND Flash memory (317) (uploading).” *Id.* ¶ 111. After being activated by the CMD_CTRL (305), the DMA_CTRL (312) obtains information associated with the DMA transfer, “such as the amount of data to be moved preferably described in number of NAND Flash pages, the starting NAND Flash Logical Page Address (LPA), and the starting SDRAM address.” *Id.*

The control circuit of Figure 3 also includes Flash memory management (FMM) circuit 311, which performs the Flash media management (FMM) processes. *Id.* ¶¶ 57, 66.¹⁰ “Volatile memory (FMM_RAM in FMM circuit 311) within the control circuit is used to store the FMM program code for execution by the embedded control circuit processor (FMM_P in FMM circuit 311).” *Id.* ¶ 66. FMM processes can include wear-leveling. *Id.* ¶ 65. Wear-leveling seeks to distribute multiple writes to the same logical address to different physical addresses to minimize the wear on a particular physical address. *Id.* ¶ 156. Lee describes

¹⁰ Lee refers to “FMM” as both “Flash memory management” (¶ 57) and “Flash media management” (¶ 65).

use of a translation table to maintain the association of logical and physical addresses, which are updated to reflect any new association between the logical and physical addresses. *Id.* When the Flash memory is accessed, “the FMM processes map the logical address space to the physical address space, and translate a logical page address (LPA) to a physical page address (PPA).” *Id.* ¶ 65.

Lee further describes “maintaining certain book-keeping records, such as one or more of logical-to-physical address translation tables, bad block locations, and physical addresses containing outdated data.” *Id.* ¶ 159. These records are “stored in the Flash memory and updated often enough to reflect the latest data arrangement in the Flash memory.” *Id.* “The FMM (311) initialization often involves finding and copying the FMM (311) book-keeping records required for Flash media management, such as address translation tables, from the NAND Flash memory (317) to the FMM_RAM or SDRAM (318).” *Id.* ¶ 169. “The FMM book-keeping records may be kept in the FMM_RAM, SDRAM (318), or both during normal operation.” *Id.* ¶ 172. “When the FMM algorithm code needs to update a portion of the book-keeping records in the SDRAM, the FMM (311) generates a new version of the portion of the book-keeping records in the FMM_RAM, and then copies the data from the FMM_RAM to the SDRAM (318) . . . to override the older version stored in the SDRAM.” *Id.* “From time to time, the FMM algorithms need to write or update certain book-keeping records in the NAND Flash memory (317), which often involves erasing various NAND Flash blocks and copying data from SDRAM (318) to NAND Flash memory.” *Id.* ¶ 173.

2. *Analysis of Independent Claim 1*

a) [1.PRE]: “A nonvolatile memory system comprising:”

Petitioner asserts that Lee teaches the preamble. Pet. 22. Specifically, Petitioner relies on Lee’s “wireless phone that includes a nonvolatile memory (‘Flash memory (104)’).” *Id.* (citing Ex. 1007 ¶ 63).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches the preamble.¹¹

b) [1.A]: “a nonvolatile memory for storage of digital information in addressable locations arranged in multiple blocks for access,”

Petitioner asserts that Lee teaches this limitation. Pet. 23. Specifically, Petitioner contends that Lee’s Flash memory 104 is in a “block” and “page” arrangement, and the blocks and pages “have physical addresses (*e.g.*, which the flash memory uses) and associated logical addresses (*e.g.*, which a host uses).” *Id.* (citing Ex. 1007 ¶¶ 63, 149, 152, 155–156); *see* Ex. 1003 ¶¶ 143–144. Petitioner further contends that “Lee’s Flash memory includes blocks that are either in the FMM-controlled section (903) or boot section (902).” *Id.* at n.7. Petitioner asserts that “Lee discloses multiple blocks for storing ‘digital information,’ *e.g.*, blocks to store information in the ‘FMM-controlled section.’” *Id.* (citing Ex. 1007 ¶ 173, Fig. 9). Dr. Levy provides testimony that “programs, user data, and book-keeping records” are stored in the “FMM-controlled section.”

¹¹ Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination that the preamble of claim 1 is limiting.

Ex. 1003 ¶ 145; *see also* Pet. 23 (“digital information, e.g., programs, user data, and book-keeping records.”).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.A.

- c) [1.B]: “*wherein reading of any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location;*”

Petitioner asserts that Lee teaches this limitation. Pet. 23–27. Specifically, Petitioner contends that Lee teaches storing programs, user data, and book-keeping records in the FMM-controlled section of nonvolatile memory (i.e., the claimed “digital information”), and transferring this data to volatile memory. *Id.* at 23–24 (citing Ex. 1007 ¶¶ 169, 207, 208, 213); Ex. 1003 ¶ 145. Petitioner asserts that the transfer to volatile memory involves reading pages from nonvolatile memory (“any portion” of the digital information) by using the starting logical page address (“an associated addressable location”). Pet. 24 (citing Ex. 1007 ¶ 200). Petitioner further contends that “processors access the SDRAM to modify the digital information.” *Id.* (citing Ex. 1007 ¶¶ 90, 91, 104–108, 120, 172). Petitioner contends that “Lee discloses writing the modified data back to the nonvolatile memory to the same logical address.” *Id.* (citing Ex. 1007 ¶¶ 111, 182). According to Petitioner, “the DMA transfer processes uses logical address (the ‘same associated address[es]’), not the physical addresses, of the pages and blocks to perform the transfers.” *Id.* at 24–25

(citing Ex. 1007 ¶ 182). However, Petitioner asserts that “the write operations result in the data being written to different physical addresses.” *Id.* at 25 (citing Ex. 1007 ¶¶ 156, 189, Fig. 9; Ex. 1003 ¶ 152). Specifically, Petitioner argues that Lee discloses a “wear-leveling technique in which the data is written to a different physical block.” *Id.* at 25–26 (citing Ex. 1007 ¶ 156). Petitioner also contends that “it would have been obvious to always write the modified data to a different physical address, e.g., a block” because it was conventional and known. *Id.* at 26 (citing Ex. 1003 ¶¶ 157–159).

Patent Owner argues that Petitioner has not shown that Lee teaches limitation 1.B. PO Resp. 31–32. Specifically, Patent Owner contends that “Lee fails to disclose or suggest a read/modify/write operation that involves a non-volatile memory.” *Id.* at 32.

As discussed in Section III.C.3, we determined that this limitation does not require a “read/modify/write operation.” Thus, these arguments by Patent Owner are unavailing.

We find Petitioner has shown that Lee teaches limitation 1.B. Petitioner identifies Lee’s user data, programs, and/or book-keeping records as disclosing the claimed “digital information.” Pet. 24. Petitioner has provided a number of citations, supported by testimony from Dr. Levy, where Lee discloses transferring data, including book-keeping records, user data, and program data, from NAND flash memory (e.g., reading) to SDRAM (e.g., writing) and vice versa. *Id.* at 23–24; *see, e.g.*, Ex. 1007 ¶¶ 111, 182, 200 (describing “Download DMA Transfer” where NAND Flash to SDRAM transfer is performed and “Upload DMA Transfer” where SDRAM to NAND Flash transfer is performed); ¶ 169 (“finding and copying the FMM (311) book-keeping records . . . from the NAND Flash

memory (317) to the FMM_RAM or SDRAM (318)"); ¶ 173 ("write or update certain book-keeping records . . . which often involves . . . copying data from SDRAM (318) to NAND Flash memory (317)"); ¶ 207 ("the Primary Processor activates a DMA transfer to copy the program code from NAND Flash to SDRAM"); ¶ 213 ("copying user data from NAND Flash memory (317) to SDRAM (318) and vice versa"); *see also* Ex. 1003 ¶¶ 148, 152. According to this disclosure, Lee generally describes transferring data to volatile memory from nonvolatile memory and vice versa, as well as explicitly describes transferring more specific types of data, e.g., book-keeping records, user data, and program data.

Petitioner has also shown that Lee teaches "reading of *any portion of the digital information in a given block from an associated addressable location.*" *See* Pet. 23. For example, Lee teaches that its "Download DMA Transfer" process "generates a first NAND Flash LPA [Logical Page Address] and its corresponding SDRAM address, and then activates the FMM (311) to read NAND Flash page of this LPA." Ex. 1007 ¶ 200. Then, "the FMM (311) performs a logical-to-physical address translation to convert the LPA to PPA and then configures and . . . activates the FLASH_CTLR (310) to read the NAND Flash page of this PPA [physical page address]." *Id.*; *see also id.* ¶¶ 111, 182. As a more specific example, Lee teaches "finding and copying the FMM (311) book-keeping records . . . from the NAND Flash memory (317) to the FMM_RAM or SDRAM (318). *Id.* ¶ 169; *see also id.* ¶ 170 ("[t]o copy data . . . from a NAND Flash page to FMM_RAM . . . read the NAND Flash page . . . and write[] the data from the FMM_RAM to SDRAM"). Dr. Levy provides undisputed testimony, which we credit, that flash memory is organized into blocks, pages, and

sectors, where a block is the smallest erasable unit, and a block is made up of multiple pages. Ex. 1003 ¶ 55; *see* Ex. 2001 ¶¶ 39, 40. Dr. Levy also provides undisputed testimony, which we credit, that the smallest accessible unit for a read or write in nonvolatile memory is a page. Ex. 1003 ¶ 102; *see* Ex. 2001 ¶¶ 39, 40.

Petitioner has also shown that Lee teaches “reading of any portion of the digital information . . . *and modification thereof* for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location.”¹² Lee describes that “[w]hen the FMM algorithm code needs to update a portion of the book-keeping records in the SDRAM, the FMM (311) generates a new version of the portion of the book-keeping records in the FMM_RAM, and then copies the data from the FMM_RAM to the SDRAM (318) via the MAD (308) to override the older version stored in the SDRAM (318).” Ex. 1007 ¶ 172. As discussed above, Lee teaches “finding and copying the FMM (311) book-keeping records . . .

¹² We note that the claim does not explicitly recite *where* the modification occurs. However, the plain language of the claim, reciting “and modification thereof *for storage back in the memory* in the same addressable location” indicates that the modification is performed somewhere other than nonvolatile memory and is then put back into nonvolatile memory. Petitioner interprets this claim limitation as describing that the digital data is transferred from nonvolatile memory into volatile memory, the modification is performed in volatile memory, and the modified data is written back to nonvolatile memory. *See* Pet. 16, 14–25. Patent Owner appears to agree. *See* PO Resp. 21 (construing this limitation as “modifying the read information in volatile memory, and writing the modified information back to the non-volatile memory”).

from the NAND Flash memory (317) to the FMM_RAM or SDRAM (318).” Ex. 1007 ¶ 169. Petitioner has, therefore, shown that Lee teaches “reading of any portion of the digital information [(e.g., copying book-keeping records from NAND Flash memory to FMM_RAM or SDRAM)] . . . and modification thereof” (e.g., updating a portion of the book-keeping records in the SDRAM). *See* Pet. 23–24; Ex. 1007 ¶¶ 169, 172.

Petitioner has also shown that Lee teaches or suggests “*for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location.*” *See* Pet. 24–27. For example, Lee teaches that the “Upload DMA Transfer” process “perform[s] a DMA transfer . . . from SDRAM (318) to NAND Flash memory (317).” Ex. 1007 ¶ 111. “The DMA_CTRL (312) obtains information associated with the DMA transfer . . . such as the amount of data to be moved preferably described in number of NAND Flash pages, the starting NAND Flash Logical Page Address (LPA), and the starting SDRAM address.” *Id.*; *see also id.* ¶ 182. “To begin the transfer of a NAND Flash page, the DMA_CTRL (312) writes the LPA and the transfer type (e.g., a ‘page read’ for Download DMA Transfer or a ‘page write’ for Upload DMA Transfer) The FMM (311) then performs the address translation to obtain the PPA and configures the FLASH_CTRL (31)) to read from or write to the NAND Flash Page of this PPA.” *Id.* ¶ 184. Specifically with respect to the book-keeping records, Lee describes “write or update certain book-keeping records . . . which often involves . . . copying data from SDRAM (318) to NAND Flash memory (317)”. *Id.* ¶ 173.

Petitioner relies on Lee’s wear-leveling to teach writing of the modified digital information *into a new physical location mapped to the same associated addressable location*. Pet. 25–27. Lee teaches that “[t]o maintain the association of the logical and physical addresses, address translation tables are usually used.” Ex. 1007 ¶ 156. “When the higher-level system software overrides an already-written logical address with new data, instead of erasing the associated physical address and writing the new data to the same physical address, the lower-level software actually finds an unwritten physical address and writes the new data to this newly found physical address.” *Id.* Dr. Levy testifies that “overrides,” as used in paragraph 156, refers to a write operation that overrides (or overwrites) the data at a logical address. Ex. 1003 ¶ 154. “The address translation tables are then updated to reflect the new association between the logical and physical addresses.” Ex. 1007 ¶ 156. The program codes, user data, and book-keeping records that are stored in the FMM-controlled section, “are moved around to different physical addresses for wear-leveling and bad-block replacement purposes, and are maintained and tracked by the FMM algorithms.” *Id.* ¶ 189; *see also* Ex. 1003 ¶ 156. We also find persuasive Petitioner’s arguments, and credit Dr. Levy’s supporting testimony, that it would have been obvious to write modified data to a different physical block. Ex. 1003 ¶¶ 157–158.

Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.B.

- d) [1.C]: “a volatile random access memory for read and write operations; and”

Petitioner asserts that Lee teaches this limitation. Pet. 27. Specifically, Petitioner contends Lee discloses a Main RAM, e.g., SDRAM, as well as read and write operations to Main RAM. *Id.* (citing Ex. 1007 ¶¶ 63, 64, 82, 104).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.C.

- e) [1.D]: “wherein the coupled volatile random access memory and nonvolatile memory for storage are controlled by one or more controllers, the one or more controllers controlling the volatile and nonvolatile memories to:”

Petitioner asserts that Lee teaches this limitation. Pet. 27–28. Specifically, Petitioner contends that Lee’s Flash memory and Main RAM both have a controller. *Id.* (citing Ex. 1007 ¶¶ 63, 111, 121, 122, 182–184).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.D.

- f) [1.E]: “perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location, wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory”

Petitioner asserts that Lee teaches this limitation. Pet. 28–31. Specifically, Petitioner relies on Lee’s “DMA download transfer” process that performs read operations on the data in the nonvolatile memory at the

associated addressable location (‘NAND Flash Logical Page Address’) to retrieve it and store it in the SDRAM.” *Id.* at 28 (citing Ex. 1007 ¶¶ 111, 169, 207–208, 213). Petitioner contends that “the data is written to the SDRAM via the SDRAM controller,” and “once the data is stored in SDRAM, it would have been understood, and certainly obvious, that Lee discloses accesses on ‘any portion of the stored retrieved digital information can be accessed from the volatile random access memory’ (e.g., accesses down to the byte level).” *Id.* at 29. According to Petitioner, such “reads and writes on the SDRAM” were “well-known in the prior art” and include “addressable accesses (read and writes) of a byte.” *Id.* (citing Ex. 1007 ¶¶ 90, 122; Ex. 1016, 107).

For the same reasons as set forth above with respect to limitation 1.B, we find Petitioner has shown sufficiently Lee teaches or suggests “perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location.”

We also find Petitioner has shown sufficiently that Lee teaches “wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory.” As discussed above in Section III.C.1 (Claim Construction), we interpret “any portion” to include accessibility at the bit or byte level. As discussed above with respect to limitation [1.B], Lee teaches that data is transferred from nonvolatile memory to volatile memory. Lee also teaches “operat[ing] the SDRAM according to the protocols of the SDRAM interface . . . [t]he data transfer protocols of the SDRAM (318) interface are well-known in the prior art and therefore not described in the present invention.” Ex. 1007 ¶ 122.

Petitioner's contentions, which are supported by Dr. Levy's testimony and additional evidence, are essentially based on the following: (1) Lee discloses reads and writes on the SDRAM that are described as "well-known in the prior art"; (2) it was well-known to access volatile memory down to the bit or byte level via reads and writes; (3) Lee discloses that its SDRAM access unit may assume any access configuration; (4) a common SDRAM configuration was addressable at byte-level access; and (5) Lee discloses a burst mode of one word, i.e., a single access of one unit of data. Pet. 29–30 (citing Ex. 1003 ¶ 172; Ex. 1007 ¶¶ 82, 86, 90, 92, 102, 122; Ex. 1016, 107; Ex. 1018, 30–31). Petitioner also asserts that for similar reasons, it "would have been obvious to access 'any portion' of the SDRAM" and provides motivation from Lee, stating that "processor's [*sic*] typically need random-access on a byte or word level." *Id.* at 30 (citing Ex. 1003 ¶¶ 172–175; Ex. 1016 at 107; Ex. 1017, 6:27–33; Ex. 1007 ¶ 8). We find Petitioner's showing as to accessibility of volatile memory at the bit or byte level in Lee is sufficient to teach this limitation.

Patent Owner does not respond to these arguments. *See generally* PO Resp. Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.E.

g) [1.F]: "*perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory,*"

Petitioner asserts that Lee teaches this limitation. Pet. 31. Specifically, Petitioner contends that Lee teaches that various entities, such as the primary processor, may perform access operations, such as reads, on data (e.g., user data and FMM book-keeping records) that was transferred to

SDRAM. *Id.* (citing Ex. 1007 ¶¶ 90, 91, 108, 112, 159, 169; Ex. 1003 ¶¶ 176–178).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, and for reasons already discussed above with respect to limitations 1.B and 1.E, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.F.

h) [1.G]: “perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein, and”

Petitioner asserts that Lee teaches this limitation. Pet. 31–33. Specifically, Petitioner asserts, for similar reasons as with respect to limitations 1.B and 1.E, that Lee discloses that data (e.g., user data and FMM book-keeping records) is transferred to the SDRAM to be accessed (e.g., read and write), and at the respective SDRAM addresses, the data can be read and overwritten. *Id.* at 32 (citing Ex. 1007 ¶¶ 91, 104–108, 120, 169, 172, 213; Ex. 1003 ¶¶ 179–183). Petitioner further asserts that the digital information is written back to the same physical location in the volatile memory because “Lee discloses a single address set for the SDRAM, not both physical and logical addresses for wear-leveling as Lee discloses for the Flash.” *Id.* (citing Ex. 1007 ¶ 104). Petitioner also argues that there is “correspondence between the SDRAM and flash logical addresses (the starting addresses for the transfer set a correspondence), and thus the SDRAM data must be written back to the same addresses to maintain the correspondence.” *Id.* at 32–33 (citing Ex. 1007 ¶¶ 111, 200–203; Ex. 1003 ¶ 182).

We find that Petitioner has shown sufficiently that Lee teaches limitation 1.G. As discussed above with respect to limitation 1.B, Petitioner has provided a number of citations, supported by testimony from Dr. Levy, where Lee discloses transferring data, including book-keeping records, user data, and program data, from NAND flash memory (e.g., reading) to SDRAM (e.g., writing). *E.g.*, Pet. 23–24, 32; Ex. 1007 ¶¶ 111, 169, 172, 182, 200, 207, 213. Lee further teaches access requests to SDRAM, to write data to or read data from SDRAM. Ex. 1007 ¶ 91 (“SDRAM access request . . . to request access to the SDRAM . . . can write data to or read data from the SDRAM”); ¶ 104 (“RAM Read,” “RAM Write,” and “address range for accessing the SDRAM”); ¶ 107 (“RAM Read” and “RAM Write”). We find persuasive Petitioner’s argument, which is supported by testimony from Dr. Levy, that Lee discloses a single address for the SDRAM, so “the SDRAM data must be written back to the same address.” Pet. 32–33; Ex. 1003 ¶¶ 179–183.

Patent Owner does not respond to these arguments. *See generally* PO Resp. Accordingly, after considering the evidence and arguments of the complete record, and for reasons already discussed above with respect to limitations 1.B and 1.E, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.G.

- i) [1.H]: “write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read.”

Petitioner asserts that Lee teaches this limitation. Pet. 33–34. Specifically, Petitioner asserts, for similar reasons as with respect to limitation 1.B, that Lee discloses that volatile memory data (e.g., user data and FMM book-keeping records) are written back to non-volatile memory. *Id.* at 33 (citing Ex. 1007 ¶¶ 111, 179, 189, 213; Ex. 1003 ¶¶ 184, 185). Petitioner also asserts that Lee discloses that “the logical address (‘same associated address’) is overwritten with data, but the data is written to a different physical block and the logical address is remapped to the different physical block.” *Id.* at 33–34 (citing Ex. 1007 ¶ 156); *see also id.* at 34 (citing Ex. 1007 ¶ 189; Fig. 9; Ex. 1003 ¶¶ 186–188).

Patent Owner does not respond to these arguments. *See generally* PO Resp. Accordingly, after considering the evidence and arguments of the complete record, and for reasons already discussed above with respect to limitations 1.B and 1.E, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.H.

3. *Analysis of Claims 2, 3, 9–16*

Petitioner contends that dependent claims 2, 3, and 9–16, which depend from independent claim 1, would have been obvious over Lee, and provides arguments as to how the prior art teaches or suggests each claim limitation. Pet. 34–42. Patent Owner does not separately respond to these arguments. *See* PO Resp. 32. We agree with and adopt Petitioner’s arguments. After considering the evidence and arguments of the complete

record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches the limitations in claims 2, 3, and 9–16.

4. *Conclusion*

Having considered the *Graham* factors,¹³ including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the challenged claims, we are persuaded, based on the current record, that Petitioner has shown, by a preponderance of the evidence, that claims 1–3 and 9–16 would have been obvious over Lee.

E. Ground 2: Obviousness Over Tsunoda and Kolokowsky

Petitioner contends that claims 1–3, 5–6, 9, 11, and 16 would have been obvious over the combination of Tsunoda and Kolokowsky. Pet. 42–62. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–3, 5–6, 9, 11, and 16 are unpatentable over the combination of Tsunoda and Kolokowsky.

1. *Tsunoda (Ex. 1008)*

Tsunoda is titled “Memory Apparatus” and generally relates to a memory apparatus which uses a volatile and nonvolatile memory. Ex. 1008, code (54), ¶ 1. Tsunoda generally seeks to improve controllability of data transfer between a volatile memory and a nonvolatile memory. *Id.* ¶ 4.

Figure 24, reproduced below, illustrates a configuration of the memory apparatus. *Id.* ¶ 35.

¹³ Patent Owner does not submit evidence of secondary considerations. *See* PO Resp.

FIG.24

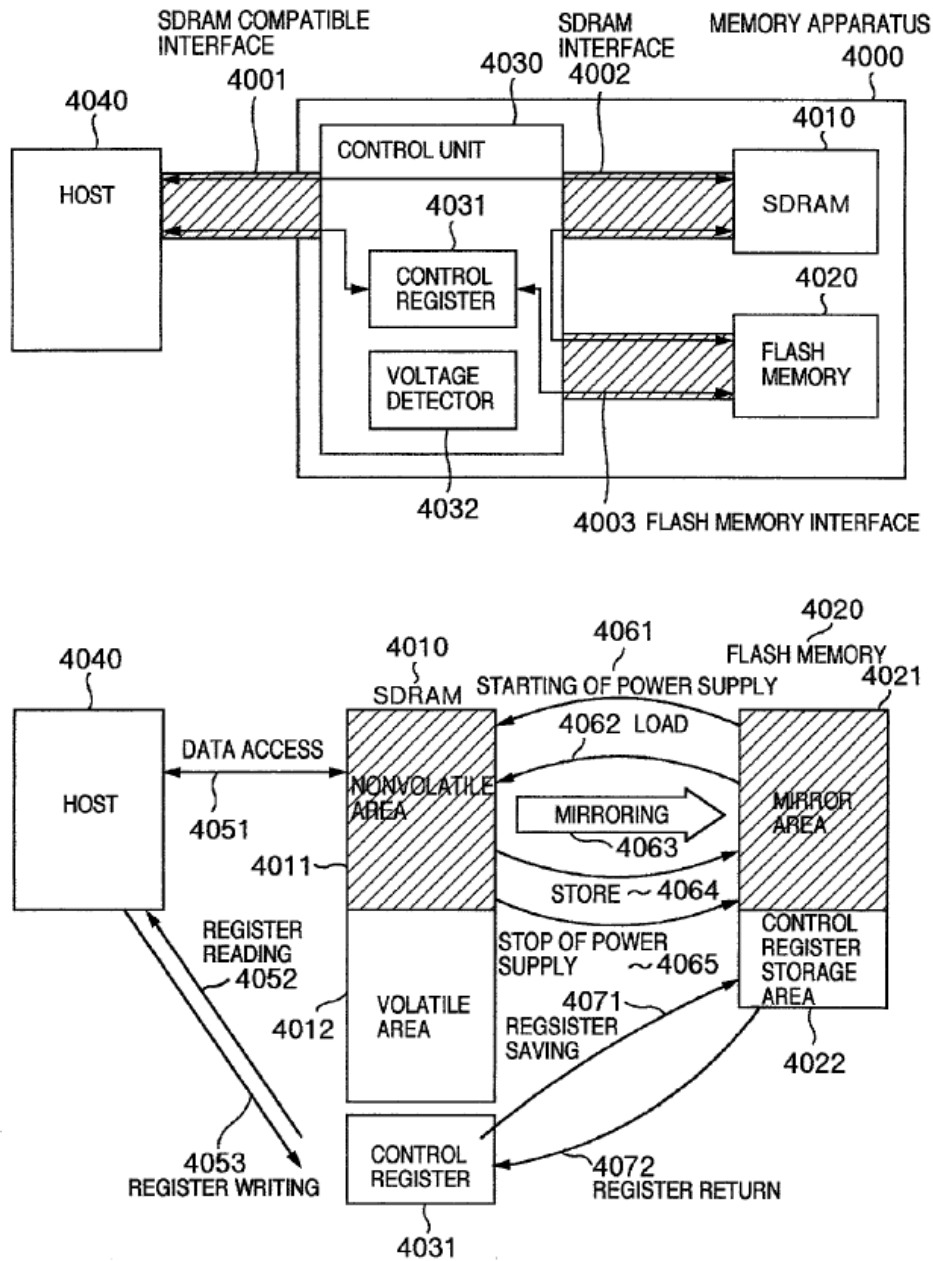


Figure 24 depicts a configuration of a memory apparatus 4000, including flash memory 4020 that is nonvolatile memory and SDRAM 4010 to be accessed randomly. *Id.* ¶¶ 35, 42. Memory apparatus 4000 “includes a function of setting a correspondence between an address of the SDRAM

4010 and an address of the flash memory 4020 according to a predetermined process.” *Id.* ¶ 50.

SDRAM 4010 includes at least one nonvolatile areas 4011 and an area (volatile area 4012) other than nonvolatile area 4011. *Id.* ¶¶ 70, 72.

Nonvolatile area 4011 is an area for performing mirroring 4063 by using the flash memory 4020. *Id.* ¶ 71. “Mirroring 4063 means that data stored in a mirror area 4021 of the flash memory 4020 is brought into coincidence with data stored in nonvolatile area 4011 of the SDRAM 4010, or that a copy of the data stored in the nonvolatile area 4011 of the SDRAM 4010 is stored in the mirror area 4021 of flash memory 4020.” *Id.* ¶ 73. Mirror area 4021 of flash memory 4020 is managed based on a logical address excluding a failed area of flash memory 4020. *Id.* Tsunoda explains that

[s]ince the SDRAM **4010** is a volatile memory, data written in the SDRAM **4010** is lost when the power supply to the memory apparatus **4000** is stopped. However, as the data stored in the nonvolatile area **4011** can be subjected to mirroring in the mirror area **4021** of the flash memory **4020**, the data can be held ever after power is turned OFF. The data stored in the volatile area **4012** is lost when the power is OFF. The host **4040** can access the nonvolatile area **4011** of the SDRAM **4010**, the volatile area **4012** of the SDRAM **4010**, and the control register **4031** by designating a predetermined address through the SDRAM compatible interface **4001**.

Id. ¶ 75.

Figure 1, reproduced below, depicts an example of an internal configuration of memory apparatus.

FIG.1

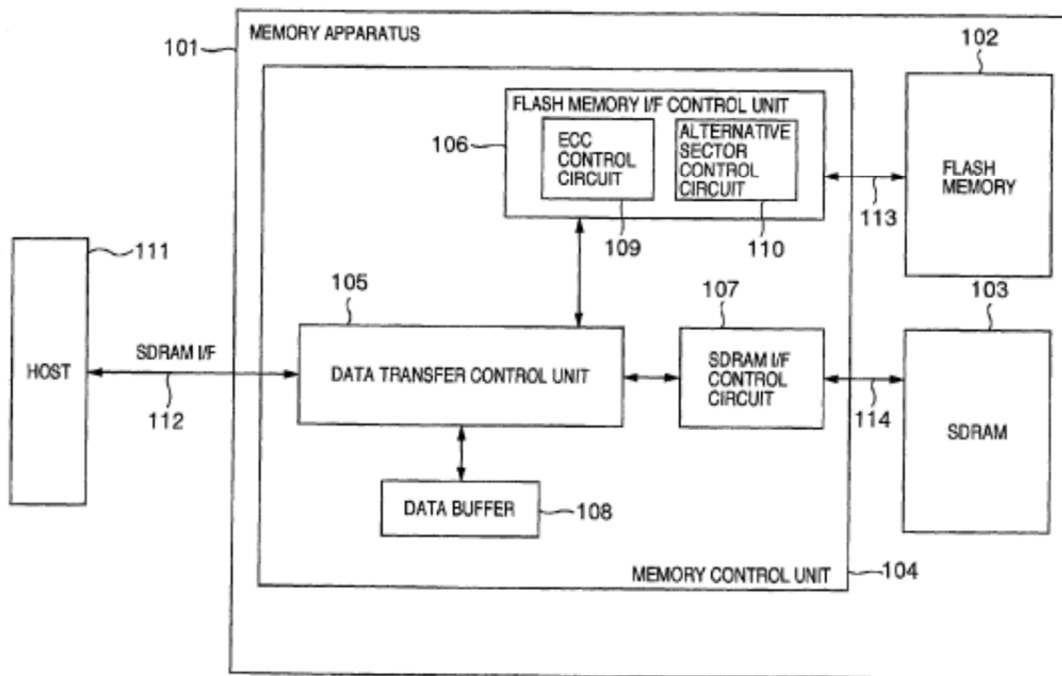


Figure 1 includes flash memory 102 as nonvolatile memory, SDRAM 103 as volatile memory, and a memory control unit 104 for controlling the memories. *Id.* ¶ 96. “The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111.” *Id.* The address space of the SDRAM 103 includes a volatile area 203 and a nonvolatile area 204. *Id.* ¶ 98. “After the power is turned ON, user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103, and the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM 102. If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102.” *Id.* ¶ 99.

2. *Kolokowsky (Ex. 1009)*

Kolokowsky is titled “Flash Drive Fast Wear Leveling” and generally describes improved wear-leveling of flash memory. Ex. 1009, code (54), 1:11–12. Figure 1, reproduced below, illustrates a memory system including a wear-leveling table. *Id.* at 1:63–65, 2:8–67.

Figure 1

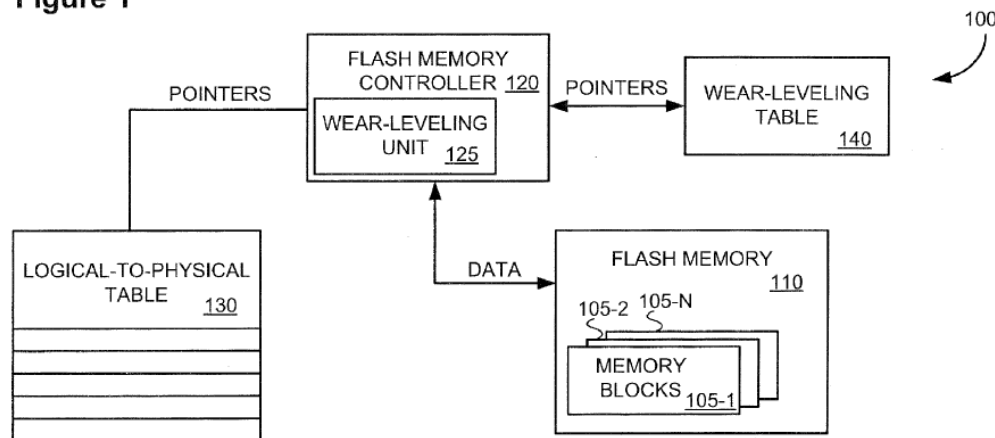


Figure 1 depicts memory system 100, including: (i) a flash memory 110, which may be NAND flash memory or other type of non-volatile memory capable of storing data and having a plurality of memory blocks 105-1 to 105-N to store the data; (ii) a flash memory controller 120 to perform memory access operations, such as read, write, and erase, on memory blocks 105-1 to 105-N; (iii) a logical-to-physical table 130 populated with pointers to the memory blocks 105-1 to 105-N, where the pointers may be addresses to physical locations of the memory blocks in flash memory 110; (iv) a wear-leveling table 140 populated with pointers to unallocated memory blocks in flash memory 110; and (v) a wear-leveling unit 125 in controller 120, used to populate the wear-leveling table 140 with pointers to unallocated memory blocks. *Id.* at 2:8–3:13. Flash memory 110 may include 1024 memory blocks, for example, with a maximum of 1000 of

the 1024 memory blocks allocated for the storage of data at any given time, the remaining unallocated memory blocks including erased or erasable memory blocks available to store data, bad or faulty memory blocks, or both. *Id.* at 2:12–20.

Kolokowsky explains the operation of memory system 100 as follows:

When prompted to write data to the flash memory 110, the flash memory controller 120 may identify one or more unallocated memory blocks in the flash memory 110 available to store the data and then write the data to the identified memory block(s).

...

When the flash memory controller 120 determines to write data to the flash memory 110, the wear-leveling unit 125 may access the wear-leveling table 140 to identify at least one erased or erasable memory block in the flash memory 110 available to store the data. The wear-leveling table 140 may also include data to indicate which of the pointers correspond to erased or erasable memory blocks and which of the pointers correspond to faulty or failed memory blocks. Since the wear-leveling table 140 includes pointers to unallocated memory blocks in the flash memory 110, the wear-leveling unit 125 may reduce the time required to identify an erased or erasable memory block during data write operations.

Id. at 2:24–32, 3:14–25.

3. *Analysis of Independent Claim 1*

a) *[1.PRE]: “A nonvolatile memory system comprising:”*

Petitioner asserts that Tsunoda teaches the preamble. Pet. 43.

Specifically, Petitioner relies on Tsunoda’s “nonvolatile memory system with flash and SDRAM memories.” *Id.* (citing Ex. 1008, Fig. 24; ¶ 96).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record,

we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches the preamble.

b) [1.A]: “a nonvolatile memory for storage of digital information in addressable locations arranged in multiple blocks for access,”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 44. Specifically, Petitioner identifies Tsunoda’s flash memory with “logical sector address[es].” *Id.* (citing Ex. 1008 ¶¶ 96, 107) (alteration in original). Petitioner asserts that the disclosure of “sectors” necessarily discloses “blocks” because it is well-known that flash memory is organized into blocks, which includes pages, which may in turn include one or more sectors. Pet. 45 (citing Ex. 1021 ¶ 6; Ex. 1001, 3:3–7, Fig. 2; Ex. 1003 ¶¶ 224–225). Petitioner further argues that Tsunoda discloses that its flash memory stores “user data,” which teaches “digital information.” *Id.* (citing Ex. 1008 ¶ 99).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.A.

- c) [1.B]: “wherein reading of any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location;”

Petitioner asserts that Tsunoda in combination with Kolokowsky teaches this limitation. Pet. 44–46. Specifically, Petitioner contends that “upon powering up, ‘user data’ is transferred from the flash memory (from its logical sector addresses) to the SDRAM, this information is read and modified, and then written back to the same ‘addressable location’ (the logical address of the sector).” *Id.* at 45 (citing Ex. 1008 ¶¶ 50, 51, 66, 99, 107; Ex. 1003 ¶¶ 227–229). Petitioner further asserts that Tsunoda discloses reading sectors from the nonvolatile memory, which teaches “any portion” of the nonvolatile memory. *Id.* (citing Ex. 1008 ¶¶ 99, 107).

Petitioner contends that Tsunoda does not disclose which physical blocks the data at the logical flash addresses are written to, and so relies on Kolokowsky to teach that it was conventional to write the modified data to a different physical block, such as an already erased block. *Id.* (citing Ex. 1009, 1:23–33). Petitioner asserts that as part of the write operation, the logical addresses is re-mapped to the new physical address. *Id.* at 46 (citing Ex. 1003 ¶¶ 231–233; Ex. 1009, 1:33–42; 2:21–3:3).

Petitioner argues that a person of ordinary skill in the art would have been motivated to combine Tsunoda and Kolokowsky because (1) “Tsunoda provides the ability for wear leveling because it implements logical addressing for the flash device”; (2) a person of ordinary skill in the art would know that using wear-leveling was advantageous because wear-leveling was known to extend the life of the device; and (3) a person of

ordinary skill in the art would know that using wear-leveling was advantageous because it ensures that different, previously erased blocks are available to which data may be written back, which decreases write operation time because the block does not have to be erased before programming. *Id.* at 60–61 (citing Ex. 1008 ¶ 107; Ex. 1014, 1:30–45; 1:46–48; Ex. 1009, 4:30–52; Ex. 1015 ¶ 9; Ex. 1003 ¶¶ 294–297). Petitioner also argues that a person of ordinary skill in the art would have had a high expectation of success in implementing Kolokowsky’s wear-leveling techniques in Tsunoda because wear-leveling was conventional and Tsunoda already uses logical addressing. *Id.* at 61 (citing Ex. 1003 ¶ 298; Ex. 1009, 1:23–33; Ex. 1008 ¶ 107; Ex. 1014, 1:46–48).

Patent Owner argues that Petitioner has not shown that the combination of Tsunoda and Kolokowsky teaches limitation 1.B. PO Resp. 31–32. Specifically, Patent Owner contends that “Patent Owner agrees with Petitioner that Tsunoda does not disclose the limitation that the data is read from a physical location and written back to a different physical location. Kolokowsky also does not disclose this limitation.” *Id.* at 32–33. Patent Owner also argues that “neither Tsunoda nor Kolokowsky teach a read/modify/write operation that involves a non-volatile memory.” *Id.* at 33; *see also id.* at 34.

As discussed in Section III.C.3, we determined that this limitation does not require a “read/modify/write operation.” Thus, these arguments by Patent Owner are unavailing.

We find that Petitioner has shown that Tsunoda and Kolokowsky teach this limitation. Petitioner has shown that Tsunoda teaches “*wherein reading of any portion of the digital information in a given block from an*

associated addressable location and modification thereof for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location.” Petitioner identifies Tsunoda’s user data as disclosing the claimed “digital information.” Pet. 45. Tsunoda discloses that

After the power is turned ON, user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103 and the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM. If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102.

Ex. 1008 ¶ 99. Tsunoda, therefore, teaches that the user data is copied from flash memory to SRAM (*i.e.*, read), and then copied back to flash memory (*i.e.*, written) if it is “slightly changed or contains an addition,” (*i.e.*, modified).

Petitioner has also shown that Tsunoda and Kolokowsky teaches or suggests “*for storage back in the memory in the same addressable location requires writing of the modified digital information into a new physical location mapped to the same associated addressable location.*” Tsunoda discloses logical sector addresses in flash memory being mapped to address space in the SDRAM. Ex. 1007 ¶¶ 50–52, 107. Because Tsunoda does not disclose to which physical blocks the data at the logical flash addresses are written, Petitioner relies on Kolokowsky to teach writing the data to a different physical address. Pet. 45. Kolokowsky discloses that “[d]uring write operations the flash driver is commonly required to identify erased memory blocks available to store data. Many flash drivers perform . . . write

operations on the most recently erased memory block.” Ex. 1009, 1:23–27. Kolokowsky describes finding available, already erased blocks more efficiently. *Id.* at 1:43–58. Kolokowsky further discloses a “logical-to-physical table,” which Petitioner contends, with supporting testimony from Dr. Levy, maps the logical address to the physical address. *Id.* at 1:43–58, 2:33–41; Pet. 45; Ex. 1003 ¶¶ 231–233. We find Petitioner’s contentions as to the combination of Tsunoda with Kolokowsky sufficient to show that the combination teaches this limitation. We additionally find that Petitioner has provided sufficient rationale for combining Tsunoda with Kolokowsky, with a reasonable expectation of success, supported by testimony from Dr. Levy, which we credit. *See* Ex. 1003 ¶¶ 294–298.

Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda and Kolokowsky teach limitation 1.B and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

d) [1.C]: “a volatile random access memory for read and write operations; and”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 46. Specifically, Petitioner contends Tsunoda teaches a volatile SDRAM that the host uses for read and write operations. *Id.* (citing Ex. 1008 ¶¶ 42, 90).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.C.

- e) [1.D]: “wherein the coupled volatile random access memory and nonvolatile memory for storage are controlled by one or more controllers, the one or more controllers controlling the volatile and nonvolatile memories to:”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 47. Specifically, Petitioner contends Tsunoda teaches an SDRAM controller (“SDRAM interface control circuit”) and a Flash memory controller (“flash memory interface control unit”) that control the respective memories. *Id.* (citing Ex. 1008 ¶ 97).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.D.

- f) [1.E]: “perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location, wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 47–49. Specifically, Petitioner asserts that Tsunoda teaches that “upon start up, user data (which is ‘digital information to be read’) is read from the flash memory at its logical address (logical sectors) and is transferred to the SDRAM (‘perform a read operation on the portion of the digital information’ and ‘retrieving and storing such from the given block at the associated addressable location’).” *Id.* at 47 (citing Ex. 1008 ¶¶ 99, 107, 110). Petitioner contends that “it would have been understood and certainly obvious, that Tsunoda discloses that its SDRAM is accessible according to conventional SDRAM access techniques such as addressable byte-level

access.” *Id.* at 48; *see* Ex. 1008 ¶¶ 90, 94. Petitioner provides further evidence, including testimony from Dr. Levy, that the addressable unit for accesses is a single byte. Pet. 48 (citing Ex. 1016 at 107; Ex. 1017, 6:27–33; Ex. 1003 ¶¶ 241, 242). Patent Owner does not respond to these arguments. *See generally* PO Resp.

For the same reasons as set forth above with respect to limitation 1.B, we find Petitioner has shown Tsunoda teaches “perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location.” As discussed above with respect to limitation 1.B, Tsunoda teaches that user data is copied from flash memory to SDRAM. Ex. 1008 ¶ 99. We also find Petitioner has shown that Tsunoda teaches “wherein any portion of the stored retrieved digital information can be accessed from the volatile random access memory,” for similar reasons as set forth above in Section III.D.2.f (analysis of limitation 1.E as to Lee).

Petitioner’s contentions, which are supported by Dr. Levy’s testimony and additional evidence, are essentially based on the following: (1) Tsunoda discloses a standard SDRAM, but states that the SDRAM could assume other forms, and discloses that SDRAM can receive instructions such as reads and writes; and (2) it was well-known to access volatile memory at the bit or byte level via reads and writes. Pet. 47–48 (citing Ex. 1008 ¶¶ 90, 94; Ex. 1016, 107; Ex. 1017, 6:27–33; Ex. 1018, 30–31; Ex. 1003 ¶ 243). Petitioner also asserts that for similar reasons, it would have been obvious to access “any portion” of the SDRAM and provides motivation from Tsunoda, stating that “access to only small bits of data may be necessary (e.g., to

retrieve user settings for applications) such as a bit or a byte.” *Id.* at 48 (citing Ex. 1003 ¶ 244).

Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.E.

g) [1.F]: “perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory,”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 49. Specifically, Petitioner contends Tsunoda discloses SDRAM with stored user data that is “accessed randomly,” and that such accesses included accesses of “any portion,” e.g., a bit or a byte. *Id.* (citing Ex. 1008 ¶¶ 42, 90, 99).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.F.

h) [1.G]: “perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein, and”

Petitioner asserts that Tsunoda teaches this limitation. Pet. 49–50. Specifically, Petitioner contends that “Tsunoda discloses standard SDRAM write operations on the read user data (‘the accessed read digital information’) and that the user data is randomly accessible.” *Id.* at 49 (citing Ex. 1008 ¶¶ 42, 90, 99). Petitioner further contends that “the writes would be used on any portion of the user data,” for similar reasons as discussed with respect to limitation 1.E. *Id.* at 50. Petitioner further contends that “it

would have been understood, and certainly obvious, that the user data is written back to the same physical location in the SDRAM.” *Id.* In support of its arguments, Petitioner argues that “Tsunoda’s memory mapping relies on the SDRAM addresses not changing” because “there is a ‘correspondence’ between the SDRAM address space and the logical addresses of flash memory that does not change.” *Id.* (citing Ex. 1008 ¶¶ 50–52, 62, 100, 107, Figs. 2, 15). Patent Owner does not respond to these arguments. *See generally* PO Resp.

As discussed above with respect to limitation 1.B, Tsunoda discloses copying data from flash memory to the nonvolatile area of the SDRAM. Ex. 1008 ¶ 99. Tsunoda further teaches SDRAM operations of writing and reading. *Id.* ¶ 90 (“memory apparatus 4000 receives various SDRAM operation instructions of reading, writing, refreshing, and the like”). We also find Petitioner has shown that Tsunoda teaches “any portion” for the same reasons as set forth in limitation 1.E. We find persuasive Petitioner’s argument, which is supported by testimony from Dr. Levy, that “Tsunoda’s memory mapping relies on the SDRAM addresses not changing.” Pet. 50 (citing Ex. 1008 ¶¶ 50–52, 62, 100, 107, Figs. 2, 15; Ex. 1003 ¶¶ 251–252). In particular, Dr. Levy testifies that “the system relies on the user data being at a particular SDRAM addresses, which have corresponding flash logical addresses. The user data must be written back, and read from, these same addresses or the correspondence would fail.” Ex. 1003 ¶ 251.

Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.G.

- i) [1.H]: “write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read.”

Petitioner asserts that Tsunoda combined with Kolokowsky teaches this limitation. Pet. 50–52. Specifically, Petitioner contends that Tsunoda discloses “‘writ[ing] the digital information stored in the volatile memory back to the nonvolatile memory’ when, e.g., changes are made to the user data (‘the digital information’) and the device is powered down.” *Id.* at 51 (citing Ex. 1008 ¶¶ 85, 86, 99, 100). Petitioner further contends that “the user data is written back to the ‘same associated address from which it was read,’ i.e., the logical address of the flash memory” because “there is a correspondence between the SDRAM addresses and flash logical addresses, and the user data is read from, and written to, the same corresponding flash logical addresses.” *Id.* (citing Ex. 1008 ¶¶ 50–52, 62, 100, 107). Petitioner contends “the user data in the SRAM is mirrored in the same range of flash logical address space.” *Id.* (citing Ex. 1008 ¶¶ 73, 74, 125–127).

Petitioner argues that, for the same reasons as discussed above with respect to limitation 1.B, a person of ordinary skill in the art would have been motivated “in view of Kolokowsky . . . to write the data to a ‘different physical location,’ e.g., different block, and update the same translation table so that the ‘same associated address’ becomes associated with the different physical block (i.e., the logical address is re-mapped to a new physical block).” *Id.* at 51–52 (citing Ex. 1003 ¶ 256).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence,

that Tsunoda and Kolokowsky teaches limitation 1.H and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

4. Analysis of Claims 2, 3, 5, 6, 9, and 11–16

Petitioner contends the combination of Tsunoda and Kolokowsky teaches the limitations in claims 2, 3, 5, 6, 9, and 11–16. Pet. 52–62. Patent Owner does not respond to these arguments. See PO Resp. 34. We agree with and adopt Petitioner’s arguments. Based on our review and consideration of the current record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda and Kolokowsky teach or suggest the limitations in claims 2, 3, 5, 6, 9, and 11–16.

5. Conclusion

Having considered the *Graham* factors, including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the challenged claims, we are persuaded, based on the current record, that Petitioner has shown, by a preponderance of the evidence, that claims 1–3, 5, 6, 9, and 11–16 would have been obvious over Tsunoda and Kolokowsky.

F. Grounds 3 and 5: Obviousness Over Lee and Li; Obviousness Over Tsunoda, Kolokowsky, and Li

Petitioner contends claim 4 would have been obvious over the combination of Lee and Li or Tsunoda, Kolokowsky, and Li. Pet. 62–65. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 4 is unpatentable over the combination of Lee and Li or Tsunoda, Kolokowsky, and Li.

1. Li (Ex. 1010)

Li is titled “Multilevel Phase-Change Memory Element and Operating Method” and describes a multilevel phase change memory element and operating method and electrodes, which are configured in a parallel structure to form a memory cell, the multilevel phase change memory element having more bits and higher capacity than that of a memory element with a single phase-change layer. Ex. 1010 at codes (54), (57). Li employs a voltage-drive mode to control and drive the memory element such that multilevel memory states may be achieved by imposing different voltage levels. *Id.*

2. Analysis of Claim 4

Claim 4 recites “The nonvolatile memory system of claim 2 wherein the nonvolatile memory for storage is a phase change memory.” Ex. 1001, 5:28–29.

Petitioner contends that Li teaches a phase change memory and provides reasoning, supported by testimony from Dr. Levy, to combine Lee or Tsunoda and Kolokowsky with Li and asserts that a person of ordinary skill in the art would have had a high expectation of success in implementing Li’s phase change memory in Lee or Tsunoda and Kolokowsky. Pet. 62–65 (citing Ex. 1010, code (54), 1:37–46 (“phase change memory”), 1:16–46; Ex. 1003 ¶¶ 301–303, 311–314; Ex. 1007 ¶ 61; Ex. 1008 ¶ 94; 1022 ¶ 5). Patent Owner does not respond to these arguments. *See* PO Resp. 35.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee and Li, or Tsunoda, Kolokowsky, and Li teach the limitations in claim 4 and that a person of ordinary skill in the art would have had a reason

to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

G. Grounds 4 and 6: Obviousness Over Lee and Miura; Obviousness Over Tsunoda, Kolokowsky and Miura

Petitioner contends claim 8 would have been obvious over the combination of Lee and Miura or Tsunoda, Kolokowsky, and Miura. Pet. 63, 66, 67. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 8 is unpatentable over the combination of Lee and Miura or Tsunoda, Kolokowsky, and Miura.

1. Miura (Ex. 1011)

Miura is titled “Memory Module, Memory System, and Information Device” and “relates to a memory system including a dynamic random access memory (DRAM) and a method of controlling the memory system.” Ex. 1011, code (54), ¶ 1.

Miura’s memory system includes large-capacity ROM and RAM in which high-speed reading and writing are enabled. *Id.* at code (57). Miura discloses a “memory system including a non-volatile memory (CHIP1), DRAM (CHIP3), a control circuit (CHIP2) and an information processing device (CHIP4),” with data in FLASH being transferred to SRAM or DRAM in advance to speed up, the data transfer between the non-volatile memory (FLASH) and DRAM (CHIP3) being performed in the background. *Id.* Miura explains “[a]s data in FLASH can be read at the similar speed to that of DRAM by securing a region in which the data in FLASH can be copied in DRAM and transferring the data to DRAM in advance

immediately after power is turned on or by a load instruction, the performance and the function of a mobile device can be enhanced.” *Id.*

2. *Analysis of Claim 8*

Claim 8 recites “The nonvolatile memory system of claim 2 wherein the volatile random access memory is a SRAM with at least one port for read and write access.” Ex. 1001, 6:5–7.

Petitioner contends that Miura teaches SRAM with at least one port for read and write access, and provides reasoning, supported by testimony from Dr. Levy, to combine Lee or Tsunoda and Kolokowsky with Miura, and argues that a person of ordinary skill in the art would have had a high expectation of success in employing Miura’s SRAM in place of Lee’s or Tsunoda’s SDRAM. Pet. 63, 66, 67 (citing Ex. 1011, code (54), ¶ 57 (“SRAM”), ¶ 59 (“SRAM interface” is a port for access); Ex. 1003 ¶¶ 306–308, 317–319; Ex. 1007 ¶ 61; Ex. 1008 ¶ 94; Ex. 1023, 1:36–60). Patent Owner does not specifically respond to these arguments. *See* PO Resp. 35.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee and Miura, or Tsunoda, Kolokowsky, and Miura teach the limitations in claim 8 and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success

IV. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner established by a preponderance of the evidence that claims 1–6 and 8–16 of the ’184 patent are unpatentable.

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–3, 9–16	103(a)	Lee	1–3, 9–16	
1–3, 5, 6, 9, 11–16	103(a)	Tsunoda, Kolokowsky	1–3, 5, 6, 9, 11–16	
4	103(a)	Lee, Li	4	
8	103(a)	Lee, Miura	8	
5	103(a)	Tsunoda, Kolokowsky, Li	4	
6	103(a)	Tsunoda, Kolokowsky, Miura	8	
Overall Outcome			1–6, 8–16	

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–6 and 8–16 of the '184 patent have been shown to be unpatentable under 35 U.S.C. § 103(a); and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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