

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

FLASH-CONTROL, LLC,
Patent Owner.

IPR2020-01710
Patent 9,792,219 B2

Before KARA L. SZPONDOWSKI, JULIA HEANEY, and
JON M. JURGOVAN, *Administrative Patent Judges*.

HEANEY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–5 and 7–13 of U.S. Patent No. 9,792,219 B2 (Ex. 1004, “the ’219 patent”). Paper 1 (“Petition” or “Pet.”). Flash-Control, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). Taking into account the arguments presented in Patent Owner’s Preliminary Response, we determined the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–5 and 7–13 of the ’219 patent, and we instituted this *inter partes* review as to all challenged claims. Paper 8 (“Dec.”).

During the course of trial, Patent Owner filed a Patent Owner Response (Paper 12, “PO Resp.”); Petitioner filed a Reply to the Patent Owner Response (Paper 14, “Pet. Reply”); Patent Owner filed a Sur-reply (Paper 15, “PO Sur-reply”). An oral hearing was held on February 8, 2022, and a transcript of the hearing is included in the record. Paper 24 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–5 and 7–13 of the ’219 patent. For the reasons discussed below, we hold that Petitioner has established by a preponderance of the evidence that all of the challenged claims are unpatentable.

A. *Related Proceedings*

The parties identify the following litigation as related matters: *Flash-Control, LLC v. Micron Technology, Inc.*, Case No. 6:20-cv-00361 (W.D. Tex.) (asserting the ’219 patent, U.S. Patent No. 9,257,184 (“the ’184 patent”), U.S. Patent No. 8,531,880 (“the ’880 patent”), and U.S. Patent No.

8,817,537 (“the ’537 patent”)); *Flash-Control, LLC v. Intel Corp.*, Case No. 6:20-cv-00360 (W.D. Tex.) (asserting the ’219 patent and the ’184 patent); *Flash-Control, LLC v. Intel Corp.*, Case No. 1:19-cv-01107 (W.D. Tex.) (asserting the ’880 patent and the ’537 patent); *Si-Flash Drives, LLC v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-02004 (C.D. Cal.) (asserting U.S. Patent No. 7,855,916 (“the ’916 patent”) and U.S. Patent No. 8,194,452 (“the ’452 patent”)); and *Si-Flash Drives, LLC v. Adata Tech. (U.S.A.) Co., Ltd.*, Case No. 8:16-cv-02005 (C.D. Cal.) (asserting the ’916 patent and the ’452 patent). Pet. 4–5; Paper 3, 2.

The parties also identify the following related IPR petitions: *Micron Technology, Inc. v. Flash-Control, LLC*, IPR2020-01709, which was filed concurrently and challenges the ’184 patent; *Adata Tech. (USA) Co., Ltd. et al. v. Si-Flash Drives, LLC et al.*, IPR2018-00194, challenging the ’452 patent; and *Adata Tech. (USA) Co., Ltd. et al. v. Si-Flash Drives, LLC et al.*, IPR2018-00193, challenging the ’916 patent. Pet. 4–5; Paper 3.

B. The ’219 Patent (Ex. 1004)

The ’219 patent, titled “Nonvolatile Memory Systems with Embedded Fast Read and Write Memories,” describes a “nonvolatile memory system . . . with novel architecture coupling nonvolatile storage memory with random access volatile memory” and “[n]ew commands [that] are included to enhance the read and write performance of the memory system.” Ex. 1004, codes (54), (57).¹ The ’219 patent explains that “[n]onvolatile memory systems, subsystems and integrated circuits . . . used in multiple consumer, computer and communications applications . . . can be a NAND

¹ Throughout this Decision, we may refer to nonvolatile memory as “NVM,” and volatile memory as “VM.”

flash memory IC or NOR flash memory,” while “[p]art of the memory system may contain volatile memory like static random access memory (SRAM) or dynamic random access memory (DRAM).” *Id.* at 1:38–44. The ’219 patent further explains that “the ‘page buffered architecture’ of today’s NAND flash memory does not lend itself to true, fast, read, and write memory access,” and is “slow compared to volatile memory systems built with SRAMs and DRAMs.” *Id.* at 1:57–58, 1:67–2:2. Accordingly, the ’219 patent “focuses on ways to modify the already existing ‘buffers’ in an optimal manner to enhance the random access performance of nonvolatile IC, subsystem, and system.” *Id.* at 2:7–10. The ’219 patent describes a preferred embodiment where the volatile random access memory provides “independent accessible access (read, write etc) at a fine grain level of a bit, or byte.” *Id.* at 2:11–14.

The ’219 patent further explains that “[t]his invention provides every page of each NVM block as an independently accessible random access memory to perform load/store applications, as well as a coupled memory to the assigned NVM block.” *Id.* at 2:37–40. The ’219 patent further explains that each NVM NAND flash may have 1,024 such blocks, each block typically 64 kilobytes in density, page for each block being 1 to 2 kilobytes, each bit being independently addressable in a random manner, as well as accessed in a random manner. *Id.* at 2:40–44. The ’219 patent further describes “[a]nother preferred embodiment [that] selects any of the currently unused blocks and uses the SRAM pages in those blocks to perform other operations as necessary” where the data manipulating operations can be arithmetic and/or logic operations; and “another preferred embodiment, [in

which] the ‘volatile memory of a page’ is a DRAM . . . independently accessible and addressable in a random manner.” *Id.* at 2:47–54.

The ’219 patent describes a preferred embodiment including

New commands with these inventions: Read page as SRAM/RAM, Write page as SRAM/RAM, Read/Modify/W Write page as SRAM/RAM, Read byte out of a page, etc; Write byte out of a page etc. Nibble mode/Serial access/double data rate are all possible.

Id. at 4:59–67.

Figure 9 of the ’219 patent, reproduced below, “shows how the invention of this patent distinguishes itself from today’s nonvolatile memory.” *Id.* at 3:10–11.

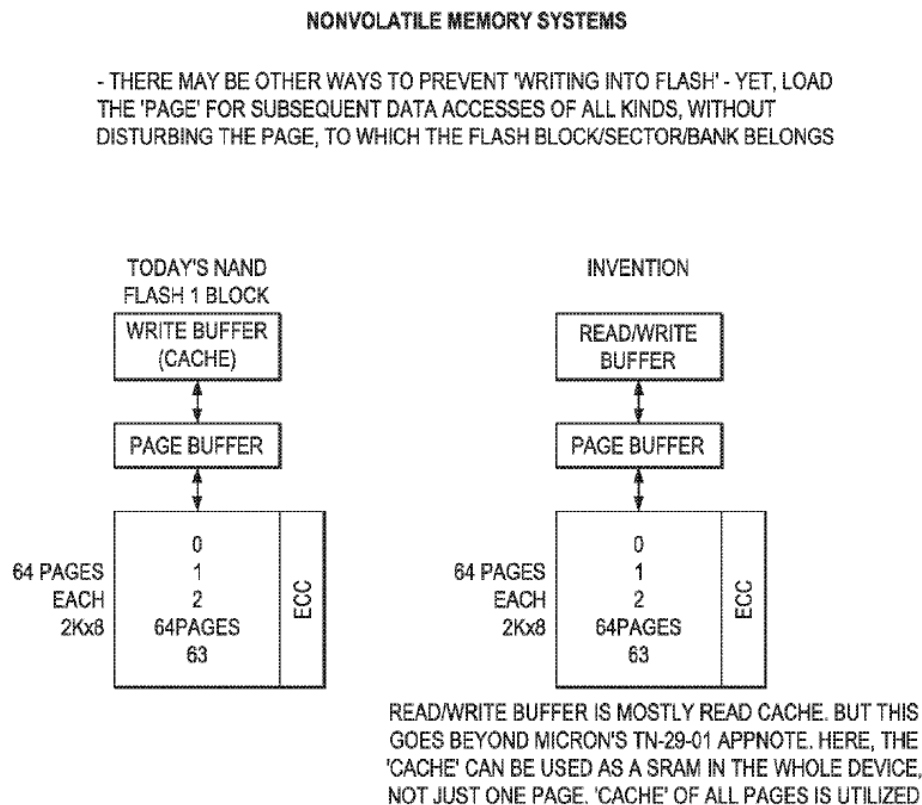


FIG. 9

Figure 9 depicts “Today’s NAND Flash 1 Block,” which is a block diagram including Write Buffer (Cache), and Page Buffer and 64 pages each 2Kx8. Figure 9 further depicts “Invention,” which is a block diagram including Read/Write Buffer, and Page Buffer 64 pages each 2Kx8. Figure 9 describes that “Read/Write Buffer is mostly read cache . . . [and] the ‘cache’ can be used as SRAM in the whole device, not just one page. ‘Cache’ of all pages is utilized.”

Figure 12 of the ’219 patent, reproduced below, shows a high level architecture of the nonvolatile memory system (“NVMS”) of the invention which comprises both nonvolatile and volatile memory. *Id.* at 3:18–20.

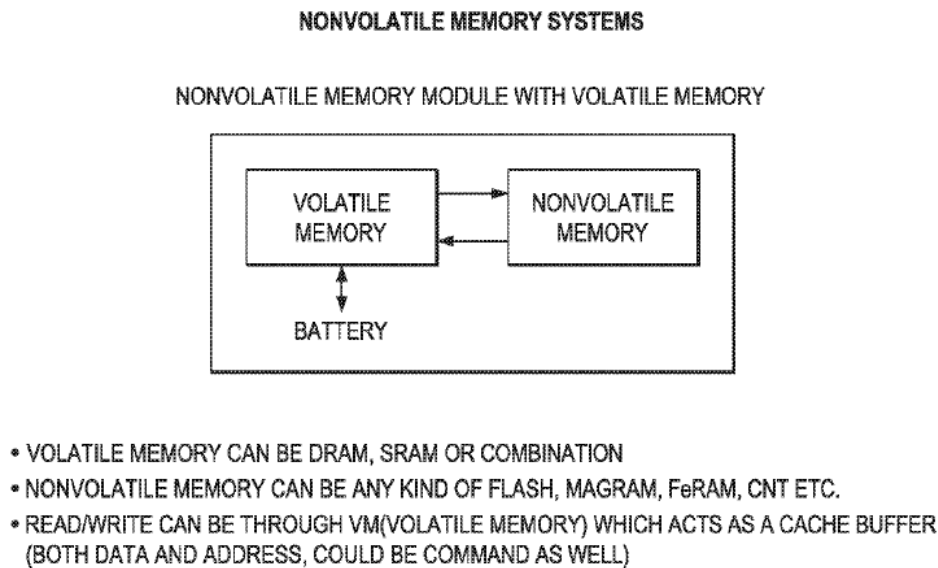


FIG. 12

Figure 12 depicts nonvolatile and volatile memory, where “volatile memory can be DRAM, SRAM or combination” and nonvolatile memory can be “any kind of flash, MagRAM, FeRAM, CNT etc.” Figure 12 further describes that “Read/write can be through VM(volatile memory) which acts as a cache buffer (both data and address, could be command as well).”

C. The Challenged Claims

Petitioner challenges claims 1–5 and 7–13 of the '219 patent. Pet. 1. Claims 2–5 and 7–13 depend from claim 1. Claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the subject matter of the challenged claims:

1. [1.PRE] A nonvolatile memory system comprising:
 - [1.A] a nonvolatile memory for storage of digital information arranged in multiple blocks for access;
 - [1.B] a volatile random access memory for read and write operations coupled to said nonvolatile memory;
 - [1.C] wherein the volatile random access memory and nonvolatile memory are controlled by one or more controllers;
 - [1.D] wherein the nonvolatile memory system is coupled to a central processing unit;
 - [1.E] wherein each block of the nonvolatile memory for storage has one or more pages of stored data accessible through the coupled volatile random access memory; and
 - [1.F] wherein each page of a block is adapted to be substituted on the fly for any other page of a different block through address mapping;
 - [1.G] wherein the one or more controllers control the volatile and nonvolatile memories to:
 - [1.H] perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location,
 - [1.I] perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory,
 - [1.J] perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein, and

[1.K] write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read.

Ex. 1004, 5:28–6:14.

D. Instituted Grounds of Unpatentability

We instituted trial to determine whether the challenged claims are unpatentable based on the following grounds:

Ground	Challenged Claim(s)	35 U.S.C. ²	Reference(s)/Basis ³
1	1, 2, 8–13	§ 103(a)	Lee ⁴
2	1, 2, 4, 5, 8, 10–13	§ 103(a)	Tsunoda ⁵ and Kolokowsky ⁶

² The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the ’219 patent claims priority from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

³ In each of Petitioner’s grounds, Petitioner separately references the knowledge of a person of ordinary skill in the art. When analyzing whether claims would have been obvious and whether it would have been obvious to modify prior art, it is always from the perspective of an ordinarily skilled artisan and one must consider knowledge generally available to one of ordinary skill in the art. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (one considers “the background knowledge possessed by a person having ordinary skill in the art”). The “knowledge of a person of ordinary skill in the art” is, therefore, always a consideration and is not a separate basis in an obviousness challenge. Therefore, we do not separately analyze the “knowledge of a person of ordinary skill in the art” and consider obviousness over the cited prior art from the perspective of the ordinarily skilled artisan.

⁴ US Patent Application Publication No. 2006/0053246 A1 to Lee, published March 9, 2006 (Ex. 1007).

⁵ US Patent Application Publication No. 2003/0028733 A1 to Tsunoda et al., published February 6, 2003 (Ex. 1008).

⁶ US Patent No. 7,853,749 B2 to Kolokowsky, issued December 14, 2010 (Ex. 1009).

Ground	Challenged Claim(s)	35 U.S.C. ²	Reference(s)/Basis ³
3	3	§ 103(a)	Lee and Li ⁷
4	7	§ 103(a)	Lee and Miura ⁸
5	3	§ 103(a)	Tsunoda, Kolokowsky, and Li
6	7	§ 103(a)	Tsunoda, Kolokowsky, and Miura

Pet. 7–8.

Petitioner relies on the Declarations of John Levy, Ph.D. (Exs. 1006, 1036). Patent Owner relies on the Declarations of Nader Bagherzaderh, Ph.D. (Exs. 2001, 2004).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of workers active in the field.” *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.*

Petitioner argues a person of ordinary skill in the art at the time of the invention

⁷ US Patent No. 7,254,059 B2 to Li et al., issued August 7, 2007 (Ex. 1010).

⁸ US Patent Application Publication No. 2006/0041711 A1 to Miura et al., published February 23, 2006 (Ex. 1011).

would have had at least a bachelor's degree in computer engineering, electrical engineering, computer science, or a similar discipline, along with 2 years of experience in the design, operation, or control of semiconductor memory devices. A more advanced degree can substitute for work experience. This POSA would be aware of and generally knowledgeable about the structure and operation of different types of memories.

Pet. 19 (citing Ex. 1006 ¶¶ 43–46). Patent Owner states that, “[f]or purposes of this proceeding, Flash-Control agrees with Petitioner’s definition of a POSA.” PO Resp. 8.

We find that Petitioner’s proposal is consistent with the level of ordinary skill in the art reflected by the ’219 patent and the asserted prior art, and therefore, adopt Petitioner’s definition of the level of ordinary skill in the art.

B. Claim Construction

1. Legal Standards

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b) (2020). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean*

Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

“It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004). “Attending to this principle, a claim construction analysis must begin and remain centered on the claim language itself, for that is the language the patentee has chosen to particularly point[] out and distinctly claim[] the subject matter which the patentee regards as his invention.” *Id.* at 1116 (citing *Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001)). “[A] court looks to those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean. Those sources include the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Id.* “The written description provides a context for the claims, and is appropriately resorted to ‘for the purpose of better understanding the meaning of a claim.’” *Id.* (citing *White v. Dunbar*, 119 U.S. 47, 51 (1886)).

2. Claim Limitations

“on the fly” (Claim 1, [1.F])

In the Institution Decision, we determined “on the fly” should be construed to mean “doing a task or process as needed without suspending or disturbing normal operations.” Dec. 11. Taking into account Petitioner’s reliance on the definition in the Microsoft Computer Dictionary (5th ed. 2002) and a previous Board panel’s adoption of that definition (Pet. 16–17

(citing Ex. 1012; Ex. 1013 at 5–9)), we adopted Petitioner’s proposed construction.

The parties have not further addressed the construction of this term. *See generally* PO Resp., Pet. Reply, PO Sur-Reply. Accordingly, we maintain the same construction that we set forth in the Institution Decision.

“any portion or all of the stored digital information in the volatile memory” (Claim 1, [1.I])

“any portion of the accessed read digital information” (Claim 1, [1.J])

In the Institution Decision, we determined “any portion” should be construed to at least include accessibility at the bit and/or byte level. Dec. 10. Based upon the disclosure in the Specification, we construed this limitation to include access of the stored retrieved digital information at the bit or byte level. *Id.*

Patent Owner “agrees with the Board’s interpretation of this limitation.” PO Resp. 18. Petitioner does not further address construction of this term. *See generally* Pet. Reply. Accordingly, we maintain the same construction that we set forth in the Institution Decision.

“wherein the one or more controllers control the volatile and nonvolatile memories to: ...” (Claim 1, [1.G])

“perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein” (Claim 1, [1.J])

Patent Owner argues a person of ordinary skill in the art would have understood limitations 1.G and 1.J to require a read/write/modify operation “resulting in information being (1) *read out of nonvolatile memory so that it*

may be modified, (2) modification thereof, and (3) writing back of that read and now modified information back to nonvolatile memory.” PO Resp. 20. Patent Owner provides the following chart setting forth its proposed construction for limitations 1.G and 1.J of claim 1:

Claim Language	Patent Owner’s Construction
[1.G] wherein the one or more controllers control the volatile and nonvolatile memories to: . . .	[1.G] wherein the one or more controllers control the volatile and nonvolatile memories to <i>perform a read/modify/write operation by performing the following:</i>
[1.J] perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein	[1.J] perform <i>a modify operation by performing a write operation</i> on any portion [i.e., the read bit or byte] of the

PO Resp. 23–24 (emphasis added by Patent Owner).

Patent Owner argues that limitation 1.J describes a data modification step because “[w]riting data to the same location in volatile memory by definition modifies the data at that location.” *Id.* at 21 (citing Ex. 2004, 59). Patent Owner also relies on Dr. Levy’s deposition testimony that a person of ordinary skill in the art would understand limitation 1.J “to suggest that that which is written is not the same data that was read in the previous step.” *Id.* at 22 (citing Ex. 2005, 96:1–18).

Petitioner argues that no express construction of limitations 1.G and 1.J⁹ is necessary. Pet. Reply 5. Petitioner contends that Patent Owner is (1) attempting to rewrite the controller limitation 1.G into performing a “read/modify/write operation”; (2) rewrite the write operation limitation into a limitation that performs some unknown “modify operation”; and (3) “interject extraneous limitations into both limitations.” *Id.*

The parties agree that this issue is dispositive. PO Resp. 5 (“The correct construction of the claims in this proceeding is dispositive”); PO Sur-reply 1. At the hearing, Patent Owner’s counsel stated “for purposes of these two proceedings [IPR2020-01709 and IPR2020-01710] we’re only relying on our claim construction argument.” Tr. 44:20–22. Petitioner’s counsel stated “There has been no dispute that the prior art doesn’t disclose controllers So the Board simply needs to reject Patent Owner’s construction to resolve the disputes.” Tr. 30:22–31:1; *see also* 7:14–16 (“it is true that the prior art does not disclose something called a Read/Modify/Write operation”). We address the parties’ arguments as to construction of limitations 1.G and 1.J below.

a) Analysis

We decline to adopt Patent Owner’s proposed construction as it departs from the plain language of limitations 1.G and 1.J in a manner that, in effect, impermissibly rewrites the claim. *See Nike Inc. v. Wolverine World Wide, Inc.*, 43 F.3d 644, 647 (Fed. Cir. 1994) (rejecting the patentee’s proposed claim construction that would, “in effect, rewrite its patent claims

⁹ Petitioner refers to limitation 1.G as the “controller limitation” and limitation 1.J as the “write operation limitation.” Petitioner refers to limitations 1.H–1.K as the “four controller operations” of claim 1. Reply 3.

to suit its needs in this litigation”); *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) (“Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee.”).

Although Patent Owner contends that claim 1 “requires a read/modify/write operation” (PO Resp. 19; *see also* PO Sur-reply 4), claim 1’s controller operations 1.H–1.K do not recite a read/write/modify operation, much less that “each of these steps is performed in order and without interruption.” PO Sur-reply 6. Patent Owner argues the proposed construction “is not a rewriting of the claim. The language of claim 1 demonstrates that it already includes the read/modify/write operation.” *Id.* at 5. But whether the scope of the claim *includes* a read/modify/write operation (*see* PO Sur-reply 4–5) is beside the point; Patent Owner is attempting to narrow claim 1 to *require* a read/modify/write operation.¹⁰ In other words, we disagree with Patent Owner that “the scope of claim 1 is unchanged by the clarification that the configurable steps recited in claim 1 are the steps of an atomic read/modify/write.” *Id.* at 15.

Patent Owner’s argument that claim 1 requires a read/modify/write operation is not persuasive because it does not adequately explain why the controller of claim 1 *must* be configured to control a read/modify/write operation. *See* Sur-reply 5–6 (citing Ex. 2004 ¶¶ 50, 59). Patent Owner’s argument that three of claim 1’s four controller operations (1.H–1.K) correspond to a read/modify/write essentially ignores step 1.I, which

¹⁰ Claim 1 uses the transitional term “comprising,” “which is well understood in patent law to mean ‘including but not limited to.’” *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009); *see* Reply 13.

involves reading data out of VM, and Dr. Bagherzadeh's deposition testimony that reading data out of VM is unnecessary for a read/modify/write operation contradicts Patent Owner's argument. *See* PO Resp. 26–28; Ex. 1034, 8:23–9:6, 11:8–17 (admitting read/modify/write operation directly overwrites data in VM without any read of VM). Similarly, Dr. Bagherzadeh's testimony that claim 1 “recites being able to read out data, modify it in VM, and read it back to the NVM” (Sur-reply 4, citing Ex. 2004 ¶ 58) is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *see also Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997) (nothing requires a fact finder to credit the inadequately explained testimony of an expert).

Patent Owner's argument that limitations 1.G and 1.J should be construed to require a read/write/modify operation is based on its assertion that a person of ordinary skill in the art would have understood that a read/modify/write is an atomic operation, i.e., “there is no ‘gap’ between the three distinct steps that are included in a read/modify/write operation that allows for intermediate or unrelated actions to occur.” PO Resp. 31.¹¹ *See* PO Sur-reply 6–7; PO Resp. 34–35 (citing Ex. 2004 ¶¶ 67–68); *see id.* at 27 (citing Ex. 2004 ¶ 63) (“a read/modify/write operation must maintain its sequential integrity without any interference from outside sources (other

¹¹ Patent Owner contends that “[a]n operation acting on shared memory is ‘atomic’ if it completes in a single linear defined sequence of steps. (Ex. 2004 at 65.) ‘Atomic’ is a term of art in this field that a POSA would have understood. (Ex. 2004 at 65).” PO Resp. 31 n. 3.

processors, interrupts, and exceptions); otherwise, during the read/modify/write operation there could be unintended consequences that would jeopardize the proper operation of the processor and the program execution.”). This appears to be undisputed. *See, e.g.*, Ex. 1036 ¶ 31 (Dr. Levy testifying that “a read/modify/write operation would require a unitary operation that involves automatically updating the NVM”); Ex. 2004 ¶ 66 (Dr. Bagherzaderh testifying that “an example of an atomic operation is a read-modify-write or operation of one requires that the read and the modification and the write occur as the unitary operation where no other operation can occur during that interval.”). Therefore, central to this claim construction dispute is whether it is appropriate to construe limitations 1.G and 1.J as requiring an atomic read/modify/write operation.

We find that the language of claim 1 does not support an atomic read/modify/write operation, for several persuasive reasons argued by Petitioner. Specifically, although claim 1 recites “operation” or “operations” four times (limitations 1.B, 1.H, 1.I, and 1.J), the controller limitation 1.G does not refer to an “operation.” *See* Pet. Reply 12; *see Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007) (when “the specification . . . suggests that the patentees knew how to” use a particular term to restrict claim coverage, use of different term in the claims must have meaning). Similarly, limitation 1.J does not recite “modify,” nor does any other limitation in claim 1. Further, Patent Owner’s reliance on Dr. Levy’s deposition testimony concerning limitation 1.J (*see* PO Resp. 22, 30–31 (citing Ex. 2005, 96:1–18)) is not persuasive because that testimony did not address whether limitation 1.J would describe a “modify” as part of an

atomic operation. In other words, the occurrence of a data modification step does not necessarily imply a read/modify/write operation.

As to the four “operations” recited in limitations 1.H–1.K, nothing in the claim language indicates that those four operations are part of a three-part, atomic read/modify/write operation. In view of Patent Owner’s position that a read/modify/write operation is a three-step atomic operation, its failure to account for the four operations of limitations 1.H–1.K undercuts its position. Further, we credit Dr. Levy’s testimony that read operation limitation 1.I, which involves reading data out of VM, is not part of a read/modify/write operation, which directly overwrites (i.e. modifies) data in the VM. *See* Ex. 1036 ¶¶ 24–25. Dr. Bagherzadeh also agreed that a read/modify/write operation directly overwrites data in VM without any read of the VM. Ex. 1034, 8:23–9:6, 11:8–17.

Patent Owner’s argument that limitation 1.F’s recitation of “on the fly” supports construing claim 1 to require an atomic read/modify/write operation also is not persuasive. *See* PO Resp. 23; PO Sur-reply 9. As discussed *supra*, we have construed “on the fly” to mean “doing a task or process as needed without suspending or disturbing normal operations.” Patent Owner does not dispute that construction. Claim 1’s description of operating “on the fly” in limitation 1.F, however, would contradict an atomic read/modify/write operation that suspends normal operation in order to prevent other programs from writing to a location in VM. *See* Ex. 2004 ¶¶ 66–68.

Thus, we agree with Petitioner that Patent Owner’s construction rewrites “the controller limitation [1.G] into one that performs a 3-step operation without intermediary steps—even though the limitation does not

recite any operation,” and rewrites the write operation limitation 1.J to perform an unrecited modify operation. *See* Reply 7.

Nor do we find that the Specification supports Patent Owner’s position. The Specification is devoid of any description of a “read/write/modify operation” as advanced by Patent Owner in its proposed construction. Patent Owner’s argument that “[t]he specification also discloses that allowing for the *performance of a read/modify/write operation* in nonvolatile memory, using coupled volatile memory, *is an important aspect of the invention*,” (PO Resp. 25, emphases added) lacks support. For example, we note that in describing the ’219 patent’s teaching, Dr. Bagherzadeh testifies that “[t]he ’219 patent is directed to novel systems and method coupling VM and NVM to improve performance by, *inter alia*, enhancing the random access performance of NVM systems allowing access at a more flexible and granular level than prior memory systems.” Ex. 2004 ¶ 41. This testimony says nothing about the “importance” of “performance of a read/modify/write operation involving nonvolatile memory using coupled volatile memory.” *See* Ex. 1004, code (57) (Abstr.), 1:59–66.

Patent Owner relies on the “new commands” described in the Abstract and Brief Summary of the Invention. PO Resp. 25 (citing Ex. 1004 at Abstract). The pertinent Summary section of the ’219 patent states:

The preferred embodiment ***adds new commands*** to be executed in the Command Register ***of the NVM (nonvolatile memory)***. In other embodiments, these commands can be shared between the NVM IC and memory controller. ***Prior art NVM IC's have limited commands*** like (1) read page in flash; (2) erase block in flash; (3) program page in flash, etc. ***With this invention, new additional commands are executed***: (4) read page in the SRAM of the block only; (5) ***read new page from*** the nonvolatile memory (***NVM***) block; (6) ***write page into SRAM of the block***,

but, not program into the NVM block until such a command is additionally given.

PO Resp. 25–26 (citing Ex. 1004, 2:26–36) (emphasis added by Patent Owner). According to Patent Owner, this passage supports that “[i]ncluded among these new commands are an instruction to read a new page from the nonvolatile memory (NVM) block and write (*e.g.*, modify) the page into the portion of volatile memory (SRAM) coupled to the nonvolatile memory (NVM block) but not program (write) this page back into the NVM block unless this additional instruction is given. *Id.* We note that this portion of the Specification does not mention a new read/modify/write operation (or command). At most, this portion of the Specification describes three “new additional commands,” (4), (5), and (6). *See* Pet. Reply 19 (arguing that the “allegedly new commands” identified in the Specification refer to “singular operations that read or write to the VM,” and “not a singular read/modify/write command or operation.”); Ex. 1036 ¶¶ 30–31.

The Specification provides additional description of the new commands: “[*n*]ew commands with these inventions: Read page as SRAM/RAM, Write page as SRAM/RAM, ***Read/Modify/W Write*** [*sic*] page as SRAM/RAM, Read byte out of a page, etc; Write byte out of a page etc.” Ex. 1004, 4:63–65 (cited at PO Resp. 26, emphasis added by Patent Owner). This is the only place in the Specification where a “read/modify/write” command is described, and this is the full extent of the description. As Petitioner points out, this “refers to writing the data ‘as SRAM/RAM,’ not writing the data to NVM,” “which [limitation 1.B] clearly states.” Pet. Reply 20 (Ex. 1036 ¶ 33). Petitioner’s expert, Dr. Levy, testifies that “on the face of it[,] it’s clearly associated with SRAM or RAM; in other words,

volatile memory.” Ex. 2005, 102:4–6. Patent Owner contends this is “wrong” because (1) “the modifier ‘as SRAM/RAM’ [is used] to indicate *how* the operation will be performed, *i.e.*, *as though* it were being performed in volatile memory”; and (2) “Dr. Levy admits that claim 1’s recited step of writing the data back to the same location in volatile memory [indicates there is] a modification.” PO Resp. 30–31. We are not persuaded by these arguments as they do not address the language in limitations 1.G and 1.J, or explain how this disclosure supports Patent Owner’s proposed construction. Dr. Levy’s testimony as to this disclosure is unrebutted, and, given the absence of any further description of this command in the Specification, we find credible Dr. Levy’s testimony that “‘Read/Modify/W Write page as SRAM/RAM’ not only say[s] nothing about updating the NVM, ‘Read/Modify/W Write page as SRAM/RAM’ also says nothing about a requirement that the update be to a different physical address.” Ex. 1036 ¶ 33.

Patent Owner also relies on the Specification’s statement that “To write to a page or pseudo page, WRITE command and immediately PROGRAM SUSPEND to invalidate writing to the NVM. The data should be in page/pseudo page.” PO Resp. 34 (citing Ex. 1004, 5:11–14). According to Patent Owner, because “the write command requires preventing other programs from writing to that location in NVM,” [t]his indicates the read, the modification, and the write occur as a unitary operation without interruption.” *Id.* The Specification does not further describe the PROGRAM SUSPEND operation. Dr. Levy provides unrebutted testimony, however, explaining why a “suspend” is different

from a read/modify/write operation. *See* Ex. 1036, ¶ 35. We find Dr. Levy’s testimony persuasive as to this point.

For the foregoing reasons, we decline to adopt Patent Owner’s proposed construction of limitations 1.G and 1.J. We agree with Petitioner that no express construction of these limitations is necessary to resolve the issues in dispute.

C. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *see KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”).

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 417. Reaching this conclusion, however, requires more than merely showing that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.” *Id.*

*D. Ground 1: Obviousness Based on Lee*¹²

Petitioner argues that claims 1, 2, and 8–13 would have been obvious over Lee. Pet. 25–44. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, and 8–13 are unpatentable over Lee.

1. Lee (Ex. 1007)

Lee is titled “Systems and Methods for Providing Nonvolatile Memory Management in Wireless Phones” and relates “to methods and systems for accessing and managing nonvolatile memory, such as in a wireless phone.” Ex. 1007, code (54) (Title), ¶ 4. Lee discloses a “wireless phone memory controller . . . that[] comprises a first interface circuit configured to be coupled to wireless phone nonvolatile memory, a second interface circuit configured to be coupled to wireless phone volatile memory,” “a first processor interface configured to be coupled to a first

¹² As set forth in Section II.B, the parties agree that claim construction of limitations 1.G and 1.J is dispositive of this proceeding. However, in the interest of completeness and providing a full record, we address Petitioner’s grounds.

wireless phone processor . . . [and] configured to provide the first processor with access to the wireless phone volatile memory,” “a second processor interface configured to be coupled to a second wireless phone processor,” and “a controller circuit configured to copy at least a portion of wireless phone nonvolatile memory data to the wireless phone volatile memory.” *Id.*, code (57) (Abstr.). Lee’s Figure 2, reproduced below, is a block diagram of a wireless phone including a memory system. *Id.* ¶¶ 24, 77.

FIG. 2

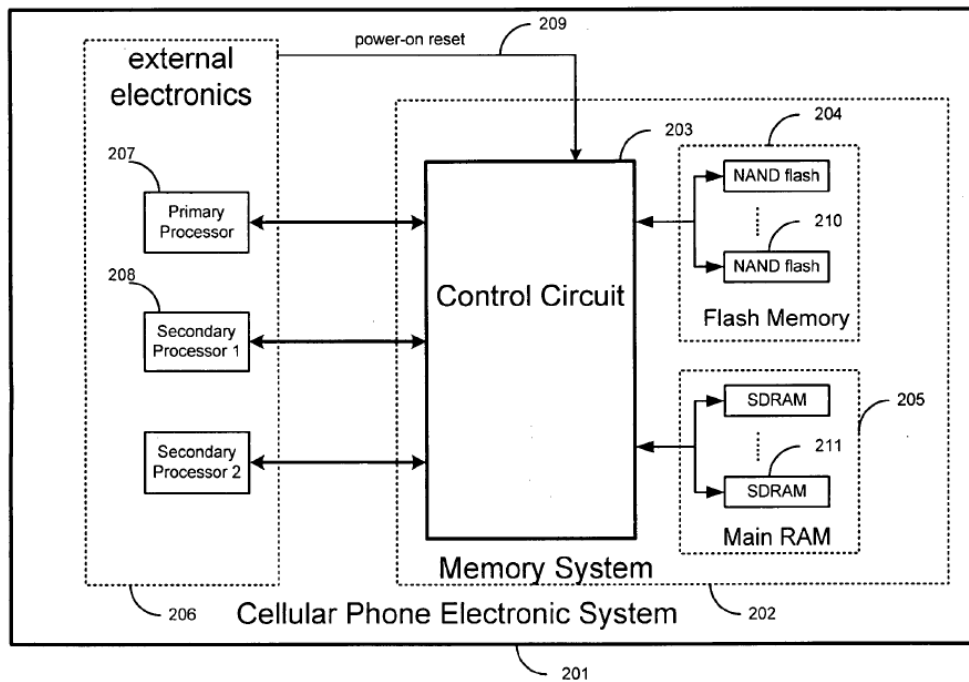


Figure 2 is a block diagram depicting Memory System 202 included in an electronic system of a wireless, cellular phone 201 that also includes other electronic portions (external electronics 206 including external processors 207, 208). *Id.* ¶ 77. Memory System 202 includes Flash Memory 204 and Main RAM 205, connected to Control Circuit 203. *Id.* ¶ 78. Control Circuit 203 provides (i) control signals to interface with and operate Flash Memory 204, and (ii) control signals to interface with and operate Main RAM 205.

Id. Control Circuit 203 also enables operations that allow the external processors to access Main RAM 205, and perform bidirectional DMA (direct access memory) transfer between Flash Memory 204 and Main RAM 205.

Id. Flash memory 204 may include one or more NAND Flash devices 210, or other types of Flash memory, such as AND Flash devices. *Id.* ¶ 82. Main RAM 205 may include one or more SDRAM devices 211, or other types of volatile random access memories. *Id.*

Lee describes seven embodiments of memory system control circuits. *Id.* ¶¶ 22–54. Lee’s Figure 3, reproduced below, is a block diagram of a first embodiment of a memory system control circuit (corresponding to Control Circuit 203 illustrated in Figure 2). *Id.* ¶¶ 25, 83.

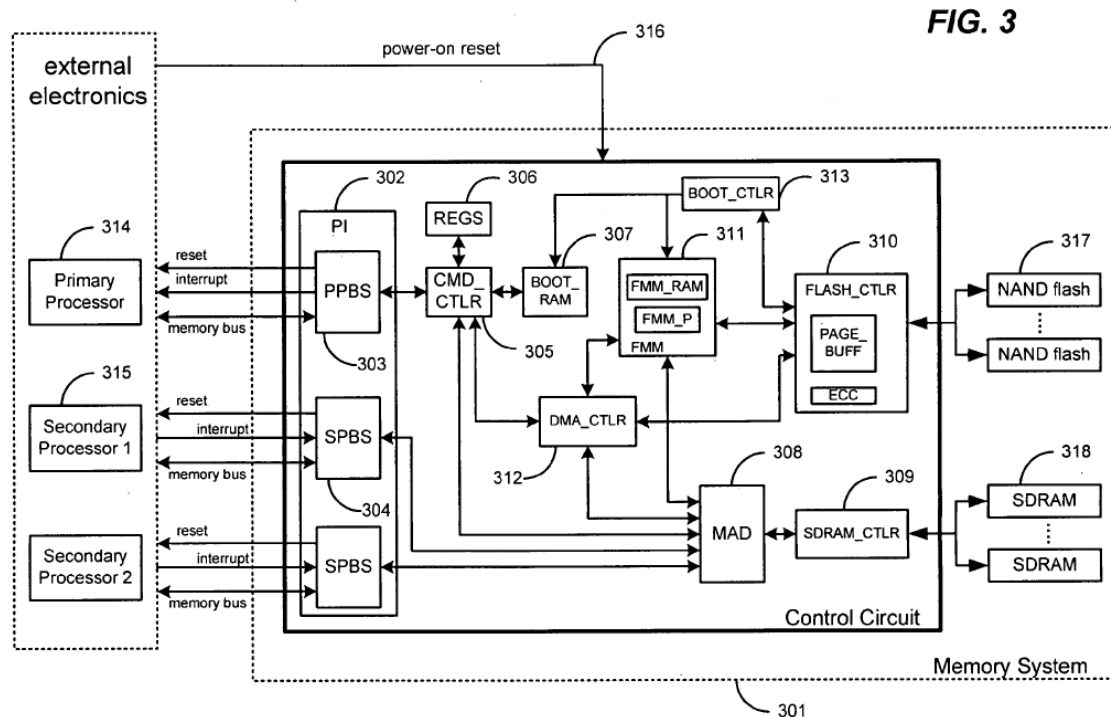


Figure 3 is a block diagram depicting Processor Interface Circuit (PI) 302 which provides an interface to external processor(s) so that the external processors configure, control and/or monitor tasks performed by the Control

Circuit, as well as access the data stored in Memory System 301. *Id.*

¶¶ 84–85. PI circuit 302 includes Processor Bus Slave circuits (PBSs) 303 (a primary PBS, or PPBS) and 304 (a secondary PBS, or SPBS) providing an interface to a corresponding individual external processor, such as external processors 314 (a Primary Processor) and 315 (a Secondary Processor). *Id.* ¶¶ 85, 88. A PBS is attached to a memory bus of its corresponding external processor, and accesses and controls the memory bus in accordance with the memory bus data transfer protocol. *Id.* Via PI 302, external processors 314, 315 can access data stored in SDRAM 318, with primary processor 314 having the additional responsibility of configuring, activating and monitoring many functions of the Control Circuit, such as the DMA data transfer between the NAND Flash (e.g., NAND Flash memory 317) and the SDRAM (318). *Id.* ¶¶ 88, 111. When accessed by primary processor 314, PPBS 303 translates the memory bus control signals into one of the following commands: “RAM Read,” “RAM Write,” “Register Read,” “Register Write,” “Download DMA Transfer,” and “Upload DMA Transfer.” *Id.* ¶¶ 90, 102. PPBS 303 then sends the command to Command Controller (CMD_CTLR) 305. *Id.* ¶ 90. Data and address signals of the memory bus provide Command Controller 305 with data and address information associated with the command. *Id.* The data signals of the memory bus are bidirectional to thereby communicate both write data and read data information. *Id.* The “Download DMA Transfer” and “Upload DMA transfer” commands cause CMD_CTLR 305 to activate a DMA controller (DMA_CTLR 312) to perform a DMA transfer from NAND Flash memory 317 to SDRAM 318 or from SDRAM 318 to NAND Flash memory 317 (uploading), respectively. *Id.* ¶ 111.

The control circuit of Figure 3 also includes an embedded control circuit processor (FMM_P, in FMM (Flash memory management) circuit 311) that performs FMM processes, and volatile memory (FMM_RAM in FMM circuit 311) used to store the FMM program code for execution by the FMM_P in FMM circuit 311. *Id.* ¶¶ 66, 117, 121, 126, 139, 182, 187. FLASH_CTLR 310, under the control of FMM 311, either accesses the NAND Flash in a DMA transfer between NAND Flash memory 317 and SDRAM 308, or performs FMM book-keeping tasks such as reading an address translation table from NAND Flash memory 317 or updating an address translation table in NAND Flash memory 317. *Id.* ¶ 129.

Lee further describes “maintaining certain book-keeping records, such as one or more of logical-to-physical address translation tables, bad block locations, and physical addresses containing outdated data.” *Id.* ¶ 159. These records are “stored in the Flash memory and updated often enough to reflect the latest data arrangement in the Flash memory.” *Id.* “The FMM (311) initialization often involves finding and copying the FMM (311) book-keeping records required for Flash media management, such as address translation tables, from the NAND Flash memory (317) to the FMM_RAM or SDRAM (318).” *Id.* ¶ 169. “The FMM book-keeping records may be kept in the FMM_RAM, SDRAM (318), or both during normal operation.” *Id.* ¶ 172. “When the FMM algorithm code needs to update a portion of the book-keeping records in the SDRAM, the FMM (311) generates a new version of the portion of the book-keeping records in the FMM_RAM, and then copies the data from the FMM_RAM to the SDRAM (318) . . . to override the older version stored in the SDRAM.” *Id.* “From time to time, the FMM algorithms need to write or update certain book-keeping records in

the NAND Flash memory (317), which often involves erasing various NAND Flash blocks and copying data from SDRAM (318) to NAND Flash memory.” *Id.* ¶ 173.

Lee’s Figure 9, reproduced below, illustrates an arrangement of NAND Flash storage space. *Id.* ¶ 31.

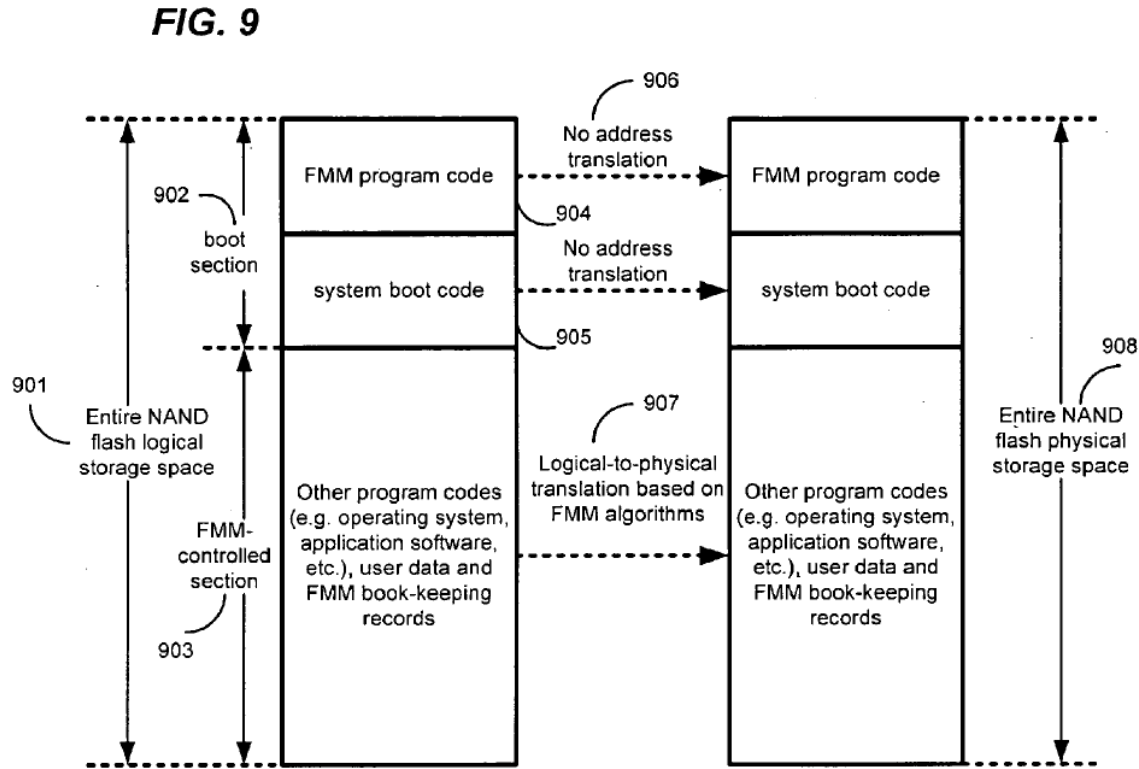


Figure 9 is a block diagram depicting NAND Flash storage space 901 divided into a boot section 902 and an FMM-controlled section 903. *Id.* ¶ 188. Boot section 902 in the NAND Flash memory (e.g., NAND Flash memory 317 in Figure 3) is the area where system boot code and FMM program code are stored. *Id.* Boot section 902 does not undergo the wear of erase-rewrite cycles as much as the rest of the NAND Flash memory does. *Id.* ¶ 189. In addition, there is no distinction between logical and physical addresses for data in boot section 902, and, therefore, logical-to-physical

address translation is not needed when accessing this section (as illustrated at 906 in Figure 9). *Id.* Data stored in FMM-controlled section 903 is moved around to different physical addresses for wear-leveling and bad-block replacement purposes, and is maintained and tracked by FMM algorithms, and therefore, logical-to-physical address translations 907 are performed by the FMM (e.g., FMM 311 in Figure 3) when accessing data in FMM-controlled section 903. *Id.* Boot section 902 contains FMM program code 904 and system boot code 905. *Id.* ¶ 190. Process 907 in Figure 9 indicates logical-to-physical address translations that are performed by the FMM (e.g., FMM 311 in Figure 3) when accessing data in FMM-controlled section 903. *Id.* ¶ 189.

2. Analysis of Claim 1

a) [1.PRE] “A nonvolatile memory system comprising:”

Petitioner contends that Lee teaches the preamble. Pet. 26. Specifically, Petitioner relies on Lee’s “wireless phone that includes a nonvolatile memory (‘Flash memory (104)’).” *Id.* (citing Ex. 1007 ¶ 63).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches claim 1’s preamble.¹³

¹³ Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination that the preamble of claim 1 is limiting.

b) [1.A] “a nonvolatile memory for storage of digital information arranged in multiple blocks for access,”

Petitioner contends that Lee teaches this limitation. Pet. 26–27.

Petitioner contends that Lee’s Flash memory 104 is in a “block” and “page” arrangement, and the blocks and pages “have physical addresses (*e.g.*, which the flash memory uses) and associated logical addresses (*e.g.*, which a host uses).” *Id.* at 26 (citing Ex. 1007 ¶¶ 63, 149, 152, 155–156; Ex. 1006 ¶¶ 142–143). Petitioner further contends that Lee discloses “storage of digital information arranged in multiple blocks for access” as recited in limitation 1.A because “Lee’s Flash memory includes blocks that are either in the FMM-controlled section (903) or boot section (902).” *Id.* (citing Ex. 1007, Fig. 9). Petitioner asserts that the data in these sections are transferred to volatile memory. *Id.* Dr. Levy’s testimony that Lee stores blocks of data in flash memory in the “FMM-controlled section” (Ex. 1006 ¶¶ 142–143) supports Petitioner’s contention.

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.A.

c) [1.B] “a volatile random access memory for read and write operations coupled to said nonvolatile memory;”

Petitioner contends that Lee teaches this limitation. Pet. 27–28.

Specifically, Petitioner contends that Lee discloses a Main RAM, *e.g.*, SDRAM, coupled to Flash memory, which reads on “a volatile random access memory . . . coupled to said nonvolatile memory.” *Id.* at 27 (citing Ex. 1007, Fig. 3, ¶¶ 63, 77, 82, 213). Petitioner further contends that Lee discloses read and write operations to the Main RAM because it discloses

“access” to Main RAM. *Id.* (citing Ex. 1007 ¶ 64). Dr. Levy’s testimony (Ex. 1006 ¶¶ 146–148) supports Petitioner’s contention.

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.B.

d) [1.C] “wherein the volatile random access memory and nonvolatile memory are controlled by one or more controllers;”

Petitioner contends that Lee teaches this limitation. Pet. 28–29. Petitioner contends that Lee discloses its Flash memory and Main RAM, e.g., SDRAM, both have a controller. Pet. 28–29 (citing Ex. 1007 ¶¶ 63, 121–122; Ex. 1006 ¶ 152).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.C.

e) [1.D] “wherein the nonvolatile memory system is coupled to a central processing unit;”

Petitioner contends that Lee discloses its memory system is coupled to “primary processor” (CPU). Pet. 29 (citing Ex. 1007, Fig. 3, ¶ 69; Ex. 1006 ¶¶ 153–155). Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.D.

f) [1.E] “wherein each block of the nonvolatile memory for storage has one or more pages of stored data accessible through the coupled volatile random access memory; and”

Petitioner contends that Lee discloses its Flash memory includes blocks and pages of data that consist of the FMM-controlled section (903) and boot section (902). Pet. 30 (citing Ex. 1007, Fig. 9, ¶¶ 128, 132, 147). Petitioner further contends that Lee discloses that all data in the non-volatile memory is accessible through the SDRAM and RAM. *Id.* (citing Ex. 1006 ¶¶ 156–161). Petitioner contends the Flash data is accessible through the coupled volatile random access memory (BOOT-RAM and SDRAM, respectively), as recited in limitation 1.E. *Id.* at 30–31 (citing Ex. 1007, Fig. 9, ¶¶ 66, 68, 162, 166, 241).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.E.

g) [1.F] “wherein each page of a block is adapted to be substituted on the fly for any other page of a different block through address mapping;”

Petitioner contends that Lee discloses that when a write to a logical address occurs, the write data is written to a new physical address, and the logical address is re-mapped to a different physical block. Pet. 31–32 (citing Ex. 1006 ¶¶ 163–164; Ex. 1007 ¶¶ 65, 156). Petitioner contends that this wear-leveling process as described in Lee occurs on the fly because the physical page of a block is substituted for any other page of a different block through address mapping, “without suspending or disturbing normal operations . . . it occurs as part of the normal write operation and occurs

transparently as pages of data are repeatedly written to the Flash memory.” *Id.* at 32 (citing Ex. 1006 ¶¶ 165–166; Ex. 1007 ¶¶ 65, 185, 189). Petitioner further contends that a person of ordinary skill would have understood from Lee that “this remapping can occur with ‘each page of a block’ being remapped to ‘any other page of a different block’” as recited in limitation 1.F, in part because it was well known that wear-leveling often involves writing to the most recently erased memory block. *Id.* at 33 (citing Ex. 1006 ¶ 168; Ex. 1007 ¶¶ 152, 189; Ex. 1009, 1:23–33).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.F.

h) [1.G] “wherein the one or more controllers control the volatile and nonvolatile memories to:”

Petitioner contends that Lee discloses that the Flash memory, Main RAM, and RAMs have controllers. Pet. 33–34 (citing Ex. 1007 ¶¶ 111, 182–184).

Patent Owner argues that Lee does not teach limitation 1.G because it fails to disclose a controller that performs a read/modify/write operation. PO Resp. 36–37. As discussed in Section II.B, we determine that this limitation does not require a read/modify/write operation. Thus, Patent Owner’s argument is not persuasive.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.G.

- i) *[1.H] perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location*

Petitioner contends Lee teaches this limitation because “data in the non-volatile memory (‘digital information to be read’ that is ‘at the associated addressable location’), such as user data and book-keeping records (of the FMM-controlled section, *see* Fig. 9), are transferred to the volatile memory (‘retriev[ed]’ and ‘stor[ed]’).” Pet. 34 (citing Ex. 1006 ¶¶ 172–177) (alteration in original). In particular, Petitioner relies on (i) Lee’s “Download DMA transfer” process that performs read operations on the data in the nonvolatile memory at the associated addressable location (“NAND Flash Logical Page Address”) to retrieve it and store it in the SDRAM; and (ii) Lee’s DMA controller that directs FMM 311 to carry out the transfer via “read” operations and configure the flash controller (FLASH_CTLR) to read the Flash memory, so that when data is written to the SDRAM via the SDRAM controller, the FMM-controlled section of Lee’s Flash memory is transferred to the SDRAM. *Id.* at 34–35 (citing Ex. 1007 ¶¶ 65–66, 111, 169, 184, 196, 207–208, 213, 169, 182–184, Fig. 3).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.H.

- j) *[1.I] perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory*

Petitioner contends that Lee teaches this limitation. Pet. 35–37. Specifically, Petitioner contends that “Lee discloses that various entities,

such as the primary processor, may perform read operations on the SDRAM, via the SDRAM controller, *e.g.*, of user data and FMM book-keeping records (the ‘stored digital information’).” *Id.* at 35 (citing Ex. 1007, Fig. 3, ¶¶ 90, 108, 122, 159, 169; Ex. 1006 ¶ 179). Petitioner contends “it would have been understood, and certainly obvious, that Lee discloses reads [*sic*] operations on ‘any portion . . . of the stored digital information in the volatile memory’” (*id.* at 35–37 (citing Ex. 1007 ¶¶ 8, 82, 86, 90, 92, 102, 122; Ex. 1006 ¶¶ 180–185)) because “Lee broadly discloses that the SDRAM data is accessible at addressable locations for granular access (*i.e.*, only portions of the SDRAM are accessed)” (*id.* at 37 (citing Ex. 1007 ¶¶ 104, 106)) and SDRAM with addressable byte level access [] was extremely well known (*id.* (citing Ex. 1006 ¶¶ 182–185; Ex. 1017, 6:27–32)).”

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.I.

k) [1.J] perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein, and

Petitioner contends that Lee teaches this limitation. Pet. 37–38. Specifically, Petitioner asserts that (i) Lee discloses transferring Flash data to the SDRAM for entities such as the host to access, and at the respective SDRAM addresses, that this data can be read and overwritten (*id.* (citing Ex. 1007 ¶¶ 91, 104–108, 120, 169, 172, 213; Ex. 1006 ¶ 187)); and (ii) Lee discloses a single address set for the SDRAM (whereas Lee discloses individual physical and logical addresses for wear-leveling for the Flash),

and “[t]here is also a correspondence between the SDRAM and flash logical addresses (the starting addresses for the transfer set a correspondence), and thus the SDRAM data must be written back to the same addresses to maintain the correspondence” (*id.* at 38 (citing Ex. 1007 ¶¶ 104, 111, 200–203; Ex. 1006 ¶¶ 187–191)).

Patent Owner argues that Lee does not teach limitation 1.J because it fails to disclose a controller that performs a read/modify/write operation. PO Resp. 36–37. As discussed in Section II.B, we determine that this limitation does not require a read/modify/write operation. Thus, Patent Owner’s argument is not persuasive.

We find that Petitioner has shown that Lee teaches limitation 1.J. As discussed above, Petitioner provides supporting evidence in Lee, and Dr. Levy’s testimony, about writing bit or byte sized portions of digital information originally stored in volatile memory back to the same physical location in volatile memory, so “the SDRAM data must be written back to the same address.” *See* Pet. 38; Ex. 1007 ¶¶ 111, 200–203; Ex. 1006 ¶¶ 187–191. Petitioner has shown where Lee discloses transferring data, including book-keeping records and user data from flash memory (e.g., reading) to SDRAM (e.g., writing) and vice versa. *Id.* at 34–35, 38; *see, e.g.*, Ex. 1007 ¶¶ 111, 182, 200 (describing “Download DMA Transfer” where NAND Flash to SDRAM transfer is performed and “Upload DMA Transfer” where SDRAM to NAND Flash transfer is performed); ¶ 169 (“finding and copying the FMM (311) book-keeping records . . . from the NAND Flash memory (317) and loaded into FMM_RAM or SDRAM (318)”); ¶ 173 (“write or update certain book-keeping records . . . which often involves . . . copying data from SDRAM (318) to NAND Flash

memory (317)"); ¶ 207 (“the Primary Processor activates a DMA transfer to copy the program code from NAND Flash to SDRAM”); ¶ 213 (“copying user data from NAND Flash memory (317) to SDRAM (318) and vice versa”); Ex. 1006 ¶¶ 187–191). Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.J.

l) [1.K] write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read.

Petitioner contends Lee teaches this limitation. Pet. 39–40.

Specifically, Petitioner asserts: (i) “Lee discloses that digital information in the volatile memory data, *e.g.*, user data and FMM book-keeping records (‘the digital information stored in the volatile memory back to the nonvolatile memory’), is written back to the nonvolatile memory” (Pet. 39 (citing Ex. 1007 ¶¶ 111, 179, 189, 213)); (ii) Lee discloses that the data is written “at a different physical location with the same associated address [the logical address] from which it was read” because Lee describes a “new association between the logical and physical addresses” is created, which indicates that “the logical address (‘same associated address’) is overwritten with data, but the data is written to a different physical block, and the logical address is remapped to the different physical block” (*id.* at 39–40 (citing Ex. 1007 ¶¶ 156, 189, Fig. 9; Ex. 1006 ¶¶ 192–197)).

Patent Owner does not respond to these arguments. *See generally* PO Resp. Accordingly, after considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches limitation 1.K.

3. Analysis of Claims 2 and 8–13

Petitioner contends dependent claims 2 and 8–13 would have been obvious over Lee, and presents argument as to how the prior art teaches each claim limitation. Pet. 40–44. Patent Owner does not separately respond to these arguments. *See* PO Resp. 37. We agree with and adopt Petitioner’s arguments. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee teaches the limitations in claims 2 and 8–13.

4. Conclusion

Having considered the Graham factors,¹⁴ including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the challenged claims, we are persuaded, based on the current record, that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, and 8–13 would have been obvious over Lee.

E. Ground 2: Obviousness Based on Tsunoda and Kolokowsky

Petitioner contends claims 1, 2, 4, 5, 8, and 10–13 would have been obvious over the combination of Tsunoda and Kolokowsky. Pet. 8, 44–64. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, 4, 5, 8, and 10–13 are unpatentable over Tsunoda and Kolokowsky.

¹⁴ Patent Owner does not submit evidence of secondary considerations. *See* PO Resp.

1. Tsunoda (Ex. 1008)

Tsunoda is titled “Memory Apparatus” and describes a memory apparatus having a volatile memory for storing data from a host, a nonvolatile memory capable of storing the data stored in the volatile memory, and a control circuit for controlling data transfer between the volatile memory and the nonvolatile memory, with a capacity of a data storage area of the volatile memory being larger than that of a data storage area of the nonvolatile memory. Ex. 1008, code (54) (Title), code (57) (Abstr.). Tsunoda’s Figure 24, reproduced below, illustrates a configuration of the memory apparatus. *Id.* ¶ 35.

FIG.24

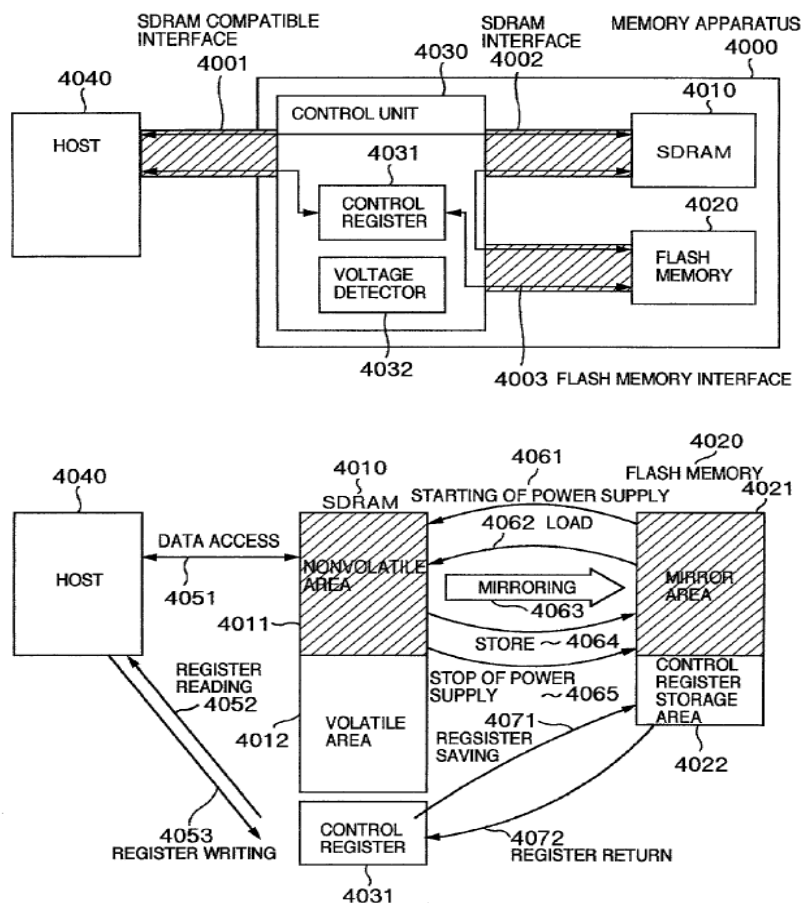


Figure 24 depicts memory apparatus 4000 including: SDRAM 4010 to be accessed randomly and having at least one or more nonvolatile areas 4011, and volatile area 4012 other than the nonvolatile area 4011; flash memory 4020 that is a nonvolatile memory; SDRAM compatible interface 4001 for enabling a host 4040 (an information processor such as a CPU or ASIC incorporated in an information terminal) to access the memory apparatus 4000; SDRAM interface 4002 of the SDRAM 4010; control unit 4030 including a control register 4031 and a voltage detector 4032 for monitoring a power supply voltage supplied from an external unit to the memory apparatus 4000; and flash memory interface 4003 connecting control unit 4030 and flash memory 4020 to each other. *Id.* ¶¶ 40, 42, 46, 54, 55, 62, 67, 70, 72. Nonvolatile area 4011 is an area for performing mirroring 4063 by using the flash memory 4020. *Id.* ¶ 71. Memory apparatus 4000 also includes, in the memory area of flash memory 4020, mirror area 4021 for performing mirroring 4063 of SDRAM 4010, and a control register storage area 4022 for storing the control register 4031. *Id.* ¶ 74. Mirror area 4021 includes an area for storing all the data stored in nonvolatile area 4011 of SDRAM 4010. *Id.* ¶ 74. Mirroring 4063 means that data stored in mirror area 4021 of flash memory 4020 is brought into coincidence with data stored in nonvolatile area 4011 of SDRAM 4010, or that a copy of the data stored in nonvolatile area 4011 of SDRAM 4010 is stored in mirror area 4021 of flash memory 4020. *Id.* ¶ 73. Mirror area 4021 of flash memory 4020 is managed based on a logical address excluding a failed area of flash memory 4020. *Id.* ¶ 73.

Tsunoda explains that

[s]ince the SDRAM 4010 is a volatile memory, data written in the SDRAM 4010 is lost when the power supply to the memory apparatus 4000 is stopped. However, as the data stored in the nonvolatile area 4011 can be subjected to mirroring in the mirror area 4021 of the flash memory 4020, the data can be held ever after power is turned OFF. The data stored in the volatile area 4012 is lost when the power is OFF. The host 4040 can access the nonvolatile area 4011 of the SDRAM 4010, the volatile area 4012 of the SDRAM 4010, and the control register 4031 by designating a predetermined address through the SDRAM compatible interface 4001.

Id. ¶ 75.

Tsunoda's Figure 1, reproduced below, depicts an example of an internal configuration of memory apparatus.

FIG.1

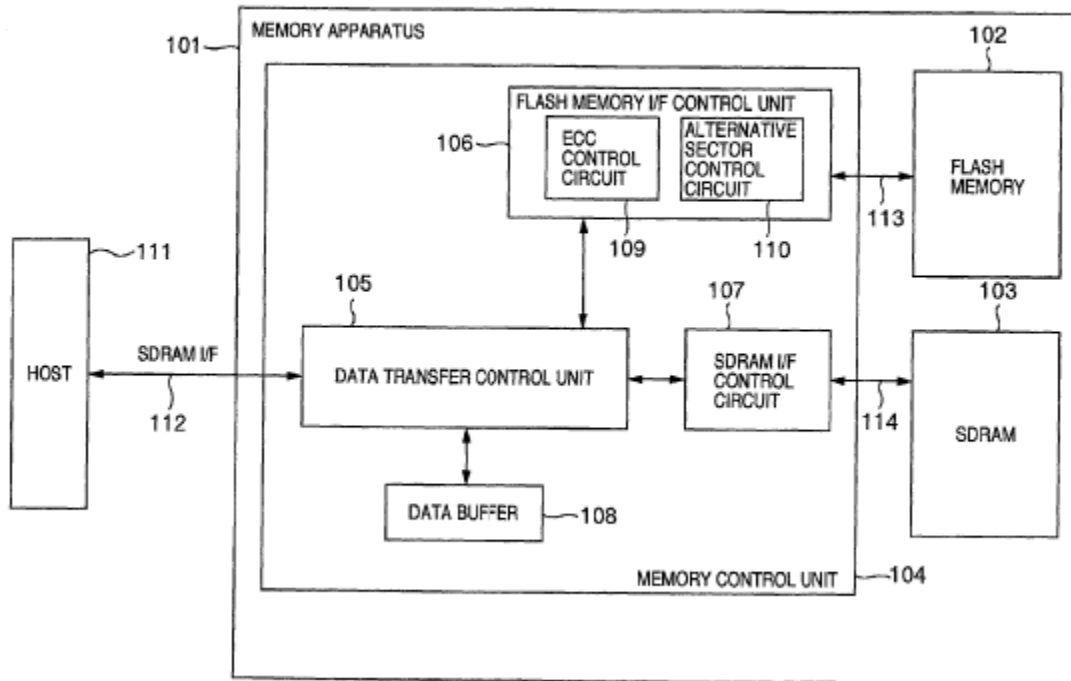


Figure 1 includes flash memory 102 as nonvolatile memory, SDRAM 103 as volatile memory, and memory control unit 104 for controlling the memories.

Id. ¶ 96. “The memory control unit 104 controls data transfer or the like between a host 111 and the memory apparatus 101, and between the flash memory 102 and the SDRAM 103 in response to a request from the host 111.” *Id.* The address space of the SDRAM 103 includes a volatile area 203 and a nonvolatile area 204. *Id.* ¶ 98. “After the power is turned ON, user data on the flash memory 102 is copied to the nonvolatile area 204 of the SDRAM 103, and the host 111 can use the user data by accessing the nonvolatile area 204 on the SDRAM 102. If the user data is slightly changed or contains an addition, the user data is copied to the flash memory 102, and held on the flash memory 102.” *Id.* ¶ 99.

2. *Kolokowsky (Ex. 1009)*

Kolokowsky is titled “Flash Drive Fast Wear Leveling” and describes a system comprising “a non-volatile memory including one or more memory blocks to store data, a controller to allocate one or more of the memory blocks to store data, and a wear-leveling table populated with pointers to unallocated memory blocks in the non-volatile memory,” with “the controller . . . identify[ing] one or more pointers in the wear-leveling table and . . . allocat[ing] the unallocated memory blocks associated with the identified pointers for the storage of data.” Ex. 1009 at code (57) (Abstr.). Kolokowsky’s Figure 1, reproduced below, illustrates a memory system including a wear-leveling table. *Id.* at 1:63–65, 2:8–67.

Figure 1

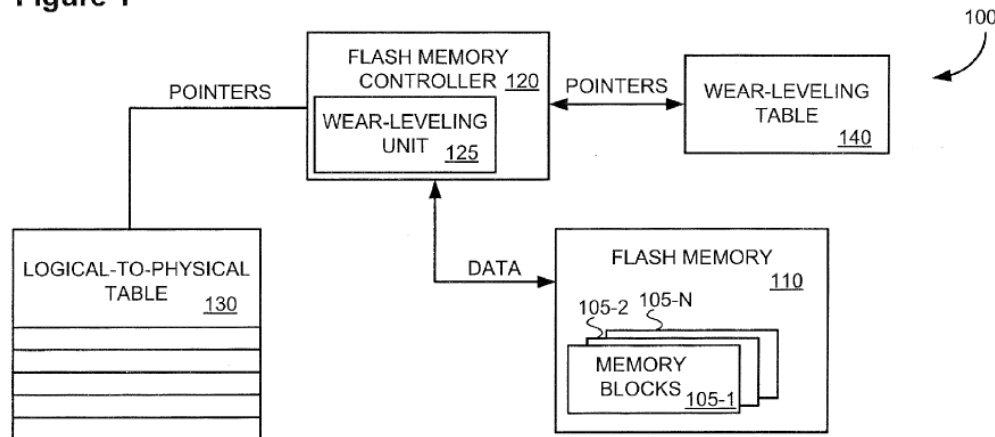


Figure 1 is a block diagram depicting memory system 100, including:

- (i) flash memory 110, which may be NAND flash memory or other type of non-volatile memory capable of storing data and having a plurality of memory blocks 105-1 to 105-N to store the data;
- (ii) flash memory controller 120 to perform memory access operations, such as read, write, and erase, on memory blocks 105-1 to 105-N;
- (iii) logical-to-physical table 130 populated with pointers to the memory blocks 105-1 to 105-N, where the pointers may be addresses to physical locations of the memory blocks in flash memory 110;
- (iv) wear-leveling table 140 populated with pointers to unallocated memory blocks in flash memory 110; and
- (v) wear-leveling unit 125 in controller 120, used to populate the wear-leveling table 140 with pointers to unallocated memory blocks. *Id.* at 2:8–3:13. Flash memory 110 may include 1024 memory blocks, for example, with a maximum of 1000 of the 1024 memory blocks allocated for the storage of data at any given time, the remaining unallocated memory blocks including erased or erasable memory blocks available to store data, bad or faulty memory blocks, or both. *Id.* at 2:12–20. Kolokowsky explains the operation of memory system 100 as follows:

When prompted to write data to the flash memory 110, the flash memory controller 120 may identify one or more unallocated memory blocks in the flash memory 110 available to store the data and then write the data to the identified memory block(s).

...

When the flash memory controller 120 determines to write data to the flash memory 110, the wear-leveling unit 125 may access the wear-leveling table 140 to identify at least one erased or erasable memory block in the flash memory 110 available to store the data. The wear-leveling table 140 may also include data to indicate which of the pointers correspond to erased or erasable memory blocks and which of the pointers correspond to faulty or failed memory blocks. Since the wear-leveling table 140 includes pointers to unallocated memory blocks in the flash memory 110, the wear-leveling unit 125 may reduce the time required to identify an erased or erasable memory block during data write operations.

Id. at 2:24–32, 3:14–25.

3. Analysis of Claim 1

a) [1.PRE] “A nonvolatile memory system comprising:”

Petitioner contends that Tsunoda teaches the preamble. Pet. 44–45. Specifically, Petitioner relies on Tsunoda’s “nonvolatile memory system with flash and SDRAM memories.” *Id.* (citing Ex. 1008, Fig. 24; ¶ 96).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches the preamble.

b) [1.A] “a nonvolatile memory for storage of digital information arranged in multiple blocks for access,”

Petitioner contends that Tsunoda teaches this limitation. Pet. 45–46. Specifically, Petitioner identifies Tsunoda’s flash memory with “logical

sector address[es].” *Id.* (citing Ex. 1008 ¶¶ 96, 107). Petitioner asserts that the disclosure of “sectors” necessarily discloses “blocks” because it is well-known that flash memory is organized into blocks, which include pages, which may in turn include one or more sectors. *Id.* (citing Ex. 1021 ¶ 6; Ex. 1004, 3:35–39, Fig. 2; Ex. 1006 ¶¶ 221–223). Petitioner further argues that Tsunoda discloses that its flash memory stores “user data,” which teaches “digital information.” *Id.* at 46 (citing Ex. 1008 ¶ 99).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.A.

c) [1.B] “a volatile random access memory for read and write operations coupled to said nonvolatile memory;”

Petitioner contends that Tsunoda teaches this limitation. Pet. 46–47. Specifically, Petitioner identifies Tsunoda’s volatile SDRAM, which is coupled to nonvolatile flash memory. *Id.* (citing Ex. 1008 ¶¶ 42, 90, 99). Petitioner further contends Tsunoda’s control register is volatile, random access memory. *Id.* at 47 (citing Ex. 1008 ¶¶ 62–64, 74, 83; Ex. 1006 ¶ 227).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.B.

a) [1.C] “wherein the volatile random access memory and nonvolatile memory are controlled by one or more controllers;”

Petitioner contends that Tsunoda teaches this limitation. Pet. 47–48. Petitioner contends that Tsunoda discloses an SDRAM and a flash memory controller, and further that control register 4031 is controlled by a controller. *Id.* (citing Ex. 1008 ¶¶ 62–64, 97; Ex. 1006 ¶ 230).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.C.

b) [1.D] “wherein the nonvolatile memory system is coupled to a central processing unit;”

Petitioner contends that Tsunoda discloses its nonvolatile memory is connected to a host that includes a CPU. Pet. 48 (citing Ex. 1008 ¶¶ 40, 42). Patent Owner does not respond to this argument. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.D.

c) [1.E] “wherein each block of the nonvolatile memory for storage has one or more pages of stored data accessible through the coupled volatile random access memory; and”

Petitioner contends that Tsunoda teaches this limitation. Pet. 48–49. Specifically, Petitioner identifies Tsunoda’s flash memory has logical sector addresses, and that it was well known that flash memory is organized into blocks that include pages of data. *Id.* at 48 (citing Ex. 1008 ¶ 107; Ex. 1021 ¶ 6; Ex. 1006 ¶ 234). Petitioner further contends that Tsunoda discloses data

in all blocks are downloaded into accessible, coupled RAM, and that flash memory including data in mirror area and control register storage area transfers to Tsunoda's SDRAM and is accessible through SDRAM. *Id.* at 48–49 (citing Ex. 1008 ¶¶ 42, 63–64, 80–84, 90; Ex. 1006 ¶¶ 235–237).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.E.

d) [1.F] “wherein each page of a block is adapted to be substituted on the fly for any other page of a different block through address mapping;”

Petitioner contends that Tsunoda in combination with Kolokowsky teaches this limitation. Pet. 49. Specifically, Petitioner contends that “upon powering up, ‘user data’ is transferred from [Tsunoda's] Flash memory (from its logical sector addresses) to the SDRAM, this information is read and modified, and then written back to the Flash memory at the same logical address.” *Id.* (citing Ex. 1008 ¶¶ 50, 51, 66, 99, 107; Ex. 1006 ¶¶ 239–240).

Petitioner contends that Tsunoda does not disclose which physical blocks the data at the logical flash addresses are written to, and so relies on Kolokowsky to teach that it was conventional to write the modified data to a different physical block, such as an already erased block. *Id.* (citing Ex. 1009, 1:23–33). Petitioner asserts that as part of the write operation, the logical address is re-mapped to the new physical address, and accordingly, the original page of the physical block with the logical address is substituted for a page of a different physical block. *Id.* at 50 (citing Ex. 1006 ¶¶ 242–244; Ex. 1009, 1:23–33, 1:43–58, 2:12–18, 2:24–28).

Petitioner argues that a person of ordinary skill in the art would have been motivated to combine Tsunoda and Kolokowsky because (1) “Tsunoda provides the ability for wear leveling because it implements logical addressing for the flash device”; (2) a person of ordinary skill in the art would know that using wear-leveling was advantageous because wear-leveling was known to extend the life of the device; and (3) a person of ordinary skill in the art would know that using wear-leveling was advantageous because it ensures that different, previously erased blocks are available to which data may be written back, which decreases write operation time because the block does not have to be erased before programming. *Id.* at 63–64 (citing Ex. 1008 ¶ 107; Ex. 1014, 1:30–45; 1:46–48; Ex. 1009, 4:30–51; Ex. 1015 ¶ 9; Ex. 1006 ¶¶ 292–295). Petitioner also argues that a person of ordinary skill in the art would have had a high expectation of success in implementing Kolokowsky’s wear-leveling techniques in Tsunoda because wear-leveling was conventional and Tsunoda already uses logical addressing. *Id.* at 64 (citing Ex. 1006 ¶ 296; Ex. 1009, 1:23–33; Ex. 1008 ¶ 107; Ex. 1014, 1:46–48).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that the combination of Tsunoda and Kolokowsky teaches limitation 1.F, and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

e) [1.G] “wherein the one or more controllers control the volatile and nonvolatile memories to:”

Petitioner contends that Tsunoda teaches this limitation because it discloses that the flash memory, SDRAM, and control register have controllers. Pet. 51.

Patent Owner argues that Tsunoda does not teach limitation 1.G because it fails to disclose a controller that performs a read/modify/write operation. PO Resp. 38–39. As discussed in Section II.B, we determine that this limitation does not require a read/modify/write operation. Thus, Patent Owner’s argument is not persuasive.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.G.

f) [1.H] perform a read operation on the portion of the digital information to be read and retrieving and storing such from the given block at the associated addressable location

Petitioner contends Tsunoda teaches this limitation because “upon start up, user data (which is ‘digital information to be read’) is read from the flash memory at its logical address (logical sectors) and is transferred to the SDRAM (‘perform a read operation on the portion of the digital information’ and ‘retrieving and storing such from the given block at the associated addressable location’).” *Id.* at 52 (citing Ex. 1008 ¶¶ 99, 107, 110; Ex. 1006 ¶¶ 248–249). Patent Owner does not respond to these arguments. *See generally* PO Resp.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.H.

g) [1.I] perform a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory

Petitioner contends Tsunoda teaches this limitation. Pet. 52–54.

Specifically, Petitioner contends Tsunoda discloses SDRAM with stored user data that is “accessed randomly,” and that such accesses included accesses of “any portion,” e.g., a bit or a byte. *Id.* (citing Ex. 1008 ¶¶ 42, 90, 94, 99; Ex. 1006 ¶¶ 254–257).

Patent Owner does not respond to these arguments. *See generally* PO Resp.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.I.

h) [1.J] perform a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein

Petitioner contends Tsunoda teaches this limitation. Pet. 55–56.

Specifically, Petitioner contends that Tsunoda discloses “standard SDRAM write operations on the user data (‘the accessed read digital information’) and that the user data is randomly accessible” and the “‘user data’ is read and updated (written) in the SDRAM”; (ii) “Tsunoda discloses, or at least renders obvious, that the writes are possible to the addressable bit and/or byte level”; and (iii) “it would have been understood, and certainly obvious, that the user data is written back to the same physical location in the SDRAM.” *Id.* (citing Ex. 1008 ¶¶ 42, 50–52, 62, 90, 99, 100, 107; Ex. 1006 ¶¶ 262–263). In support of its arguments, Petitioner argues that “Tsunoda’s memory mapping relies on the SDRAM addresses not changing” because

“there is a ‘correspondence’ between the SDRAM address space and the logical addresses of flash memory that does not change.” *Id.* at 56 (citing Ex. 1008 ¶¶ 50–52, 62, 100, 107; Ex. 1006 ¶¶ 262–263).

Patent Owner argues Tsunoda does not teach limitation 1.J because it fails to disclose a controller that performs a read/modify/write operation. PO Resp. 38–39. As discussed in Section II.B, we determine that this limitation does not require a read/modify/write operation. Thus, Patent Owner’s argument is not persuasive.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda teaches limitation 1.J.

i) *[1.K] write the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read*

Petitioner contends that Tsunoda combined with Kolokowsky teaches this limitation. Pet. 56–58. Specifically, Petitioner contends that Tsunoda discloses “‘writ[ing] the digital information stored in the volatile memory back to the nonvolatile memory’ when, *e.g.*, changes are made to the user data (‘the digital information’) and the device is powered down.” *Id.* at 56–57 (citing Ex. 1008 ¶¶ 85, 86, 99, 100; Ex. 1006 ¶ 267). Petitioner further contends that “the user data is written back to the ‘same associated address from which it was read,’ *i.e.*, the logical address of the flash memory” because “there is a correspondence between the SDRAM addresses and flash logical addresses, and the user data is read from, and written to, the same corresponding flash logical addresses.” *Id.* at 57 (citing Ex. 1008 ¶¶ 50–52, 62, 100, 107). Petitioner contends “the user data in the SRAM is mirrored in

the same range of flash logical address space.” *Id.* (citing Ex. 1008 ¶¶ 73, 74, 125–127).

Petitioner argues that, for the same reasons as discussed above with respect to limitation 1.F, a person of ordinary skill in the art would have been motivated “in view of Kolokowsky . . . to write the data to a ‘different physical location’ and update the translation table so that the ‘same associated address’ becomes associated with the different physical block (*i.e.*, the logical address is re-mapped to a new physical block).” *Id.* at 57–58 (citing Ex. 1009, 1:23–33, 2:24–28; Ex. 1014, 1:46–48; Ex. 1003 ¶ 268).

Patent Owner does not respond to these arguments. *See generally* PO Resp. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that the combination of Tsunoda and Kolokowsky teaches limitation 1.K and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

4. Claims 2, 4, 5, 8, and 10–13

Petitioner contends dependent claims 2, 4, 5, 8, and 10–13 would have been obvious over the combination of Tsunoda and Kolokowsky, and presents argument as to how the prior art teaches each claim limitation. Pet. 58–63. Patent Owner does not separately respond to these arguments. *See* PO Resp. 39. We agree with and adopt Petitioner’s arguments. After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Tsunoda and Kolokowsky teach the limitations in claims 2, 4, 5, 8, and 10–13.

5. Conclusion

Having considered the Graham factors, including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the challenged claims, we are persuaded, based on the current record, that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, 4, 5, 8, and 10–13 would have been obvious over the combination of Tsunoda and Kolokowsky.

F. Grounds 3 and 5: Obviousness Based on Lee and Li (Ground 3) and Tsunoda, Kolokowsky, and Li (Ground 5)

Petitioner contends claim 3 would have been obvious over the combination of Lee and Li, and the combination of Tsunoda, Kolokowsky, and Li. Pet. 7, 64–68. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 3 is unpatentable over these combinations.

1. Li (Ex. 1010)

Li is titled “Multilevel Phase-Change Memory Element and Operating Method” and describes a multilevel phase change memory element and operating method and electrodes, which are configured in a parallel structure to form a memory cell, the multilevel phase change memory element having more bits and higher capacity than that of a memory element with a single phase-change layer. Ex. 1010, codes (54), (57). Li employs a voltage-drive mode to control and drive the memory element such that multilevel memory states may be achieved by imposing different voltage levels. *Id.*

2. Analysis of Claim 3

Claim 3 depends from claim 1 and additionally recites that “the nonvolatile memory for storage is a phase change memory.” Ex. 1004,

6:18–19. Petitioner contends Li discloses a phase change memory, and that it would have been obvious to use a phase change memory in place of Lee’s flash memory, with a reasonable expectation of success, because phase-change nonvolatile memory was well known and offered advantages relative to false memory such as small volume and fast operation speed. Pet. 64–65 (citing Ex. 1006 ¶¶ 299–301; Ex. 1007 ¶ 61; Ex. 1010, 1:16–46; Ex. 1022 ¶ 5). Petitioner provides reasoning, supported by testimony from Dr. Levy, to combine Lee with Li. *Id.* Similarly, Petitioner provides reasoning, supported by testimony from Dr. Levy, to combine Tsunoda and Kolokowsky with Li. *Id.* at 67–68 (citing 1006 ¶¶ 309–311; Ex. 1008 ¶ 94; Ex. 1010, code (57) (Abstr.), 1:16–46; Ex. 1022 ¶ 5).

Patent Owner does not respond to these arguments. *See generally* PO Resp. 39–40.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee and Li, or Tsunoda, Kolokowsky, and Li teach the limitations in claim 3 and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

A. Grounds 4 and 6: Obviousness Based on Lee and Miura (Ground 4) and Tsunoda, Kolokowsky, and Miura (Ground 6)

Petitioner contends claim 7 would have been obvious over the combination of Lee and Miura, and the combination of Tsunoda, Kolokowsky, and Miura. Pet. 8, 65–70. After reviewing the entire record developed at trial, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 7 is unpatentable over these combinations

1. Miura (Ex. 1011)

Miura is titled “Memory Module, Memory System, and Information Device” and “relates to a memory system including a dynamic random access memory (DRAM) and a method of controlling the memory system.” Ex. 1011, code (54) (Title), ¶ 1. Miura’s memory system includes large-capacity ROM and RAM in which high-speed reading and writing are enabled. *Id.* at code (57) (Abstr.). Miura discloses a “memory system including a non-volatile memory (CHIP1), DRAM (CHIP3), a control circuit (CHIP2) and an information processing device (CHIP4),” with data in FLASH being transferred to SRAM or DRAM in advance to speed up, the data transfer between the non-volatile memory (FLASH) and DRAM (CHIP3) being performed in the background. *Id.* Miura explains “[a]s data in FLASH can be read at the similar speed to that of DRAM by securing a region in which the data in FLASH can be copied in DRAM and transferring the data to DRAM in advance immediately after power is turned on or by a load instruction, the performance and the function of a mobile device can be enhanced.” *Id.*

2. Analysis of Claim 7

Claim 7 depends from claim 1 and additionally recites that “the volatile random access memory is a SRAM with at least one port for read and write access.” Ex. 1004, 6:26–28. Petitioner contends Miura discloses SRAM with at least one port for read and write access, and that it would have been obvious to use Miura’s SRAM in place of Lee’s or Tsunoda’s SDRAM, with a reasonable expectation of success, because it was widely known that SRAM had advantages relative to DRAM, including speed and not requiring refresh operations. Pet. 65–67 (citing Ex. 1006 ¶¶ 303–306;

Ex. 1007 ¶¶ 61, 118; Ex. 1011, code (57) (Abstr.); Ex. 1023, 1:36–60). Petitioner provides reasoning, supported by testimony from Dr. Levy, to combine Lee with Miura. *Id.* Similarly, Petitioner provides reasoning, supported by testimony from Dr. Levy, to combine Tsunoda and Kolokowsky with Miura. *Id.* at 68–70 (citing 1006 ¶¶ 315–317; Ex. 1008 ¶ 94; Ex. 1011, code (57) (Abstr.), ¶¶ 57, 59; Ex. 1016, 57; Ex. 1022 ¶ 5; Ex. 1023, 1:36–60).

Patent Owner does not respond to these arguments. *See* PO Resp. 39–40.

After considering the evidence and arguments of the complete record, we determine that Petitioner has shown, by a preponderance of the evidence, that Lee and Miura, or Tsunoda, Kolokowsky, and Miura teach the limitations in claim 7 and that a person of ordinary skill in the art would have had a reason to combine the references in the manner Petitioner proposes, with a reasonable expectation of success.

III. CONCLUSION¹⁵

Based on the arguments and evidence presented by the parties during this entire proceeding, we determine that Petitioner has established by a

¹⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

preponderance of the evidence that claims 1–5 and 7–13 of the '219 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 1–5 and 7–13 of the '219 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 2, 8–13	103(a)	Lee	1, 2, 8–13	
1, 2, 4, 5, 8, 10–13	103(a)	Tsunoda and Kolokowsky	1, 2, 4, 5, 8, 10–13	
3	103(a)	Lee and Li	3	
7	103(a)	Lee and Miura	7	
3	103(a)	Tsunoda, Kolokowsky, and Li	3	
7	103(a)	Tsunoda, Kolokowsky, and Miura	7	
Overall Outcome			1–5, 7–13	

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