

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

IMPINJ, INC.,
Petitioner,

v.

NXP B.V.,
Patent Owner.

IPR2021-00001
Patent 6,819,092 B2

Before MIRIAM L. QUINN, MICHELLE N. WORMMEESTER, and
STACY B. MARGOLIES, *Administrative Patent Judges*.

QUINN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Impinj, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–4 of U.S. Patent No. 6,819,092 B2 (Ex. 1001, “the ’092 patent”). Paper 1 (“Pet.”). After considering the merits of the Petition and the arguments against institution by Patent Owner, we instituted *inter partes* review. Paper 14 (“Decision on Institution,” “Dec. on Inst.”).

During the trial phase, Patent Owner filed a Response (Paper 16, “PO Resp.”), Petitioner filed a Reply (Paper 19, “Reply”), and Patent Owner filed a Sur-reply (Paper 20, “Sur-reply”). We held oral argument on February 8, 2022, the transcript of which is filed in the record. Paper 29 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claims 1–4 of the ’092 patent are unpatentable. See 35 U.S.C. § 316(e) (2018).

A. *Real Parties in Interest*

Petitioner identifies itself as a real party in interest. Pet. 1. Patent Owner identifies the following entities as real parties in interest: NXP B.V., NXP USA, Inc., NXP Semiconductors N.V., and Freescale Semiconductor Holdings V, Inc. Paper 4, 1.

B. *Related Matters*

The parties indicate that the ’092 patent has been asserted in the following proceeding: *NXP USA, Inc. and NXP B.V. v. Impinj, Inc.*, Case No. 1:19-cv-01875-RGA (D. Del.). Pet. 1. Petitioner indicates that the district court proceeding had been transferred to the Western District of Washington: *NXP USA, Inc., and NXP B.V. v. Impinj, Inc.*, Case No. 2:20-cv-01503-RSM-MAT (W.D. Wash.). Pet. 1; Paper 4, 1.

C. The '092 Patent

The '092 patent relates to a digitally switchable current source. Ex. 1001, code (54). The '092 patent states that “an object of the invention” is “to provide a digitally switchable current source for arbitrary current values at which no dangerous current peaks are produced at the switching instants.” *Id.* at 1:19–22. Figure 1, reproduced below, is a circuit diagram of the current source. *Id.* at 1:49–50.

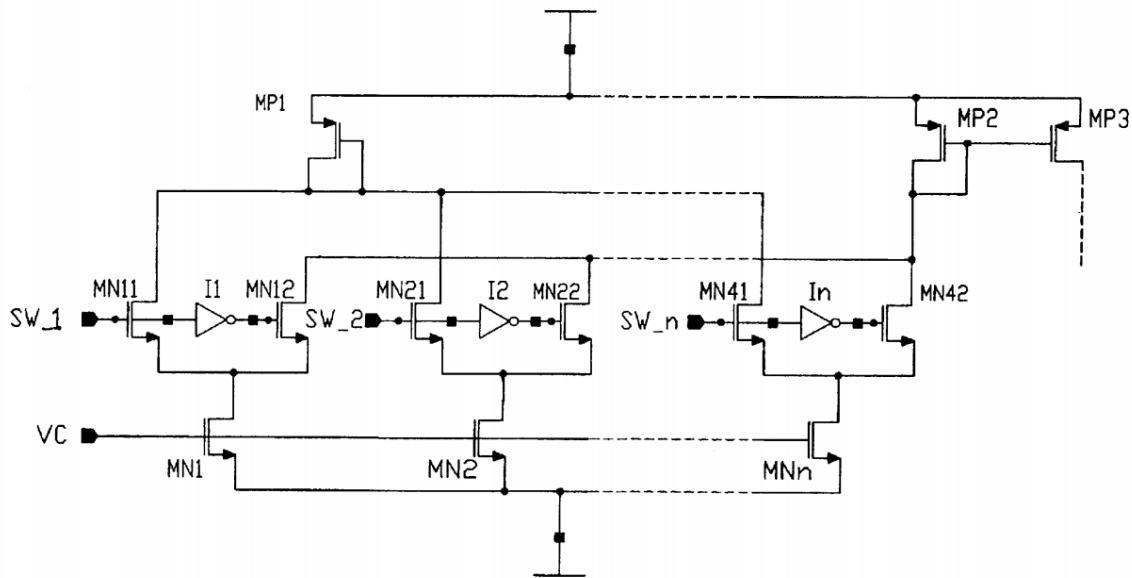


FIG.1

Figure 1 illustrates a plurality of adjusting transistors MN1–MNn controlled by a common analog voltage VC and operating as a current source. *Id.* at 1:53–56. Two switching transistors MN11 and MN12 are arranged in series with adjusting transistor MN1, and two switching transistors MN21 and MN22 are arranged in series with adjusting transistor MN2. *Id.* at 1:56–60, Fig. 1. The control electrodes or gates of the switching transistors are controlled by a digital signal SW (and its inverse signal). *Id.* at 1:56–60. For example, MN11 is digitally controlled by signal

SW₁ and MN12 is digitally controlled by the inverse of the SW₁ signal. *Id.* at Fig. 1. The outputs of the switching transistors are connected to load transistors, MP1 and MP2, resulting in alternate current paths. *Id.* at 1:60–63. Specifically, the '092 patent explains that when “applying a high signal to the switching inputs SW₁ . . . SW_n, there is a switch-over from a current through the transistor MP1 to a current path through the transistor MP2.” *Id.* at 1:63–66. And that because one of the switching transistors is controlled by the inverse of the switching input, at switch-back to a lower signal, one of the switching transistors is controlled to output current in the forward direction. *Id.* at 1:66–2:5. “Since the current flow through the transistors MN1 . . . MN_n is thus not interrupted, no current spikes occur at the switching instants.” *Id.* at 2:5–7.

The '092 patent further describes adapting the current source for a phase-locked loop (“PLL”) circuit. *Id.* at 2:13–15. A PLL circuit “is a frequency-selective circuit in which a phase detector, a filter, an amplifier[,] and a voltage-controlled oscillator (VCO) are arranged to form a control circuit.” *Id.* at 2:14–17. The digitally switchable current source is modified to convert a control voltage (VC) of the oscillator to an equivalent current that is applied, through three possible paths, to the output transistor MP2. *Id.* at 2:17–22. The output current then influences the frequency of the oscillator. *Id.* “[T]he advantage of the circuit is particularly the reduction of frequency jitter of the oscillator because current spikes are avoided during the switching instants.” *Id.* at 2:42–45.

D. Illustrative Claim

Of the challenged claims, claims 1 and 4 are independent. Claims 2 and 3 depend from claim 1, which is reproduced below.

1. A digitally switchable current source, characterized in that two switching transistors, which are controllable by means of a digital control signal, are arranged in series with at least two current source transistors which are controllable by means of an analog voltage and are parallel arranged in a branch, wherein current flowing through the source transistors remains constant during state transitions of the digital control signal.

Ex. 1001, 2:56–63. Claim 4 is directed to a phase-locked loop circuit and recites the same limitations as claim 1, except that it further recites “a voltage-controlled oscillator adapted to provide an output frequency in response to the current source transistors.” *Id.* at 4:5–7.

E. Evidence and Grounds

The asserted grounds in this proceeding involve the following prior art references:

- a) *Tamura*: US 6,247,138 B1, filed on June 8, 1998 and issued June 12, 2001, filed as Exhibit 1003;
- b) *Brown*: US 5,121,085, filed on June 28, 1991 and issued June 9, 1992, filed as Exhibit 1004; and
- c) *Smith*: US 5,402,358, filed on October 29, 1993 and issued March 28, 1995, filed as Exhibit 1005.

Petitioner asserts the following grounds of unpatentability (Pet. 3):

Claims Challenged	35 U.S.C. §	Reference(s)
1–3	102(e)	Tamura

Claims Challenged	35 U.S.C. §	Reference(s)
1–4	103(a)	Tamura
1–4	103(a)	Tamura and the knowledge of a person of ordinary skill in the art
1–4	103(a)	Tamura, Smith
1–4	102(b)	Brown
1–4	103(a)	Brown and the knowledge of a person of ordinary skill in the art

Petitioner also relies on a Declaration of James Stevenson Kenney, Ph.D., filed as Exhibit 1006 (“Kenney Decl.”) and a Reply Declaration of James Stevenson Kenney, Ph.D., filed as Exhibit 1016 (“Reply Kenney Decl.”). Patent Owner relies on a declaration of Vijay K. Madiseti, Ph.D. in support of its Patent Owner Response. Ex. 2006 (“Madiseti Decl.”).

II. DISCUSSION

A. Claim Construction

In an *inter partes* review requested in a petition filed on or after November 13, 2018, we apply the same claim construction standard used in district courts, namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written

description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner contends that a phrase recited in independent claims 1 and 4 may require construction because the plain language creates at least two ambiguities. Pet. 9. The claims recite “two switching transistors . . . are arranged in series with at least two current source transistors which are controllable by means of an analog voltage and are parallel arranged in a branch.” Ex. 1001, 2:57–61 (the “current source transistors” limitation). Petitioner proposes a construction for this phrase as follows: “at least two sets of two switching transistors, each set arranged in series with a current source transistor, where the sets of two switching transistors are in respective branches that are arranged in parallel.” Pet. 14. Petitioner argues that Figure 1 and the prosecution history of the ’092 patent support Petitioner’s proposed construction. *Id.* at 10–14.

In our Decision on Institution, we adopted Petitioner’s proposed construction after considering that Patent Owner did not address Petitioner’s proposed claim construction. Dec. on Inst. 6–7 (citing Prelim. Resp. 8). During trial, another issue concerning the scope of the “current source transistors” limitation arose with respect to the meaning of “controllable.” For example, Petitioner argues that Tamura discloses pMOS transistors that are “controllable by means of an analog voltage” because they are operated by applying a fixed reference voltage V_r , which is an analog voltage. Pet. 21–22 (citing Ex. 1003, 48:2–4; Kenney Decl. ¶ 89); Reply 4–6 (arguing that applying a voltage to a transistor’s gate controls the transistor and that the ’092 patent does not require more). And Patent Owner responds that the

term “controllable” cannot be interpreted to merely turn on the required transistors. PO Resp. 6–7. According to Patent Owner, the ’092 patent requires that the analog voltage “control” the current flow in the adjusting transistors (i.e., the claimed “current source transistors”), and, therefore, the term “controllable” would mean: “adjusted by means of a common analog voltage to regulate (e.g., increase or decrease) the current flow.” PO Resp. 1, 10 (citing Madisetti Decl. ¶ 139); Sur-reply 1. In other words, Patent Owner argues that the applied voltage must vary; it cannot merely be a fixed voltage.

“Controllable” Term

The issue for us to decide is whether the ordinary and customary meaning of the term “controllable” in the context of the ’092 patent, as that term would have been understood by a person of ordinary skill in the art at the time of the invention, would have required adjusting “to regulate (e.g., increase or decrease) the current flow.” PO Resp. 10; *see Phillips*, 415 F.3d at 1312–13. After evaluating the parties’ arguments concerning the proper scope of the term, we determine that “controllable” does not require adjusting by increasing or decreasing current flow, as argued by Patent Owner.

The claim recites the term “controllable” with regard to two distinct transistor operations, informing us that the term should not be limited to account for the operation of only the “current source transistors.” For example, the claim recites, as we have stated above, that the “current source transistors” are “controllable by means of an analog voltage.” Ex. 1001, 2:59–60. But the claim also recites that the “two switching transistors” are “controllable by means of a digital control signal.” *Id.* at 2:57–58. Thus,

both the “current source transistors” and the “switching transistors” are “controllable” by means of the recited applied voltage, either digital or analog. This use of the word “controllable” in this manner informs us that the claim does not specify any particular adjustment of the recited voltage in relation to the recited transistors. In other words, however the analog voltage impacts the “current source transistors” must be similar to the impact the digital voltage has on the “switching transistors.” Thus, it is not persuasive, in the context of the claim language, to argue that the word “controllable,” as it refers to the “current source transistors,” would involve adjusting to increase or decrease the current flow without explaining how such adjustment would also be applicable to the “switching transistors” (which are “controllable by means of a digital control signal”—and, thus, not involving a varying voltage that increases or decreases the current flow).

We are also not persuaded that the ’092 patent specification warrants interpreting “controllable” to include the adjustment of current flow argued by Patent Owner. Patent Owner relies on the ’092 patent description of “adjusting transistors” as corresponding to the claimed “current source transistors” and as providing the contour of the “controlling” recitation. For instance, Patent Owner posits that the “claimed invention is a controllable current source that includes both adjusting transistors and switchable output stages,” and that the specification describes “controllable current sources” as including “adjusting transistors [that] are driven by an analog control voltage” and “switchable output stages.” Sur-reply 4 (citing Ex. 1001, 1:6–13). According to Patent Owner, in the embodiment shown in Figure 1, the amount of the current that flows through a switched path “is controlled (e.g., adjusted, regulated) by the analog control voltage VC.” *Id.* (citing Madisetti Decl. ¶ 134). Patent Owner also argues that the embodiment of

Figure 2 supports its contention because the control voltage VC is “converted . . . to an equivalent current and applied via three possible paths to the output transistor MP2 which thereby influences the frequency of the oscillator.” PO Resp. 7 (citing Ex. 1001, 2:17–22); *See also* Sur-reply 4–5 (citing Madisetti Decl. ¶ 36); Tr. 34:5–22. In such an embodiment, according to Patent Owner, “control voltage adjustments would regulate the current in order to adjust the oscillator frequency.” PO Resp. 7 (citing Madisetti Decl. ¶ 136).

We do not agree with Patent Owner that the ’092 specification supports the desired construction. First, the specification describes the “controllable current sources” as including “adjusting transistors . . . driven by an analog voltage.” Ex. 1001, 1:10–11. This description does not specify in what manner the adjusting transistors are “driven”—whether the output of these adjusting transistors must be of a varying current flow as a result of a varying voltage. Further, the specification describes known “constant current sources” as having “switchable output stages” and those whose “output current must be corrected to a given value after the manufacturing process or whose output current must be varied within given limits.” *Id.* at 1:6–9, 12–13. This description too lacks any specificity regarding how transistors in a “constant current source” are applied a varying voltage or when and how their output is varied, so that we could interpret that a transistor is “controllable,” in the context of the ’092 patent, as Patent Owner argues.

Other parts of the specification are equally vague and, thus, unpersuasive as support for Patent Owner’s desired construction. For instance, with respect to the Figure 1 embodiment, the specification

describes “a plurality of adjusting transistors MN1 . . . MNn controlled by a common analog voltage VC and operating as a current source.” Ex. 1001, 1:54–56. The “controlling” is not explained in any manner that is discernible from the given explanation. Nor do we see the ’092 patent describe “controlling” by how the adjusting transistors are connected to and interact with the next stage of switchable transistors. In another portion, the specification describes that “always one of the switching transistors . . . are controlled in the forward direction.” *Id.* at 2:3–5. The specification also expresses a desired outcome of this control operation: “Since the current flow through the [adjusting] transistors MN1 . . . MNn is thus not interrupted, no current spikes occur at the switching instants.” *Id.* at 2:5–7. In this manner, the specification describes the “control” operation of switching transistors to be on or off, and to direct the path of the current that is output by the adjusting transistors. But the controlling of the adjusting transistors is not explained in a way that requires modifying an analog voltage to increase or decrease current as needed. The specification describes the arrangement of the adjusting transistors and the switchable transistors with focus on the continuous supply of a current source (i.e., without interruptions or spikes), regardless of whether that current source must vary in value, independently of the switching operation, and according to an applied voltage.

The description of the embodiment shown in Figure 2 also does not support Patent Owner’s contentions. The specification explains that the control voltage applied to the adjusting transistors is converted to an equivalent current and applied to the load via three different paths to influence the oscillator frequency. *Id.* at 2:17–21. That is, whatever current

is output by the various adjusting transistors is passed to the load depending on which switching transistors are switched on. *Id.* at 2:22–27. The explanation of this Figure-2 embodiment proffered by Petitioner’s expert, Dr. Kenney, is informative and persuasive. He explains, and we credit this testimony, that according to the signal UP or DOWN provided to the switching transistors, the transistor current output by specific combinations of adjusting transistors will be summed and passed to the load. Reply Kenney Decl. ¶¶ 12–13. The specification’s description of Figure 2 does not attribute to the adjusting transistors any operation of varying outputs of current depending on the voltage applied to those transistors. *See* Tr. 35:2–36:2 (Patent Owner arguing that operation of Figure 2 as described by Petitioner is not disputed yet focuses on switchable control, but the patent does not describe adjusting the control voltage VC). In sum, we do not read the Figure-2 embodiment as supporting Patent Owner’s contention.

Now we turn to whether the expert testimony sheds light into the customary meaning of the word “controllable” in the context of the ’092 patent as the term would be understood by a person of ordinary skill in the art. Dr. Madisetti opines that in the context of the ’092 patent, the word “control” is synonymous to “regulate,” as he explains that “an analog voltage is used to control (or regulate) the current flow in contrast to a digital voltage that is used to switch current on or off.” Madisetti Decl. ¶ 135. He agrees with Dr. Kenney’s general explanation of how transistors work in analog mode and as switches. *Id.* But Dr. Madisetti, without stating whether the “current source transistors” are controlled in an analog mode, nevertheless states that “adjustments of the analog control voltage would regulate the current in order to adjust the oscillator frequency,” referring to

the embodiment of Figure 2, and that the '092 patent specification “is inconsistent with a design that used a fixed voltage, such as a digital voltage, to simply turn on or off the transistors.” *Id.* ¶ 136.

In contrast, Dr. Kenney opines on the basic operation of a transistor in that an analog voltage applied to the current source transistors *would control* the transistor because a voltage applied to a gate terminal controls what the transistor does. Reply Kenney Decl. ¶¶ 6–7. He explains that an analog voltage above 0 volts but below the supply voltage, applied to the gate terminal of the transistor, “[will] set the current passing from source to drain to be proportional to the value of the applied voltage.” *Id.* ¶ 7. When operating as a switch, Dr. Kenney testifies, a HIGH value digital signal (i.e., a voltage close to, or at, the supply voltage) will cause the transistor to pass the full current from source to drain. *Id.* And, according to Dr. Kenney, whether operating in switch or analog mode, when connecting the gate to GROUND (applying near 0 volts) no current will pass from source to drain of the transistor. *Id.* Thus, we understand Dr. Kenney’s testimony to explain the “controlling” of a transistor by an *analog voltage* because depending on the voltage applied, the transistor will output a proportional value of current. And controlling the transistor by a HIGH voltage (one of the two values of a *digital voltage*) would set the transistor to output the full current. We find Dr. Kenney’s testimony in this regard persuasive as it explains the “controlling” of a transistor in the context of both digital and analog voltage applications, consistent with the recitation of controlling transistors by analog and digital voltages in the '092 patent claims.

Furthermore, Dr. Kenney explains what a person of ordinary skill in the art would have understood by “adjusting” a transistor according to the operation of the '092 patent embodiments in a manner that is consistent with

the claim language. Specifically, Dr. Kenney testifies that the “adjusting” of the “adjusting transistors” indicates to a person of ordinary skill in the art that the “transistor is capable of being adjusted to set some desired current output, but [that person] would not understand [the ‘adjusting’] to imply, let alone require, that the transistors actually must be adjusted up or down.”

Reply Kenney Decl. ¶ 56. Dr. Kenney also explains that in transistor operation, “regulating” (which Patent Owner equates with “controlling”) the output of a transistor does not require changing the voltage *during the operation of the circuit*. *Id.* ¶ 11. He testifies that “a [person of ordinary skill in the art] would understand that applying a fixed voltage to a transistor to produce a fixed current would be considered regulating the transistor to produce that current.” *Id.* We agree with this testimony and give it credit over the testimony of Dr. Madisetti, who supports his testimony with a narrow reading of the ’092 patent (requiring adjustments not described) and a narrow interpretation of how a transistor may be “controlled” by requiring adjustments of voltage levels during operation of the circuit without sufficient support in the ’092 patent or the claim language.

Rather, we are persuaded that Dr. Kenney’s testimony aligns more closely with the disclosure of the ’092 patent, which is silent on any adjustments of applied voltage levels during operation of the circuit, as discussed above. Dr. Kenney’s explanation is also more consistent with the claim language itself, which does not differentiate between controlling the “current source transistors” and the “switching transistors,” leading us to conclude that the word “controlling” means what Dr. Kenney explains: applying a voltage at a particular level to obtain a desired current, without requiring changing that voltage during the circuit operation. *See also* Ex. 1001, 1:37–38 (“The invention has the advantage that an output current

of a defined value can be generated.”), 1:42–43 (“The value of the generated current results as a sum from the actively switched paths.”). In other words, the claims do not exclude controlling a “current source transistor” by applying an analog voltage that is *fixed*, such that the “current source transistor” would have a certain current value during operation of the circuit.

Accordingly, we reject Patent Owner’s proposed claim construction that limits the term “controllable” for the “current source transistors” to adjusting to regulate (e.g., increase or decrease) the current flow.

Patent Owner’s proposed construction of “controlling” also includes another phrase seeking to limit the analog voltage to a “common” analog voltage. We need not resolve that issue because it is not necessary for us to determine the patentability of the challenged claims in this Final Written Decision. We also need not construe explicitly any other term for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The “person of ordinary skill in the art” is a hypothetical construct, from whose

vantage point obviousness is assessed. *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). “This legal construct is akin to the ‘reasonable person’ used as a reference in negligence determinations” and “also presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Petitioner proffers that a person having ordinary skill in the art “would have had at least a bachelor’s degree in electrical engineering and at least 1-2 years of experience in circuit design, or equivalent industry experience in analog circuit design.” Pet. 8 (citing Kenney Decl. ¶¶ 20–24). Patent Owner neither challenges Petitioner’s formulation nor suggests an alternative level of a person having ordinary skill in the art. *See generally* PO Resp.; *see generally* Madisetti Decl. (Patent Owner’s declarant also not discussing this issue). We adopt Petitioner’s level of ordinary skill in the art as it aligns with the technology of the ’092 patent and descriptions of the art in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (stating that the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown); *see, e.g.*, Ex. 1001, Abstr. (describing arrangement of transistors to provide digitally switchable current source so no dangerous current spikes are produced); Ex. 1003, Abstr. (describing a timing adjusting circuit to generate a command signal that adjusts the clock).

C. Obviousness Based on Tamura

Petitioner asserts that claims 1–4 would have been obvious over Tamura. Pet. 3, 15–33. Our analysis of this obviousness ground begins with an overview of Tamura.

1. Overview of Tamura (Ex. 1003)

Tamura relates to timing signal generating circuits. Ex. 1003, 1:11–19. In particular, Tamura uses a phase interpolator that generates from a plurality of clocks with different delay amounts a new clock having an intermediate delay amount. *Id.* at 3:41–47. One embodiment of such a phase interpolator utilizes constant current sources or bias signals. *Id.* at Fig. 80, 45:66–46:1, 46:8–12, 46:43–47. An embodiment of a bias signal generating circuit for a phase interpolator is shown in Figure 82, reproduced below.

Fig. 82

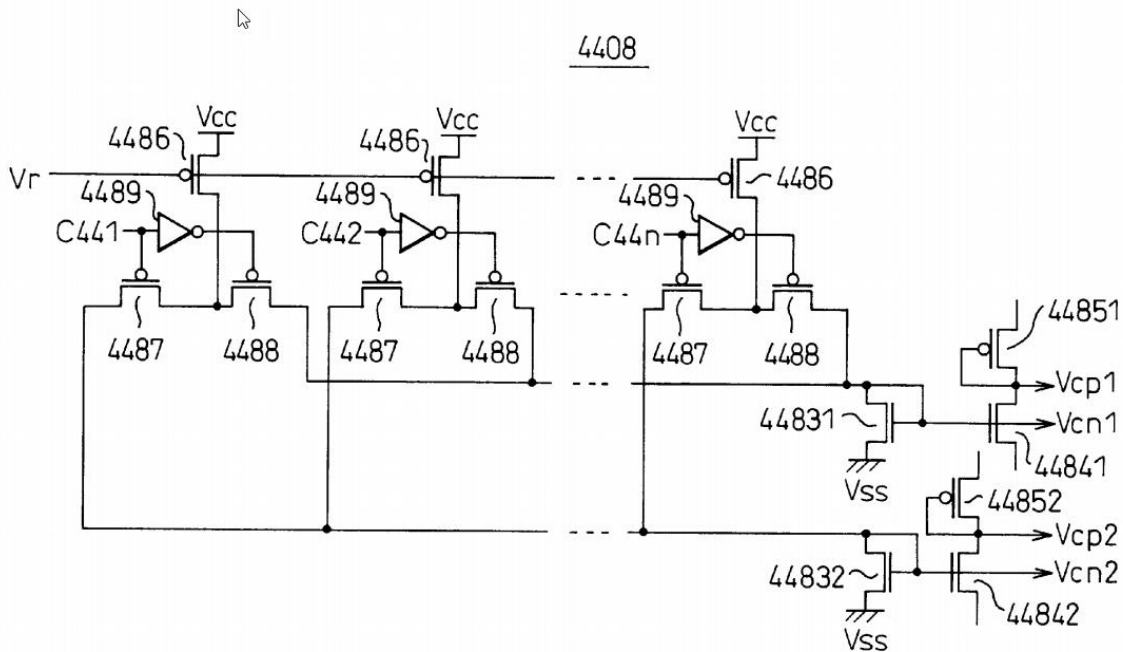


Figure 82 depicts each pMOS transistor 4486 being supplied with a reference voltage (V_r) and connected to one end of each of pMOS transistors 4487 and 4488, which are arranged in pairs. *Id.* at 48:1–5. The switching operation of transistors 4487 and 4488 is controlled by digital signals C441 to C44n. *Id.* at 48:5–7. In particular, Tamura explains that transistors 4487, in the respective transistor pairs, are supplied at their gates with corresponding control signals C441 to C44n, while the transistors 4488 in the respective transistor pairs are supplied at their gates with the control signals ($/C441$ to $/C44n$) inverted by respective inverters 4489. *Id.* at 48:7–12. “Accordingly, in each transistor pair[,], one of the transistors, 4487 or 4488, is ON and the other is OFF.” *Id.* at 48:11–13. The other ends of transistors 4487 in the respective transistor pairs are connected in common so that the sum of the currents flowing through transistors 4487, when in the ON state, flows to nMOS transistor 44832. *Id.* at 48:14–17. The other ends

of transistors 4488 in the respective transistor pairs are also connected in common so that the sum of the currents flowing through transistors 4488 in the ON state flows to nMOS transistor 44831. *Id.* at 48:17–21. From the currents output by nMOS transistors 44831 and 44832 the bias signals Vcp1, Vcn1 and Vcp2, Vcn2 are obtained. *Id.* at 48:21–28.

Tamura explains that the “output of the current-control type D/A converter for controlling the output value of the current source is switched for connection to the complementary output nodes.” *Id.* at 48:29–33. More specifically, Tamura states that “the output current of the D/A converter is always maintained constant” and that “the resulting advantage [is] that transient response spikes, as seen when the current is interrupted, are eliminated.” *Id.* at 48:33–37.

2. Obviousness Analysis

The Petition sets forth that Tamura teaches or suggests all the recited limitations of claims 1–4. Pet. 19–27. Patent Owner presents two arguments in opposition. PO Resp. 10–17; Sur-reply 10–15. First, as to claim 1, Patent Owner argues that Tamura does not disclose the “controllable” limitation addressed above in connection with claim construction. PO Resp. 13–14; Sur-reply 10–12. Second, as to claim 4, Patent Owner argues that Petitioner’s challenge relies on a combination of multiple embodiments of Tamura without sufficient motivation to combine. PO Resp. 15–17; Sur-reply 12–15. After considering the evidence and arguments of record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–4 would have been obvious over Tamura alone.

i. *Independent Claim 1*

We start our analysis with the preamble (although neither party alleges that the preamble is a limitation): “A digitally switchable current source.” The Petition addresses how Tamura teaches the preamble by disclosing a bias signal generating circuit as shown in Figure 82, reproduced below, with annotations provided by Petitioner. Pet. 19, 21.

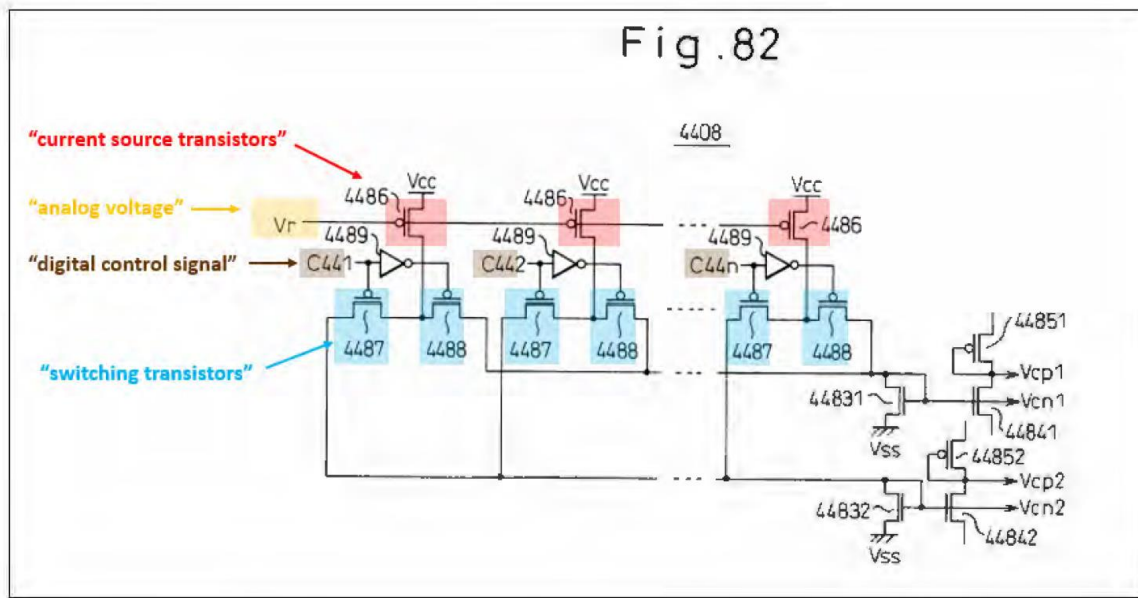


Figure 82 of Tamura is a circuit diagram illustrating an example of a circuit for generating a bias signal in a phase interpolator. Ex. 1003, 11:44–46. According to Petitioner, the depicted bias signal generator is a current source because “the output of the current-control type D/A converter for controlling the output value of the current source is switched for connection to the complementary output nodes.” *Id.* at 48:30–32. We agree with Petitioner. In this passage, Tamura explains that the bias signal generator comprises a current source whose output is digitally switched. Patent Owner does not present argument otherwise. We agree with Petitioner that Tamura teaches the preamble, although it has not been shown to be, and we take no position on whether it is, a claim limitation.

(1) Two Switching Transistors

Claim 1 next recites the “two switching transistors, which are controllable by means of a digital control signal.” For these “two switching transistors” limitation, the Petition points to Tamura’s disclosure of pairs of pMOS transistors 4487 and 4488, that are each controlled by digital control signals C44n. Pet. 19–20 (citing Ex. 1003, 48:2–11). Figure 82 reproduced previously shows multiple pairs of transistors 4487 and 4488 highlighted in blue and the digital control signals C44n highlighted in brown. We agree with Petitioner that Tamura discloses the recited “two switching transistors” and that these are “controllable by means of a digital control signal” because pMOS transistors 4487 and 4488 are switched ON and OFF according to the control signals applied. Ex. 1003, 48:5–13 (stating in particular that the transistors 4487 are supplied at their gates with control signals C441 to C44n, while transistors 4488 are supplied at their gates with the inverted control signals /C441 to /C44n and that, therefore, in each transistor pair, one transistor is ON while the other is OFF); Kenney Decl. ¶ 86. Patent Owner does not present argument concerning this limitation. We determine that Petitioner has shown by a preponderance of the evidence that Tamura teaches the “two switching transistors,” as recited in claim 1.

(2) At Least Two Current Source Transistors

Now we address the next pair of recited transistors: “at least two current source transistors which are controllable by means of an analog voltage.” Petitioner relies on Tamura’s pMOS transistors 4486 (highlighted in red in the annotated Figure 82 discussed above) as being the “at least two current source transistors.” Pet. 20–21 (citing Ex. 1003, 42:2–5); Kenney Decl. ¶¶ 87–91. Petitioner states that Tamura’s pMOS transistors 4486 are

connected to the source of each of pMOS transistors 4487 and 4488, and that, therefore, a person of ordinary skill in the art would have understood that transistors 4486 are “current sources.” *Id.* (citing Ex. 1003, 48:15–21; Kenney Decl. ¶ 88). In particular, Petitioner explains that transistors 4486 are the source of the current that flows through pMOS transistors 4487 and 4488 (the recited “switching transistors”), that ultimately feed nMOS transistors 44831 and 44832. *Id.* at 21. We agree with Petitioner that transistors 4486 are current sources because their output current flows through the transistor pair 4487 and 4488 and thereby are the source of the current that flows to the transistors that obtain the bias signals. Ex. 1003, 48:15–21; Kenney Decl. ¶ 88.

The claim further requires that these “current source transistors” be “controllable by means of an analog voltage.” The Petition sets forth that Tamura’s Figure 82 embodiment shows a voltage V_r (highlighted in yellow in the annotated Figure 82 discussed above) applied to the gate of transistors 4486, and Tamura explains that transistors 4482 are each supplied with a reference voltage V_r . Pet. 21 (citing Ex. 1003, 48:2–4). According to Petitioner, reference voltage V_r is an analog voltage. *Id.* (relying on Kenney Decl. ¶ 89). Dr. Kenney testifies that a person of ordinary skill in the art “would understand reference voltage V_r to be analog, because it sets the current in the transistors 4486 to a specific value dependent on the voltage supplied to the transistor gates.” Kenney Decl. ¶ 89. Dr. Kenney further testifies that Tamura also describes the reference voltage V_r as being $\frac{1}{2}$ VCC, which is not a standard digital logic level, indicating that V_r is analog, not digital. *Id.* (further explaining that Tamura’s voltage V_r is analog because it is compared with an analog voltage waveform for a comparator to

output a digital value based on the comparison between the two analog waveforms (one of which is V_r). We agree that Tamura discloses that voltage V_r applied to the gates of transistors 4486 (the recited “current source transistors”) is an analog signal. Ex. 1003, 48:2–4; Kenney Decl. ¶ 89. Patent Owner also does not dispute that V_r is an analog voltage. Tr. 15:1–19, 38:1–7; *see generally* PO Resp., Sur-reply.

The issue Patent Owner raises is whether the application of V_r would be such that the current of transistors 4486 would be adjusted during operation of the circuit in accordance with the claim construction Patent Owner put forth for the claim term “controllable.” *See* PO Resp. 13–14 (arguing that “Tamura does not teach V_r as a control voltage that is used to adjust transistors 4486 or to set the current to some specific value” and that V_r is “fixed and thus is not ‘controllable.’”). We analyze the scope of this limitation above with regard to claim construction of the term “controllable” and determine that this limitation does not require that the analog voltage be applied so as to increase and decrease the output current as the circuit operates. *See supra* Section II.A. We are persuaded by and agree with Dr. Kenney’s testimony that a fixed analog voltage is not excluded by the scope of how a person of ordinary skill in the art would understand a transistor to be controlled by an analog voltage. Reply Kenney Decl. ¶ 11.

Thus, we are unpersuaded by Patent Owner’s arguments that Tamura’s transistor 4486 is not “controllable” by Tamura’s voltage V_r merely because V_r is a “fixed” analog voltage. We also are not persuaded by Dr. Madisetti’s testimony that the analog voltage V_r does not “set” the current in transistors 4486. Madisetti Decl. ¶ 146 (stating that “it is my opinion that V_r is *not* used to adjust transistors 4486 to control the current

flow or to set the current”(emphasis added)). Rather, we credit the testimony of Dr. Kenney who testifies that Tamura’s “transistors 4486 are operating in an analog mode to produce a constant current related to the voltage V_r .” Reply Kenney Decl. ¶ 17. As discussed above, it is undisputed that Tamura’s transistors 4486 are applied an analog voltage. And according to Dr. Kenney’s testimony, which we credit, the analog voltage V_r controls transistors 4486 because in an analog mode a transistor would output a current proportional to the voltage applied. *Id.* ¶ 7 (“[A] voltage applied to the gate terminal controls what the transistor does. In its simplest terms, applying an analog voltage above 0 volts, but below the supply voltage to the gate[,] can set the current passing from source to drain to be proportional to the value of the applied voltage.”).

Consequently, we determine that Petitioner has demonstrated by a preponderance of the evidence that Tamura teaches “at least two current source transistors which are controllable by means of an analog voltage.”

(3) “Arranged in Series” and “Parallel Arranged in a Branch”

We turn now to determine whether Petitioner has shown that the above-identified transistors are arranged as the claim requires. First, claim 1 requires that the two switching transistors are “arranged in series with” the at least two current source transistors. Petitioner relies on Tamura’s Figure 82, reproduced below.

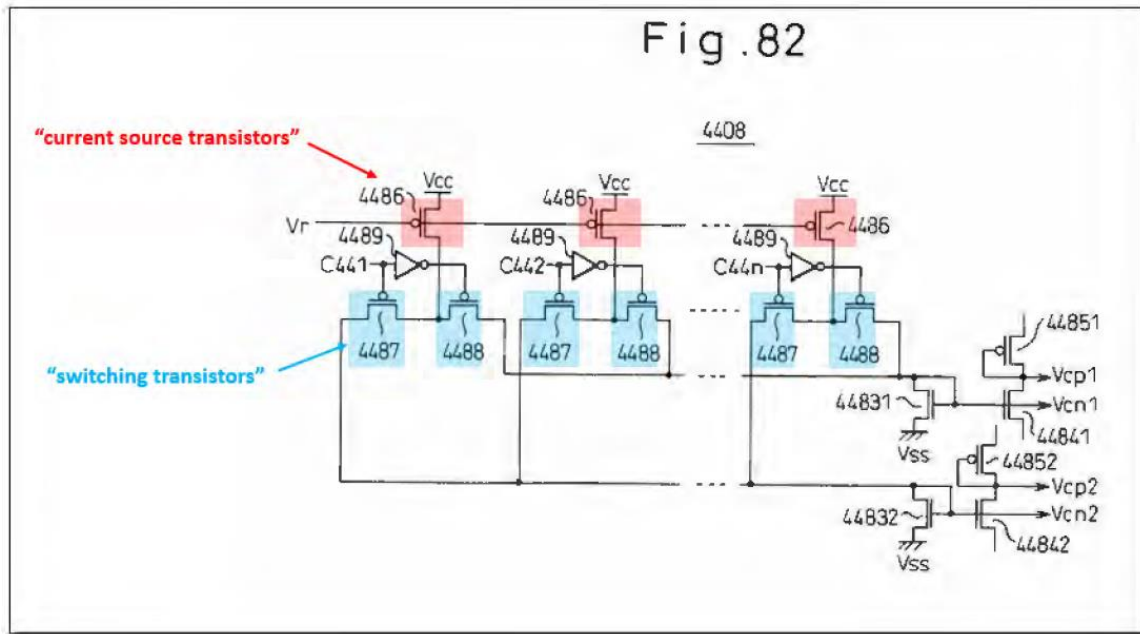


Figure 82 of Tamura shows a circuit diagram with annotations added by Petitioner showing the “current source transistors” (transistors 4486) highlighted in red and the “switching transistors” in Tamura (transistors 4487 and 4488) highlighted in blue. Pet. 23. Petitioner argues, and we agree, that one transistor pair 4487 and 4488 (“switching transistors”) is arranged in series with a transistor 4486 (“current source transistors”), as required by claim 1. *See also* Kenney Decl. ¶ 93.

Petitioner also argues, and we agree that Tamura’s transistor pair 4487/4488 is arranged in a branch in parallel with other transistor pairs 4487/4488. Pet. 23. Dr. Kenney testifies, and we credit this testimony, that Tamura arranges the transistor 4486 and its corresponding switching transistor pair 4487/4488 in a branch and that multiple branches are provided, all connected across a common input Vcc and two common outputs to load transistors 44831 and 44832. Kenney Decl. ¶ 93. Patent Owner does not challenge this evidence or Petitioner’s arguments. We determine that Petitioner has demonstrated by a preponderance of the

evidence that Tamura discloses transistors arranged as the claim language requires.

(4) “Constant Current” Limitation

Now we move on to the last limitation of claim 1 that recites “wherein current flowing through the source transistors remains constant during state transitions of the digital control signal.” Ex. 1001, 2:61–63 (“constant current” limitation). Petitioner relies on Tamura’s digitally controlled switching of pMOS transistors 4487 and 4488 to output current to the pMOS transistors 4486 in an uninterrupted manner during transitions. Pet. 26–27 (citing Ex. 1003, 48:1–13, 48:29–39 (stating that the output current “is always maintained constant” and the “resulting advantage [is] that transient response spikes, as seen when the current is interrupted, are eliminated”); Kenney Decl. ¶¶ 95–96). We agree that the cited passages of Tamura show the claim requirement that the current flowing through the current source transistors remains constant during state transitions of the digital control signal. As Dr. Kenney testifies, and we credit this testimony, the current produced by Tamura’s source transistors 4486 is constant during transitions because one of the switching transistors (either 4487 or 4488) is always switched ON and will allow current to flow uninterrupted from the source transistor 4486. Kenney Decl. ¶ 95. Patent Owner has not presented argument concerning this limitation.

We determine that Petitioner has shown by a preponderance of the evidence that Tamura teaches the “constant current” limitation.

(5) Conclusion as to Claim 1

Having reviewed the record and arguments presented by Petitioner in connection with claim 1, and having considered Patent Owner’s argument

and evidence in opposition, we determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 1 of the '092 patent would have been obvious over Tamura.

ii. *Claim 2*

Claim 2 depends from claim 1 and further recites the “digitally switchable current source as claimed in claim 1, characterized in that the relevant digital control signal of each branch is applied in an inverted form to one of the two switching transistors.” Ex. 1001, 2:64–67. For this claim, Petitioner argues that Tamura’s control signals C441–C44n (the recited “relevant digital control signal of each branch”) are supplied in their inverted form to transistor 4488, which is one of the two transistors in the switching pair. Pet. 27–28 (citing Ex. 1003, Fig. 82, 48:5–14). For instance, Petitioner provides annotated Figure 82 of Tamura, reproduced below, showing the inverted digital control signal.

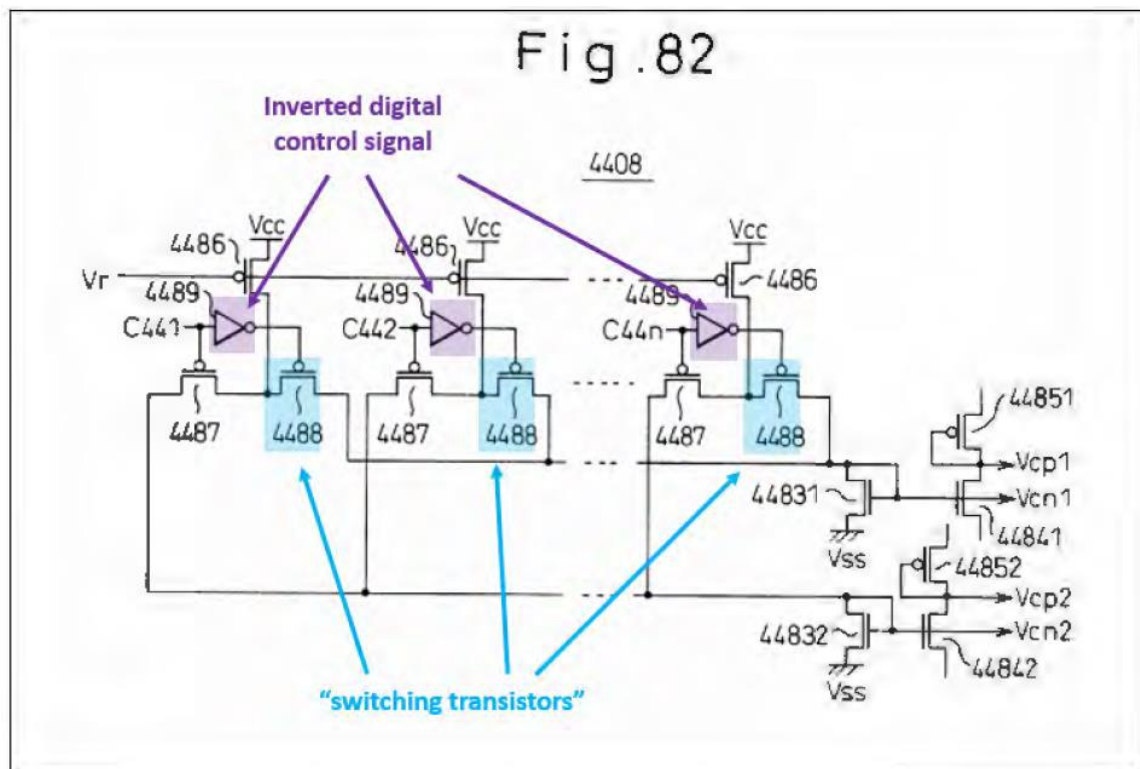


Figure 82 of Tamura has been annotated by Petitioner to illustrate in blue the “switching transistors” 4488 and the inverted digital control signal highlighted in purple. Pet. 27. According to Petitioner, and we agree, the relevant digital control signal C441 to C44n of each branch is applied in an inverted form to each switching transistor 4488. *Id.*; Kenney Decl. ¶ 98. Patent Owner has not presented argument for this claim.

Therefore, we determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over Tamura.

iii. Claim 3

Claim 3 also depends from claim 1 and recites the “digitally switchable current source as claimed in claim 1, characterized in that the outputs of the switching transistors terminate either in the current path to be controlled or in a parallel, load-equivalent, passive current path.” Ex. 1001, 3:1–4. Petitioner argues, and we agree, that the outputs of Tamura’s pMOS transistors 4487 and 4488 terminate in one of two current paths that flow to load transistors 44831 or 44832. Pet. 29 (citing Kenney Decl. ¶¶ 99–101). Further, Petitioner points out that

[t]he outputs of the transistor 4487 from each pair of switching transistors were “connected in common so that the sum of the currents flowing through the transistors 4487 in the ON state flows to an nMOS transistor 44832,” while the outputs of the transistor 4488 in each of the pairs were likewise “connected in common so that the sum of the currents flowing through the transistors 4488 in the ON state flows to an nMOS transistor 44831.”

Id. (citing Tamura 48:15–22). To put it succinctly, when the 4487 transistors are turned ON, the current flowing through them are all fed to one

load (transistor 44832). When the 4487 transistors are turned OFF, the 4488 transistors are switched ON and the current flowing through them are fed to another load (transistor 44831). In this manner, Tamura teaches that outputs of each switching transistor flow to one of two load transistors, thus terminating in a current path to be controlled. Petitioner's annotated Figure 82, reproduced below, illustrates the point.

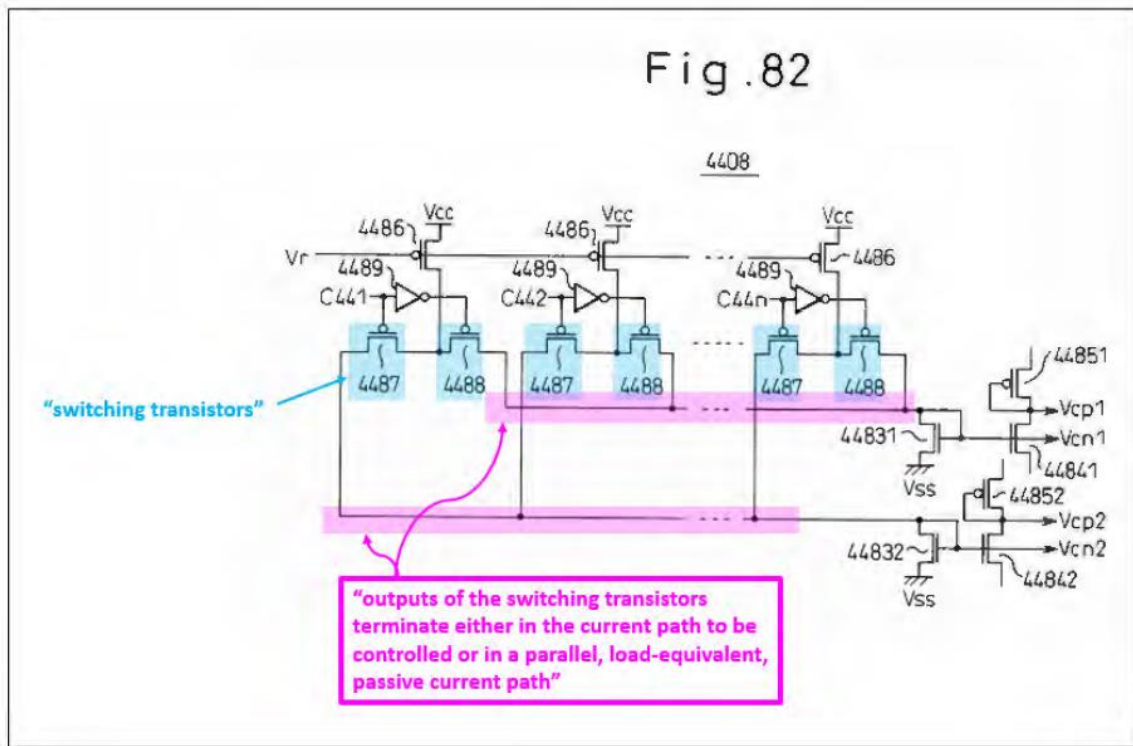


Figure 82 of Tamura above shows annotations by Petitioner depicting the switching transistors highlighted in blue and how the output of those transistors terminate in the current paths to be controlled highlighted in pink. Pet. 30; Kenney Decl. ¶ 101. Petitioner has shown persuasively that Tamura's transistors 4487 and 4488 (the "switching transistors") terminate their output as required by claim 1. Patent Owner has presented no argument for this claim.

We determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 3 would have been obvious over Tamura.

iv. Claim 4

Claim 4 is an independent claim directed to a “phase-locked loop circuit,” reciting the same limitations of claim 1 except it further recites a “voltage-controlled oscillator adapted to provide an output frequency in response to the current source transistors” (the “VCO” limitation).

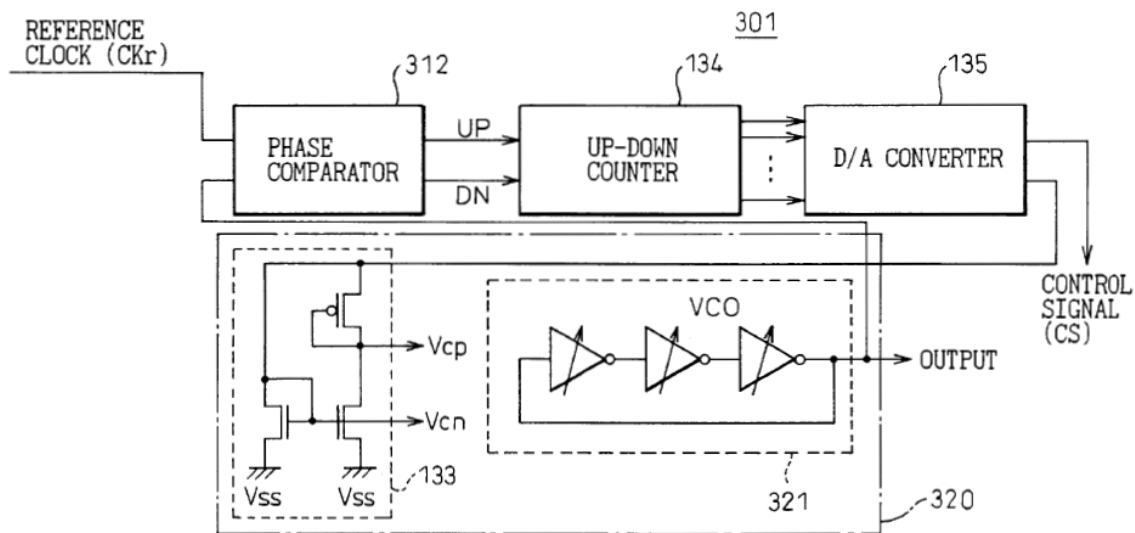
Ex. 1001, 4:5–7. Petitioner relies on the same arguments and evidence presented for claim 1 for the substantially similar claim limitations.

Pet. 30–32. For the VCO limitation, Petitioner argues that Tamura’s teachings render obvious claim 4 because, for example, Tamura teaches a phase-lock-loop (PLL) circuit. *Id.* at 31 (citing Ex. 1003, 38:44–48, Fig. 64). And, according to Petitioner, Tamura teaches a voltage-controlled oscillator (“VCO”) as recited. *Id.* at 32 (citing Ex. 1003, 38:50–39:4; Kenney Decl. ¶ 105). Petitioner argues that it would have been obvious to a person of ordinary skill in the art to use the “bias signal generating circuit 4408 of Figure 82 to control the VCO.” *Id.* (citing Kenney Decl. ¶¶ 106–109).

Patent Owner challenges Petitioner’s assertions on the basis of a lack of motivation to combine the circuit of Figure 82 with the embodiment that includes a VCO described in Figure 64. PO Resp. 15. According to Patent Owner, Petitioner failed to establish reasoning, with a rational underpinning, for why a person of ordinary skill in the art would have replaced components in the D/A converter of Figure 64 with the bias signal generating circuit described in Figure 82. *Id.* Patent Owner posits that Tamura discloses 36

This alone suggests, Patent Owner’s argument goes, that it was not obvious to present the combination Petitioner proposes. *Id.* We are not persuaded by Patent Owner’s arguments.

Fig. 64



31

Decl. ¶¶ 106–109. We credit this testimony as it is supported by the disclosure of Tamura and provides a rational explanation for the motivation. For instance, Dr. Kenney explains that Tamura’s circuit 133 (of Figure 64) outputs control signals V_{cp} and V_{cn} in response to the output of the D/A converter. *Id.* ¶ 107 (citing Ex. 1003, 38:51–61). And “[c]ircuit 133 is arranged in substantially the same way as Figure 82 transistors 44832, 44842, and 44852 that form one current-to-voltage conversion producing V_{cn2} and V_{cp2} , and transistors 44831, [44841, and 44851 that form a second current-to-voltage conversion producing V_{cp1} and V_{cn1} at the output.” *Id.* (citing Ex. 1003, Figs. 64, 82). Further, Dr. Kenney explains that the digitally controlled current source of Figure 82 performs the same function as the combination of the D/A converter 135 and voltage-to-current converter 133 in Figure 64 and produces the same result: a digitally controlled current source whereby the output current is converted to a voltage. *Id.* Thus, according to Dr. Kenney, “the circuit in Figure 82 could be used in place of the D/A converter 135 and voltage-to-current converter 133 in Fig. 64 to control the frequency of the VCO 321.” *Id.* Therefore, according to this testimony and the Tamura disclosures, we find that a person of ordinary skill in the art would have understood that the circuit of Figure 82 could replace the D/A converter and the voltage-to-current converter circuit 133 from Figure 64. Petitioner’s evidence thus shows that a person of ordinary skill in the art understood the interchangeability of these circuits and that their operability would not change such that the Figure 82 circuit is a “mere substitution of one element for another known in the field” where the combination does no more than yield a predictable result. *KSR*, 550 U.S. at 416, 418.

Petitioner, however, has done more than allege a mere substitution. According to Dr. Kenney, a person of ordinary skill in the art “would have been motivated to replace the D/A converter 135 and voltage-to-current converter 133 with digitally controlled current source 4408 of Figure 82” because that circuit is simpler than the D/A circuit 135, which is shown in Figure 53 of Tamura. Kenney Decl. ¶ 108 (citing Ex. 1003, 34:64–67, Figs. 53, 82). Dr. Kenney explains further the cost-saving and power-consumption implications of using a simpler circuit:

Using the simpler circuit 4408 of Figure 82 instead of D/A circuit 135 would have saved substantial space on the integrated circuit and would have consumed less power than the circuit in Figure 53 because far fewer transistors would have been used as compared to the matrix cell type D/A converter.

Id. (citing Ex. 1003, 34:64–65). This explanation is rational, and is expressed with support from Tamura, and, therefore, we find it persuasive. Patent Owner’s arguments to the contrary challenge Dr. Kenney’s testimony as insufficient because Dr. Madisetti was unable to review facts or data underlying a deeper technical analysis. Madisetti Decl. ¶¶ 152–153. According to Dr. Madisetti, Dr. Kenney’s reasoning is too generic because alleging a “simpler” circuit, saving “substantial space,” and “consumed less power,” are not detailed enough—i.e., Dr. Madisetti would have needed “detailed schematics” “or an analysis that estimated the number of transistors required for each design.” *Id.* ¶ 154. We do not agree with Patent Owner’s contention and Dr. Madisetti’s testimony that more technical detail is warranted here.

As Petitioner argues, and we agree, Dr. Kenney provides an explanation for his conclusion that the substitution would be advantageous for specific reasons: reducing the number of transistors, reducing complex

circuitry, and saving space on an integrated circuit. These are not generic assumptions that run afoul of our jurisprudence on sufficient reasoning. *See ActiveVideo Networks, Inc. v. Verizon Comm., Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (finding that expert testimony of motivation to combine “to build something better,” be “more efficient, cheaper, or” something that “had more features” was generic and insufficient). We find persuasive that the reasoning to select one circuit over another may be reasonably based on design considerations, such as reducing number of parts, especially in a case, such as this one, where there is uncontested testimony that the circuits would perform the same function. Kenney Decl. ¶ 107.

Furthermore, there is no evidence contradicting the testimony of Dr. Kenney in this regard. As Petitioner points out, and we agree, Dr. Kenney’s statements and support in Tamura are not contradicted. Reply 19; *see* Madisetti Decl. ¶¶ 152–155 (opining that Petitioner’s rationale lacked supporting detail sufficient for Dr. Madisetti to be able to review Dr. Kenney’s conclusions). Patent Owner has challenged Dr. Kenney’s opinions as insufficiently supported, without providing any countervailing evidence. *See* PO Resp. 15–17, Sur-reply 14–15 (arguing that Petitioner’s declaration testimony is conclusory and it is Petitioner’s burden to establish obviousness). There is no allegation that Dr. Kenney’s assessment is wrong or untenable given the disclosures of Tamura, which, in any event, describe the D/A converter used in Figure 64 in detail and Dr. Kenney explains further how such a circuit would have required 32 transistors in comparison with Figure 82’s use of a mere 16. Reply Kenney Decl. ¶ 21; Ex. 1003, 34:64–67, Fig. 53. Accordingly, we do not agree with Patent Owner’s

assessment that Petitioner's evidence of reasons to combine the Tamura embodiments is insufficient.

Now we address Patent Owner's argument that a person of ordinary skill in the art would not have been motivated to make the asserted combination because the operation of the Figure-64 circuit would be altered. PO Resp. 16–17. More specifically, Patent Owner argues that the Control Signal output by D/A converter 135 would be eliminated and the Figure-82 circuit does not disclose a Control Signal. *Id.* at 16 (citing Madisetti Decl. ¶ 150). According to Patent Owner, Petitioner's assertions fail to explain the omission, and the mere elimination of the control signal warrants finding that a person of ordinary skill in the art would not have been motivated to modify the reference because it contradicts a basic teaching or makes it inoperable for its intended purpose. *Id.* at 17 (citing *Univ. of Md. Biotechnol. Inst. v. Presens Precis. Sensing GmbH*, 711 F. App'x 1007, 1010 (Fed. Cir. 2017)). We are not persuaded by these arguments for two reasons.

First, Patent Owner's argument does not establish that the mere elimination of the Control Signal either contradicts a basic teaching or makes Tamura inoperable. There is no evidence that eliminating the Control Signal results in inoperability. Dr. Madisetti's testimony does not explain why that would be the case. In any event, even if the modification changed some functionality by eliminating the Control Signal, which Patent Owner does not explain, we determine that the advantages of making the combination, discussed above, are evidence of obviousness that outweigh the unstated drawbacks of the alleged elimination. *See Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) ("Although modification of the movable blades may impede the

quick change functionality disclosed by Caterpillar, “[a] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.” (quoting *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006))).

Second, Dr. Kenney rebuts Dr. Madisetti’s testimony on this point by explaining that Figure 82 of Tamura discloses a Control Signal. Reply Kenney Decl. ¶ 23. We credit this testimony over the testimony of Dr. Madisetti because it is supported by a rational explanation of Tamura’s description. *Id.* For instance, Dr. Kenney explains that a person of ordinary skill in the art would have understood “that the current output of transistors 44831 or 44832 shown in [Figure] 82 is the same as the current output CS shown in [Figure] 53 or 64, as the output of those transistors is converted into control signals Vcn and Vcp.” *Id.* (citing Ex. 1003, Figs. 82, 64, 51, 34:30–35). Dr. Kenney also testifies that the D/A converter of Figure 53 only has a single output, and, therefore, a person of ordinary skill in the art would have understood that the two lines shown coming out of the D/A converter in Figure 64 are the same output CS. *Id.* ¶ 24. This is significant because it shows that Figure 82 already has a control signal, but that if another were needed (and there is no allegation that this would be the case), a simple tap of output transistor 44831 or 44832 of Figure 82 is all that would be required. *Id.* That is, whatever control signal is needed for the operation of the combined teachings is already present in the circuit of Figure 82, and to the extent a person of ordinary skill in the art would need another control signal, Figure 82 has the transistors to tap for such a signal. No evidence of record contradicts Dr. Kenney’s testimony, and there is no evidence that the asserted combination of the circuits of Figures 82 and 64 of Tamura would have been uniquely challenging or difficult to a person of

ordinary skill in the art. *See KSR*, 550 U.S. at 417 (stating that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill”).

Finally, Patent Owner challenges Dr. Kenney’s testimony on this issue as untimely because it should have been presented in the Petition. PO Resp. 14–15 (citing 37 C.F.R. § 42.22(a)(2); Consolidated Trial Practice Guide (Nov. 2019) at 80). We do not agree. Petitioner may present new evidence in an *inter partes* review after the petition stage if that evidence is a legitimate reply to evidence introduced by Patent Owner. *Anacor Pharm., Inc. v. Iancu*, 889 F.3d 1372, 1380–81 (Fed. Cir. 2018). Patent Owner introduced testimonial evidence from Dr. Madisetti implying that the elimination of the control signal would alter the operation of the embodiment of Figure 64, and Patent Owner argued inoperability based on that testimony. PO Resp. 16–17; Madisetti Decl. ¶¶ 150. Faced with this allegation, we do not fault Petitioner for marshalling new evidence in support of its allegation that a person of ordinary skill in the art would have had reason to make the combination of teachings as asserted in the Petition. Accordingly, we are not persuaded by Patent Owner’s arguments that Petitioner improperly introduced new evidence in the form of testimony by Dr. Kenney concerning the control signal issue raised by Patent Owner’s inoperability argument.

Having reviewed the evidence of record and the arguments presented, we are persuaded that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 4 would have been obvious over Tamura.

3. Conclusion Regarding Petitioner's Additional Grounds Based, at Least in Part, on Tamura

We determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–4 would have been obvious over Tamura.

We need not determine whether Tamura would also anticipate or whether Tamura together with Smith or other knowledge of a person of ordinary skill in the art also would render the claims unpatentable because we have found that all the challenged claims would have been unpatentable as obvious over Tamura alone. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (non-precedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding” and, thus, agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

D. Grounds Based on Brown

Petitioner asserts that claims 1–4 are anticipated by Brown alone or would have been obvious over Brown in combination with the knowledge of a person of ordinary skill in the art. Pet. 34–48, 58–60. Having determined, however, that Petitioner has demonstrated by a preponderance of the evidence that all challenged claims are unpatentable for obviousness over Tamura, we need not reach additional overlapping grounds.

III. CONCLUSION

As explained above, we have addressed each challenged claim of the '092 patent and determine that Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.¹ Consistent with 35 U.S.C. § 318, this Final Written Decision therefore disposes of all patent claims challenged by Petitioner. *SAS*, 138 S. Ct. at 1359.

¹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	102(e) ²	Tamura		
1–4	103(a)	Tamura	1–4	
1–4	103(a) ³	Tamura, Smith		
1–4	103(a) ⁴	Tamura, knowledge of a person of ordinary skill in the art		
1–4	102(b) ⁵	Brown		
1–4	103(a) ⁶	Brown, knowledge of a person of ordinary skill in the art		
Overall Outcome			1–4	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–4 of the '092 patent have been proven to be unpatentable; and

FURTHER ORDERED because this is a Final Written Decision, parties to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

² We do not reach whether Tamura anticipates claims 1–3 because we have determined those claims are unpatentable as obvious over Tamura.

³ We do not reach this ground because we have found claims 1–4 unpatentable for obviousness over Tamura alone.

⁴ See *supra* n.3.

⁵ See *supra* n.3.

⁶ See *supra* n.3.

IPR2021-00001
Patent 6,819,092 B2

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