

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,¹
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2021-00130
Patent 6,459,625 B1

Before KRISTEN L. DROESCH, JASON W. MELVIN, and
BRIAN D. RANGE, *Administrative Patent Judges*.

DROESCH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ STMicroelectronics, Inc. was joined as a petitioner in this proceeding based on a petition and motion for joinder filed in IPR2021-01230, which were granted. These proceedings were terminated as to petitioner Qualcomm Incorporated. *See* Paper 37.

I. INTRODUCTION

We have authority to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that STMicroelectronics Inc. (“STMicroelectronics”) establishes by the preponderance of the evidence that claims 1–12 and 14 (“challenged claims”) of U.S. Patent No. 6,459,625 B1 (Ex. 1001, “’625 Patent”) are unpatentable.

A. Procedural History

Qualcomm Incorporated (“Qualcomm”) filed a Petition requesting an *inter partes* review of claims 1–12 and 14 of the ’625 Patent. Paper 1 (“Pet”). Monterey Research, LLC (“Patent Owner”) elected not to file a preliminary response.

After reviewing the Petition (Paper 1) we instituted *inter partes* review. Paper 6 (“Institution Decision,” “Dec.”). Following institution, STMicroelectronics filed a petition for *inter partes* review and a Motion for Joinder in IPR2021-01230, requesting that STMicroelectronics be joined as a petitioner in IPR2021-00130. *STMicroelectronics, Inc. v. Monterey Research, LLC*, IPR2021-01230, Papers 1, 3. We instituted trial in IPR2021-01230, granted the Motion for Joinder, and added STMicroelectronics as a petitioner to IPR2021-00130. *Id.*, Paper 7. A copy of that decision was entered in the record of IPR2021-00130. Paper 15.

After institution of trial, Patent Owner filed a Response (Paper 14, “PO Resp.”), to which Qualcomm and STMicroelectronics filed a Reply (Paper 19, “Pet. Reply”), to which Patent Owner filed a Sur-reply (Paper 26, “PO Sur-reply”).

On May 9, 2021, pursuant to our authorization, Qualcomm and Patent Owner filed a Joint Motion to Terminate as to Qualcomm. Paper 35. The Joint Motion to Terminate was granted and Qualcomm was terminated from the proceeding. Paper 37. The proceedings are maintained between Patent Owner and STMicroelectronics (“Petitioner”). *See id.*

Petitioner relies on a Declaration of Pradeep Lall, Ph.D., (Ex. 1006) to support the Petition. Patent Owner relies on a Declaration of Nader Bagherzadeh, Ph.D., (Ex. 2003) to support its Response. Dr. Lall and Dr. Bagherzadeh were cross-examined during trial, and transcripts of Dr. Lall’s deposition (Ex. 2002) and Dr. Bagherzadeh’s deposition (Ex. 1019) are included in the record.

Oral argument was held on March 21, 2022. A transcript of the oral argument is included in the record. Paper 34.

B. Real Parties-in-Interest

Petitioner states that the real parties-in-interest are STMicroelectronics, Inc., STMicroelectronics N.V., and STMicroelectronics International N.V. *STMicroelectronics, Inc. v. Monterey Research, LLC*, IPR2021-01230, Paper 1, 2.

Patent Owner states that the real parties-in-interest are Monterey Research, LLC and IPValue Management. Paper 4, 1.

C. Related Matters

The parties indicate that the following proceedings involve the ’625 Patent and are ongoing: *Monterey Research, LLC v. STMicroelectronics NV*, No. 1:20-cv-00089 (D. Del. 2020); and *Monterey Research, LLC v. Qualcomm Inc.*, No. 1:19-cv-02083 (D. Del. 2019). *See* Pet. 2; Paper 4, 1.

The parties also indicate that the following proceedings involved the '625 Patent and have concluded: *Marvell Semiconductor Inc. v. Monterey Research, LLC*, No. 3:20-cv-03296 (N.D. Cal. 2020); *Monterey Research, LLC v. Marvell Technology Group, Ltd. et al.*, No. 1:20-cv-00158 (D. Del. 2020); *Macronix International Co., Ltd. v. Spansion LLC*, IPR2014-00104 (PTAB 2014) (the "Macronix IPR"); *In re Certain Flash Memory Chips and Products Containing Same*, ITC- 337-TA-893 (ITC 2013); *Spansion LLC v. Macronix International Co., Ltd., et al.*, No. 3:13-cv-03566 (N.D. Cal. 2013); *In re Certain Flash Memory Chips and Products Containing the Same*, ITC-337-TA-735 (ITC 2010); and *Spansion LLC v. Samsung Electronics Co. Ltd. et al.*, No. 5:10-cv-03446 (N.D. Cal. 2010). See Pet. 2–3; Paper 4, 1; *STMicroelectronics, Inc. v. Monterey Research, LLC*, IPR2021-01230, Paper 1, 3, Paper 5, 1.

D. The '625 Patent (Ex. 1001)

The '625 Patent relates to the optimization of layout density in a periphery area of a flash memory device using a three-metal layer interconnection process. See Ex. 1001, 1:9–14, 2:42–44, 2:61–64.

Figure 1 of the '625 Patent is reproduced below.

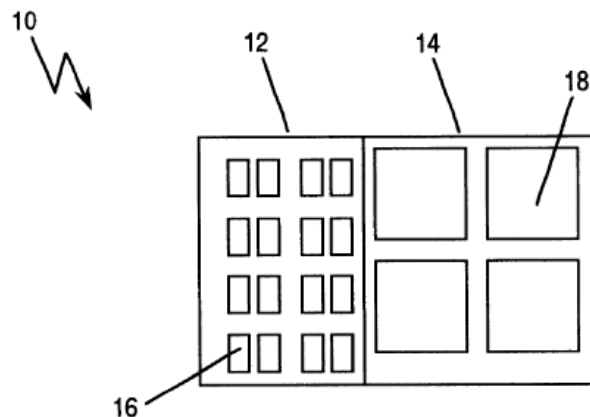


Figure 1 depicts flash memory 10 according to one embodiment. *See* Ex. 1001, 4:34–36. Flash memory 10 includes core cell area 12 for performing memory functions and periphery area 14 for performing logic functions. *See id.* at 1:35–37, 4:36–37. Core cell area 12 includes core memory cells 16, and periphery area 14 includes sub-circuits 18, made up of various types of circuit components such as transistors, capacitors, and resistors. *See id.* at 4:37–42.

Figure 2 of the '625 Patent is reproduced below.

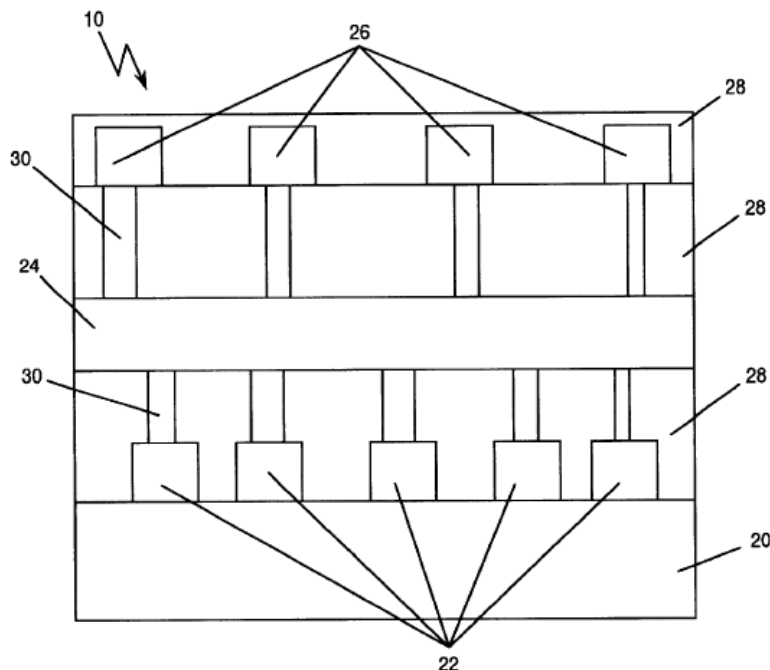


Figure 2 depicts a cross-sectional view of flash memory 10. *See* Ex. 1001, 4:16–17, 5:24–25. Flash memory 10 includes substrate 20 where electrical components are formed during fabrication. *See id.* at 5:25–28. Flash memory 10 also includes first metal interconnect layer (M1) 22, second metal interconnect layer (M2) 24, and third metal interconnect layer (M3) 26, separated by dielectric layers 28. *See id.* at 5:28–32. Metal interconnect layers (M1) 22, (M2) 24, and (M3) 26 are be deposited on

periphery area 14 of flash memory 10 to electrically interconnect the components of each electrical circuit 40 of each sub-circuit 18. *See id.* at 6:18–21, 6:44–46. Contact holes 30 (or “vias”) are created and filled with conductive material during fabrication to penetrate dielectric layers 28 in predetermined locations of flash memory 10 to provide electrical interconnections between metal interconnect layers (M1) 22, (M2) 24, and (M3) 26. *See id.* at 5:45–52.

Figure 3 of the '625 Patent is reproduced below.

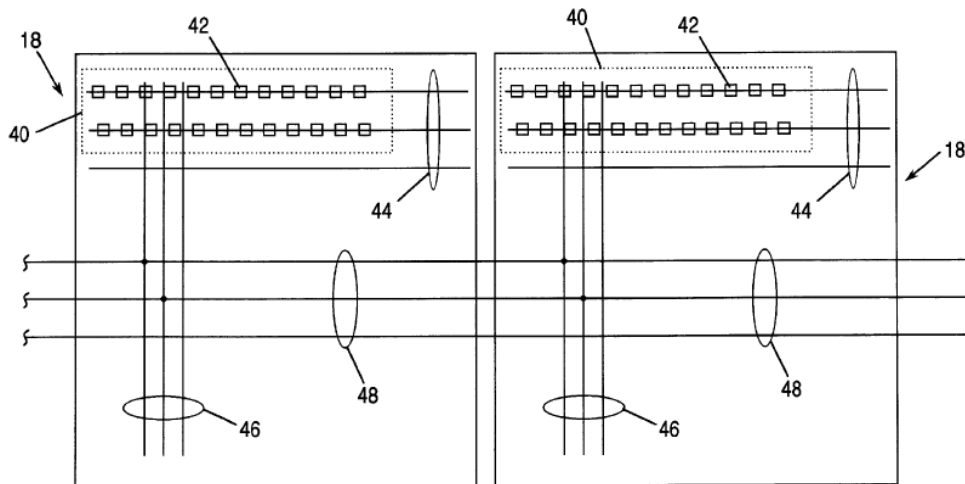


Figure 3 depicts a top-view of two sub-circuits 18 within periphery area 14 of flash memory 10. *See Ex. 1001, 5:59–61.* First metal interconnect layer (M1) 22 includes first metal layer lines 44, which extend parallel to the row of transistors 42 within each electrical circuit 40, and provide interconnecting surface “wiring” of the components of electrical circuits 40. *See id.* at 6:23–29. Second metal interconnect layer (M2) 24 includes second metal layer lines 46, which are substantially perpendicular to first metal layer lines 44, and also provide surface “wiring” of the electrical circuits 40 to complete the predetermined circuit configuration and formation of sub-circuits 18. *See id.* at 6:41–44, 6:47–50. Third metal

interconnect layer (M3) 26 includes third metal layer lines 48, which are formed perpendicular to second metal layer lines 46, and electrically interconnect one respective sub-circuit 18 to another. *See id.* at 7:7–15. Third metal layer lines 48 also electrically interconnect sub-circuits 18 with core memory cells 16 within core cell area 12 of flash memory 10. *See id.* at 7:21–24.

E. Illustrative Claims

Claims 1, 6, and 10 are independent, claims 2–5 depend ultimately from claim 1, claims 7–9 depend ultimately from claim 6, and claims 11, 12, and 14 depend ultimately from claim 10. Claims 1 and 6 are illustrative and reproduced below:

1. A method of electrically interconnecting a periphery area in a flash memory, comprising:
 - providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electrical circuit having a plurality of circuit components,
 - partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction;
 - completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are oriented substantially perpendicular to said first metal layer lines, and electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines.

6. A method of optimizing circuit layout in a flash memory, comprising:

forming a plurality of sub-circuits in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electric circuit having a row of transistors, depositing a first metal interconnect layer on said substrate to partially electrically interconnect the transistors of the sub-circuits, wherein said first metal interconnect layer forms a plurality of first metal layer lines that are oriented to extend substantially in the same direction as said row of transistors,

depositing a second metal interconnect layer above said first metal interconnect layer to complete the electrical interconnection of said respective transistors within said sub-circuits, wherein said second metal interconnect layer forms a plurality of second metal lines oriented to extend substantially perpendicular to said first metal layer lines, and

depositing a third metal interconnect layer above said second metal interconnect layer to electrically interconnect the respective sub-circuits, wherein said third metal layer forms a plurality of metal layer lines oriented to extend substantially parallel to said first metal layer lines.

F. Asserted Challenges to Patentability and Asserted Prior Art

Petitioner asserts that claims 1–12 and 14 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1–5, 10–12, 14	103(a) ²	How-767 ³ ,
6–9	103(a)	How-767, Feild ⁴
1–5, 10–12, 14	103(a)	How-767, Baker ⁵
6–9	103(a)	How-767, Feild, Baker
1–5, 10–12, 14	103(a)	How-767, Baker, Akaogi ⁶
6–9	103(a)	How-767, Feild, Baker, Akaogi

II. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is “a prism or lens” through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). The person of ordinary skill in the art is a hypothetical person presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In determining the level of ordinary skill in the art, we may consider certain factors, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made;

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the ’625 Patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

³ Ex. 1003, US 6,242,767 B1, issued June 5, 2001 (“How-767”).

⁴ Ex. 1011, US 6,433,436 B1, issued Aug. 13, 2002 (“Feild”).

⁵ Ex. 1005, R. Jacob Baker et al., *CMOS Circuit Design, Layout and Simulation* (Stuart K. Tewksbury ed. 1998) (“Baker”).

⁶ Ex. 1010, US 5,452,251, issued Sept. 19, 1995 (“Akaogi”).

sophistication of the technology; and educational level of active workers in the field.” *Id.* (internal quotation marks and citation omitted).

Petitioner asserts that

A person of ordinary skill in the art [] as of February 25, 2000—the ’625 Patent’s earliest claimed priority date []—would have had at least a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in design, development and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 7 (citing Ex. 1006 ¶ 44). Petitioner also asserts that “[t]he prior art and the ’625 Patent also evidence this level of ordinary skill,” citing Baker’s disclosure that a “successful CMOS integrated circuit design engineer has knowledge in the areas of device operation, circuit design, layout, and simulation.” *Id.* at 8 (citing Ex. 1005, 23; Ex. 1006 ¶¶ 43–45).

In the Decision on Institution, we adopted Petitioner’s proposed definition of a person of ordinary skill in the art, stating that it “appear[ed] to be consistent with the level of skill reflected by the ’625 Patent Specification and the asserted prior art.” Dec. 11–12.

In the Response, Patent Owner contends that Petitioner’s witness Dr. Lall does not agree with Petitioner’s definition of a person of ordinary skill in the art adopted by the Board in the Institution Decision. *See* PO Resp. 25 (quoting Dec. 11–12, Pet. 7–8; citing Ex. 1006 ¶ 43; Pet. 7); PO Sur-reply 10. Yet, according to Patent Owner, “[r]egardless, none of that makes a difference. Given the complexity of the field and the different considerations involved with semiconductor integrated circuit layout and memory cell layout, a [person of ordinary skill in the art] would have had at

least a bachelor's degree in electrical engineering and/or computer engineering, and at least two years of experience in design and/or development of the layout of memory circuits and/or related hardware design.” *Id.* (citing Ex. 2003 ¶ 93). But, in the Sur-reply, Patent Owner asserts that “[t]he Board quoted and adopted [Petitioner]’s proposal. . . . That is the level applicable to this inquiry.” PO Sur-reply 10 (citing Dec. 10–11).

There does not appear to be a meaningful dispute between the parties regarding the definition of a person of ordinary skill in the art. Accordingly, we again adopt Petitioner’s definition as it is consistent with the level of skill reflected by the ’625 Patent Specification and the asserted prior art.

B. Dr. Lall’s Qualifications

Related to the discussion of the definition of a person of ordinary skill in the art, Patent Owner contends that Petitioner’s witness, Dr. Lall, does not qualify as a person of ordinary skill in the art based on the level of skill advanced in the Petition and adopted in the Institution Decision and, therefore, Dr. Lall’s opinions should be given little to no weight. *See* PO Resp. 25 (citing Ex. 2003 ¶¶ 91–92), 28 (quoting Dec. 11; citing Dec. 11–12; Ex. 2003 ¶ 99), 31 (citing Ex. 2003 ¶ 104); *see also* PO Sur-reply 13 (similar argument). In support of its arguments, Patent Owner reproduces paragraph 43 of Dr. Lall’s declaration with added highlighting to show the differences between it and the definition of a person of ordinary skill in the art provided in the Petition. *See* PO Resp. 26 (quoting Ex. 1006 ¶ 43; citing Ex. 2003 ¶ 94), PO Sur-reply 10. According to Patent Owner, Petitioner’s proposed person of ordinary skill in the art “would require a ‘bachelor’s degree in electrical engineering, computer engineering or a

related field,’ while Dr. Lall’s proposed [person of ordinary skill in the art] includes ‘mechanical engineering with focus on semiconductor packaging, mechatronics . . . applied physics, or a related field (e.g., device operation, circuit design, layout, and simulation).’” PO Resp. 26–27 (citing Pet. 7; Ex. 1006 ¶ 43). Patent Owner further points out that Dr. Lall’s definition “adds that a [person of ordinary skill in the art] would have ‘at least two years of experience in . . . manufacturing, and/or testing of memory circuits . . . with additional graduate education substituting for experience and vice versa.’” *Id.* at 27 (quoting Ex. 1006 ¶ 43). Patent Owner also asserts that “Dr. Lall (but not [Petitioner]) opines that a [person of ordinary skill in the art] would have experience ‘with a specialization in semiconductor manufacturing and at least one year of work or research experience in that same field.’” *Id.* (quoting Ex. 1006 ¶ 43). Patent Owner asserts that Dr. Lall’s testimony “seems tailored to fit his own educational degrees and foci” and “appears to be an attempt to qualify himself as a [person of ordinary skill in the art].” *Id.* (citing Ex. 1015; Ex. 2003 ¶¶ 95–96).

Patent Owner contends that Dr. Lall cannot qualify as a person of ordinary skill in the art because he does not have a degree in electrical or computer engineering. *See* PO Resp. 28–29 (quoting Ex. 2002, 38:11–25; citing Ex. 2002, 9:22–25, 10:1–12:18; Ex. 1015, 1; Ex. 2003 ¶¶ 100–101). Patent Owner further argues that Dr. Lall did not have the relevant experience in design and/or development of the layout of memory circuits as of February 25, 2000—the undisputed priority date of the ’625 Patent. *See id.* at 29–30 (quoting Ex. 2002, 23:5–17; citing Ex. 1001, codes (54), (57); Ex. 1006 ¶¶ 7–9; Ex. 2003 ¶¶ 102–103).

In Reply, Petitioner contends “none of P[atent Owner]’s criticisms of the level of ordinary skill formulation or Dr. Lall’s qualifications impact the issues before the Board.” Pet. Reply 7. Petitioner asserts the Petition and Dr. Lall’s formulations of the level of ordinary skill in the art are fully aligned because the Petition directly cites to Dr. Lall’s formulation, which expands upon relevant related fields set forth in the Petition. *See id.* at 7–8 (citing Pet. 7). Petitioner further contends that Dr. Lall’s education and experience more than qualify him to provide expert testimony in this area. *See id.* at 8 (quoting Ex. 1006 ¶¶ 6, 7, 9, 10, 13). Petitioner further contends that Patent Owner’s “assertion that Dr. Lall is not a [person of ordinary skill in the art], even if true, is irrelevant as the Board’s Consolidated Trial Practice Guide⁷ [(“CTPG”)] makes clear that ‘[a] person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be qualified in the pertinent art.’” *Id.* at 8 (quoting CTPG 34).

In the Sur-reply, Patent Owner contends that Dr. Lall’s education in mechanical engineering does not qualify as a related field for the purposes of this case. *See* PO Sur-reply 10 (quoting Ex. 2003 ¶ 101; citing Reply 7–8; Dec. 11; PO Resp. 28–29). Patent Owner asserts that Petitioner’s citations to paragraphs 43 and 44 of Dr. Lall’s Declaration do not establish that mechanical engineering is a related field. *See id.* (citing Reply 8; Ex. 1006 ¶¶ 43–44). Patent Owner asserts that the cited paragraphs specify a person of ordinary skill in the art as of the priority date would have had at least a bachelor’s degree in a related field (e.g., device operation, circuit design,

⁷ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

layout, and simulation), but there is no evidence that Dr. Lall had any of those credentials at that time of the priority date. *See id.* at 10–11 (quoting Ex. 1006 ¶ 43).

Patent Owner further asserts that it is relevant whether Dr. Lall is a person of ordinary skill in the art because every question regarding obviousness depends on analysis from the perspective of a person of ordinary skill in the art. *See* PO Sur-reply 11 (quoting *Sundance, Inc. v. Demonte Fabricating Ltd.*, 550 F.3d 1356, 1361 (Fed. Cir. 2008)). Patent Owner contends that “Dr. Lall’s opinions derive from his own knowledge, which does not and cannot derive from his personal knowledge as a [person of ordinary skill in the art] at the time of the invention.” *Id.* at 11–12. According to Patent Owner, “whether Dr. Lall was himself a [person of ordinary skill in the art] at the time of the invention is a crucial inquiry.” *Id.* at 12. Patent Owner asserts that the *Sundance* opinion does not compel a different result because, according to Patent Owner, the court “explain[ed] that a non-POSITA could **not** testify on issues that require a POSITA’s perspective” and “if anything, confirms the unremarkable proposition that an expert need qualify as a POSITA to give expert opinion testimony.” *Id.* at 12–13 (quoting *Sundance*, 550 F.3d at 1363 n.5, 1364). Patent Owner contends that Dr. Lall’s testimony should be afforded little weight because he was not a person of ordinary skill in the art at the time of the invention, he does not have personal knowledge as to what a person of ordinary skill in the art would or would not have known, and lacks credibility as a person of ordinary skill in the art to opine on those issues compared to Patent Owner’s witness Dr. Bagherzadeh. *See id.* According to Patent Owner, “the Board regularly weighs the testimony of individuals who purport to provide

testimony regarding what a [person of ordinary skill in the art] would have known at the time of the invention and discounts putative experts whose opinions are not based on the perspective of a [person of ordinary skill in the art.]]” *See id.* at 14 (citations omitted).

We do not agree with Patent Owner’s arguments that Dr. Lall’s testimony is entitled to little or no weight. Putting aside the parties’ competing arguments regarding Dr. Lall’s formal education and experience, Patent Owner’s arguments misstate the holding of *Sundance* because *Sundance* does not hold that an expert must qualify as a person of ordinary skill in the art to give expert opinion testimony. *See* PO Sur-reply 12–13; *Sundance*, 550 F.3d at 1363. As pointed out by Petitioner, the Consolidated Trial Practice Guide explains that “[a] person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be ‘qualified in the pertinent art.’” CTPG 34 (citing *Sundance*, 550 F.3d at 1363–64). Failure to possess certain characteristics of the level of ordinary skill in the art “may not preclude an expert from providing testimony that is helpful to the Board, so long as the expert’s experience provides sufficient qualification in the pertinent art.” *Id.* Further, there is “no requirement of a perfect match between the expert’s experience and the relevant field.” *Id.* (citing *SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010)).

Here, based on Dr. Lall’s experience and qualifications (Ex. 1006 ¶¶ 3–14; Ex. 1015), we view Dr. Lall as qualified in the pertinent art and consider his testimony helpful in our analysis. For example, as noted by Petitioner, Dr. Lall has extensive teaching, research, and work experience in

electronics and electronics device design. *See* Pet. Reply 8 (quoting Ex. 1006 ¶¶ 6, 7, 9, 10, 13).

C. Claim Construction

The Board applies the same claim construction standard as applied in federal courts in a civil action under 35 U.S.C. § 282(b), which is generally referred to as the *Phillips* standard. *See* 37 C.F.R. § 42.100(b) (2020); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Under the *Phillips* standard, words of a claim are generally given their ordinary and customary meaning. *Phillips*, 415 F.3d at 1312.

Preambles of Claims 1, 6, and 10

Petitioner identifies the following phrases recited in claims 1, 6, and 10 of the '625 Patent as relevant to construing the challenged claims:

Claim	Preamble	Body
1	“a periphery area in a flash memory”	“a periphery area of a silicon substrate”
6	“in a flash memory”	“a periphery area of a silicon substrate”
10	“a periphery area in a memory device”	“a periphery area of a silicon substrate”

Petitioner argues that the phrase “a periphery area of a silicon substrate,” as recited in the body of each of claims 1, 6, and 10, should be construed as limited by the preamble of each respective claim. Pet. 20–23. According to Petitioner, “Claims 1 and 6 should be limited to periphery areas of flash memory, and Claim 10 should be limited to periphery areas of a memory device.” *Id.* at 22; *see id.* at 20–21. In support of this argument, Petitioner contends that, similar to *Deere v. Bush Hog*,

[T]he description [of the '625 Patent] repeatedly emphasizes “the present invention” as related to interconnections in the

periphery area of “flash memory” or a “memory device,” and makes clear that the invention did not go beyond memory devices: “The invention may be used with any type of memory device; however, the preferred embodiment of the invention is designed for a flash memory.”

Pet. 23 (quoting Ex. 1001, 4:30–33; citing *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1538 (Fed. Cir. 2012); Ex. 1001, Abstract, 1:9–14, 2:42–44). According to Petitioner, “the preamble ‘is necessary to understand the subject matter encompassed by the claim, which otherwise generally recites’ interconnections in a periphery area of any silicon substrate.” *Id.* (quoting *Deere v. Bush Hog*, 703 F.3d at 1358). Petitioner further argues that “[s]eparate from the preamble, the ’625 Patent’s repeated ‘present invention’ statements also limit the claims to, at a minimum, a memory device.” *Id.*

Petitioner asserts that this construction is consistent with prior decisions, including an International Trade Commission (ITC) Administrative Law Judge’s finding that the preambles of all three independent claims are limiting. Pet. 21 (citing Ex. 1009, 80–82, 84–85). Petitioner further contends that although “PTAB previously preliminarily found the preambles were not limiting, it did so under [the broadest reasonable interpretation] and focused on whether th[e preambles] provided antecedent basis to the body.” *Id.* at 22 (citing Ex. 1007, 9–10).

Petitioner also asserts that “[t]he parties in past proceedings have generally agreed upon . . . the meaning of ‘periphery area.’” Pet. 24. According to Petitioner, “[t]he ITC explained that ‘the parties agree that the periphery area of a memory device is *outside the core* memory cell area.’” *Id.* (quoting Ex. 1009, 83). Petitioner asserts that the Board “interpreted ‘a periphery area of a silicon substrate as an area of a silicon substrate that *lies*

beyond the strict limits of a core area, or as an area on a silicon substrate *outside a core area.*” *Id.* (quoting Ex. 1007, 13). Petitioner asserts that the plain and ordinary meaning of “periphery area” applied to each possible claim scope (e.g., preamble not limiting, preamble limited to a memory device, preamble limited to flash memory) results in the following constructions for each scope: “(A) an area of **a silicon substrate** outside a core area, (B) an area of a *memory device* outside the core *memory* cell area, and (c) an area of *a flash memory* outside the core *flash memory* cell area.” *Id.*

Patent Owner agrees that the preambles should be limiting. *See* PO Resp. 31–32 (citing Ex. 1001, claims 1, 6, 10; Ex. 1009, 81; Pet. 20). Patent Owner, however, disagrees that “periphery area” needs to be further construed. *See id.* at 32 (citing Pet. 20–24). According to Patent Owner, a person of ordinary skill in the art “would have instead understood: ‘the claimed periphery area is outside the core memory cell area of the claimed memory, and that it otherwise has its plain and ordinary meaning.’” *Id.* (quoting Ex. 1009, 84).

In the Reply, Petitioner asserts that there does not appear to be a meaningful dispute between the parties’ positions. *See* Pet. Reply 3. Petitioner also contends that a ruling on this issue would simplify certain issues. *See id.* at 3–4.

In the Sur-reply, Patent Owner asserts that “‘periphery area’ is a common concept and needs no further construction.” PO Sur-reply 3 (quoting Ex. 1003, 5:49–52). According to Patent Owner, “[t]he Board should construe the term consistent with its plain and ordinary meaning: the area outside the core memory cell area of the claimed memory.” *Id.*

The parties appear to agree to the following: (1) the preambles of claims 1 and 6 are limited to a flash memory; (2) the preamble of claim 10 is limited to a memory device; and (3) a “periphery area” is “an area outside the core memory cell area.” Accordingly, we adopt the parties’ construction that the preambles of claims 1 and 6 are limited to a flash memory, the preamble of claim 10 is limited to a memory device, and a “periphery area” is “an area outside the core memory cell area.” We do not need to further construe these claim terms in order to address the parties’ disputes. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Other Claim Terms

Aside from the discussion in Section II.E.4.e. below addressing “a third interconnect layer” and “electrically interconnecting,” as demonstrated in the analysis below, we need not expressly construe any other claim terms or phrases. *See Nidec Motor Corp.*, 868 F.3d at 1017.

D. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any

differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) if in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).⁸

*E. Challenge to Patentability of Claims 1–5, 10–12, and 14 over
How-767, Baker, and Akaogi*⁹

1. Overview of How-767 (Ex. 1003)

How-767 discloses a routing architecture for interconnecting application specific integrated circuit (ASIC) devices to form a customized circuit. *See* Ex. 1003, 1:4–7. How-767 incorporates by reference Application No 08/821,475, which issued as U.S. Patent No, 6,014,038 A (Ex. 1004, “How-038”). How-767 describes that “[i]n forming ASICs generally, several layers will be required,” with active layers 110 (including devices such as transistors and diodes) being formed on a semi-conductor substrate independently of one another. *See id.* at 1:20–26.

⁸ The parties do not present evidence of secondary considerations.

⁹ Because we determine that Petitioner demonstrates by a preponderance of the evidence that claims 1–5, 10–12, and 14 are unpatentable based on How-767, Baker, and Akaogi, and that claims 6–9 are unpatentable based on How-767, Field, Baker, and Akaogi, it is unnecessary to address Petitioner’s alternative challenges addressing these same claims.

Figure 1 of How-767 is reproduced below.

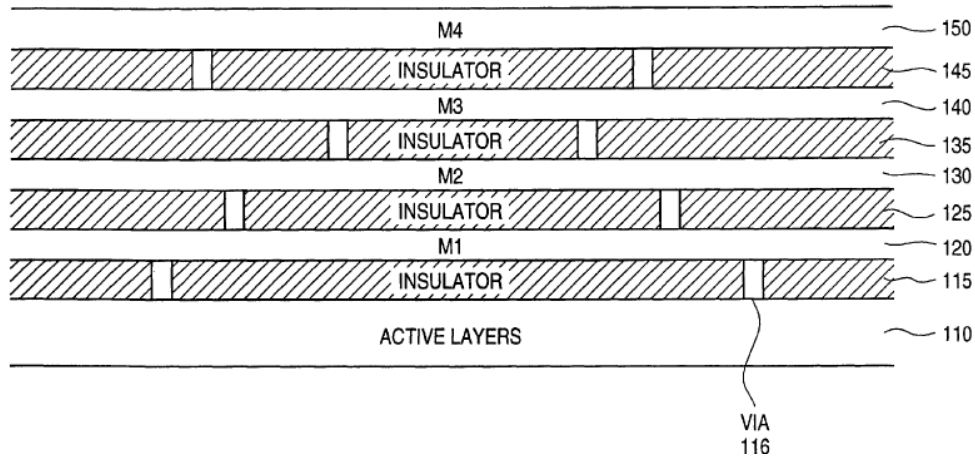


Figure 1 depicts a cross-sectional view of a generic integrated circuit. *See* Ex. 1003, 1:21–22. Once active layers 110 are formed, four metal layers M1 120, M2 130, M3 140, and M4 150 are formed over active layers 110 to interconnect the devices, thereby forming a circuit. *See id.* at 1:26–28, 1:30–31. Between each metal layer is insulating layer 115, 125, 135, or 145, which prevent shorts between the metal layers. *See id.* at 1:34–36.

How-767 further discloses that “[a]t the active layer level, ASIC active devices are generally arranged to form an array of function blocks,” and “[t]o interconnect active devices within each function block (i.e., form ‘local interconnections’) a series of horizontal and vertical connection lines formed in the metal layers are utilized.” Ex. 1003, 1:60–65. According to How-767, “typically, horizontal connections are formed in a first metal layer (M1) 120 and vertical connections are formed in a second metal layer (M2) 130 with an insulating layer 125 having vias 116 formed between M1 and M2.” *Id.* at 2:2–5. How-767 explains that “‘horizontal’ is meant to describe all metal lines running in a first direction such that all horizontal lines lie substantially parallel to one another,” and “‘vertical’ is

meant to convey all lines that run in a second direction which is substantially perpendicular to the first (horizontal) direction.” *Id.* at 2:6–11.

Figure 4 of How-767 is reproduced below.

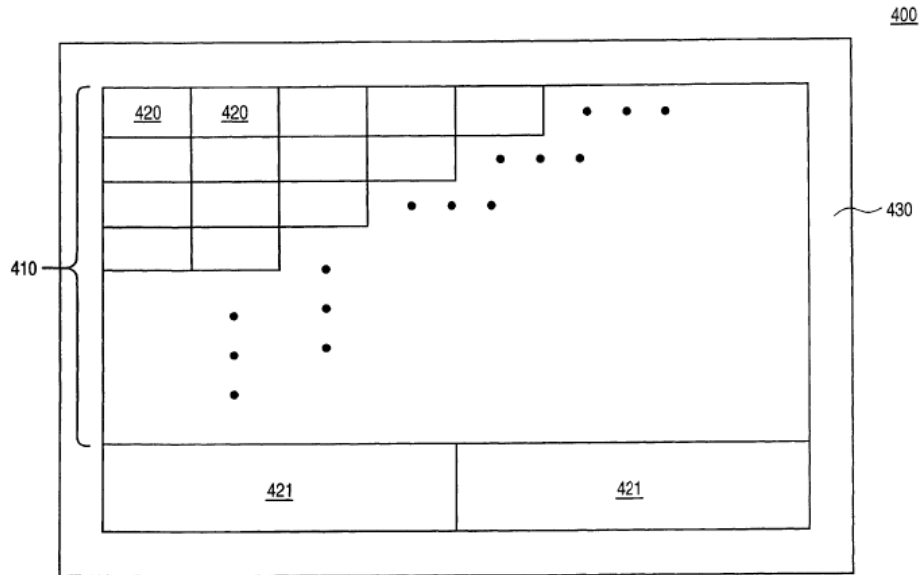


Figure 4 depicts a block diagram of an ASIC 400 according to one embodiment. *See* Ex. 1003, 5:7–8. ASIC 400 may include an array 410 of function blocks 420, and one or more other specialized regions 421, which may include circuitry such as memory blocks or logic cores. *See id.* at 5:42–43, 4:47–49, 8:36–38. Surrounding array 410 is periphery area 430, which includes circuitry such as input/output (IO) pads and other support circuitry for array 410. *See id.* at 5:49–52, 11:4–7. Function block 420 can be configured to perform combinatorial functions, sequential functions, or memory functions (e.g., SRAM¹⁰). *See id.* at 5:53–55. How-038, incorporated by reference in How-767, discloses a 2-port, 2-bit SRAM cell, a SRAM array, strong drivers required at the edge of an SRAM bit array,

¹⁰ Static Random Access Memory. Ex. 1005, 135.

and SRAM control logic implemented in a separate function block. *See* Ex. 1004, 12:8–10, 12:49–52, 12:55–64, 13:4–10, Figs. 3, 5, 16, 17. How-767 discloses that each function block 420 has a fixed internal transistor structure with fixed connections between the transistors or other active devices within each function block 420. *See id.* at 6:11–14. “[A]ll of the routing internal to each function block 420 will be fixed (non-customizable) and lower metal layers, e.g., M1 and M2, can be pre-formed in a fixed and predetermined manner, using horizontal connectors in M1 and vertical connectors in M2 (or vice versa).” *Id.* at 6:14–19. How-767 further discloses that its routing architecture allows for routing between function blocks of an array to be customized using the uppermost two metal layers (M3 and M4). *See id.* at 6:27–32.

Figure 6 of How-767 is reproduced below.

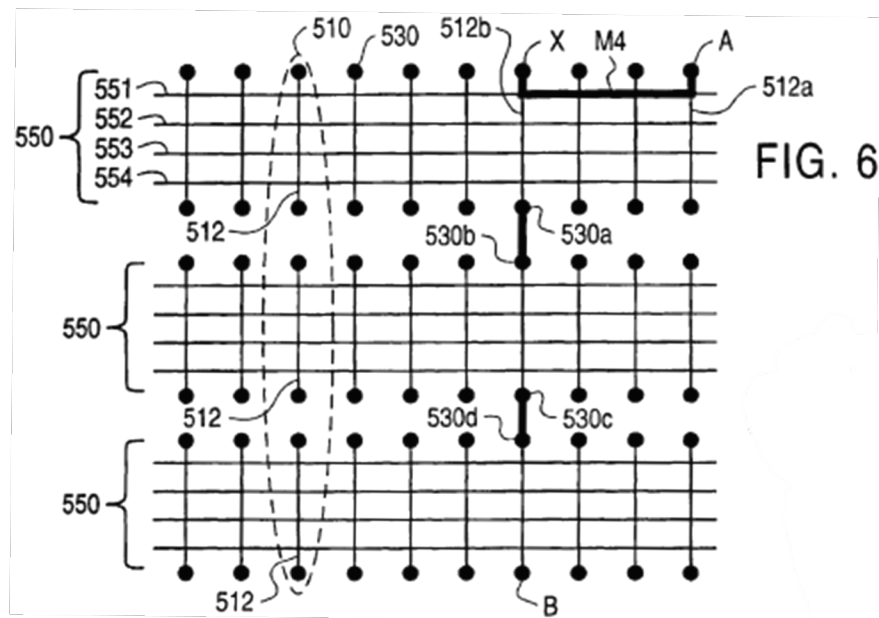


Figure 6 depicts a preliminary routing structure for implementing a routing architecture according to one embodiment. *See* Ex. 1003, 6:38–40.

Although not shown in Figure 6, How-767 describes that local

interconnections within each function block are formed in lower metal layers M1 and M2. *See id.* at 6:41–42. As shown in Figure 6, the second-to-uppermost metal layer—third metal layer M3—is composed of parallel, segmented conducting lines 510, each composed of multiple segments 512. *See id.* at 6:43–46. Each segment 512 has vias 530 formed at respective ends to enable connections to uppermost metal layer M4 above. *See id.* at 6:46–48. In metal layer M4, horizontal tracks 550 run perpendicular to segmented conducting lines 510 and are not fixed metal, but rather represent predesignated areas where metal can be placed in layer M4 to form an interconnection. *See id.* at 6:48–52. Thus, How-767 discloses that “FIG. 6 represents a structure that allows horizontal and vertical connections to enable routing, where the vertically placed metal is fixed and pre-formed and the horizontally placed metal is customizable in a predesignated manner.” *Id.* at 6:52–56.

2. Overview of Baker (Ex. 1005)

Baker is a textbook for use in courses on the physical design of CMOS¹¹ digital integrated circuits and CMOS analog circuit design. *See* Ex. 1005, 23–24.¹² Notably, Baker includes the following disclosures:

(1) “CMOS circuits are fabricated on and in a silicon wafer” (*id.* at 51);

(2) In a RAM, the row and column logic are external to the memory array (*id.* at 135–136, Fig. 17.1; *see also id.* at 145, Fig. 17.11);

¹¹ Complementary Metal Oxide Semiconductor. Ex. 1005, 31.

¹² We cite to the Exhibit page number at the bottom of the Exhibit here and throughout rather than to the reference page number at the top of the page.

(3) Flash memory is an existing type of memory cell that “is programmed using hot electrons and erased using Fowler-Nordheim tunneling” (*id.* at 154, 156);

(4) “An important consideration when implementing a VLSI¹³ chip design is regularity”—“[t]he layout should be an orderly arrangement of cells” (*id.* at 124–25, Fig. 15.2, depicting a floor plan of an overall chip);

(5) “The CMOS inverter is a basic building block for digital circuit design” (*id.* at 99); and

(6) Multiple inverters may be needed to drive a signal over a long line in a memory chip, and a standard layout of an inverter includes transistors and metal layer lines both running vertically (*see, e.g., id.* at 110–11, 114, 116, 121, 126, 127, 147, Figs. 11.13, 11.17, 11.18, 15.3, 15.5(a)–(d), 17.13).

Figure 17.13 is reproduced below.

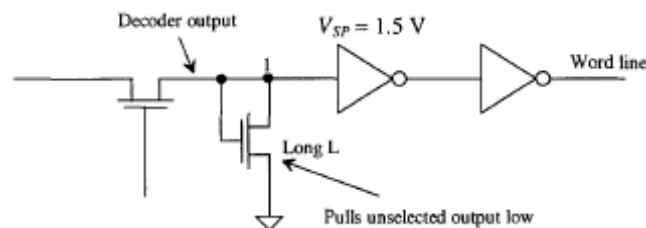


Figure 17.13 depicts an output buffer used in a row decoder of a DRAM¹⁴, in which two inverters are used to drive the word line capacitance. *See* Ex. 1005, 147.

¹³ Very-large-scale-integration. Ex. 1005, 115.

¹⁴ Dynamic Random Access Memory. Ex. 1005, 135.

Figure 15.3 is reproduced below.

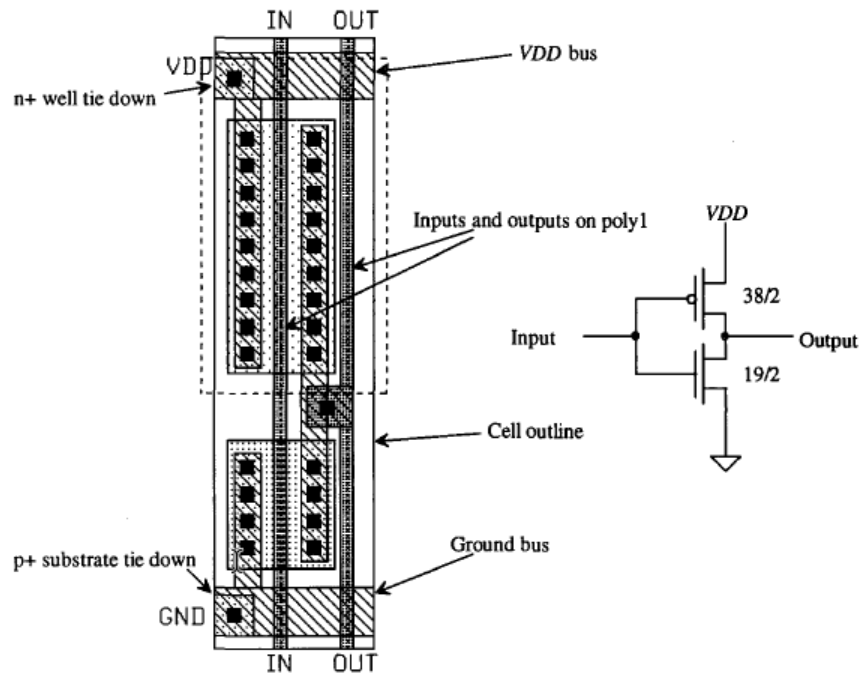


Figure 15.3 depicts a standard-cell layout of an inverter. *See* Ex. 1005, 126. As shown in Figure 15.3, transistors (represented as black squares) and metal lines (represented as a rectangular area with a diagonal line pattern surrounding the transistors) are both running vertically. *Id.*, Fig. 15.3.

3. Overview of Akaogi (Ex. 1010)

Akaogi is directed to a flash memory device. *See* Ex. 1010, 1:8–12.

Figure 1 of Akaogi is reproduced below.

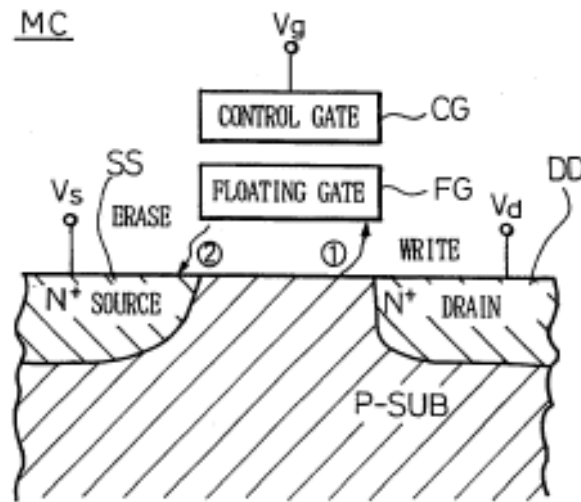


Figure 1 depicts a memory cell (“MC”) of a flash memory. *See* Ex. 1010, 10:49–51. MC has a floating gate “located between a source and a drain and [] insulated from other regions,” and a control gate “formed above the floating gate.” *Id.* at 10:52–56. By setting one or more of voltages V_d , V_g , and V_s in a particular way, electrons may be injected into floating gate or pulled therefrom in order to write data to or erase data from cell transistor MC. *See id.* at 10:57–11:8, *see also id.* at 23:65–67 (“To write or erase data to or from cell transistors of a flash memory, the floating gates of the cell transistors are charged or discharged.”). “To read data from the cell transistor MC, the gate voltage V_g is equalized to the power source voltage V_{cc} , the drain voltage V_d to about one volt, and the source voltage V_s to zero,” so that it can be “checked to see whether or not a drain current flows, to determine if the data stored in the cell transistor MC is ‘1’ or ‘0’.” *Id.* at 11:8–14.

Figure 2 of Akaogi is reproduced below.

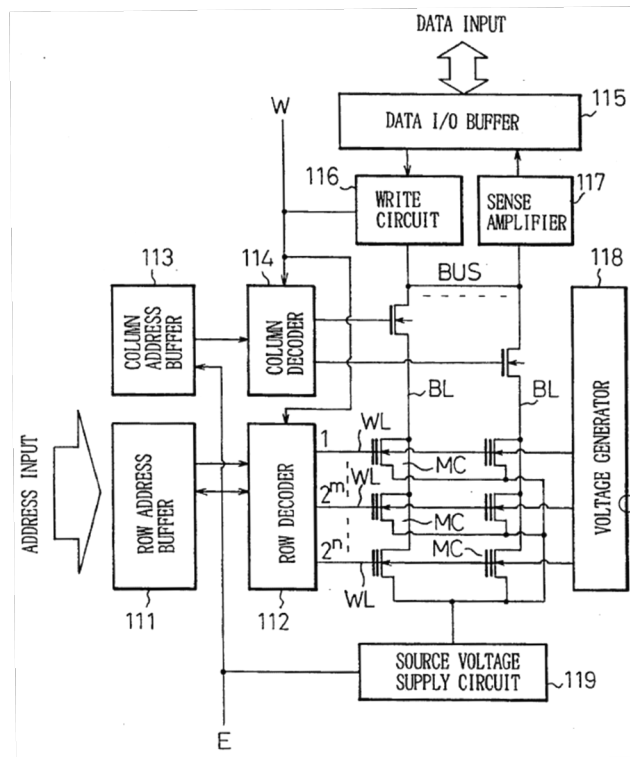


Figure 2 depicts a conventional semiconductor memory device including row address buffer 111, row decoder 112, column address buffer 113, column decoder 114, data I/O buffer 115, write circuit 116, sense amplifier 117, negative voltage generator 118, and source voltage supply circuit 119. *See* Ex. 1010, 11:17–22. The semiconductor memory device involves bit lines BLs, word lines WLs, write control signal W that will be high level H when writing data, and erase control signal E that will be high level H when erasing data. *See id.* at 11:22–26. Akaogi discloses:

When reading data from a memory cell (cell transistor) MC, a row address is given to select a word line WL, and a column address to select a bit line BL, thereby selecting the memory cell,” and “[t]he sense amplifier 117 senses whether or not a current flows through the selected memory cell, to determine whether data stored in the cell is “1” or “0”.

Id. at 11:27–33.

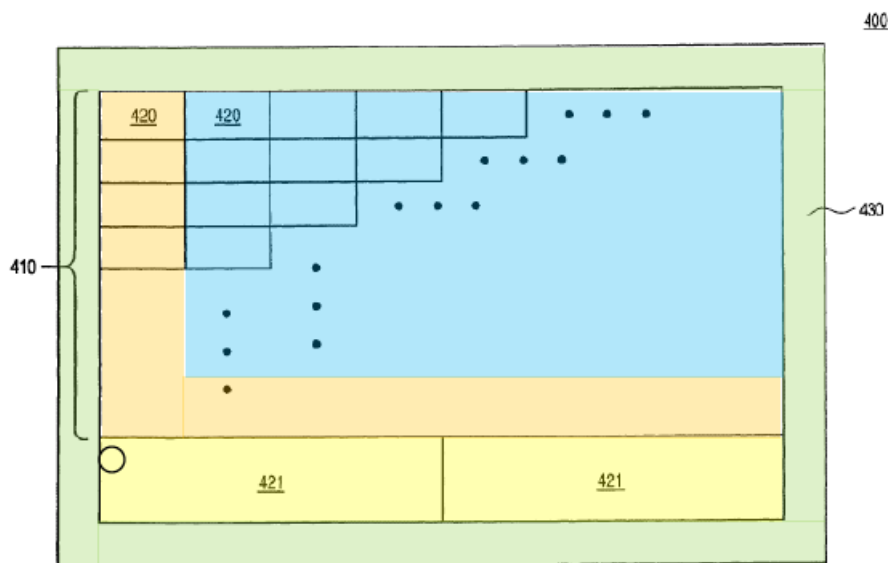
4. Claims 1 and 10

a. 1[p] *A method of electrically interconnecting a periphery area in a flash memory, comprising:*

10[p] *An electrical interconnection system to optimize layout of a periphery area in a memory device, comprising:*

Petitioner contends that How-767 teaches, suggests, and renders obvious the preamble recitations of claims 1 and 10. *See* Pet. 39–41 (reproducing Ex. 1003, Fig. 4 (color added); citing Ex. 1003, 5:41–52; Ex. 1006 ¶¶ 99–103; Pet. 24, 35–39, 42–48), 57 (citing Pet. 24, 35–39; Ex. 1003, Fig. 4; Ex. 1006 ¶¶ 132–133). Petitioner asserts that How-767 teaches or renders obvious configuring ASIC 400 as an SRAM memory device having a core memory area and read/write operation logic circuitry area based on How-767’s teaching that each function block 420 of array 410 can be configured to perform memory functions (e.g., SRAM). *See id.* at 32 (quoting Ex. 1003, 5:53–56; citing Ex. 1003, 5:41–56, 6:1–7; Ex. 1006 ¶¶ 78–84), 78 (similar argument, citing Ex. 1006 ¶ 180).

Petitioner’s colorized version of How-767 Figure 4 is reproduced below:



Pet. 33. Referencing the colorized version of How-767 Figure 4 reproduced above, Petitioner asserts that How-038, which is incorporated by reference in How-767, discloses an exemplary configuration in which some function blocks act as SRAM cells in a SRAM array forming a core area (shown in blue), while SRAM control logic is implemented in a separate function block outside the core area (shown in orange). *See id.* at 32–33 (citing Ex. 1004, 12:8–10, 12:49–52, 12:55–64, 13:4–10; Ex. 1006 ¶¶ 80–83, 85). According to Petitioner, “How-038’s exemplary configuration is consistent with a [person of ordinary skill in the art]’s understanding that, because functional blocks may be configured to perform ‘memory functions,’ ASIC 400 could be beneficially configured as a memory device, which necessarily has both a core memory area and a read/write operation logic circuitry area in order to operate.” *Id.* at 33–34 (citing Ex. 1003, 5:53–56; Ex. 1006 ¶¶ 78–83, 85). Petitioner further asserts that “[c]onfiguring ASIC 400 as a memory device would have provided a degree of customizability to a memory device, making it more suitable for various specific applications.” *Id.* at 34 (citing Ex. 1003, 1:11–17).

Petitioner further contends, “[i]n addition to its specific SRAM configuration, a [person of ordinary skill in the art] would have understood How-767’s reference to ‘memory functions’ to include flash (a well-known memory type) and, thus, disclose or at least suggest configuring ASIC 400 as a flash memory device.” Pet. 34 (citing Ex. 1003, 5:53–56; Ex. 1006 ¶ 86), 99 (citing Ex. 1003, 5:53–56; Ex. 1006 ¶ 211; Pet. 34–35). Petitioner asserts that consistent with How-038’s specific exemplary configuration of SRAM, a flash memory device consists of a core flash memory area and a

read/write operation logic circuitry area. *See id.* (citing Ex. 1004, 13:8–10; Ex. 1006 ¶ 86; Ex. 1010, 11:15–26; Ex. 1014, 146–147).

Petitioner also asserts that a person of ordinary skill in the art “would have further understood that flash memory cells were well-known and could be substituted into the core area for exemplary function blocks 420.” Pet. 34 (citing Ex. 1006 ¶ 87). Petitioner contends How-767 contemplates using different function blocks, and that using flash cells for the core memory array does not affect any claim elements because the challenged claims do not recite a core area. *See id.* at 34–35 (citing Ex. 1003, 5:43–47).

According to Petitioner, a person of ordinary skill in the art “would have understood that SRAM and other types of flash devices equally include read/write operation logic circuitry area apart from the core memory area in order to operate.” *Id.* at 35 (citing Ex. 1006 ¶ 87). Petitioner further asserts that a person of ordinary skill in the art would have understood flash memory to have advantages over SRAM and DRAM memory types, such as, the ability to store data bits even in the absence of power and not needing to be continually refreshed. *See id.* (citing Ex. 1006 ¶ 87).

Petitioner contends that Baker bolsters how a person of ordinary skill in the art would implement How-767’s ASIC 400 as a memory device (*see* Pet. 79 (citing Ex. 1006 ¶ 182)), and confirms the knowledge of a person of ordinary skill in the art in the areas of silicon substrates, memory device layout, flash as a known type of memory device, circuit layouts with rows of transistors parallel to metal interconnect lines, use of resistors in circuitry of periphery of memory devices, and adhering to design rules in laying out source/drain regions. *See* Pet. 79–95 (citations omitted). Petitioner contends that it would have been obvious to one of ordinary skill in the art to use the

background information that Baker provides on interconnect and circuit layers, exemplary circuit elements, and memory device functionality in implementing How-767's ASIC 400 because: (1) a person of ordinary skill in the art would have understood How-767's instruction to configure blocks 420 to perform memory functions to disclose or render obvious configuring ASIC 400 as a memory device for a memory core and accompanying control circuitry, and (2) an obviousness analysis based on How-767's disclosure necessarily requires considering a person of ordinary skill in the art's general knowledge as set forth in Baker. *See id.* at 78 (quoting Ex. 1005, 23; *Koninklijke Philips v. Google*, 948 F.3d 1330, 1337 (Fed. Cir. 2010); citing Ex. 1003, 5:53–56; Ex. 1006 ¶ 180); *KSR*, 550 U.S. at 418.

Petitioner further asserts a person of ordinary skill in the art would have understood “memory functions,” as disclosed by How-767, includes flash memory, as confirmed by Akaogi. *See* Pet. 99 (quoting Ex. 1010, 1:8–10; citing Ex. 1006 ¶ 211). Petitioner contends that a person of ordinary skill in the art “would have understood, as Akaogi confirms, that implementing How-767's ASIC 400 as a flash memory is fully compatible with implementation of other types of memory devices.” *Id.* at 100 (citing Ex. 1006 ¶ 215). Petitioner asserts that Akaogi discloses a flash memory device having an array of memory cells surrounded by support circuitry including row address buffer 111, row decoder 112, column address buffer 113, and column decoder 114, which Petitioner asserts is fully compatible with How-038's disclosure of SRAM cells in a SRAM array separate from SRAM control logic. *See id.* at 100–101 (reproducing Ex. 1010, Fig. 2 (color added); Ex. 1003, Fig. 4 (color added); quoting

Ex. 1010, 11:17–19; citing Ex. 1010, 11:15–33, Fig. 2; Ex. 1004, 12:8–10, 12:49–64, 13:4–10). Petitioner contends that Akaogi’s disclosure matches Baker’s disclosure of a RAM block diagram showing memory array surrounded by row and column logic including row and column address latches, decoders, and buffers. *See id.* at 101 (reproducing Ex. 1010, Fig. 2 (color added); Ex. 1005, Fig. 17.11 (color added); citing Ex. 1005, 142–147). According to Petitioner, “at the level of detail captured in the ’625 Patent claims or disclosed in the ’625 Patent specification, an SRAM memory device and flash memory device are indistinguishable” because SRAM and flash devices each include a core cell area having a plurality of core memory cells and a periphery area having a plurality of sub-circuits. *Id.* at 102–103 (reproducing Ex. 1001, Fig. 1 (color added); citing Ex. 1001, 4:34–42; Ex. 1006 ¶ 217). Petitioner contends that implementing How-767’s ASIC 400 as a flash memory device involves only simple substitutions of components at a level of detail lower than relevant to the claims. *See id.* at 103–104 (citing Ex. 1003, 5:43–47; Ex. 1010, 10:49–11:53, Fig. 1; Ex. 1003, 5:43–55; Ex. 1006 ¶¶ 218–222; Pet. 83–89). Petitioner asserts that it would have been obvious to one of ordinary skill in the art to implement How-767’s ASIC 400 as a flash memory, and in doing so, use the background information that Baker provides on interconnect and circuit layers, exemplary circuit elements, and memory device functionality, as well as information that Akaogi presents regarding flash memory functionality and components because: (1) How-767 discloses, or, at a minimum, renders obvious configuring ASIC 400 as a flash memory by disclosing configuring function blocks 420 to perform memory functions; and (2) Akaogi lists specific advantages of flash memory such as not

needing to be continually refreshed. *See* Pet. 98–99 (quoting Ex. 1003, 5:53–56; Ex. 1010, 1:8–10; citing Ex. 1010, 1:14–30; Ex. 1006 ¶¶ 210–213; Pet. 34–35).

In Response, Patent Owner asserts that How-767 does not disclose or suggest “electrically interconnecting a periphery area in a flash memory,” and “a periphery area in a memory device,” as recited in claims 1 and 10. *See* PO Resp. 61, 64 (citing Ex. 2003 ¶ 163). Patent Owner argues that How-767 fails to disclose a flash memory or any memory device at all. *See id.* at 61–62. Patent Owner contends that an ASIC is not a memory device. *See id.* at 62. According to Patent Owner, “[a]t best, How-767 discloses that an ASIC can include sub-components configured to function in a similar manner as an SRAM or provide similar routing for a ROM.” *Id.* (citing Ex. 1003, 5:53–55, 11:10–13). According to Patent Owner, “an ASIC with sub-components configured to function similar to SRAM does not make How-767’s ASIC 400 ‘a flash memory’ or ‘a memory device.’” *Id.* at 62–63 (citing Ex. 2003 ¶ 158).

Patent Owner further asserts that no person of ordinary skill in the art would have looked to How-767’s ASIC to design the peripheral circuitry in a memory device, because the structure, performance, and purpose of memory devices are different from ASICs. *See* PO Resp. 62–63 (citing Pet. 48; Ex. 2003 ¶ 159), 64 (citing Ex. 2003 ¶ 162). In support of its argument, Patent Owner asserts: (1) the ’625 Patent does not equate ASICs and memory (quoting Ex. 1001, 1:51–60); (2) Baker describes distinguishing characteristics of flash memory, including its reduced size and relative oxide thickness (citing Ex. 1005, 156; Ex. 2003 ¶ 160); and (3) Dr. Lall agrees that the architecture of flash memory is significantly different from previous

generations of memory devices (citing Ex. 1003, Figs. 4, 6; Ex. 2002, 55:5–56:17, 57:17–59:14; Ex. 2003 ¶ 161). *See id.* at 63–64.

In Reply, Petitioner asserts that, although Patent Owner contends that an ASIC is not a memory device, Patent Owner “fails to identify any characteristics of the mapped implemented/modified versions of ASIC 400 that are the subject of the Petition that would distinguish such devices from a memory device.” Pet. Reply 12 (citing PO Resp. 61–67). Petitioner contends that Patent Owner does not dispute that How-767, through incorporated teachings of How-038, expressly discloses that each function block 420 of array 410 can be configured to perform memory functions (e.g., SRAM), configuring multiple function blocks as SRAM cells, and arranging them together to form an SRAM array. *See id.* (citing Pet. 32–33).

Petitioner asserts that Patent Owner’s argument that an ASIC with subcomponents configured to function similar to a SRAM does not make How-767’s ASIC device a flash memory or a memory device “fails to provide any explanation or identification of any specific feature distinguishing ‘function[ing] similar to a SRAM’ from a ‘memory device.’” Pet. Reply 12–13. Petitioner contends that the ’625 Patent describes a flash memory device and a generic memory device based on function and Patent Owner’s witness, Dr. Bagherzadeh stated that a memory device stores data. *See id.* at 13 (quoting Ex. 1001, 1:35–37; quoting Ex. 2019, 20:16–8; citing Ex. 1001, 4:30–33). Petitioner contends that How-767 explicitly discloses configuring function blocks to perform memory functions consistent with how the ’625 Patent and Dr. Bagherzadeh describe the characteristics of a memory device. *See id.*

Petitioner further points out that the Petition also includes an argument that flash memory cells were well-known and could be substituted into the core area for How-767's exemplary function blocks 420. *See* Pet. Reply 13 (quoting Pet. 34). Petitioner contends that where the core area includes flash memory cells in place of exemplary function blocks 420, Patent Owner's criticisms of ASIC function blocks do not apply. *See id.*

In the Sur-reply, Patent Owner argues that apart from Dr. Lall's conclusory testimony, there is no support that a person of ordinary skill in the art would view the How-767 ASIC as a memory device. *See* PO Sur-reply 17. Patent Owner contends that Dr. Bagherzadeh clarified that the How-767 ASIC 400 is not a memory device. *See id.* (citing Ex. 2003 ¶ 158).

We do not agree with Patent Owner's arguments regarding "a memory device." We are unable to appreciate any distinction between "a memory device" recited in the preamble of claim 10 and Patent Owner's assertion that How-767 discloses "an ASIC with subcomponents configured to function similar to SRAM." We credit Dr. Lall's testimony that How-767 teaches or suggests a memory device because it is supported by objective evidence—the SRAM function blocks and SRAM cell array disclosures of How-767 and How-038. *See* Ex. 1003, 5:53–56, 6:1–7; Ex. 1004, 5:45–47, 12:8–10, 12:49–52, 12:55–64, 13:4–10. Dr. Bagherzadeh's opinion that "an ASIC with function blocks configured to function similar to SRAM does not make How-767's ASIC 400 . . . 'a memory device'" is unsupported by objective evidence. Ex. 2003 ¶ 158. Accordingly, we find that How-767 teaches "a memory device" as recited in the preamble of claim 10.

We also do not agree with Patent Owner's same arguments with respect to How-767's ASIC and "a flash memory." *See* PO Resp. 62–63.

As pointed out by Petitioner, Patent Owner's argument that "an ASIC with function blocks configured to function similar to SRAM does not make How-767's ASIC 400 'a flash memory'" is not applicable to Petitioner's argument regarding substitution of flash memory cells into the core area for How-767's function blocks. *See* Pet. Reply 13.

As to the teachings of How-767, in view of the teachings of Baker, and Akaogi, Patent Owner presents several arguments. First, Patent Owner contends that "Akaogi's supposed advantage of flash memories over magnetic storage devices is completely irrelevant to How-767's ASIC and would not have [led] a [person of ordinary skill in the art] to the claimed invention." PO Resp. 75 (citing Pet. 99; Ex. 2003 ¶ 191); Pet. Reply 25 (citing PO Resp. 74–75).

In the Reply, Petitioner contends that "How-767 explicitly teaches an ASIC having function blocks that could be configured for 'memory functions (e.g., SRAM),' and a [person of ordinary skill in the art] would have understood that 'memory functions' includes flash memory." Pet. Reply 27 (citing Pet. 98–99). On this basis, Petitioner asserts that flash is relevant to implementing memory functions as disclosed by How-797, and Akaogi's listing of specific advantages of flash memory would motivate a person of ordinary skill in the art to use flash memory. *See id.* (citing Pet. 98–99).

We do not agree with Patent Owner's argument regarding the irrelevance of flash memory advantages to How-767's ASIC because it is premised on Patent Owner's previous argument that How-767's ASIC is not "a memory device." As explained above, we find How-767 teaches "a memory device" as recited in the preamble of claim 10.

Patent Owner also asserts that Petitioner fails to explain how the ASIC of How-767 would be configured as a flash memory device. *See* PO Resp. 75 (citing Ex. 2003 ¶ 191). According to Patent Owner, a person of ordinary skill in the art “would not have been motivated to modify How-767 to implement a function block as flash memory, i.e., to include a floating gate, because as Dr. Lall admitted a floating gate can predominantly be used for flash memories.” *Id.* (citing Ex. 2002, 57:17–21; Ex. 2003 ¶ 191). Patent Owner also contends that implementing a function block as flash memory would defy How-767’s intended purpose of reconfiguring the function blocks. *See id.* Patent Owner asserts that “Dr. Lall admitted, as of February 2000, flash memories were standalone chips, and therefore a [person of ordinary skill in the art] would not have been motivated to integrate them within an ASIC.” *Id.* (citing Ex. 2002, 53:25–54:3).

In the Reply, Petitioner asserts that Patent Owner’s argument that the Petition does not explain how Akaogi’s flash memory is bodily incorporated into How-767’s ASIC fails as a matter of law. *See* Pet. Reply 27 (citing *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973)). Petitioner reiterates that the Petition explains that using flash cells for the core memory array does not affect any claim elements because the challenged claims do not claim a core area. *See id.* (citing Pet. 35). Petitioner further contends that Patent Owner’s demands for details are inconsistent with the sparse level of detail the ’625 Patent provides of flash memory cells. *See id.* According to Petitioner, “the ’625 Patent discloses nothing other than referencing ‘a core cell area’ having ‘a plurality of core memory cells,’ shown in FIG. 1 in stylistic fashion.” *Id.* (citing Ex. 1001, 4:34–42). Petitioner asserts that its mapping provides more detail than the disclosure of the ’625 Patent. *See id.*

We do not agree with Patent Owner's arguments. Contrary to Patent Owner's arguments regarding integrating a standalone flash memory within an ASIC, the Petition proposes substituting flash memory cells for How-767's function blocks 420. *See* Pet. 34, 103. To the extent that Patent Owner argues that flash memory cells cannot be substituted for How-767's function blocks 420 due to floating gates, we do not agree with Patent Owner's undeveloped argument. Patent Owner does not meaningfully explain why floating gates would be an obstacle to the substitution of flash memory cells for function blocks 420. *See* PO Resp. 75; Ex. 2003 ¶ 191. We also do not agree with Patent Owner's argument that the substitution would defy How-767's intended purpose of reconfiguring the function blocks, because it is not supported by objective evidence. Patent Owner and Dr. Bagherzadeh do not direct us to evidence to support its assertion that How-767's intended purpose is reconfiguration of function blocks. *See* PO Resp. 75; Ex. 2003 ¶ 191. Instead, How-767's intended purpose is directed to customization of a routing architecture between function blocks. *See, e.g.,* Ex. 1003, 1:4–7, 4:19–61, 6:22–31.

Patent Owner also argues that this patentability challenge fails on the basis that it does not identify with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the ground for the challenge to each claim. *See* PO Resp. 74 (quoting 35 U.S.C. § 312 (a)(3); citing 37 C.F.R. § 42.104 (b)); *see also id.* at 73 (arguing that patentability challenges based on How-767 and Baker are catch-all grounds). According to Patent Owner, Petitioner “does not even map a combination of How-767, [] Baker, and Akaogi to the claimed invention.” *Id.* at 74 (quoting Pet. 100; citing Pet. 97–104; Ex. 2003 ¶ 190);

see id. at 73 (similar argument regarding patentability challenges based on How-767 and Baker); PO Sur-reply 24 (quoting Pet. 95–96; citing Pet. 77–95), 25 (citing Pet. 97–104; Pet. Reply 26–27). Patent Owner asserts that to the extent Petitioner is attempting to rely on Baker and Akaogi to satisfy a limitation not disclosed by How-767, or How-767 and Baker, this patentability challenge is an improper “catch-all” grounds. *See id.* at 73 (citing *Adaptics Ltd. v. Perfect Co.*, IPR2018-01596, Paper 20 (PTAB March 6, 2019)), 74 (citing *Adaptics*).

In the Reply, Petitioner contends that this patentability challenge is not a catch-all grounds and is distinguishable from *Adaptics*. *See* Pet. Reply 25. According to Petitioner, “in *Adaptics*, the Board found that the petitioned grounds were not identified with particularity under 35 U.S.C. § 312(a)(3) because the petitioner asserted ‘a large number of secondary references connected by and/or resulting in a multiplicity of grounds.’” *Id.* (citing *Adaptics*). Petitioner contends that the Petition uses Baker and Akaogi for the targeted purpose of providing written evidence of background information and flash memory devices that a person of ordinary skill in the art is presumed to already possess. *See id.* at 25 (quoting Pet. 79; citing Pet. 79–94, 96), 26 (citing Pet. 102–104). Patent Owner further asserts that *Adaptics* is focused on discretionary denial under 35 U.S.C. § 312(a), whereas the Board has already instituted *inter partes* review in these proceedings, and found no issues with particularity or voluminous grounds. *See id.* at 25–26 (citing Dec. 38–40).

In the Sur-reply, Patent Owner quotes *Supercell Oy v. Gree Inc.*, IPR2021-00500, Paper 7 at 9 (PTAB Aug. 16, 2021) for explaining that *Adaptics* explains the importance of the statutory requirement for

particularity. *See* PO Sur-reply 23–24, 25. Patent Owner contends that *Supercell* and *Adaptics* apply to Petitioner’s patentability challenges because the Petition prevents evaluation of Petitioner’s grounds. *See id.* at 24.

We do not agree with Patent Owner’s arguments because we do not discern any impropriety with Petitioner’s use of Baker and Akaogi as evidence of the knowledge and understanding of a person of ordinary skill in the art. *See, e.g.*, Pet. 79–83 (Baker “confirms the knowledge of a [person of ordinary skill in the art] in the following areas (a) Silicon substrates . . . (b) Memory device layout . . . (c) Flash as a known type of memory device.”), 99 (“Akaogi lists specific advantages of flash memory that would motivate a [person of ordinary skill in the art] to use flash memory.”), 100 (A person of ordinary skill in the art “would have understood, as Akaogi confirms, that implementing How-767’s ASIC 400 as a flash memory is fully compatible with implementation of other types of memory devices as previously mapped.”)

Based on the entire trial record, we find that the combination of How-767, Baker, and Akaogi teaches, suggests, and renders obvious “[a] method of electrically interconnecting a periphery area in a flash memory,” as recited in claim 1, and “[a]n electrical interconnection system to optimize layout of a periphery area in a memory device,” as recited in claim 10.

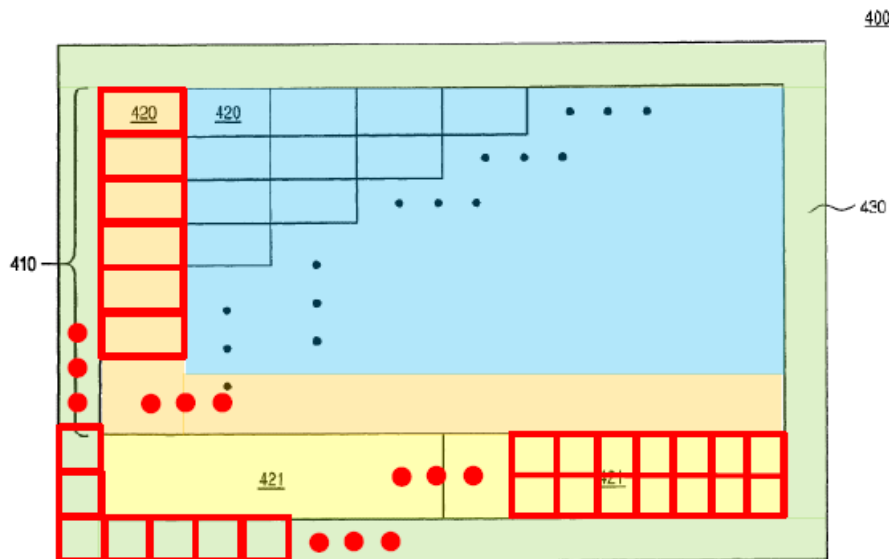
b. 1[a1] providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate,

10[a1] a plurality of sub-circuits fabricated in a periphery area of a silicon substrate

Petitioner contends that How-767 discloses or renders obvious “providing a plurality of sub-circuits fabricated in a periphery area of a

silicon substrate,” as recited in claim 1, and recited similarly in claim 10, based on providing a plurality of function blocks in all regions of ASIC 400, which, according to Petitioner (referring to a colorized reproduction of How-767 Figure 4) includes orange SRAM control logic function blocks outside blue core area of SRAM array, yellow specialized regions 421, and green periphery area 430. *See* Pet. 42 (citing Ex. 1003, 5:41–56, 12:8–10, 12:49–64, 13:4–10; Ex. 1006 ¶ 104; Pet. 25–35), 58 (citing Pet. 42–44); Pet. Reply 16 (similar argument). Petitioner also asserts that How-767 teaches or renders obvious subdividing each of specialized regions 421 and periphery area 430 into function blocks, and that these multiple function blocks in each area constitute a plurality of sub-circuits. *See* Pet. 42–43 (reproducing Ex. 1003, Fig. 4 (annotations and color added); citing Ex. 1003, 6:11–63, 11:4–7; Ex. 1006 ¶ 105; citing Pet. 27–31).

Petitioner’s colorized and annotated version of How-767 Figure 4 is reproduced below:



Petitioner asserts that periphery area 430 has IO pads and other support circuitry. *See id.* at 25 (citing Ex. 1003, 5:41–52, 11:4–7), 43 (quoting

Ex. 1003, 5:48–52; citing Ex. 1003, 5:47–64). Petitioner contends that How-767 discloses using lower metal layers for routing within function blocks and upper metal layers for routing between function blocks. *See id.* at 26–27 (reproducing Ex. 1003, Fig. 6 (color added); quoting Ex. 1003, 2:6–11, 6:14–19, 6:43–50; citing Ex. 1003, code (57), 2:6–63, 6:11–19, 6:43–50; Ex. 1006 ¶¶ 67–69). Petitioner asserts that, in addition to using lower metal layers for internal routing and upper metal layers for between routing for array 410, How-767 also discloses routing for specialized regions 421 can be done in accordance with the invention, and various IO and periphery circuitry 430 can also be configurable with a method in accordance with the invention. *See id.* at 27–28 (quoting Ex. 1003, 8:36–37, 11:4–7; citing Ex. 1003, 6:11–63; Pet. 26–27); Pet. Reply 18 (quoting Ex. 1003, 8:36–37, 11:4–7). Petitioner contends that How-767, therefore, discloses function block routing architecture in each of array 410, specialized regions 421, and periphery circuitry 430. *See* Pet. 28. (reproducing Ex. 1003, Fig. 4 (color added); citing Ex. 1006 ¶ 72).

According to Petitioner, “[b]ecause How-767’s internal/between function block routing architecture ‘in accordance with the invention’ requires an internal/external demarcation and uses ‘function blocks’ as that demarcation, a [person of ordinary skill in the art] would have understood How-767 as disclosing, or at a minimum rendering obvious, sub-dividing each of specialized regions 421 and periphery circuitry 430 into a number of function blocks just as with array 410.” Pet. 29 (citing Ex. 1006 ¶ 73). Petitioner points out that How-767 describes function block demarcation as conceptual and provides generic illustrations with dashed lines in Figures 2 and 3. *See id.* at 29–30 (reproducing Ex. 1003, Figs. 2, 3; citing Ex. 1003,

2:35–44, 3:20–23). Petitioner contends that, as a result, a person of ordinary skill in the art “would have applied the same type of ‘conceptual’ function block demarcation to each of specialized regions 421 and periphery circuitry 430 . . . because doing so was a necessary step to implement the internal/between function block routing architecture in those regions as How-767 instructs.” *Id.* at 30–31 (reproducing Ex. 1003, Fig. 4 (annotations and color added); citing Ex. 1006 ¶ 75); *see* Pet. Reply 19 (similar argument, reproducing Ex. 1003, Figs. 2, 3; citing Pet. 27–31; Ex. 1006 ¶¶ 71–77). Petitioner also asserts that a person of ordinary skill in the art would have understood specialized regions 421 and periphery circuitry 430 “would benefit from reducing wasted on-chip space (e.g., routing channels, unused function blocks, etc.) while maintaining high performance, which may be achieved by How-767’s function-block-based routing architecture.” Pet. 30–31 (citing Ex. 1006 ¶ 75).

Patent Owner contends that How-767 does not disclose a plurality a sub-circuits fabricated in a periphery area of a silicon substrate, as required by claims 1 and 10. *See* PO Resp. 55–61. Patent Owner contends that Petitioner’s colorized and annotated reproductions of How-767’s Figure 4 “are, at best, fanciful extrapolations of How-767.” *Id.* at 57; *see id.* at 58 (similar argument, citing Pet. 40; Ex. 2002, 246:22–247:13; Ex. 2003 ¶ 150). Patent Owner contends that “arbitrary orange region of the ASIC 400 . . . is part of ‘an array 410 of function blocks 420.’” *Id.* at 58 (citing Ex. 1003, 5:43–44). According to Patent Owner, “[t]he array 410 of function blocks 420 cannot be part of the periphery area 430 **surrounding array 410**, especially when the ‘periphery area includes circuitry such as IO pads and other support circuitry **for array 410**.” *Id.* (quoting Ex. 1003, 5:50–52).

Patent Owner contends that the array 410 cannot be the periphery for itself because How-767 distinguishes it from the periphery 430. *See id.* at 57–58 (citing Ex. 2003 ¶ 149). Patent Owner further asserts that How-767 does not suggest that function blocks 420 can be in the other region/specialized region 421, or periphery area 430. *Id.* at 58. Patent Owner argues that there is no disclosure in How-767 about specialized regions 421 including function blocks, but instead explicitly states that specialized regions 421 contain blocks or cores that are different from function blocks. *See id.* (quoting Ex. 1003, 5:43–49).

In the Reply, Petitioner contends that Patent Owner’s arguments fail because it assumes, contrary to Patent Owner’s proposed claim construction for “periphery area” that because How-767 labels one area periphery area 420 that other areas cannot meet the requirements of the claimed periphery area. *See* Pet. Reply 18. Petitioner asserts that Patent Owner’s construction for the claimed periphery area is “outside the core memory cell area of the claimed memory.” *See id.* (citing Pet. 24; PO Resp. 32).

According to Petitioner, applying this construction for periphery area, green periphery area 430, as well as yellow specialized regions 421 and orange function blocks 420 for SRAM control logic are outside of the blue core function blocks 420 for SRAM memory cells. *See id.*; *see id.* at 17 (reproducing Ex. 1003, Fig. 4 (color added); citing Pet. 37; Ex. 1006 ¶ 92). According to Petitioner, the colorized reproduction of How-767’s Figure 4 “illustrates How-767’s express teaching that, when implementing an SRAM array using function blocks, ‘SRAM control logic [for a memory function block is] implemented in a *separate function block*,’ which are different than function blocks performing memory functions and may be arranged ‘at

the edge of an SRAM bit array.” *Id.* at 17–18 (quoting Ex. 1004, 12:63–64, 13:9–10; citing Ex. 1004, 12:8–10, 12:49–52, 12:55–63, 13:4–9; Ex. 1006 ¶¶ 83–87). Petitioner points out that Patent Owner does not challenge that Petitioner’s colorized reproduction of How-767’s Figure 4 reflects How-767’s express disclosure. *See id.* at 18.

In the Sur-reply, Patent Owner asserts that Petitioner admits that How-767 labels one area “periphery 430” but considers that label to be irrelevant. *See* PO Sur-reply 22 (citing Pet. Reply 18). Patent Owner contends that the labeling is relevant to whether a person of ordinary skill in the art would understand that How-767’s defined periphery area is not really a periphery area. *See id.*

We do not agree with Patent Owner’s arguments regarding a periphery area because they are not consistent with the claim construction advanced by Patent Owner and adopted in Section II.C. As explained above in Section II.C., Patent Owner asserts that the claim term “periphery area” should be construed as “the area outside the core memory cell area of the claimed memory.” PO Resp. 32; PO Sur-reply 3. Patent Owner’s argument, however, is premised on periphery area being construed as only the area labeled periphery area in How-767. Patent Owner also misapprehends Petitioner’s position as modifying array 410 of function blocks 420 to be part of the specialized regions 421 or periphery area 430. *See* PO Resp. 57–58. The Petition does not propose modifying array 410 of function blocks 420, or the SRAM logic function blocks outside core SRAM memory cells to be part of periphery area 430. *See* Pet. 25–43. Patent Owner’s arguments also overlook that Petitioner relies on How-767’s teachings that incorporate by reference

How-038's teachings of a SRAM array, SRAM control logic in a separate function block, and requiring strong drivers at the edge of a SRAM array. *See* Pet. 32–34. Based on the entire trial record, we find that How-767's SRAM control logic function blocks outside core area of SRAM array, specialized regions 421, and periphery area 430 teaches “a periphery area” as recited in claims 1 and 10 and construed according to the parties' agreed upon construction.

Patent Owner also argues the How-767 does not contemplate any division or subdivision of specialized regions 421 or periphery area 430. *See* PO Resp. 58–59 (quoting Ex. 1003, 5:47–51; Ex. 2003 ¶ 151), 59 (similar argument, citing Ex. 1003), 66 (similar argument, citing Ex. 1003; Ex. 2003 ¶¶ 168–169). Patent Owner asserts that there is no disclosure that characterizes the specialized regions 421 as being in a subdivided area of the periphery. *See id.* at 59 (quoting Ex. 1003, 8:36–38; citing Ex. 1003). Patent Owner contends that Petitioner makes a conclusory leap that just because routing can be performed for specialized regions 421, a person of ordinary skill in the art would have understood How-767 to disclose or render obvious subdividing each of specialized regions 421 and periphery circuitry 430 into a number of function blocks just like function block array 410. *See id.* (quoting Pet. 13, 29; citing Ex. 2002, 250:7–22; Ex. 2003 ¶ 152). Patent Owner further contends that Petitioner's statement provides no reason why and how a person of ordinary skill in the art would be motivated to subdivide specialized regions 421 and periphery circuitry 430. *See id.* at 65 (citing Ex. 2003 ¶ 166). Patent Owner contends that the modification would render How-767's ASIC inoperable. *See id.* at 65–66 (citing Ex. 2003 ¶¶ 166–167).

Related to the previous argument, Patent Owner argues that Dr. Lall's testimony is conclusory and not competent evidence when he testifies that a person of ordinary skill in the art would have applied the same type of conceptual function block demarcation to specialized regions 421 and periphery circuitry because it was a necessary step to implement the internal/between function block routing architecture in those areas. *See* PO Resp. 66 (quoting Pet. 30; *TQ Delta v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019); citing Ex. 2003 ¶¶ 168–169). Patent Owner contends that no person of ordinary skill in the art “would have read How-767 and understood the entire circuit shown in Figure 4 could be chopped up into one giant set of function blocks because doing so would never work.” *Id.* at 67 (citing Ex. 1003, Fig. 4; Ex. 2003 ¶ 169). According to Patent Owner, “[i]nstead, a [person of ordinary skill in the art] would have understood the specialized regions 421 and periphery circuitry 430 in How-767 are integral to the operability of its ASIC and could not be replaced.” *Id.* (citing Ex. 1003, 8:36–38, 11:4–7; Ex. 1005, 136; Ex. 2003 ¶ 170).

Related to the previous arguments, Patent Owner contends that, based on certain disclosures of How-767, a person of ordinary skill in the art “would have understood that, in How-767, function blocks can be formed to have local interconnections in lower layers M1, M2.” PO Resp. 60; *see id.* at 59–60 (quoting Ex. 1003, 6:40–43, 8:3–5; citing Ex. 2003 ¶ 153), 66–67 (similar argument, quoting Ex. 1003, 8:36–38, 11:4–7; citing Ex. 2003 ¶ 169). On this basis, Patent Owner contends that a person of ordinary skill in the art “would not have understood that M1 and M2 routing within function blocks 420 would teach sub-dividing specialized regions 421 and periphery circuitry 430. How-767's routing architecture is actually agnostic

to the lower layer routing and therefore the underlying circuitry.” *Id.* at 60 (quoting Ex. 1003, claim 1, 2:3–5). Patent Owner contends that, as a result, a person of ordinary skill in the art would have understood How-767’s Figure 4 to, at best, show already divided function blocks 420, specialized regions 421, and periphery circuitry 430. *See id.* at 60–61 (reproducing Ex. 1003, Fig. 4 (colored lines added)); Ex. 2003 ¶ 154.

In the Reply, Petitioner asserts that Patent Owner misstates Petitioner’s position. *See* Pet. Reply 20 (citing PO Resp. 58). Petitioner contends that the Petition does not propose replacing the circuitry of specialized region 421 or periphery area 430 with function blocks. *See id.* Petitioner asserts that instead the Petition states that a person of ordinary skill in the art would have applied the same type of conceptual function block demarcation to specialized regions 421 and periphery area 430. *See id.* (quoting Pet. 29–30). Petitioner asserts that How-767’s description of the circuitry contained in specialized regions 421 and periphery area 430 is left intact and simply implements routing of that circuitry, which is otherwise unspecified, in accordance with How-767’s own description. *See id.*

Petitioner further contends that Patent Owner’s cited disclosures of How-767 contradict Patent Owner’s position. Pet. Reply 20. According to Petitioner, “rather than suggesting that F[igure] 6 is agnostic to lower-layer routing, How-767 states: ‘It is to be understood with reference to FIG 6 that **local interconnections within** each function block are formed **in lower metal layers, e.g., M1 and M2, which are not shown.**’” *Id.* at 20–21 (quoting Ex. 1003, 6:40–43; citing Ex. 1003, 4:32–34). Petitioner contends the description of Figure 6 is fully consistent with other portions of the specification describing the complimentary internal/between routing in

which upper-layer routing (e.g., M3/M4) is intended for routing and interconnections between function blocks, while the lower-layers (e.g., M1/M2) provide routing and interconnections internal to function blocks. *See id.* at 21 (quoting 6:14–19, 6:40–43; citing Pet. 11–12, 26–27, 46–47; Ex. 1003, 4:22–34; Ex. 1006 ¶¶ 66–70).

We do not agree with Patent Owner’s arguments because Petitioner does not propose physically subdividing specialized regions 421 and periphery area 430. *See* Pet. 27–31. Contrary to Patent Owner’s arguments, as explained in the Petition, “How-767’s internal/between function block routing architecture ‘in accordance with the invention’ requires an internal/external demarcation, and uses ‘function blocks’ as that demarcation,” and describes function block demarcation as conceptual. *Id.* at 29. As also explained in the Petition, How-767 discloses: (1) routing for specialized regions 421 can be done in accordance with the invention; and (2) not only is routing between function modules configurable, but various IO and periphery circuitry 430 can also be easily configurable with a method in accordance with the invention. *See id.* at 27–28 (quoting Ex. 1003, 8:36–37, 11:4–7). We agree with Petitioner that How-767 therefore “discloses using the internal/between functional block routing architecture (i.e., a conceptual function block demarcation) in each of [] array 410, [] specialized regions 421, and [] periphery circuitry 430.” *Id.* at 28 (citing Ex. 1006 ¶ 72). The cited disclosures of How-767 supports Dr. Lall’s testimony that a person of ordinary skill in the art “would have applied the same type of ‘conceptual’ function block demarcation to each of specialized regions 421 and periphery circuitry 430 . . . , because doing so was a necessary step to implement the internal/between function block

routing architecture in those regions as How-767 instructs.” *Id.* at 30 (citing Ex. 1006 ¶ 75).

We also do not agree with Patent Owner’s arguments characterizing How-767’s Figure 6, which is a generalized block diagram of an “architecture in accordance with the invention.” Ex. 1003, 5:11–14, 6:38–40. As Petitioner points out, Patent Owner overlooks that Figure 6 includes, but does not show, local interconnections within each function block formed in lower metal layers M1 and M2, and focuses on showing upper metal layers M3 and M4. *See id.* at 6:38–63. As Petitioner explains, How-767’s disclosure of Figure 6 is consistent with other portions of How-767 describing upper-layer routing (e.g., M3/M4) for routing and interconnections between function blocks and lower-layer routing (e.g., M1/M2) for routing and interconnections internal to function blocks. *See* Pet. Reply 21. Accordingly, we do not agree that How-767’s disclosures related to Figure 6 undermine Petitioner’s position that a person of ordinary skill in the art “would have applied the same type of ‘conceptual’ function block demarcation to each of specialized regions 421 and periphery circuitry 430.” Pet. 30 (citing Ex. 1006 ¶ 75).

Based on the entire trial record, we find that How-767’s teaches, suggests, and renders obvious “providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate,” as recited in claim 1 and similarly recited in claim 10.

c. 1[a2], 10[a2] wherein each sub-circuit includes at least one electrical circuit having a plurality of circuit components,

Petitioner contends that How-767 teaches, suggests, or renders obvious “wherein each sub-circuit includes at least one electrical circuit

having a plurality of circuit components,” as recited in claims 1 and 10, based on How-767’s disclosure that active layer devices are formed independently of one another and require interconnects to interconnect the devices thereby forming a circuit, and using two layers of metal interconnects for internal interconnections within each function block. *See* Pet. 44 (quoting Ex. 1003, 1:24–28; citing Ex. 1003, 6:11–63); 58 (citing Pet. 44). Petitioner asserts that the existence of internal routing with a function block to connect active layer devices necessarily requires the function block contain a plurality of active layer devices interconnected to form at least one electrical circuit. *See id.* at 44 (citing Ex. 1006 ¶ 107).

Patent Owner does not dispute Petitioner’s assertions addressing this limitation. *See generally* PO Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

Based on the entire trial record, we find that How-767 teaches “each sub-circuit includes at least one electrical circuit having a plurality of circuit components” as recited in claims 1 and 10 for the reasons discussed in the Petition. *See* Pet. 44, 58.

- d. 1[b] partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction;*
- 10[b] a first metal interconnect layer comprising a plurality of first metal layer lines that partially electrically connect the circuit components of said electric circuits, wherein said first metal layer lines are fabricated to be oriented to extend substantially in one direction;*

1[c] completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are oriented substantially perpendicular to said first metal layer lines, and

10[c] a second metal interconnect layer comprising a plurality of second metal layer lines that complete the electrical connection of said circuit components of said electric circuits, wherein said second metal layer lines are fabricated to be oriented to extend substantially perpendicular to said first metal layer lines; and

Petitioner contends that How-767 teaches or suggests “partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction” and “completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are oriented substantially perpendicular to said first metal layer lines,” as recited in claim 1, and similarly recited in claim 10, based on How-767’s disclosure that routing internal to each function block uses horizontal connectors M1 and vertical connectors M2 (and vice versa). *See* Pet. 44–45 (citing Ex. 1003, 1:62–2:5, 6:14–19), 58 (citing Pet. 44–46). Petitioner asserts that all metal lines in the M1 layer run in a first direction such that all the lines lie substantially parallel to one another. *See id.* at 45 (citing Ex. 1003, 2:6–11; Ex. 1006 ¶ 109). Petitioner asserts that connectors in M2 are in the direction (horizontal or vertical) that are not used by M1 and are run substantially perpendicular to the first direction used for metal lines of M1. *See id.* at 46 (citing Ex. 1003, 2:6–17, 6:14–19; Ex. 1006 ¶ 112). According to Petitioner, “[b]ecause M1 and M2 collectively accomplish internal routing, M1 . . . **partially** electrically interconnects

circuit components in a function block,” and “M2 . . . *completes* electrical interconnections of circuit components in a given function block.” *Id.* at 44–45 (citing Ex. 1006 ¶ 108), 45–46 (citing Ex. 1006 ¶ 111). Petitioner further contends that How-767 discloses partially interconnecting circuit components using M1 and completing interconnections using M2 in all areas of ASIC 400, and therefore, in all periphery areas. *See id.* at 45 (citing Ex. 1003, Fig. 4, 5:41–56, 12:8–10, 12:49–64, 13:4–10; Ex. 1006 ¶ 110; Pet. 27–31), 46 (citing Ex. 1003, Fig. 4, 5:41–56, 12:8–10, 12:49–64, 13:4–10; Ex. 1006 ¶ 113; Pet. 27–31).

Patent Owner does not dispute Petitioner’s assertions addressing this limitation. *See generally* PO Resp. In any event, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we find that How-767 teaches the aforementioned limitations of claims 1 and 10 for the reasons discussed in the Petition. *See* Pet. 44–46, 58.

e. 1[d] electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines.

10[d1] a third metal interconnect layer comprising a plurality of third metal layer lines that electrically interconnect said plurality of sub-circuits,

Petitioner contends that How-767 teaches “electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines,” as recited in claim 1, and similarly recited in claim 10, based on How-767’s disclosure of using uppermost metal layers M3 and M4

to provide routing between function blocks. *See* Pet. 46 (quoting Ex. 1003, 6:27–37), 59 (citing Pet. 46–48). According to Petitioner, “each of M3 and M4 is independently a claimed third metal interconnect layer and each performs the claimed electrical interconnecting of sub-circuits.” *Id.* at 46–47 (reproducing Ex. 1003, Fig. 6 (color added); citing Ex. 1003, 6:43–50; Ex. 1006 ¶¶ 114–116), 59 (citing Pet. 46–48). In a footnote, Petitioner explains

The claimed “electrically interconnecting” in this limitation stands in contrast to the more specific “partially electrically interconnecting” and “completing the electrical interconnection” of Limitations 1[b]-1[c]. Each of M3 and M4’s role in *collectively* interconnecting function blocks, the claimed sub-circuits, independently meets the claim language. Further, to the extent the mapped layer (M3 or M4) is not used for interconnecting a particular function block, that function block would not be part of the “plurality” of sub-circuits mapped for Claim 1.

Pet. 47, n.9 (citing Ex. 1006 ¶ 115). Petitioner asserts that How-767 discloses using M3 and M4 to interconnect a predetermined number of function blocks in all areas of ASIC 400, and in all periphery areas. *See id.* at 48 (citing Ex. 1003, Fig. 4, 5:41–56, 12:8–10, 12:49–64, 13:4–10; Ex. 1006 ¶ 118; Pet. 27–31).

Patent Owner asserts that the ’625 Patent claims a single third metal interconnect layer that electrically interconnects the sub-circuits. *See* PO Resp. 37–40 (reproducing Ex. 1001, Figs. 2, 3 (color added); quoting Ex. 1001, code (57), 3:33–36, 3:66–4:1, 7:10–13; Ex. 2002, 84:21–22, 85:2, 85:6–7, 92:16–18; Ex. 1006 ¶¶ 50–51; citing Ex. 1001, 2:66–3:2, 3:31–44, 6:5–17, claims 1, 2, 3, 10; Ex. 2002, 85:9–86:14, 91:25–92:18, 94:15–99:7; Ex. 1006 ¶ 48; Ex. 2003 ¶¶ 60, 124–131). According to Patent Owner,

“[w]hen considering the claims of the ’625 patent as a whole, a [person of ordinary skill in the art] would have understood that the claimed ‘a third metal interconnect layer including a plurality of third metal layer lines’ ‘electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits’ refers to a single metal layer.”

Id. at 41–42 (citing Ex. 2003 ¶¶ 132–133). Patent Owner asserts that a person of ordinary skill in the art

would have understood that reading the claimed “a third interconnect metal layer” as more than one metal layer wherein the multiple layers are oriented in different directions would be **inconsistent** with the specification because the ’625 patent even states that the advantages are that “the third metal lines can be substantially straight and be routed on top of the sub-circuits such that consumption of the periphery area is minimized” (Ex-1001, 4:1-4) and “no additional layout area is required between the sub-circuits 18 for the third metal interconnect layer (M3) 26 and consumption of the periphery area 14 is further minimized” (Ex-1001, 8:42-47).

Id. at 42 (citing Ex. 2003 ¶¶ 132–133).

Patent Owner also contends that How-767 does not disclose a third metal interconnect layer because Petitioner “relies on a combination of two separate and distinct layers [M3 and M4] to meet the claim limitation.” PO Resp. 37 (quoting Pet. 46, 60, 73–74; citing Ex. 2003 ¶¶ 111–112); *see id.* at 47–48 (arguing Dr. Lall confirms M3 and M4 are distinct layers, quoting Ex. 2002, 102:25–103:7, 111:20–23, 111:25–112:2; citing Ex. 2003 ¶¶ 121–122). Patent Owner asserts that separate and distinct layers M3 and M4 do not interconnect and, by themselves do not form an electrical connection at all. *See* PO Resp. 42–44 (reproducing Ex. 1003, Fig. 6; quoting Ex. 1006 ¶ 68; Ex. 1003, 6:34, 6:43–52; citing Ex. 2002, 98:5–99:4;

Ex. 2003 ¶¶ 113–115, 134). Patent Owner further contends that “to the extent any electrical interconnection is formed at those layers, there is also no dispute that How-767 requires **both** metal layers for that connection.” *Id.* at 44 (quoting Ex. 1003, 6:56–63; citing Ex. 1003, 6:40–63; Ex. 2003 ¶ 117); *see id.* at 45–47 (reproducing Ex. 1003, Fig. 6 (annotations and color added); quoting Ex. 1003, code (57), 4:22–24, 6:26–31, 11:24–27; citing Ex. 2003 ¶¶ 118–120). Patent Owner asserts that M3 alone cannot electrically interconnect function blocks and M4 alone cannot electrically interconnect function blocks. *See id.* at 48 (citing Ex. 2003 ¶ 123). Patent Owner asserts that a person of ordinary skill in the art

would have understood that the claimed “electrically interconnecting” of sub-circuits with a metal layer requires actually forming an electrical interconnection, i.e., a structure that can route an electrical signal between two points in an electrically interconnected circuit. A wire in an open circuit does not electrically interconnect anything or form any electrical interconnection. It is just a wire.

PO Resp. 49–50 (citing Ex. 2003 ¶ 137). Patent Owner contends that the ’625 Patent, How-767, How-038, and Baker confirm that electrically interconnecting requires more than a single wire in an open circuit. *See id.* at 50–51 (quoting Ex. 1001, code (57), 3:31–33, 3:66–4:1; Ex. 1003, 1:26–30; Ex. 1004, 1:15–17, 2:3–6; Ex. 1005, 78, 125; citing Ex. 2003 ¶¶ 138–140). According to Patent Owner, “[b]y definition, an open circuit is not an electrical connection and does not electrically interconnect sub-circuits.” *Id.* at 50 (citing Ex. 2003 ¶ 138).

Patent Owner further asserts that Petitioner and Dr. Lall attempt to rewrite the claims because Petitioner “and Dr. Lall appear to contend that the claimed ‘**electrically interconnecting** each respective sub-circuit with a

predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines’ . . . requires no more than a wire in an open circuit.” PO Resp. 48–49 (quoting Pet. 47 n.9; Ex. 1006 ¶ 115; Ex. 2002, 194:14–195:2, 196:3–8; citing Ex. 1001, claims 1, 10; Ex. 2002, 202:3–16, 206:1–16, 122:10–15; Ex. 2003 ¶¶ 135–136). Patent Owner contends that, even accepting Dr. Lall’s theory that a third metal layer line need only interconnect sub-circuits without any degree of completion, would mean the same interconnect structure could simultaneously be electrically interconnecting and not-electrically interconnecting two points. *See id.* at 51–54 (reproducing Ex. 1003, Fig. 6 (annotations and color added); quoting Ex. 2002, 194:14–195:2; citing Ex. 2003 ¶¶ 141–143).

Patent Owner contends that “How-767’s M3 and M4 metal layers do not ‘independently’ electrically interconnect anything.” PO Resp. 54 (quoting Ex. 1003, claim 1). Patent Owner asserts that How-767 describes the opposite when describing a fixed metal layer M3, insulating layer and customizable metal layer M4 on top of the insulating layer. *See id.* at 54–55 (quoting Ex. 1003, 4:28–34, 4:35–39, 4:44–49; citing Ex. 1003, 4:18–50; Ex. 1006 ¶ 115; Ex. 2003 ¶ 144).

In the Reply, Petitioner asserts that the Patent Owner Response does not formally propose a construction of “a third metal interconnect layer” and “electrically interconnecting” but extensively argues the meaning of the claim phrases. *See* Pet. Reply 4 (quoting PO Resp. 40, 43; citing PO Resp. 40–43, 49–50). According to Petitioner, Patent Owner’s “arguments therefore depend on a construction requiring the third metal interconnect layer *solely* or *exclusively* ‘electrically interconnecting.’” *Id.* (quoting

Ex. 1019, 25:16–26:2). Petitioner contends that Patent Owner’s “interpretation improperly adds a ‘narrowing modifier before an otherwise general term that stands unmodified in a claim.’” *Id.* at 4–5 (quoting *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998)). Petitioner asserts that the plain language of a layer “electrically interconnecting” is broad enough to include two layers collectively interconnecting, as demonstrated by the surrounding claim language. *See id.* at 5 (quoting *Phillips*, 415 F.3d at 1305; citing Pet. 47 n.9). Petitioner points out that “the independent claims separately recite lines in a first metal layer that ‘**partially** electrically interconnect’ ‘circuit components’ and lines in a second, separate metal layer ‘that **complete** the electrical connection **of said circuit components**.’” *Id.* (citing Ex. 1001, 10:14–24); *see id.* at 6 (asserting the ’625 Patent Specification discloses the same, quoting Ex. 1001, 3:14–24). Petitioner argues that the third metal interconnect layer language recites “electrically interconnecting” without any modifier, and therefore, is broad enough to include the narrower phrase “partially electrically interconnects” language. *See id.* at 5, 6–7. Petitioner also argues that Patent Owner’s position that the third metal layer must exclusively accomplish electrical interconnections is contradictory to the claims use of the open-ended transition phrase “comprising” which does not exclude additional structures. *See id.* at 6 (quoting *Vehicular Techs. Corp. v. Titan Wheel Int’l, Inc.*, 212 F.3d 1377, 1383, (Fed. Cir. 2000)). Petitioner contends that the ’625 Patent disclosure of an embodiment where interconnections between sub-circuits completely formed within a single metal layer is not a proper basis for limiting the construction of claim terms to that specific embodiment. *See id.* (quoting *Phillips*, 415 F.3d at 1323).

According to Petitioner, the claims and '625 Patent Specification “demonstrate that the plain language of a layer ‘electrically interconnecting’ is broad enough to include either a single layer providing the electrical interconnection, or multiple layers collectively providing the electrical interconnection, and [Patent Owner] identifies no basis to override this plain language.” *Id.* at 7.

Petitioner contends that Patent Owner’s arguments are premised on Patent Owner’s erroneous claim construction. *See* Pet. Reply 8–9 (quoting PO Resp. 40, 54; citing Pet. Reply 4–7). Petitioner asserts, that when correctly construed, there is no dispute that How-757’s M3 and M4 layers collectively interconnect function blocks. *See id.* at 9 (quoting PO Resp. 16, 24; Pet. 51; citing Ex. 1002, 110:21–111:7, 112:3–113:24; Ex. 1003, 4:28–34, 4:38–42). Petitioner contends that Patent Owner’s “annotations to How-767’s [Figure] 6 support the complementary roles of How-767’s M3/M4 layers in electrically interconnecting function blocks.” *Id.* at 9–11 (reproducing Petitioner’s annotated reproductions of Ex. 1003, Fig. 6 (with Patent Owner’s annotations); quoting PO Resp. 53–54; citing Ex. 2002, 205:25–207:14; Pet. Reply 4–7). Petitioner further argues that Patent Owner’s “characterizations of why How-767’s M3 and M4 are insufficient focus on a single layer in isolation, ignoring the reality that each such layer does not exist in isolation, but are part of a multilayer design.” *Id.* at 11. Petitioner asserts that there is no basis to characterize How-767 as disclosing “a single wire in an open circuit.” *See id.* (citing PO Resp. 49–51).

According to Petitioner,

to the extent M3 includes “a single wire,” that wire is not “in an open circuit” but is undisputedly part of an interconnection

scheme connecting to M1 and M2 below and M4 above. It is only an “open circuit” if M1, M2 and M4 do not exist, which is not what How-767 discloses.

Pet. Reply 11–12.

In the Sur-reply, Patent Owner asserts that it is Petitioner “that seeks to stretch the plain meaning of [the] claims, which require ‘*a* third metal interconnect *layer*.’” PO Sur-reply 4 (citing Ex. 1001, claim 10). According to Patent Owner, Petitioner “cannot override the claim requirement that *a* third metal interconnect *layer* performs the claimed connection.” *Id.* Patent Owner argues that Petitioner’s attempts to support its construction through the other claim language undermines its argument because, “if the inventors had intended that the third metal interconnect layer only partially connect the sub-circuits, then they would have recited that the third metal interconnect layer ‘partially electrically interconnect’ those sub-circuits.” *Id.*

Patent Owner also argues that Petitioner’s arguments regarding the claim construction are untimely because Petitioner did not propose a construction for this term and the Board did not address it in the Institution Decision. *See* PO Sur-reply 5 (citing Pet. 20–24; Dec. 10). Patent Owner argues that the Board need not consider newly proposed claim constructions in Petitioner’s Reply. *See id.* (quoting *Dolby Labs., Inc., v. Intertrust Techs. Corp.*, IPR2020-01123, Paper 33 at 17 (PTAB. Dec. 15, 2021); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330–31 (Fed. Cir. 2019); citing CTPG, 73–74; 37 C.F.R. § 42.23(b)).

As an initial matter, we do not agree that Petitioner’s arguments are untimely. Petitioner does not present or request an express claim construction in the Reply. *See* Pet. Reply 4–7. Petitioner’s Reply arguments instead are consistent with its position in the Petition (*see* Pet. 46–48) and

respond to Patent Owner's Response (*see* PO Resp. 37–42, 49–51) that the claims require a single third metal interconnect layer and electrically interconnecting requires actually forming an electrical interconnection and requires more than a wire in an open circuit (i.e., a complete electrical interconnection). *See* Pet. Reply 4–7, 8–12.

We also do not agree with Patent Owner's arguments that the claims require a single third metal interconnect layer based on the recitation "a third metal interconnect layer." "[A]n indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000). It is more than a presumption or a convention that "a" or "an" can mean "one or more;" it is best described as a rule. *Baldwin Graphics Sys., Inc. v. Seibert Inc.*, 512 F.3d 1338, 1343 (Fed. Cir. 2008). "An exception to the general rule . . . only arises where the language of the claims themselves, the specification, or the prosecution history necessitate a departure from the rule." *Id.* at 1343–1344. Although Patent Owner points to the '625 Patent Specification as disclosing only a structure that includes three metal interconnect layers (*see* PO Resp. 37–42), we do not agree because "particular embodiments appearing in the written description will not be used to limit claim language that has a broader effect." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004). "[E]ven where a patent describes only a single embodiment, claims will not be 'read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.'" *Id.* (quoting *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed.

Cir. 2004)). Accordingly, we find no reason to depart from the general rule that “a” or “an” can mean “one or more,” and therefore, that “a third metal interconnect layer” is not limited to “a single third metal interconnect layer.”

We also do not agree with Patent Owner that a single third metal interconnect layer must completely electrically interconnect sub-circuits (“i.e., a structure that can route an electrical signal between two points in an electrically interconnected circuit.”). We do not agree that any modifier such as “completely” should be added to “electrically interconnecting” or “electrically interconnect.” We look to the words of the claims themselves to define the scope of the patented invention. *See Phillips*, 415 F.3d at 1312. “[A]n analysis that adds words to the claim language without support in the intrinsic evidence does not follow standard canons of claim construction.” *Vagabond Sys. Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1299–1300 (Fed. Cir. 2014). “The context in which a term is used in the [] claim can be highly instructive.” *Phillips*, 415 F.3d at 1315 (claim term “steel baffles” strongly implies that the term “baffles” does not inherently mean objects made of steel). As pointed out by Petitioner, claim 1 recites “partially electrically interconnecting” and “completing the electrical interconnection” in the context of a first metal interconnect layer and a second metal interconnect layer but uses the term “electrically interconnecting” in the context of a third metal interconnect layer. We agree with Petitioner’s argument that “electrically interconnecting,” absent a modifier, means that “electrically interconnecting” is broader than, and may include within its scope, “partially interconnecting” and “completely interconnecting.” We do not agree with Patent Owner’s unsupported attorney argument that “if the inventors had intended that the third metal interconnect layer only partially

connect the sub-circuits, then they would have recited that the third metal interconnect layer ‘partially electrically interconnect’ those sub-circuits.”

PO Sur-reply 4. Argument of counsel cannot take the place of objective evidence. *See Gemtron Corp. v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009) (unsworn attorney argument is not evidence).

Based on the entire trial record, we find that How-767’s disclosures of each of metal layer M3 and metal layer M4 teaches the aforementioned limitations of claims 1 and 10.

f. 10[d2] wherein said third metal layer lines are fabricated to be oriented to extend substantially parallel to said first metal layer lines.

Petitioner contends that How-767 teaches “wherein said third metal layer lines are fabricated to be oriented to extend substantially parallel to said first metal layer lines,” as recited in claim 10, based on How-767’s disclosure of an embodiment where M1’s interconnect lines are parallel to M3’s interconnect lines, and an embodiment where M1’s interconnect lines are parallel to M4’s interconnect lines. *See* Pet. 59–60 (reproducing Ex. 1004, Fig. 6 (color added); citing Ex. 1003, 6:43–50; Ex. 1006 ¶¶ 139–140).

Patent Owner does not dispute Petitioner’s assertions addressing this limitation. *See generally* PO Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, we find that How-767 teaches “each sub-circuit includes at least one electrical circuit having a plurality of circuit components,” as recited in claim 10, for the reasons discussed in the Petition. *See* Pet. 59.

g. Conclusion Regarding the Analysis of Claims 1 and 10

For the foregoing reasons, and after having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine that Petitioner has established by a preponderance of the evidence that claims 1 and 10 are unpatentable under 35 U.S.C. § 103(a) over How-767, Baker, and Akaogi.

5. Dependent Claim 2

Claim 2 depends from claim 1 and recites “depositing a dielectric layer between said first, second and third metal interconnect layers.” Ex. 1001, 9:7–9. Petitioner contends that How-767’s disclosure of insulating layers 115, 125, 135, 145 in Figure 1 by a deposition process teaches the limitations of claim 2. *See* Pet. 49–50 (reproducing Ex. 1003, Fig. 1 (color added); quoting Ex. 1003, 1:28–36, 1:42–43; citing Ex. 1003, 1:40–43; Ex. 1006 ¶¶ 119–120), 77–104. In the Institution Decision, we stated that “Petitioner [] does not explain sufficiently why How-767’s disclosure of insulating layers teaches ‘a *dielectric* layer.’” Dec. 23. Patent Owner does not address claim 2 in its Response. *See generally* PO Resp.

In the Reply, Petitioner asserts that the “identification of the ‘insulating layer’ language in How-767 was sufficient and no further explanation was needed because a [person of ordinary skill in the art] would know that How-767’s reference to ‘insulating layers’ conveys dielectric layers.” Pet. Reply 22. In support of its argument, Petitioner quotes disclosures from the ’625 Patent describing a dielectric layer as providing an insulating layer. *See id.* at 22–23 (quoting Ex. 1001, 5:32–41). Petitioner also supports its argument with quoted disclosures of additional patents using the terms interchangeably and describing a dielectric insulation layer

as including silicon dioxide. *See id.* at 23 (quoting Ex. 1020, 4:1–13; Ex. 1021, 1:26–35; Ex. 1022, 1:26–33; citing Ex. 1020, 1:38–47). Petitioner notes that Patent Owner’s Response does not raise any issues with Petitioner’s mapping of How-767’s insulating layer to the claimed “dielectric layer.” *See id.* According to Petitioner,

Dr. Bagherzadeh acknowledged with reference to How-767’s disclosure that (1) the purpose of placing insulating layers between the metal layers in an integrated circuit is to prevent the metal layers from undesirably contacting each other and causing a short, (2) a [person of ordinary skill in the art] would understand silicon dioxide is a material that would be used to implement such insulating layers, and (3) silicon dioxide is a known dielectric material.

Pet. Reply 23 (citing Ex. 1019, 33:14–34:1, 34:24–25, 35:4–6¹⁵; Ex. 1003, 1:34–38; Ex. 2003 ¶ 65).

In the Sur-reply, Patent Owner points out that it objected to Petitioner’s new theories of unpatentability and new evidence. *See* PO Sur-reply 25 (citing Paper 20). Patent Owner contends that Petitioner introduces three new exhibits as evidence of its new arguments. *See id.* at 26 (citing Paper 20). Patent Owner contends that the Board should not consider any new issues raised for the first time in the Reply. *See id.* (quoting CTPG 73).

We are not persuaded that Petitioner presents a new theory of unpatentability. Petitioner’s theory remains the same—that How-767’s disclosure of insulating layers by a deposition process teaches depositing a dielectric layer between the first, second and third metal interconnect layers. A petitioner is permitted to address issues discussed in the institution decision in its reply brief. *See* CTPG 73; *see also* *Chamberlain Grp., Inc. v.*

¹⁵ Petitioner incorrectly cited Ex. 1019, 33:4–6.

One World Techs., Inc., 944 F.3d 919, 925 (Fed. Cir. 2019) (“Parties are not barred from elaborating on their arguments on issues previously raised”).

The issue of whether an insulating layer teaches a dielectric layer was raised in the Institution Decision, and Petitioner’s Reply addresses this issue. *See* Dec. 23; Pet. Reply 22–23. In addition, a petitioner may submit rebuttal evidence in support of its reply (*see* CTPG 73), and may introduce evidence to document the knowledge of a person of ordinary skill in the art (*see Anacor Pharms., Inc. v. Iancu*, 889 F.3d 1372, 1380–81 (Fed. Cir. 2018)).

Based on the entire trial record, we find that How-767’s disclosure of insulating layers 115, 125, 135, 145 in Figure 1 by a deposition process, in view of the knowledge of a person of ordinary skill in the art, teaches “depositing a dielectric layer between said first, second and third metal interconnect layers.”

Accordingly, in addition to the reasons explained above addressing claim 1, based on the entire trial record, we determine Petitioner has established by a preponderance of the evidence that claim 2 is unpatentable under 35 U.S.C. § 103(a) over How-767, Baker, and Akaogi.

6. Dependent Claims 3–5, 11, 12, and 14

Claims 3–5 depend ultimately from claim 1, and claims 11, 12, and 14 depend ultimately from independent claim 10. *See* Ex. 1001, 9:10–20, 10:31–39, 10:46–48. We have reviewed Petitioner’s contentions and supporting evidence addressing how the combination of How-767, Baker, and Akaogi teaches or suggests the additional limitations recited in dependent claims 3–5, 11, 12, and 14. *See* Pet. 50–57, 60–61, 77–104. Based on the record before us, Petitioner establishes sufficiently that the combination of How-767, Baker, and Akaogi teaches or suggests each of the

additional limitations recited in dependent claims 3–5, 11, 12, and 14 for the reasons stated in the Petition.

Patent Owner does not address Petitioner’s patentability challenges to dependent claims 3–5, 11, 12, and 14. *See generally* PO Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

For these reasons, in addition to those explained above addressing independent claims 1 and 10, based on the entire trial record, we determine that Petitioner has established by a preponderance of the evidence that claims 3–5, 11, 12, and 14 are unpatentable under 35 U.S.C. § 103(a) over How-767, Baker, and Akaogi.

F. Challenge to Claims 6–9 based on How-767, Baker, Akaogi, and Feild

1. Overview of Feild (Ex. 1011)

Feild is directed to an on-chip interconnect structure and methods for fabricating the same. *See* Ex. 1011, 1:6–9. For example, Feild describes a method including a combined one step etch process for fabricating a multilevel via/interconnect structure. *See id.* at 4:27–5:63, Figs. 4a–g. According to the method, “a first metal layer 204 is deposited on the surface of substrate 200,” and a second metal layer 202 may be deposited on the surface of first metal layer 204. *See id.* at 4:41–43, 5:5–8, Fig. 4a. Subsequently, a layer of masking material 206 with a low dielectric constant (such as oxide or nitride) may be deposited on second metal layer 202; a resist 205 may be deposited on masking layer 206, exposed for vias, and then patterned; and masking layer 206 may be etched partially to delineate vias in the structure. *See id.* at 5:12–24, Fig. 4b. Next, resist 207 may be formed on the structure, and the resist and pattern mask may be employed in

defining the vias and metal lines in the structure. *See id.* at 5:25–27, Fig. 4c. Thereafter, metal layers 202 and 204 may be etched to form via region 202' and metal line region 204'. *See id.* at 5:27–31, Fig. 4d. Then, a high density plasma oxide or other low dielectric constant material 208 may be deposited between via pillars and lines, and region 208 may be polished off up to via 202'. *See id.* at 5:43–48, Fig. 4e. According to Feild, “[t]he various processing steps described above may be repeated any number of times to provide multiple interconnect levels on the structure.” *See id.* at 5:54–56.

Figure 4g of Feild is illustrative and reproduced below.

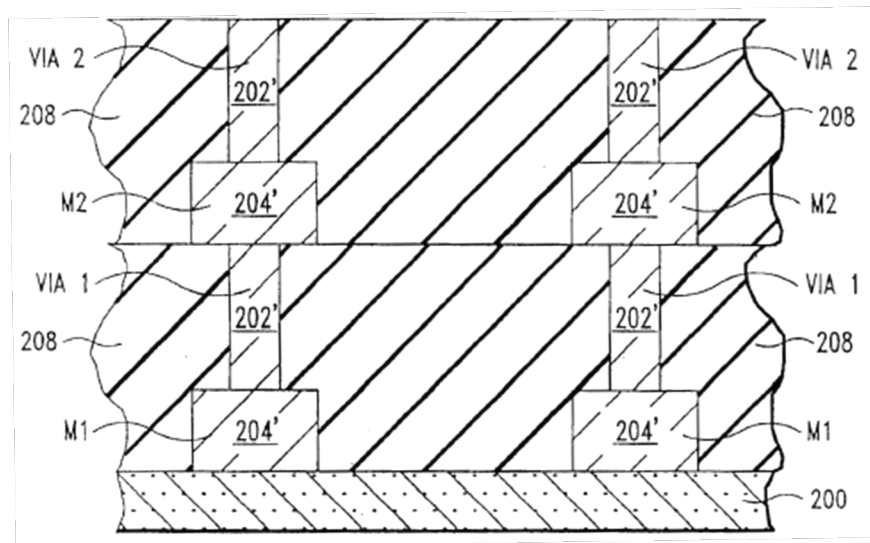


Figure 4g is a cross-sectional view depicting a fabricated multilevel via/interconnect structure. *See Ex. 1011, 4:7–11.* As shown in Figure 4g, first metal layer M1 204' is in contact with the top surface of substrate 200. *See id.* at 4:41–43. VIA1 202' connects first metal layer M1 204' to second metal layer M2 204', and VIA2 202' connects second metal layer M2 204' to another metal level or to an external device. *See id.* at 5:57–60. Figure 4g also shows multiple metal lines 204' and vias 202' spaced apart by region 208. *See id.* at 5:51–53.

2. *Claim 6*

a. *6[p] A method of optimizing circuit layout in a flash memory, comprising:*

Petitioner asserts that How-767, Baker, and Akaogi teach, suggest, and render obvious the preamble recitation of claim 6. *See* Pet. 24, 35–41 (citing Pet. 24, 35–39), 67 (citing Ex. 1003, Fig. 4; Ex. 1006 ¶ 156; Pet. 24, 35–39), 77–104. Patent Owner does not dispute Petitioner’s assertions addressing this limitation, apart from its arguments addressing claim 1. *See generally* PO Resp. 31–32, 67–72. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

For the same reasons as those explained above in Section II.E.4.a. addressing claims 1 and 10, based on the entire trial record, we find that the combination of How-767, Baker, and Akaogi teaches, suggests, and renders obvious “[a] method of optimizing circuit layout in a periphery area in a flash memory,” as recited in claim 6.

b. *6[a1] forming a plurality of sub-circuits in a periphery area of a silicon substrate,*

6[a2] wherein each sub-circuit includes at least one electric circuit having a row of transistors,

Petitioner contends that the combination of How-767, Baker, and Akaogi teach, suggest, and renders obvious “forming a plurality of sub-circuits in a periphery area of a silicon substrate,” as recited in claim 6. *See* Pet. 25–35, 42–44, 67, 77–104. Petitioner also contends that How-767 teaches, suggests, or renders obvious “wherein each sub-circuit includes at least one electric circuit having a row of transistors,” as recited in claim 6, based on How-767’s disclosure of active layer devices formed independently of one another and requiring interconnects to form a circuit. *See id.* at 67

(citing Ex. 1003, 1:24–28). According to Petitioner, a person of ordinary skill in the art “would have further understood that each function block includes at least one electrical circuit having a plurality of transistors because absent such components, there would be no ‘internal’ routing.” *Id.* (citing Ex. 1006 ¶ 158). Petitioner further relies on its analysis addressing dependent claim 4, and asserts “it would have been, at a minimum, obvious, to arrange transistors in rows substantially parallel with the M1 ‘metal lines’ ‘running in a first direction . . . substantially parallel to one another’ in order to align the two from a plan view and in order to connect the components.” *Id.* at 68 (citing Ex. 1003, 2:6–11, 6:14–19; Ex. 1006 ¶ 160; Pet. 52–56).

Patent Owner does not dispute Petitioner’s assertions addressing these limitations, apart from its arguments addressing claim 1. *See generally* PO Resp. 31–32, 67–72. In any event, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

Based on the entire trial record, including the reasons explained above in Section II.E.4.b. addressing claims 1 and 10, we find that How-767 teaches, suggests, and renders obvious the aforementioned limitations of claim 6 for the reasons discussed in the Petition. *See* Pet. 42–44, 52–56, 67–68.

- c. 6[b] depositing a first metal interconnect layer on said substrate to partially electrically interconnect the transistors of the sub-circuits, wherein said first metal interconnect layer forms a plurality of first metal layer lines that are oriented to extend substantially in the same direction as said row of transistors,*
- 6[c] depositing a second metal interconnect layer above said first metal interconnect layer to complete the electrical interconnection of said respective transistors within said sub-circuits, wherein said second metal interconnect layer forms a plurality of second metal lines*

oriented to extend substantially perpendicular to said first metal layer lines, and

Petitioner contends the combination of How-767 and Feild, teaches, suggests, and renders obvious these limitations of claim 6. Petitioner asserts that How-767 teaches, suggests, or renders obvious a first metal interconnect layer to partially electrically interconnect the transistors of the sub circuits, wherein the first metal interconnect layer forms a plurality of first metal layer lines that are oriented to extend substantially in the same direction as the row of transistors. *See* Pet. 69–70 (quoting Ex. 1003, 6:14–19; citing Ex. 1003, 1:49–51, 5:41–56, 12:8–10, 12:49–64, 13:4–10, Fig. 4; Ex. 1006 ¶¶ 162, 164; Pet. 27–31, 44–45). Petitioner asserts “it was, at a minimum, obvious to orient the row of transistors to [extend] substantially in the same direction as the M1 ‘metal lines’ in order to enable interconnections.” *Id.* at 70 (citing Ex. 1006 ¶ 163; Pet. 67–68). Petitioner asserts that How-767 teaches, suggests, or renders obvious a second metal interconnect layer above the first metal interconnect layer to complete the electrical interconnection of the respective transistors with the sub-circuits, wherein the second metal interconnect layer forms a plurality of second metal lines oriented to extend substantially perpendicular to the first metal layer lines. *Id.* at 71–72 (citing Ex. 1003, 1:62–2:5, 5:41–56, 6:8–21, 12:8–10, 12:49–64, 13:4–10, Fig. 4; Ex. 1006 ¶¶ 165, 167; Pet. 27–31, 45–46).

Petitioner asserts that Feild teaches depositing a first metal interconnect layer on the substrate, and depositing a second metal interconnect layer above the first metal interconnect layer, based on Feild’s teachings of first metal layer 204 corresponding to M1 deposited on the surface of substrate 200, and disclosure that its steps for forming metal

interconnect layers may be repeated any number of times, and depiction in Figure 4g of second metal layer M2 above first metal layer M1. *See* Pet. 69 (reproducing Ex. 1011, Fig. 4g (color added); citing Ex. 1006 ¶ 161; Ex. 1011, 4:40–43), 71–72 (reproducing Ex. 1011, Fig. 4g (color added); citing Ex. 1006 ¶ 166; Ex. 1011, 5:5–9, 5:54–60). Petitioner contends that it would have been obvious to one of ordinary skill in the art to use Feild’s cross-sectional layer arrangement (i.e., with M1 deposited on the substrate and M2 deposited above M1) to fabricate a device using How-767’s plan-view interconnect architecture in order to obtain Feild’s identified benefits of reducing fabrication steps, eliminating polishing steps, and obtaining high electromigration performance, while leaving How-767s plan-view interconnect architecture unchanged. *See* Pet. 63 (citing Ex. 1003, Figs. 6, 12a-c; Ex. 1006 ¶¶ 148–149; Ex. 1011, 2:48–3:10), 65–66 (reproducing Ex. 1011, Fig. 4g (color added); citing Ex. 1006 ¶ 154; Ex. 1011, 4:40–43, 5:54–56). According to Petitioner, a person of ordinary skill in the art “would have understood that other cross-sectional interconnect arrangements could also be used” because “How-767 presents FIG. 1 as an exemplary ‘cross-sectional view of an integrated circuit’” and “never suggests that the precise structure of FIG. 1 is required.” *Id.* at 65 (quoting Ex. 1003, 1:21–22; citing Ex. 1006 ¶ 152). Petitioner further contends that a person of ordinary skill in the art “would have understood that forming How-767’s routing structure according to the interconnect structure taught by Feild would involve a simple substitution of one known element (e.g., Feild’s cross-sectional interconnect structure) for another (e.g., How-767’s exemplary cross-sectional interconnect structure) to obtain predictable results.” *Id.* (citing Ex. 1006 ¶ 153).

Patent Owner contends that “no [person of ordinary skill in the art] would have been motivated to utilize Feild’s teachings to fabricate How-767 because How-767 and Feild disclose different layout arrangements. *See* PO Resp. 69; PO Sur-reply 23. Patent Owner asserts that Feild’s second metal layer M2 is parallel to first metal layer M1. *See* PO Resp. 69 (reproducing Ex. 1011, Fig. 4g (color added); citing Ex. 1011 4:41–43, 5:5–9, 5:27–31, 5:56–60, Figs 4a–4g; Ex. 2003 ¶ 177). Patent Owner contends that Feild does not disclose metal layer M2 is perpendicular to M1 as in the embodiment of How-767 relied upon by Petitioner. *See id.* According to Patent Owner, “a [person of ordinary skill in the art] would not have looked to Feild to fabricate How-767’s different architecture.” *Id.* (citing Ex. 2003 ¶ 178); *see* PO Sur-reply 23. Patent Owner contends that Petitioner “fails to explain how Feild’s processing steps, directed to forming parallel metal lines, could be used to form How-767’s M1 and M2 metal lines.” PO Resp. 70 (quoting Pet. 71; *Trivascular Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016); *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011); citing Ex. 2003 ¶ 179).

Patent Owner asserts that Petitioner does not “explain how any of the supposed advantages of Feild are relevant to How-767 or how the combination would achieve these supposed advantages” and “relies solely on conclusory expert testimony.” PO Resp. 70–71 (quoting *TQ Delta*, 942 F.3d at 1359; *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1074 (Fed. Cir. 2018); citing Pet. 62–77; Ex. 2003 ¶¶ 180–181; *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015)); PO Sur-reply 23. According to Patent Owner, “no [person of ordinary skill in the art] would have been motivated to modify How-767 to allegedly ‘obtain the multiple

benefits Feild identifies’—‘reducing fabrication steps, eliminating polishing steps, and high electromigration performance,’ as [Petitioner] contends.” *Id.* at 70 (quoting Pet. 63).

In the Reply, Petitioner asserts that Patent Owner’s “parallel versus perpendicular distinction fails because the Petition relies upon Feild for its disclosure of vertically stacking of layers, not the orientation of lines in those layers.” *See* Pet. Reply 24–25 (quoting *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973)). Petitioner also contends that the Petition explains how Feild’s layer arrangement is fully compatible with How-767 and how the benefits Feild identifies would be obtained by applying those teachings to How-767. *See id.* at 25 (citing Pet. 63–64).

In the Sur-Reply, Patent Owner contends that Petitioner does not refute Patent Owner’s substantive arguments, but attempts to minimize its reliance on Feild while reiterating conclusory statements regarding compatibility of How-767 and Feild. *See* PO Sur-reply 23 (citing Pet. Reply 24–25).

We do not agree with Patent Owner’s arguments that a person of ordinary skill in the art would not have looked to or been motivated to use Feild’s teachings to fabricate the structure of How-767 on the basis that Feild teaches a different layout arrangement or architecture from How-767. To the extent that Patent Owner contends that Feild’s methods of fabrication are limited only to stacked metal layers oriented in parallel, and, therefore, are inapplicable to How-767’s stacked metal layers, we do not agree because a prior art “reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect.” *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898,

907 (Fed. Cir. 1985) (emphasis omitted). Thus, we do not agree that the teachings of Feild are limited to stacked metal layers oriented in parallel, as suggested by Patent Owner.

We also do not agree with Patent Owner's assertion that the Petition does not explain how any of the supposed advantages of Feild are relevant to How-767 or how the combination would achieve these supposed advantages. Petitioner identifies reducing fabrication steps, eliminating polishing steps, and high electromigration performance as benefits of Feild's fabrication method. *See* Pet. 63 (citing Ex. 1011, 2:48–3:10; Ex. 1006 ¶ 149).

Dr. Lall's cited testimony identifies these advantages compared to the prior art techniques discussed in Feild that use additional polishing steps, multiple-step processing, and the use of chemical mechanical polishing. *See* Ex. 1006 ¶ 149 (citing Ex. 1011, 2:16–32, 2:20–30, 2:48–3:10). Petitioner also asserts that How-767 presents Figure 1 as an exemplary cross-sectional view of a generic integrated circuit and never suggests that the precise structure of Figure 1 is required. *See* Pet. 65 (citing Ex. 1003, 1:21–22). On this basis Petitioner contends that a person of ordinary skill in the art would have understood that other cross-sectional interconnection arrangements could be used. *See id.* (citing Ex. 1006 ¶ 152). Petitioner asserts that a person of ordinary skill in the art would have understood that forming How-767's routing structure according to the interconnect structure taught by Feild would involve a simple substitution of Feild's cross-sectional interconnect structure for How-767's exemplary cross-sectional interconnect structure to obtain predictable results. *See id.* (citing Ex. 1006 ¶ 153).

Accordingly, we understand that Feild's advantages of reducing fabrication steps, eliminating polishing steps, and high electromigration performance

would be achieved by forming How-767's routing structure according to Feild's cross-sectional interconnect structure.

In sum, based on the entire trial record, we determine that Petitioner sets forth sufficient articulated reasoning with rational underpinning to support the conclusion that it would have been obvious to a person of ordinary skill in the art to modify How-767 by "forming How-767's routing structure according to the interconnect structure taught by Feild" in order to obtain the advantages of reducing fabrication steps, eliminating polishing steps, and high electromigration performance. *See* Pet. 62–65 (citations omitted); *KSR*, 550 U.S. at 418.

Based on the entire trial record, including the reasons explained above in Section II.E.4.d. addressing claims 1 and 10, we find that the combination of How-767 and Feild, teaches, suggests, and renders obvious the aforementioned limitations of claim 6.

d. 6[d] depositing a third metal interconnect layer above said second metal interconnect layer to electrically interconnect the respective sub-circuits, wherein said third metal layer forms a plurality of metal layer lines oriented to extend substantially parallel to said first metal layer lines.

Petitioner contends that the combination of How-767 and Feild teaches, suggests, and renders obvious "depositing a third metal interconnect layer above said second metal interconnect layer to electrically interconnect the respective sub-circuits, wherein said third metal layer forms a plurality of metal layer lines oriented to extend substantially parallel to said first metal layer lines," as recited in claim 6, relying primarily on its arguments addressing limitation 1[d] of claim 1. *See* Pet. 72–74 (reproducing Ex. 1003, Fig. 6 (color added); citing Ex. 1003, 6:16–17, 6:27–37, 6:43–50; Ex. 1006 ¶¶ 168–171; Pet. 46–48). Petitioner contends that "[i]n an embodiment in

which M1's interconnect lines are parallel to M3, M3 is the claimed third metal layer.” *Id.* at 73–74 (citing Ex. 1006 ¶ 170). Petitioner also asserts that “[i]n an embodiment in which M1's interconnect lines are parallel to M4, M4 is the claimed third metal layer.” *Id.* at 74 (citing Ex. 1006 ¶ 170). Petitioner further contends that Feild discloses its processing steps may be repeated any number of times to provide multiple interconnect levels on the structure. *See id.* (quoting Ex. 1011, 5:5–9, 5:54–56). According to Petitioner, a person of ordinary skill in the art “would have understood M3 and M4 are similarly deposited.” *Id.* (citing Ex. 1006 ¶ 171).

Patent Owner argues that Petitioner “does not explain how to utilize Feild's ‘processing steps’ to form How-767's M3 and M4 metal layers.” *See* PO Resp. 71 (citing Ex. 2003 ¶ 182; *Trivascular*, 812 F.3d at 1066; *Unigene Labs.*, 655 F.3d at 1360). Patent Owner notes that How-767 discloses its third metal layer is composed of a plurality of parallel segmented conducting lines and contends that Petitioner does not explain how Feild's processing steps would have been utilized to form these segments in M3 when Feild does not actually disclose a third metal layer or forming segments in a metal layer. *See id.* at 72 (quoting Ex. 1003, 6:43–48; citing Ex. 2003 ¶ 184).

We do not agree with Patent Owner's arguments because, as Petitioner points out, Feild expressly discloses that its processing steps may be repeated any number of times to provide multiple interconnect levels on the structure. *See* Pet. 74 (quoting Ex. 1011, 5:54–56; citing Ex. 1011, 5:5–9). Although Feild explicitly discloses first and second metal layers or interconnect levels in Figure 4g, consistent with Feild's suggestion that the processing steps can be repeated any number of times, Feild further discloses “M1 denotes the first metal or wiring level, VIA1 is the first via

which connects M1 to M2; M2 is the second metal or wiring level; and VIA2 is the second via connecting M2 to either *another metal level* or an external device.” Ex. 1011, 5:56–60; *see* Pet. 76 (quoting Ex. 1011, 5:57–60). We need not address Patent Owner’s arguments addressing How-767’s M4 layer, because as explained above in Section II.E.4.e. addressing claims 1 and 10, we find that How-767’s disclosures of metal layer M3 teaches a third metal interconnect layer electrically interconnecting the sub-circuits.

Based on the entire trial record, including the reasons explained above in Sections II.E.4.e. and II.E.4.f. addressing claims 1 and 10, we find that the combination of How-767 and Feild teaches, suggests, and renders obvious the aforementioned limitations of claim 6.

e. Conclusion

For the foregoing reasons, in addition to the reasons explained above addressing claims 1 and 10, and after having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine that Petitioner has established by a preponderance of the evidence that claim 6 is unpatentable under 35 U.S.C. § 103(a) over How-767, Feild, Baker, and Akaogi.

3. Dependent Claims 7–9

Claims 7–9 depend ultimately from independent claim 6. *See* Ex. 1001, 9:46–10:3. We have reviewed Petitioner’s contentions and supporting evidence addressing how the combination of How-767, Feild Baker, and Akaogi teaches or suggests the additional limitations recited in dependent claims 7–9. *See* Pet. 75–104. Based on the record before us, Petitioner establishes sufficiently that the combination of How-767, Feild

Baker, and Akaogi teaches or suggests each of the additional limitations recited in dependent claims 7–9 for the reasons stated in the Petition.

Patent Owner does not address substantively Petitioner’s patentability challenges to dependent claims 7–9. *See generally* PO Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

For these reasons, in addition to those explained above addressing independent claim 6, based on the entire trial record, we determine that Petitioner has established by a preponderance of the evidence that claims 7–9 are unpatentable under 35 U.S.C. § 103(a) over How-767, Feild, Baker, and Akaogi.

G. Challenges to Claims 1–5, 10–12 and 14 based on How-767 alone, and How-767 and Baker, and Challenges to Claims 6–9 based on How-767 and Feild, and How-767, Feild, and Baker

Petitioner also challenges claims 1–5, 10–12, and 14 under 35 U.S.C. § 103(b) as unpatentable over How-767 alone and over How-767 and Baker, and claims 6–9 under 35 U.S.C. § 103(b) as unpatentable over How-767 and Feild, and over How-767, Feild, and Baker. *See* Pet. 25–96. We need not determine the merits of those challenges because, as explained above, Petitioner has demonstrated the unpatentability of claims 1–5, 10–12, and 14 as unpatentable over How-767, Baker, and Akaogi, and claims 6–9 over How-767, Feild, Baker, and Akaogi. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but can “greatly ease the burden on [an

agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

H. New and Nonresponsive Arguments

In the Sur-reply, Patent Owner contends that Petitioner admittedly maps different portions of How-767 not designated by How-767 to be periphery areas to the claimed periphery area. *See* PO Sur-reply 21 (quoting Pet. 42; citing Pet. Reply 16). Patent Owner asserts that Petitioner concedes that its unpatentability theory requires a conceptual subdividing of non-periphery areas with periphery area 430. *See id.* at 22 (citing Pet. Reply 19). Patent Owner argues for the first time in the Sur-reply that Petitioner’s position “requires an unnatural reading of How-767 Figure 4, and it requires a [person of ordinary skill in the art] to reallocate existing connections that are not in area 430 to the periphery. A [person of ordinary skill in the art] would not have made that choice.” *Id.* at 21 (citing Ex. 2003 ¶¶ 147–155). Patent Owner also argues for the first time that the statements in How-767 cited by Petitioner do not support ignoring How-767’s express designation of periphery and non-periphery areas. *See id.* at 22 (citing Ex. 1003, 5:49–52, Fig. 4:430). According to Patent Owner, “[b]y mapping **additional** functional blocks 420 and regions 421 as ‘periphery area’ in addition to the **actual** periphery area 430 of How-767, [Petitioner’s] re-interpretation of How-767 **increases** the number of necessary metal layers in the periphery area.” *Id.* Patent Owner asserts that the point of the ’625 Patent is to reduce the amount of the metal layers, and therefore a person of ordinary skill in the art would not have made the proposed modification of How-767. *See id.* at 22–23 (quoting Ex. 1001, 2:36–38, 2:58–60; citing Ex. 1006 ¶ 49; Ex. 2003 ¶ 52).

Patent Owner's Sur-reply does not identify arguments in Petitioner's Reply or issues raised in the Institution Decision to which these arguments respond. *See id.* Instead, Patent Owner's arguments address Petitioner's position originally advanced in the Petition. *See* Pet. 29 (conceptual function block demarcation, subdividing specialized regions 421 and periphery circuitry 430), 42 (function blocks 420 outside core area, specialized regions 421 and periphery area 430 constituting periphery areas). Patent Owner does not raise these same arguments in its Response. *Compare* PO Sur-reply 21 *with*, PO Resp. 55–58. Patent Owner's new Sur-reply arguments exceed the proper scope of a sur-reply and have not been considered in rendering this Final Written Decision. *See* CTPG 73–74.

In the Reply, Petitioner asserts that How-767 renders obvious a “standalone chip” performing memory or flash memory functions. *See* Pet. Reply 14–15. On its face, Petitioner's argument appears to be responsive to Petitioner's characterization that Patent Owner “asserts that a ‘memory device’ and a flash memory device must be ‘standalone chips.’” *Id.* at 14 (quoting PO Resp. 75). However, more accurately, Patent Owner contends that “Dr. Lall admitted, as of February 2000, flash memories were standalone chips, and therefore a [person of ordinary skill in the art] would not have been motivated to integrate them within an ASIC.” PO Resp. 75 (citing Ex. 2002, 53:25–54:3). Petitioner's Reply argument also quotes Dr. Bagherzadeh's testimony that “[w]hen you buy a memory device, you get a memory device. That's a standalone.” Pet. Reply 14 (quoting Ex. 1019, 21:1–16). Petitioner uses Patent Owner's argument and Dr. Bagherzadeh's testimony regarding standalone chips as a springboard to define a memory device that is a standalone, and assert that the Petition

discloses and maps multiple configurations that are standalone chips. *See id.* at 14–15 (citing Pet. 37–38).

Petitioner’s Reply argument is not responsive to Patent Owner’s argument that a person of ordinary skill in the art would not have been motivated to integrate a standalone flash memory within an ASIC. *See* PO Resp. 75 (citing Ex. 2002, 53:25–54:3). Instead, Petitioner’s Reply arguments appear to proceed in a new direction with a new approach as compared to the positions advanced in the Petition. Accordingly, Petitioner’s new and non-responsive Reply arguments exceed the proper scope of a reply and have not been considered in rendering this Final Written Decision. *See* CTPG 73–74.

III. CONCLUSION¹⁶

For the reasons explained above, we conclude:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–5, 10– 12, 14	103(a)	How-767 ¹⁷		

¹⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

¹⁷ As explained above in Section II.G., we do not reach this rejection.

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
6–9	103(a)	How-767, Feild ¹⁸		
1–5, 10– 12, 14	103(a)	How-767, Baker ¹⁹		
6–9	103(a)	How-767, Feild, Baker ²⁰		
1–5, 10– 12, 14	103(a)	How-767, Baker, Akaogi	1–5, 10–12, 14	
6–9	103(a)	How-767, Feild, Baker, Akaogi	6–9	
Overall Outcome			1–12, 14	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–12, and 14 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

¹⁸ As explained above in Section II.G., we do not reach this rejection.

¹⁹ As explained above in Section II.G., we do not reach this rejection.

²⁰ As explained above in Section II.G., we do not reach this rejection.

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