

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY
CORPORATION, U.S.A., and NANYA TECHNOLOGY CORPORATION
DELAWARE,
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2021-00170
Patent 7,158,429 B1

Before JOHN F. HORVATH, JASON W. MELVIN, and
BRIAN D. RANGE, *Administrative Patent Judges*.

RANGE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Nanya Technology Corporation, Nanya Technology Corporation U.S.A., and Nanya Technology Corporation Delaware (the three entities, collectively referred to as “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–3 of U.S. Patent No. 7,158,429 B1 (Ex. 1001, “the ’429 patent”). Monterey Research, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). We instituted this *inter partes* review of all challenged claims based on all grounds asserted in the Petition. Paper 8 (“Dec.”). Thereafter, in a timely sequence, Patent Owner filed a Response (Paper 16, “Resp.”), Petitioner filed a Reply (Paper 19, “Reply”), and Patent Owner filed a Sur-reply (Paper 27, “Sur-Reply”). The parties presented final arguments in a hearing held by video on March 22, 2022. *See* Paper 31 (“Tr.”) (hearing transcript).

We have jurisdiction under 35 U.S.C. § 6. The evidentiary standard is a preponderance of the evidence. *See* 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019). We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

In this decision, we determine that Petitioner has demonstrated the unpatentability of claim 1 but has not met its burden of demonstrating that claims 2 and 3 of the ’429 patent are unpatentable.

II. BACKGROUND

A. Related Matters

The parties identify the following as related matters: *Cypress Semiconductor Corporation v. GSI Technology, Inc.*, 0-11-cv-00789 (D. Min. 2011), *Cypress Semiconductor Corporation v. GSI Technology, Inc.*,

3-13-cv-03757 (N.D. Cal. 2013), *Monterey Research, LLC v. Nanya Technology Corp. et al.*, 1:19-cv-02090 (D. Del. 2019). Pet. 2; Paper 4, 1.

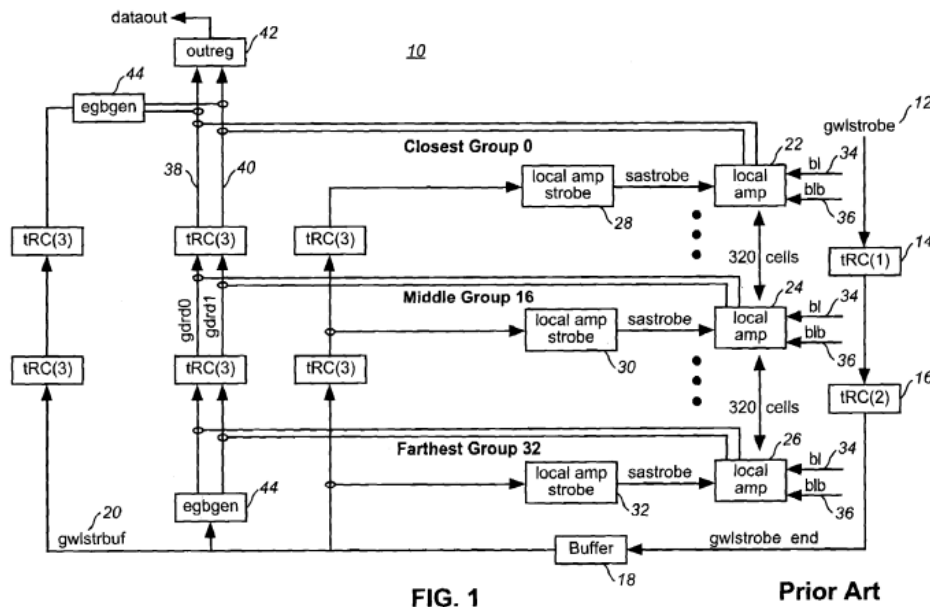
B. Real Parties in Interest

Petitioner identifies Nanya Technology Corporation, Nanya Technology Corporation U.S.A., and Nanya Technology Corporation Delaware as real parties in interest. Pet. 1–2. Patent Owner identifies Monterey Research, LLC, and IPValue Management as the real parties in interest. Paper 4, 1. For purposes of this Decision, we accept the parties’ contentions regarding real parties in interest.

C. The ’429 Patent (Ex. 1001)

The ’429 patent is titled “System for Read Path Acceleration.” Ex. 1001, code (54). The challenged claims relate to a system for read path acceleration for a memory core integrated circuit. *Id.* at 1:19–25.

Below, we reproduce Figure 1 of the ’429 patent.



The '429 patent describes Figure 1 as “an exemplary embodiment of conventional solution 10 to the read path problem in a memory core.”

Ex. 1001, 1:26–27. Figure 1 depicts some, but not all, of the '429 patent's claim elements. In particular, Figure 1 depicts a memory core having a memory array divided into a plurality of segments (groups 0, 16, 32) where each segment has a local amplifier (local amps 22, 24, 26). *Id.* at 1:30–33. Each local amplifier is coupled to global read data (gdrd) lines 38 and 40. *Id.* at 1:36–40. The global read data lines are coupled to output register 42. *Id.* at 40–46. The specification explains that conventional solution 10 can lead to certain timing and speed problems:

The output register 42 must latch before the equalization circuit 44 resets the values on the gdrd lines 38 & 40 and before the local amplifier[s] 22, 24, 26 are turned off by the falling edge of the global strobe buffer 20 signal. Failure of these timing requirements can cause virtual data or a crowbar situation for the local amplifiers 22, 24, 26. One solution is to increase the time the local amplifiers have to present the data to the gdrd lines, however this slows down the read access time.

Id. at 1:39–48.

After providing this background, the specification describes the invention as “[a] system for read path acceleration that overcomes these problems.” *Id.* at 1:55–57. We reproduce Figure 2 of the '429 patent below.

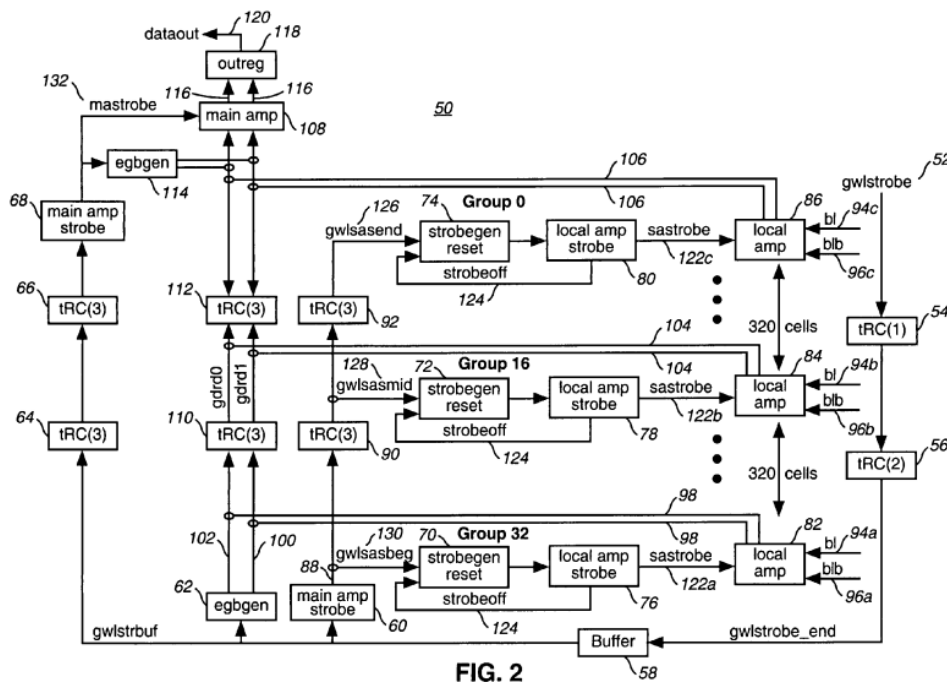


Figure 2 is a block diagram of a system for read path acceleration in accordance with an embodiment of the '429 patent. *Id.* at 2:40–42.

The system of Figure 2 is similar to the conventional system shown in Figure 1, but Figure 2 adds certain features recited by the challenged claims that are not present in Figure 1. In particular, Figure 2 adds main amplifier 108, which is coupled to global read data lines 100 and 102 and coupled to output register 118. *Id.* at 3:38–42. Figure 2 also adds first main amplifier strobe circuit 60, which is coupled to local amplifiers 82, 84, and 86, and adds a second main amplifier strobe 68, which is coupled to equalization circuit 114 and to main amplifier 108. *Id.* at 2:61–3:18.

The specification explains that main amplifier strobe 60 is used to ensure that local amplifiers 82, 84, 86 have sufficient time to transfer correct data to the global read data lines and latch the data in main amplifier 108. *Id.* at 4:9–13. This function is accomplished via strobe reset circuits 70, 72, and 74, which activate, for example, “based on both the strobe off signal

(strobeoff) 124 being high and the output 88 from the first main amplifier strobe circuit 60 being high.” *Id.* at 3:60–4:2.¹ The specification states that use of equalization circuits 62 and 114 “reduces the time to equalize the global data read lines,” and that the patent’s technique “reduces the allowed time for equalization approximately in half.” *Id.* at 4:20–24.

C. Challenged Claims

Petitioner challenges claims 1–3 of the ’429 patent. Pet. 4. Claim 1 is the only challenged independent claim. Claim 1 is illustrative of the claimed subject matter and is reproduced below with added bracketed identifiers to identify claim elements.

1. [Pre] A system for read path acceleration, comprising:
 - [1.A.] a memory core divided into a plurality of segments each segment having a plurality of local amplifiers each coupled to a pair of global read data lines;
 - [1.B.] a main amplifier having an input coupled to the pair of global read data lines and having an output coupled to an output register; and
 - [1.C.] a main amplifier strobe coupled to each of the plurality of local amplifiers.

Ex. 1001, 6:11–19; *see also* Pet. 8–9 (annotating claim 1 with the same identifiers).

¹ The specification mistakenly identifies the strobe reset circuits as circuits 76, 78, and 80. Elsewhere, the specification correctly identifies circuits 76, 78, and 80 as local amplifier strobe circuits. *See* Ex. 1001, 3:6–9, Fig. 2. The specification also identifies the strobe reset circuits, which receive strobe off signal 124 and main amplifier strobe 88, as circuits 70, 72, and 74. *See id.* at 2:65–6, Fig. 2. We correct that mistake here.

D. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1–3	103 ²	Winograd, ³ Issa, ⁴ Merritt ⁵
2	1–3	102	Merritt
3	1–3	103	Manning, ⁶ Merritt
4	1	102	Issa
5	2	103	Issa, Winograd, Merritt, Monzel ⁷
6	3	103	Issa, Winograd, Merritt
7	1	103	Winograd, Issa, Monzel
8	2	103	Winograd, Monzel
9	1	103	Merritt, Issa, Monzel
10	2	103	Merritt, Monzel
11	1	103	McClure, ⁸ Winograd, Merritt, Issa, Kawasumi ⁹
12	1–3	103	Merritt, Issa

Pet. 6–7. The Petition is supported by the Declaration of Dr. Erik Chmelar.

Ex. 1003; *see also* Ex. 1004 (curriculum vitae of Dr. Chmelar). The

Response is supported by the Declaration of Dr. Marwan Hassoun.

Ex. 2001; *see also* Ex. 2003 (curriculum vitae of Dr. Hassoun).

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application that resulted in the ’429 patent was filed before this date, the pre-AIA versions of §§ 102 and 103 apply.

³ US 6,646,954 B2, issued Nov. 11, 2003 (Ex. 1005).

⁴ US 6,480,424 B1, issued Nov. 12, 2002 (Ex. 1011).

⁵ US 5,598,376, issued Jan. 28, 1997 (Ex. 1006).

⁶ US 5,729,503, issued Mar. 17, 1998 (Ex. 1007).

⁷ US 6,667,912 B1, issued Dec. 23, 2003 (Ex. 1009).

⁸ US 5,802,004, issued Sept. 1, 1998 (Ex. 1008).

⁹ US 6,424,554 B1, issued July 23, 2002 (Ex. 1010).

Based on their statements of qualifications and curricula vitae, we determine that Dr. Chmelar and Dr. Hassoun are qualified to provide testimony about the knowledge, understanding, and opinions of a person of ordinary skill in the art at the time of the invention. Ex. 1003 ¶¶ 1–16 (Dr. Chmelar explaining his background); Ex. 1004 (Dr. Chmelar’s curriculum vitae); Ex. 2001 ¶¶ 1–13 (Dr. Hassoun explaining his background); Ex. 2003 (Dr. Hassoun’s curriculum vitae).

III. ANALYSIS

We organize our analysis into four main sections: (A) the level of ordinary skill in the art at the relevant time; (B) claim construction; and (C) whether, for each ground, Petitioner establishes by a preponderance of the evidence that the challenged claims are unpatentable.

A. Person of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art would have been a technical person having “a Bachelor’s degree in electrical engineering, computer engineering, applied physics, or a related field, and approximately two years of experience working in the design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.” Pet.

11. For purposes of this *inter partes* review, Patent Owner adopts Petitioner’s definition. Resp. 13. Based on the totality of the record including the ’429 patent specification, cited references, and expert testimony, we find that Petitioner’s definition for a person of skill in the art is appropriate.

B. Claim Construction

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Under that standard, the “words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Ordinary and customary meaning applies “unless the patentee demonstrated an intent to deviate from [it] . . . by redefining the term or by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Teleflex, Inc. v. Ficosa N. America Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002); *see also Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). Only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner initially argued that all claim terms should be given their plain and ordinary meaning. Pet. 12. Similarly, referring back to the institution decision, Patent Owner states in the Response that it adopts “the Board’s application of the plain and ordinary meaning of the terms.” Resp. 13. But as we explain below, the parties’ superficial agreement belies the parties’ sincere dispute over the meaning of the term “main amplifier strobe” as it appears in claim 1 of the ’429 patent.

In particular, Patent Owner argues that the claimed strobe cannot encompass signals or a mere wire. *See, e.g.,* Resp. 21; Sur-Reply 3–9. Similarly, Patent Owner argues that the main amplifier strobe must be a

circuit. Resp. 8–12; Sur-Reply 2–3. Patent Owner further argues that the main amplifier strobe must relate to the main amplifier. Sur-Reply 9–11. Petitioner, in contrast, argues that a “strobe” may include strobe signals carried on a wire. Reply 1–5. Petitioner also argues that the “main amplifier strobe” may be “main” in the sense that it is primary as compared to local amplifier strobes. *Id.* at 5–6. Moreover, as our discussion of Petitioner’s grounds illustrates, construction of “main amplifier strobe” is important when comparing the prior art to claim 1. Because the parties’ dispute regarding the meaning of claim 1’s “main amplifier strobe” impacts our analysis of Petitioner’s asserted grounds of unpatentability, it is necessary to expressly construe that term.

We first address the parties’ dispute over what it means for claim 1’s “main amplifier strobe” to be “main.” We observe that claim 1 recites “a main amplifier strobe coupled to each of the plurality of local amplifiers.” Ex. 1001 6:18–19. Claim 2 recites “a second main amplifier strobe coupled to the main amplifier.” *Id.* at 6:20–21. The specification refers to two different main amplifier strobes that correspond to the main amplifier strobes of claims 1 and 2: a main amplifier strobe “coupled to each segment of a number of local strobe reset circuits” and “[a] second main amplifier strobe [] coupled to the main amplifier.” *Id.* at 1:60–64; *see also id.* at 4:6–9 (explaining relationship between the main amplifier strobe circuit 60 and local amplifiers 82, 84, 86), 4:15–18 (explaining relationship between second main amplifier strobe circuit 68 and main amplifier 108). Figure 2 depicts two different “main amp strobes.” *Id.* at Fig. 2.

In view of the claims and the specification, the “main amplifier strobe” of claim 1 corresponds to main amplifier strobe 60 (coupled to local

amplifiers) and the “second main amplifier strobe” of claim 2 corresponds to second main amplifier strobe 68 (directly coupled to main amp 108).

Because claim 1’s main amplifier strobe is closely associated with the local amplifiers, we agree with Petitioner that the “main amplifier strobe” is “main” in the sense that it has a hierarchical relationship with local amplifiers (as opposed to Patent Owner’s contention that some relationship with a main amplifier is necessary). Reply 5–6.

We next address the parties’ dispute over whether or not claim 1’s “main amplifier strobe” can be a mere signal or line carrying a signal. To address this dispute, we observe that the stated purpose of the ’429 patent is to avoid virtual data or crowbar situations present in the conventional circuit that Figure 1 illustrates. *Id.* at 1:27–52. A primary difference between conventional Figure 1 and allegedly inventive Figure 2 is the presence of main amplifier strobe 60 and second main amplifier strobe 64. The circuits depicted in Figure 1 and Figure 2 both provide a strobe global word line input (gwlstrobe 12 and gwlstrobe 52, respectively) to the system. *Id.* at 1:26–27; 2:59–61. In Figure 1, after gwlstrobe 12 signal passes through two resistance capacitance delays (14 and 16) and buffer 18, it is renamed global strobe buffer signal (gwlstrbuf 20). Gwlstrbuf signal 20 is then split into two branches. The right branch extends upward toward local amplifiers 22, 24, and 26, and passes through the area where, in Figure 2, main amplifier strobe 60 appears. Below, we annotate Figure 1 to illustrate this path:

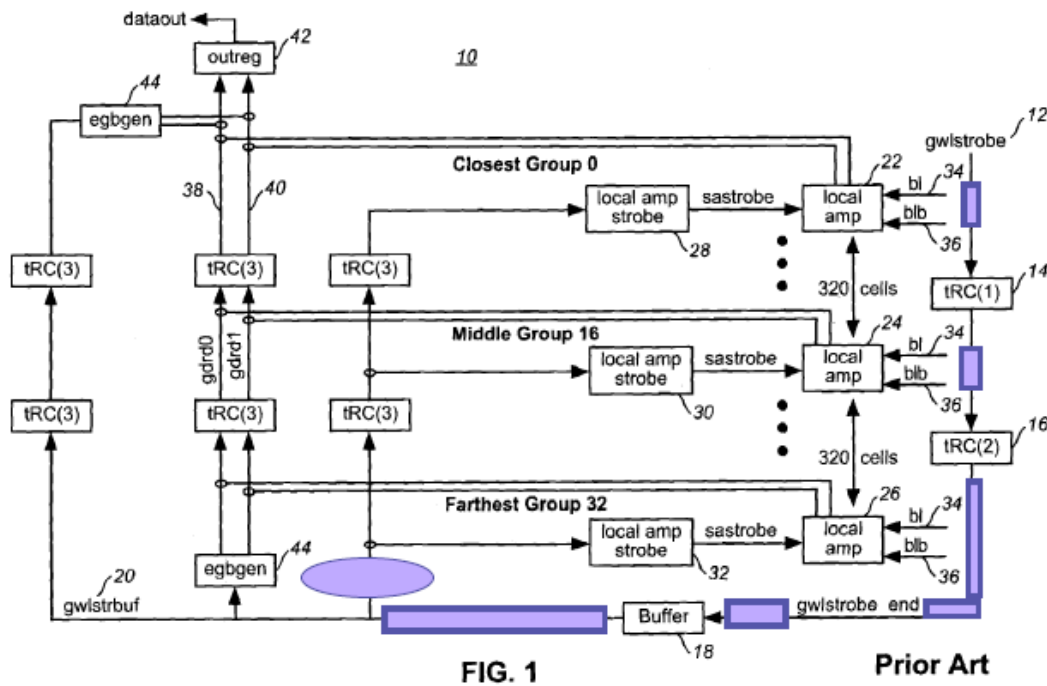


Figure 1 of the '429 patent depicts “conventional solution 10 to the read path problem in a memory core.” *Id.* at 2:38–39. We annotate Figure 1 above with purple boxes to indicate a portion of the path of the gwlstrobe 12 / gwlstrobe 20 signal. A purple oval marks the place where Figure 2 adds a main amplifier strobe.

In Figure 1, the portion of the line that we mark with a purple oval carries a strobe signal (gwlstrobe 20). If, as Petitioner contends, claim 1’s “main amplifier strobe” can be merely a strobe signal or a line carrying a strobe signal, then Figure 1 would have a “main amplifier strobe” at the location of the purple oval. Figure 1 does not, however, indicate a “main amplifier strobe” at this location the way Figure 2 does. Rather, the specification distinguishes Figure 1’s lack of this main amplifier strobe from Figure 2’s inclusion of this main amplifier strobe. *Id.* at Figs. 1, 2, 1:55–2:34 (identifying the main amplifier strobe in the summary of invention), 5:43–63 (explaining that the “present design” advantageously controls the local

amplifiers “by the strobe reset generator instead [of] by the strobe global word line (gwlstrobe) 52”). The Figure 1 apparatus, at the location of the purple oval, merely conveys a strobe signal (gwlstrbuf 20) on a line without substantially changing that signal. *Id.* Fig. 1. The Figure 2 apparatus, however, illustrates main amp strobe 60 generating output signal 88 by delaying the gwlstrbuf signal output by buffer 58. *Id.* at 4:6–9, Fig. 2. Given the context of the ’429 patent specification, we decline to construe “main amplifier strobe” in a manner that would fail to distinguish Figure 2’s main amplifier strobe from Figure 1’s unlabeled strobe-carrying line (identified with a purple oval above). *See id.* (identifying main amp strobe 60 as a “main amplifier strobe circuit 60”).

If Figure 2’s identification of a “main amplifier strobe 60” is to be distinguishable from Figure 1’s lack of any identified main amplifier strobe 60, the main amplifier strobe has to be more than just a mere strobe signal or line that carries a strobe signal. The ’429 patent specification explains that “first main amplifier strobe circuit 60 delays the rising edge of the output of the buffer 58” to “ensure[] that the local amplifiers 82, 84, 86 stay on until the main amplifier 108 is on.” *Id.* at 4:6–9. While we decline to import this exact functionality from the specification into claim 1’s “main amplifier strobe,” based on the discussion above, the main amplifier strobe must affect the transmitted signal and it must affect the signal consistent with the word “strobe.” *See Phillips*, 415 F.3d at 1323 (“[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.”).

Petitioner provides two definitions of “strobe” from technical dictionaries. Reply 4. *The Wiley Electrical and Electronics Engineering*

Dictionary (2004) defines strobe in the context of strobe lights, flashes, or display devices. Ex. 1013, 752. The *Wiley* definitions are not particularly relevant in the '429 patent's context. *The Microsoft Computer Dictionary Fifth Edition* (2002) defines strobe as "[a] timing signal that initiates and coordinates the passage of data, typically through an input/output (I/O) device interface, such as a keyboard or printer." Ex. 1014, 500. This definition is congruent with the '429 patent's usage of the word "strobe"; the strobe affects circuit timing. *See, e.g.*, Ex. 1001, 2:19–21, 3:43–4:24.

Given the language of claim 1, the context provided by the '429 patent, and the relevant dictionary definition consistent with the '429 patent's context, we construe claim 1's recited "main amplifier strobe" as *a circuit that generates a primary timing signal used to control a secondary device*. This construction reflects (1) the specification's identification of the main amplifier strobe as a circuit, (2) the main amplifier strobe's primary nature as compared to secondary devices such as local amplifier strobes and (3) the requirement that the main amplifier strobe affect a signal in a manner consistent with a strobe. *See* Sur-Reply 2–7 (providing citations to Specification and deposition testimony confirming that the main amplifier strobe is a circuit). When addressing Petitioner's grounds below, we address claim 1's "main amplifier strobe" based upon this construction.

Finally, we note that Petitioner and Patent Owner debate whether a line carrying a signal may be a circuit. Reply 4–5; Sur-reply 7–9. We need not resolve this debate. Whether or not a mere line that carries a signal without substantially modifying the signal might be a circuit in some contexts, claim 1's "main amplifier strobe" requires more than a line carrying a signal for the reasons explained above (in other words, if every

line carrying a strobe signal were a main amplifier strobe, the prior art circuit shown in Figure 1 would include main amp strobes 60 and 68, which are described as parts of the invention shown in Figure 2).

C. Analysis of the Asserted Grounds

1. *Ground One: Obviousness of Claims 1–3 Based on Winograd in view of Issa or Merritt*

Petitioner asserts that claims 1–3 would have been obvious over Winograd in view of Issa or Merritt. Pet. 6. For this ground, Petitioner asserts that Winograd discloses “a main amplifier strobe coupled to each of the plurality of local amplifiers.” *Id.* at 22. Petitioner identifies “genL 780” as being the main amplifier strobe. *Id.* at 23.

Winograd suggests that genL 780 is a line, a signal on a line, or both. Sometimes, Winograd refers to structure 780 as “genL *line* 780.” Ex. 1005, 17:54–57 (emphasis added); *see also* 18:24–27 (twice referring to the “genL line 780”); 18:49–52 (referring to “genL line 780”). Winograd also states that LSA 712 is controlled by various “lines, or signals on those lines” one of which is “genL 780.” *Id.* at 17:16–23¹⁰; *see also id.* at 18:14–22 (“the LxCTRL 714 coordinates such activities by exercising certain lines including . . . the genL 780.”).

Petitioner’s declarant, Dr. Chmelar, refers to genL as a “line.” Ex. 1003 ¶ 75 (“the genL line is coupled to a plurality of local sense amps”); *see also* Ex. 2002, 171:7–12 (stating that GenL “does not appear to be a circuit, it is a, a line or a signal”). Patent Owner’s declarant, Dr. Hassoun,

¹⁰ LSA stands for local sense amps. *Id.* at 12:50-56 (referencing “local sense amps 312 (alternatively referred to as ‘LSA 712’)”).

testified that genL 780 is a signal rather than a “main amplifier strobe.” Ex. 2001 ¶ 80; Ex. 1014, 34–35.

Whether genL is a signal, a line that carries a signal, or both, Petitioner has not established by a preponderance of the evidence that genL is equivalent to or suggests claim 1’s main amplifier strobe based on our claim construction above. Petitioner has not established that Winograd discloses or suggests that genL is a *circuit* that generates a primary timing signal used to control a secondary device. Rather, at best for Petitioner, genL is a line that carries a signal that may be used as a timing reference by local amplifiers (*see, e.g.*, Reply 8), but such a disclosure is akin to the admitted prior art of ’429 patent Figure 1, which illustrates a signal line carrying timing signal gwlsrbuf 20 to local amplifiers 22–26 as explained above.

Thus, for the reasons above, Petitioner has not met its burden of demonstrating that claims 1–3 of the ’429 patent are unpatentable over Winograd in view of Issa or Merritt.

2. *Ground Two: Anticipation of Claims 1–3 by Merritt*

Petitioner asserts that claims 1–3 are anticipated by Merritt. Pet. 6. A reference anticipates a claim if it “disclose[s] each and every element of the claimed invention, whether it does so explicitly or inherently.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (citation omitted). The elements “must be arranged or combined in the same way as in the claim.” *Id.* (internal quotes and citation omitted). As explained below, Petitioner fails to establish by a preponderance of the evidence that Merritt discloses every element of claims 1–3 arranged in the same way as in each claim.

Claim 1 recites “a memory core divided into a plurality of segments each segment having a plurality of local amplifiers each coupled to a pair of

global read data lines.” Petitioner identifies “sense amplifier[s] 66” associated with sub-array region 54 as being a plurality of local amplifiers and also identifies LSA 112 as being a local amplifier. Pet. 27 (“The memory core is divided into a plurality of segments, or array regions 54, each having a plurality of local amplifiers, or sense amplifier 66.”), 28 (“The local amplifier, or LSA 112, is coupled to a pair of global read lines.”); *see also* Reply 19 (Petitioner stating that “[t]he Petition explained that Merritt’s local amplifiers, including LSA 112, are ‘coupled to a pair of global read lines, or LIO and LIO* 106’”). As explained below, Petitioner does not establish by a preponderance of the evidence that either sense amplifier 66 or LSA 112 can be local amplifiers that meet all of the requirements for local amplifiers recited in claim 1.

We first address whether sense amplifier 66 can meet claim 1’s local amplifier requirements. Claim 1 requires that the local amplifiers be coupled to a pair of global read data lines. The Petition does not, however, explain how sense amplifier 66 is coupled to global read data lines. Pet. 26–27. Instead, Petitioner identifies LIO and LIO* as being global read data lines. *See, e.g.*, Pet. 28; Reply 19. Sense amplifier 66 includes lines LIO and LIO* *within* its structure. Ex. 1006, Fig. 4. Below, we reproduce Figure 4 of Merritt (as Petitioner annotates it) to illustrate this point.

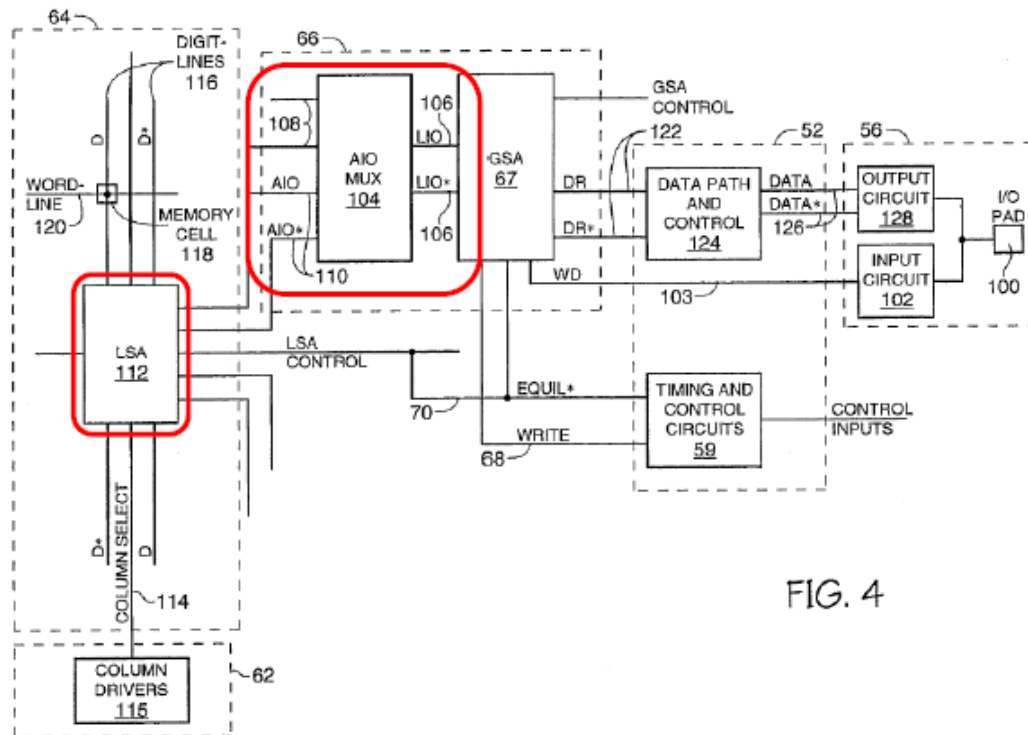


FIG. 4

Pet. 28; *see also* Ex. 1006, Fig. 4. Figure 4 elaborates on Figure 3 by showing “[a] block level schematic of a data path portion of the device of FIG. 3.” Ex. 1006, 10:47–48. Petitioner draws red shapes around local sense array amplifier (LSA) 112 and also around AIO line multiplexer 104 and its associated input/output lines. *Id.* at 10:47–11:3 (explaining Figure 4). Sense amplifier 66 is the dotted box that surrounds AIO MUX 104, GSA 67, and various lines including LIO and LIO* 106. Figure 4 demonstrates that sense amplifier 66 cannot be “coupled to” LIO and LIO* because LIO and LIO* are entirely within or are a part of sense amplifier 66.

We next address whether LSA 112 can meet claim 1’s local amplifier requirements. Aside from requiring that local amplifiers be coupled to a pair of global read data lines, claim 1 also requires “a main amplifier strobe coupled to each of the plurality of local amplifiers.” Petitioner argues that claim 1’s main amplifier strobe is met by some combination of (i) write

enable signal 68, (ii) the line that carries write enable 68, and (iii) write control circuit 58 that is the source of write enable 68. Pet. 31–33; Pet. Reply 17.¹¹ Figure 4, however, demonstrates that write enable signal 68 is coupled to GSA 67 rather than LSA 112. *See also* Ex. 1006, Fig. 3 (illustrating write control 58’s connection to the line labeled 68). Petitioner identifies GSA 67 as corresponding to claim 1’s main amplifier. Pet. 29. Because write enable signal 68 is coupled to what Petitioner calls the main amplifier, Petitioner fails to establish by a preponderance of the evidence that write enable signal 68 (or its associated line or write control circuitry 58) is coupled to a plurality of local amplifiers, LSA 112.

Petitioner argues that “coupled” in claim 1’s context does not have to be direct. Reply 21 (Petitioner making this argument in the context of whether Merritt discloses a main amplifier coupled to an output register). Petitioner, however, does not establish by a preponderance of the evidence that write enable signal 68 is even indirectly coupled to LSA 112. Rather, write enable signal 68 controls the timing of GSA 67. Ex. 1006, 10:56–60 (“Write data is driven from write data lines 103 to I/O lines 106 [through GSA 67] when enabled by a logical combination of the equilibrate signal 70 and the write enable 68.”); *id.* at 11:4–8 (“Read data follows the same path from the memory cell to the global sense amp where it is then driven on

¹¹ Patent Owner disputes whether the Petition identifies anything other than write enable signal 68 as mapping to claim 1’s main amplifier strobe. Resp. 31–32; Sur-Reply 20–21. We do not need to address this issue because even if we accept that the Petition properly identified write control circuitry 58 as part of the alleged main amplifier strobe, Petitioner fails to establish by a preponderance of the evidence that Merritt anticipates claim 1 for the reasons explained herein.

complimentary data read lines 122 , , , under control of . . . timing circuits 59.”). Merritt does not suggest that write enable 68 is ever carried on the lines that go from GSA 67 to LSA 112 (i.e., local I/O data pair 106, array I/O lines 110). Merritt instead teaches that lines 106 and 110 are data lines that carry data rather than a timing signal. *Id.* at 10:53–11:8 (describing the process by which data is driven over write lines 103, read lines 122, local I/O lines 106, and array I/O lines 110).

Because neither sense amplifier 66 nor LSA 112 can be “local amplifiers” that meet all of claim 1’s recitations, Petitioner fails to demonstrate by a preponderance of the evidence that Merritt anticipates claim 1. Because claims 2 and 3 depend from claim 1, Petitioner also fails to demonstrate by a preponderance of the evidence that Merritt anticipates claims 2 or 3.

3. *Ground Three: Obviousness of Claims 1–3 over Manning in view of Merritt*

Petitioner asserts that claims 1–3 would have been obvious over Manning in view of Merritt. Pet. 6. As we explain below, Petitioner’s assertion is not supported by a preponderance of the evidence for reasons similar to the reasons we provide with respect to anticipation by Merritt.

Manning is in the same patent family as Merritt. *Compare* Ex. 1007, code [63], *with* Ex. 1006, code [63] (showing both patents claim priority to the same parents). Figure 3 of Manning is identical to Figure 4 of Merritt. *Compare* Ex. 1007, Fig. 3, *with* Ex. 1006, Fig. 4. Petitioner maps Manning’s LSA 112 to claim 1’s local amplifiers. Pet. 38–39 (reproducing Manning Fig. 3). Petitioner argues that it would have been obvious to combine Merritt’s alleged main amplifier strobe (as we discuss above) with the device

of Manning “to further accelerate the read path of Manning.” Pet. 42. Petitioner then refers to Merritt’s Figure 3 to argue that write enable signal 68 (alleged main amplifier strobe) is coupled to each LSA 112 (alleged local amplifiers). *Id.* at 42–43 (citing Ex. 1006, 10:20–46).

But Manning’s Figure 3, which is identical to Merritt’s Figure 4, illustrates that write enable signal 68 (and its associated line) connects directly to and controls GSA 67. Ex. 1007, Fig. 3, 8:49–53 (“Write data is driven from write data lines 103 to I/O lines 106 when enabled by a logical combination of the equilibrate signal 70 and the write enable signal 68 from timing circuit 59”), 8:64–9:1 (“Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimentary data read lines 122 . . . under control of . . . timing circuits 59”). For the reasons we explain above when addressing alleged anticipation by Merritt, Petitioner fails to show by a preponderance of the evidence that write enable signal 68 is “coupled” to LSA 112 within claim 1’s meaning. Petitioner, thus, does not show by a preponderance of evidence that claim 1 is obvious over Manning in view of Merritt. Claims 2 and 3 depend from claim 1, and Petitioner also does not show by a preponderance of the evidence that claims 2 or 3 are obvious over Manning in view of Merritt.

4. *Ground Four: Anticipation of Claim 1 by Issa*

Petitioner alleges that claim 1 is anticipated by Issa. Petitioner identifies Issa’s SenseOn as mapping to claim 1’s main amplifier strobe. Pet. 51–52. SenseOn, however, is a signal. *See, e.g.*, Ex. 1011, 8:61–9:4 (referring to the “SenseOn signal”); *see also* Resp. 39; Ex. 2001 ¶¶ 116–124 (Dr. Hassoun explaining why Issa’s SenseOn signal cannot map to claim 1’s main amplifier strobe). Patent Owner raised this point in its Response (Resp.

39), and Petitioner did not dispute that SenseOn is a signal in the Reply. Reply 25 (referring to the “SenseOn ‘signal’”).

As we explain in our discussion of claim construction above, claim 1’s recited “main amplifier strobe” must be *a circuit that generates a primary timing signal used to control a secondary device*. A mere signal cannot meet this claim limitation. Petitioner, thus, fails to establish by a preponderance of the evidence that Issa anticipates claim 1.

5. *Grounds Five and Six: Obviousness of Claim 2 over Issa in view of Winograd, Merritt, or Monzel and Obviousness of Claim 3 over Winograd or Merritt*

Petitioner alleges that claim 2 would have been obvious over Issa in view of Winograd, Merritt, or Monzel and alleges claim 3 is obvious over Issa in view of Winograd or Merritt. Pet. 6. For these allegations, Petitioner relies on Issa’s SenseOn signal as being claim 1’s main amplifier strobe. Petitioner fails to establish these obviousness allegations by a preponderance of the evidence for the reasons we express above when explaining why Issa does not anticipate claim 1.

6. *Ground Seven: Obviousness of Claim 1 over Winograd in view of Issa or Monzel*

Petitioner alleges that claim 1 would have been obvious over Winograd in view of Issa or Monzel. Pet. 7. As to claim 1’s main amplifier strobe, Petitioner argues that it would have been obvious to incorporate Issa’s SenseOn signal or Monzel’s local sense strobe line 15 into Winograd’s memory core. *Id.* at 55–56.¹² The Issa argument fails to

¹² The Petition is not completely clear in explaining what claim element allegedly corresponds to Monzel’s local sense strobe line 15. Pet. 55–56.

establish obviousness by a preponderance of the evidence for the reasons we express above when explaining why Issa does not anticipate claim 1.

As to the Monzel argument, Petitioner does not identify any portions of Monzel that support Petitioner's position. Pet. 56. Moreover, Petitioner's identification of Monzel's local sense strobe line 15 appears to only identify a line that carries a signal. This identification is not adequate to establish that Monzel teaches a main amplifier strobe (i.e., a circuit that generates a primary timing signal used to control a secondary device). Resp. 49. Petitioner also does not adequately explain why it would have been obvious to incorporate any alleged main amplifier strobe from Monzel into Winograd's memory core. Pet. 56. Petitioner does little to clarify its position or address Patent Owner's arguments regarding Monzel (Resp. 49–52) in the Reply. Reply 27.

Petitioner, thus, fails to establish these obviousness allegations by a preponderance of the evidence.

7. *Ground Eight: Obviousness of Claim 2 over Winograd in view of Monzel*

Petitioner alleges that claim 2 would have been obvious over Winograd in view of Monzel. Pet. 7. Claim 2 depends from claim 1, and Petitioner appears to again rely on Monzel's local sense strobe line 15 for claim 1's first main amplifier strobe. Pet. 55–57. As we explain above, Petitioner fails to establish by a preponderance of the evidence that Monzel's

Our understanding, based on context, is that Petitioner maps local sense strobe line 15 to claim 1's main amplifier strobe because Petitioner addresses claim 1's "a main amplifier strobe coupled to each of the plurality of local amplifiers" by alleging that local sense strobe line 15 would have been coupled to each local sense amplifier of Winograd's LSA array 712. *Id.*

local sense strobe line 15 can meet claim 1's main amplifier strobe limitation. Petitioner, thus, fails to establish this obviousness allegation by a preponderance of the evidence.

8. *Grounds Nine and Ten: Obviousness of Claim 1 over Merritt in view of Issa or Monzel and Obviousness of Claim 2 over Merritt in view of Monzel*

Petitioner alleges that claim 1 would have been obvious over Merritt in view of Issa or Monzel and alleges that claim 2 is obvious over Merritt in view of Monzel. Pet. 7. Similar to grounds seven and eight, Petitioner relies on Issa's SenseOn or Monzel's local sense strobe line 15 to meet claim 1's main amplifier strobe limitation. Pet. 58–59. For the reasons we provide above when addressing grounds seven and eight, Petitioner fails to establish these obviousness allegations by a preponderance of the evidence because Petitioner has not adequately established that Issa's SenseOn or Monzel's local sense strobe line 15 can meet claim 1's main amplifier strobe limitation.

9. *Ground Eleven: Obviousness of Claim 1 over McClure in view of Winograd, Merritt, Issa, or Kawasumi*

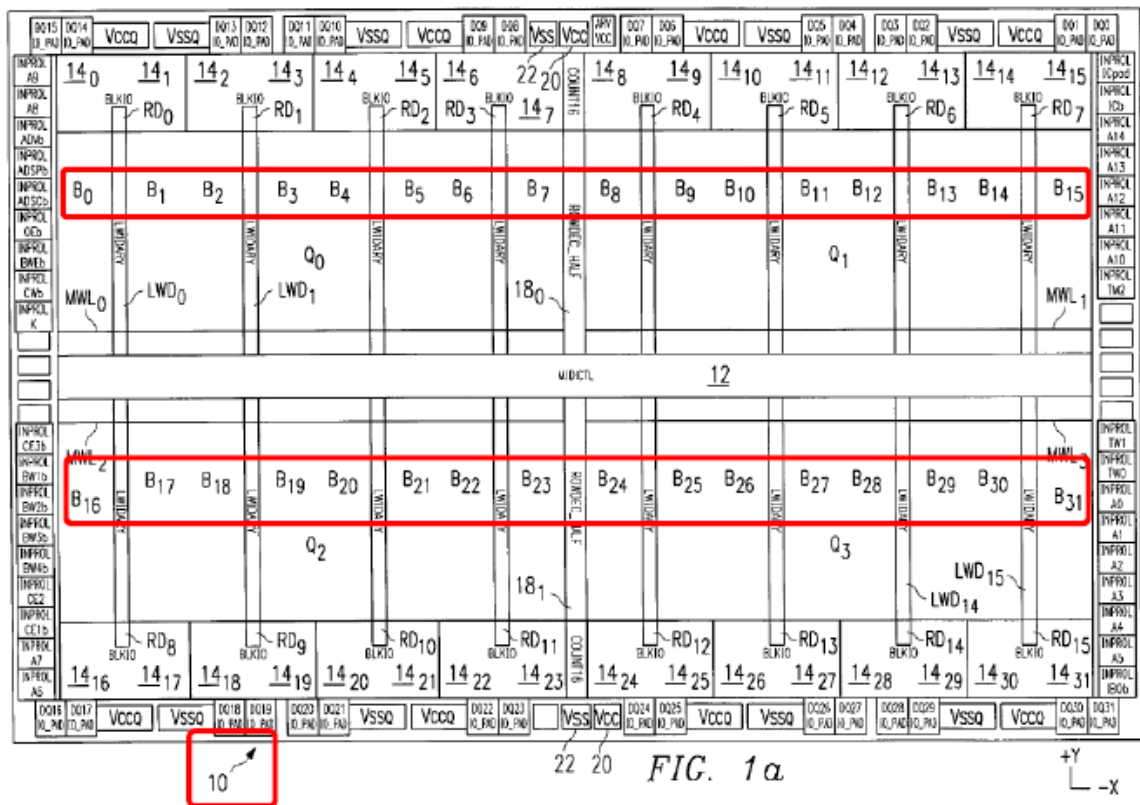
Petitioner alleges that claim 1 would have been obvious over McClure in view of Winograd, Merritt, Issa, or Kawasumi. Pet. 7. As explained below, Petitioner establishes by a preponderance of the evidence that claim 1's subject matter, as a whole, would have been obvious to a person of ordinary skill in the art at the time of the invention based upon McClure in view of Merritt, Issa, or Kawasumi.¹³

¹³ Because Petitioner's allegation based on McClure in view of Merritt, Issa, or Kawasumi is adequate to establish unpatentability, we do not need to

Claim 1's preamble recites, "A system for read path acceleration, comprising." To the extent claim 1's preamble is limiting, a preponderance of the evidence supports that McClure discloses a "system for read path acceleration" including conveying a sense amplification signal to a plurality of sense amplifiers. Pet. 61; Ex. 1008, 5:54–47. McClure teaches that its integrated circuit memory structure allows the sense amplifier associated with a memory cell to be enabled at the same time the memory cell is accessed. Ex. 1008, 2:31–51. McClure seeks to avoid prior designs that decrease total speed of the memory device. *Id.* at 2:3–23. Patent Owner does not dispute that McClure teaches a system for read path acceleration. Resp. 59–63.

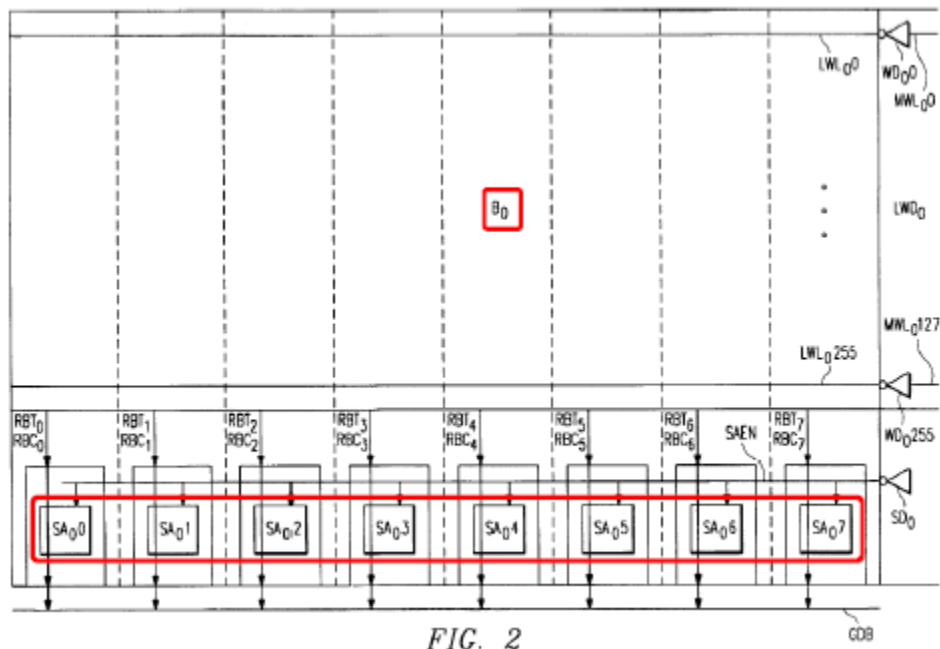
Claim 1 next recites "a memory core divided into a plurality of segments each segment having a plurality of local amplifiers each coupled to a pair of global read data lines." Petitioner annotates McClure Figure 1a when explaining how McClure teaches this limitation, and we reproduce that annotated figure below.

address the combination with Winograd.



Pet. 61. McClure Figure 1a is an electrical diagram, in block form, of an integrated circuit memory device. Ex. 1008, 3:9–10. Petitioner draws red boxes around McClure’s 32 memory blocks labeled B₀ to B₃₁. *Id.* at 3:29–51. Petitioner also draws a red box around the label 10 which refers to memory device 10. *Id.* at 3:35–36. Figure 1a shows that memory device 10 (a memory core) is divided into a number of segments or blocks B₀ to B₃₁. Pet. 61–62; Ex. 1008, 3:29–37 (explaining B₀ to B₃₁); Ex. 1003 ¶ 212 (Petitioner’s declarant, Dr. Chmelar, addressing McClure’s memory segments).

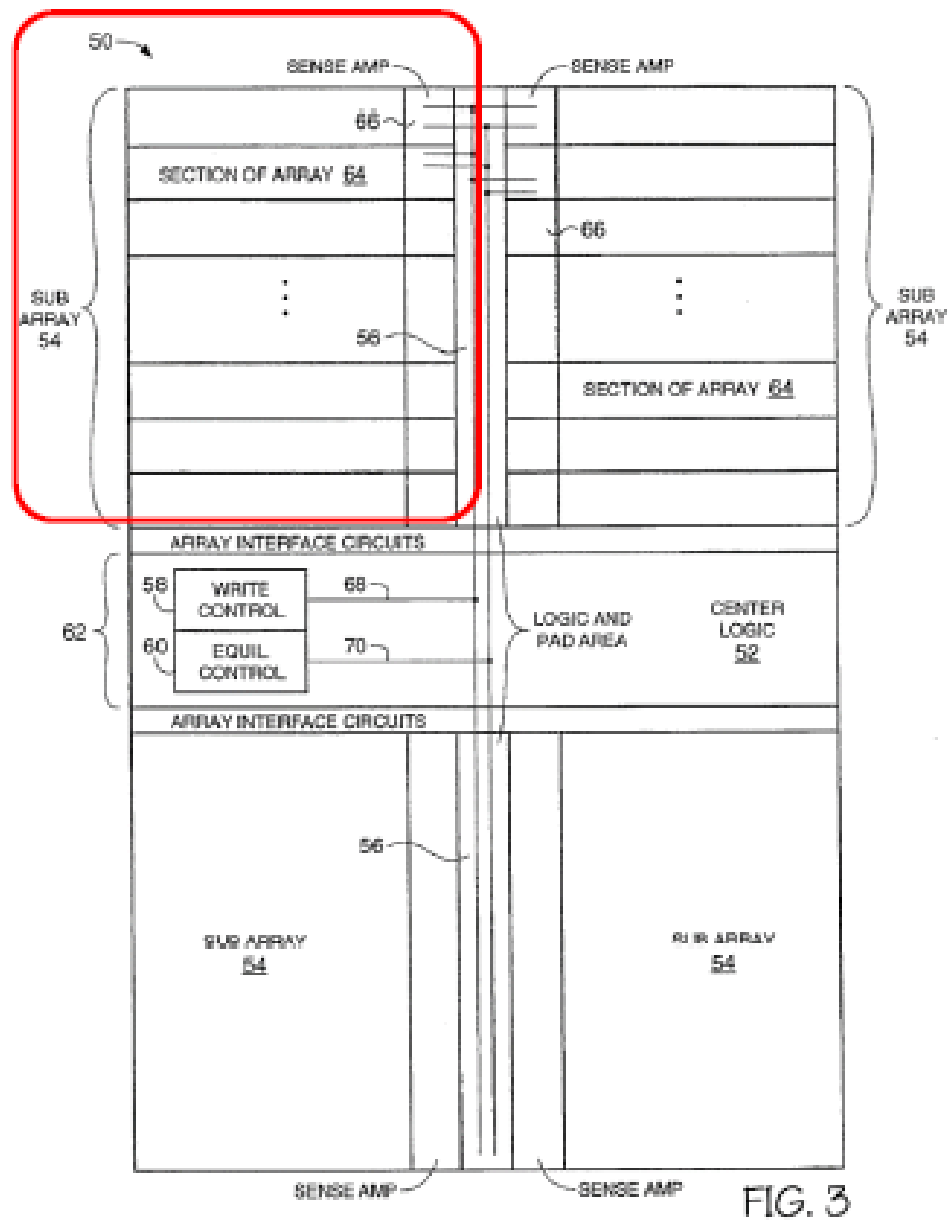
Petitioner also annotates McClure Figure 2, and we reproduce that figure below.



Pet. 62–63. McClure Figure 2 is an electrical diagram, in block form, of a block of Figure 1’s integrated circuitry. Ex. 1008, 3:13–14. Petitioner annotates Figure 2 by putting a red box around its B₀ label (labeling the area as block B₀) and around sense amplifiers SA₀₀ through SA₀₇. Pet. 63; *see also* Ex. 1008, 4:4:22–30 (McClure explaining Figure 2). McClure’s figures and text thus confirm that McClure shows memory segments (B₀ to B₃₁) that each have a plurality of amplifiers (sense amplifiers SA₀₀ through SA₀₇).

With respect to global read data lines, Petitioner argues that Merritt, Issa, and Kawasumi all teach “a memory core divided into a plurality of segments each segment having a plurality of local amplifiers each coupled to a pair of global read data lines.” Pet. 64–65. The preponderance of the evidence supports this position for each reference for the reasons we explain below:

Merritt. We reproduce Merritt’s depiction of its memory core, Figure 3, as annotated by Petitioner below.



Pet. 27. Merritt Figure 3 depicts a memory core divided into a plurality of segments (array regions 54¹⁴) each having subarray regions 64. Ex. 1006, Fig. 3; 10:42–46. Petitioner draws a red shape around sub array 54. Pet. 27.

¹⁴ Merritt’s text refers to “array regions 54” of memory device 50 (Ex. 1006, 10:22–24), but Figure 3 labels 54 “SUB ARRAY 54.”

(explaining Figure 4). Local sense array amplifier (LSA) 112 is a part of subarray region 64 (also referred to as “array section 64”). *Id.*

Merritt Figure 4 indicates that each subarray region 64 has an LSA 112 within it. Ex. 1006, Fig. 4. Figures 3 and 4 together, therefore, evidence that Merritt teaches claim 1’s requirement that a memory core (memory device 50) is divided into a plurality of segments (array regions 54) where each segment has a plurality of local amplifiers (the plurality of LSA 112, which are located in the multiple subarray regions 64).

We next address whether Merritt teaches that its plurality of LSAs 112 are “each coupled to a pair of global read data lines” as claim 1 requires. Petitioner identifies Figure 4’s LIO and LIO* 106 as being a pair of global read lines. Pet. 28. Figure 4 shows that lines 110 go from subarray region 64’s LSA 112 to AIO line multiplexer 104 within the sense amplifier 66 area. Ex. 1006, Fig. 4. The LIO and LIO* lines 106 then exit AIO line multiplexer 104. *Id.* The LIO and LIO* lines then move on to global sense amp 67 and then complementary data lines 122 and 126. *Id.* at Fig. 4, 11:4–9. Complimentary data on data lines 126 are driven to I/O (input/output) pad 100 through output circuit 128. *Id.*

Patent Owner argues that LIO and LIO* are not global read lines. In particular, Patent Owner emphasizes that LIO and LIO* are within what Merritt calls “global sense amplifier 66.” Resp. 38. Petitioner, however, argues that LIO and LIO* 106 are global because they are shared by the local sense amplifiers selected by AIO line multiplexer 104 for connection to global sense amplifier (GSA) 67. Reply 19–21.

The preponderance of the evidence supports Petitioner’s argument. Merritt Figure 3 shows that multiple subarray regions 64 are connected to

each sense amplifier 66. Ex. 1006, Fig. 3. By using Figure 4 to examine the details of subarray regions 64 and sense amplifier 66, we can see that the two figures together demonstrate that many local sense amplifiers 112 connect to one set of LIO and LIO* lines 106 through the use of AIO MUX 104. *Id.* at Figs. 3, 4. Therefore, although LIO and LIO* lines 106 are within what Merritt calls sense amplifier 66, they nonetheless are global read data lines within the context of claim 1 because they are connected to many local amplifiers (LSA 112). Petitioner is correct that it is the structure of the art that matters here, not the labeling. Reply 19 (citing *Gleave*, 560 F.3d at 1334 (explaining that “the reference need not satisfy the *ipsissimus verbis* [in the same words] test”).

Patent Owner also argues that Merritt teaches away from global read lines by teaching, “For example, I/O line multiplexer 104 would not be necessary if there is a global sense amp 67 *for each pair* of array I/O lines.” Resp. 34 (quoting Ex. 1006, 11:12–14). This sentence, however, addresses an alternative embodiment of Merritt. The Figure 3 embodiment discussed above, on which Petitioner relies, includes AIO MUX 104. This sentence from Merritt combined with the presence of AIO MUX 104 in Figure 3 suggests that, for the Figure 3 embodiment, there is *not* a global sense amp 67 for every pair of data lines coming from every LSA 112. The sentence, thus, further confirms that global sense amp 67 is global because it handles multiple pairs of I/O lines from multiple LSAs 112. *See* Ex. 1003 ¶ 93 (Petitioner’s declarant, Dr. Chmelar, explaining that this sentence means that “the I/O line multiplexer 104 couples the pair of LIO and LIO* lines 106 from the plurality of local sense amplifiers 112 to the input of a common global sense amp 67”).

Issa. Issa teaches a memory core (memory block 300) divided into a plurality of segments (column 1 through column N) with each segment having local sense amplifiers 308 a-e. Pet. 47–49; Ex. 1011, Fig. 5, Ex. 1011, 3:7–10, 5:56–63; *see also* Ex. 1003 ¶ 136 (Petitioner’s declarant, Dr. Chmelar, explaining this aspect of Issa). Each local sense amplifier is coupled to global read data lines, bit lines 304 and 306. Pet. 48–49; Ex. 1011, 5:56–63.

Kawasumi. Kawasumi teaches local amplifiers (local sense amplifier 1), each coupled to a pair of global read data lines (data bus 2). Pet. 65; Ex. 1010, Fig. 1 (illustrating what Kawasumi describes as prior art to its disclosure); *see also* Ex. 1003 ¶¶ 206–207, 223 (Petitioner’s declarant, Dr. Chmelar, explaining Kawasumi’s teachings).

Petitioner argues that a person having ordinary skill in the art would have modified McClure’s memory core “such that each sense amplifier 602 is coupled to a pair of global read data lines as taught by Winograd, Merritt, Issa, and Kawasumi.” Pet. 66. The preponderance of the evidence supports this position at least as to Merritt, Issa, and Kawasumi. Petitioner’s declarant, Dr. Chmelar, states that a person of skill in the art would have modified McClure to “reduce power consumption, circuit areas, and/or read-access time because the plurality of global data bus drivers 606 . . . could be eliminated.” Ex. 1003 ¶ 215. Dr. Chmelar’s testimony on this point is credible and well-supported by the evidence. As explained above, Merritt, Issa, and Kawasumi all teach local amplifiers coupled to global read data lines, and a person of skill in the art would have recognized the advantages of the global read data line configuration by studying those references.

Petitioner's position is further supported by the '429 patent which admits that a structure of local amplifiers connected to global read data lines was known prior art. In particular, Figure 1 of the '429 patent illustrates "conventional solution" prior art having local amplifiers 22, 24, and 26 connected to global read data lines 38 and 40. Ex. 1001, Fig. 1, 1:26–48 ("The local amplifiers 22, 24, 26 then drive the gdrd (global read data) lines 38, 40."); *see also* Pet 8–9 (mapping claim elements to Figure 1).

Patent Owner argues that Petitioner does not establish reason to combine the references' teachings. Resp. 60–62. We disagree for the reasons explained above. The record as a whole, even if the '429 patent's disclosure were not considered, supports by a preponderance of the evidence that connecting local amplifiers to global read data lines was a well-known configuration. *See supra* 27–32. Connecting McClure's local amplifiers to global read data lines is no more than use of a known method to yield predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007).

Patent Owner also argues that Kawasumi criticizes its Figure 1 prior art "for its arrangement of having multiple amplifiers connected to global data lines." Resp. 61–63; *see also* Ex. 2001 ¶ 176 (Patent Owner's declarant Dr. Hassoum stating that Kawasumi says the Figure 1 arrangement is problematic). Patent Owner does not, however, persuasively dispute that use of main amplifiers with global read data lines was a known configuration or that implementation of such a configuration would have been within the abilities of a person of ordinary skill in the art. Reply 28–29. Instead, Kawasumi, for example, teaches that its arrangement of local sense amplifiers 1 providing data to the data bus 2 is a workable configuration. Ex. 1010, 1:49–63. Although Kawasumi teaches that this configuration may

require more power to shorten sensing times, Kawasumi also suggests that solutions are available to address this problem. *Id.* at 1:49–2:12. Moreover, a person of skill recognizing problems of Kawasumi’s approach would have been able to weigh these known problems against potential advantages. Dr. Chmelar credibly identifies advantages of the global read data line approach. Ex. 1003 ¶¶ 215–219. Known advantages and disadvantages do not make the combination less obvious here. *Cf. Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (“a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine”).

Claim 1 next recites “a main amplifier having an input coupled to the pair of global read data lines and having an output coupled to an output register.” As we explain below, a preponderance of the evidence supports Petitioner’s argument that Merritt, Issa, and Kawasumi each disclose this element and that it would have been obvious for a person of ordinary skill in the art to modify McClure so that each sense amplifier 602 is coupled to a pair of global read data lines (as explained above), which in turn are coupled to a main amplifier having an output coupled to an output register. Pet. 66–67. We first address the relevant teachings of Merritt, Issa, and Kawasumi.

Merritt. Merritt teaches a main amplifier, GSA 67, coupled to global read data lines LIO and LIO* 106 and output register 130. Pet. 29–31; Ex. 1006 Figs. 4, 6, 13:39–40. The main amplifier, GSA 67, has output data lines 122 that connect to memory data bus 126, which is coupled via output circuit 128 to data bus buffer 130. Pet. 29–31; Ex. 1006, Fig. 4, 13:48–53; *see also* Ex. 1003 ¶¶ 93–98, 216 (explaining how Merritt teaches this recitation).

Issa. Issa teaches a main amplifier, global sense amplifier 302, with input connected to global read data lines, bit lines 304 and 306. Pet. 49–51; Ex. 1011, Fig. 5, 5:56–63. The main amplifier, global sense amplifier 302, has an output coupled to an output register (I/O interface 8 coupled to I/O port 6) or (sense amplifier assembly 108 connected to I/O register and buffer 112 via data bus 116). Pet. 49–51; Ex. 1011, Figs. 1, 2, 11, 3:53–57, 4:16–18, 4:49–57; *see also* Ex. 1003 ¶¶ 137–139, 217 (explaining how Issa teaches this recitation).

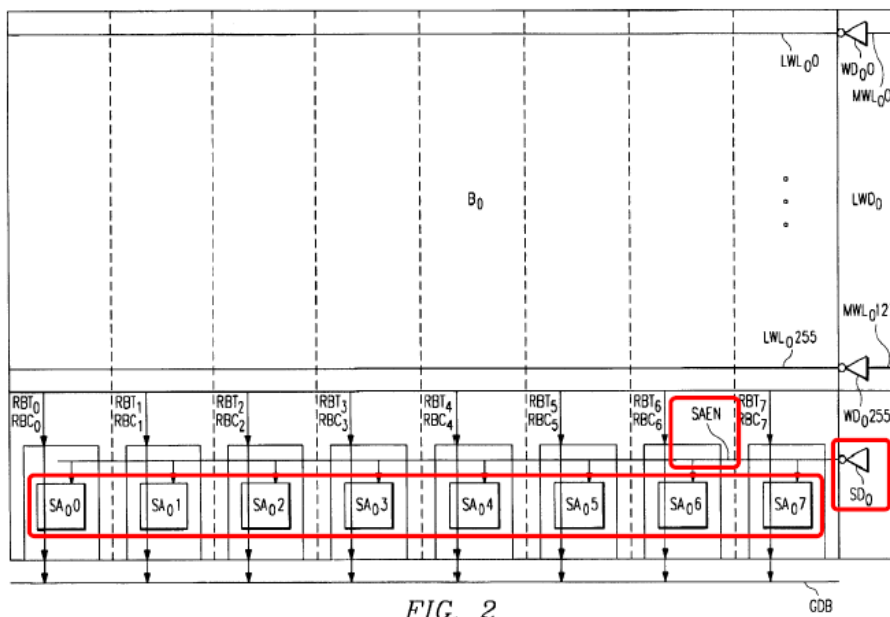
Kawasumi. Kawasumi teaches a main amplifier, global sense amplifier 3, coupled to global read data lines, data bus 2. Pet. 64–66; Ex. 1010, Fig. 1. The main amplifier, global sense amplifier 3, has an output coupled to an output register, output buffer 4. Pet. 54–55; Ex. 1010, Fig. 1; *see also* Ex. 1003 ¶ 218 (explaining Kawasumi’s teaching).

Petitioner argues that a person having ordinary skill in the art would have modified McClure’s memory core “such that each sense amplifier 602 is coupled to a pair of global read data lines, which are in turn coupled to a main amplifier, as taught by Winograd, Merritt, Issa, and Kawasumi” with the main amplifier being connected to an output register as also taught by these references. Pet. 66–67; *see also* Ex. 1003 ¶¶ 220–223 (explaining obviousness combination including output registers). The preponderance of the evidence supports this position at least with respect to Merritt, Issa, and Kawasumi. Petitioner’s declarant, Dr. Chmelar, states that a person of skill in the art would have modified McClure to couple a plurality of local sense amplifiers to a main sense amplifier in order to “reduce power consumption, circuit areas, and/or read-access time because the plurality of global data bus drivers 606 . . . could be eliminated.” Ex. 1003 ¶¶ 215–220. Dr. Chmelar’s

testimony on this point is credible and well-supported by the evidence; as explained above, Merritt, Issa, and Kawasumi all teach a main amplifier having inputs attached to global read data lines and an output coupled to an output register. A person of skill in the art would have recognized the advantages of the global read data line configuration by studying those references.

Patent Owner argues that Petitioner does not establish reason to combine the references' teachings. Resp. 60–63. We disagree for the reasons explained above. The record as a whole supports Petitioner's position. Connecting McClure's local amplifiers to global read data lines that are connected to a main amplifier and then output register is no more than use of a known structure to yield predictable results. *KSR Int'l Co.*, 550 U.S. at 401.

Finally, claim 1 recites “a main amplifier strobe coupled to each of the plurality of local amplifiers.” Petitioner identifies how McClure teaches this limitation by annotating McClure Figure 2. We reproduce the annotated figure below.



Pet. 67–68 (reproducing Ex. 1008, Fig. 2). McClure Figure 2 “is an electrical diagram, in block form, of a block in the integrated circuit memory of” McClure’s device. Ex. 1008, 3:13–14. Petitioner annotates Figure 2 by drawing red boxes around sense amplifiers SA₀0 through SA₀7, sense amplifier enable line SAEN, and sense amplifier driver SD₀. Pet. 68; *see also* Ex. 1008, 5:23–38 (McClure explaining abbreviations). Petitioner also states, “The main amplifier strobe, or SAEN, is coupled to each of the plurality of local amplifiers, or sense amplifier SA₀1 through SA₀7.” Pet. 68. In the Reply, Petitioner further emphasizes that “McClure’s sense amplifier enable line SAEN is driven by sense amplifier drive SD_[0] (‘strobe circuit’).” Reply 28.

Petitioner’s argument that the combination SAEN and SD₀ are a main amplifier strobe coupled to local amplifiers is supported by a preponderance of the evidence. Figure 2, as we reproduce it above, illustrates that the SAEN signal is generated by SD₀ and connected to the local amplifiers. Ex. 1008, Fig. 2. McClure teaches that “[a] second signal is generated on the sense amplifier driver SD₀ and driven on the sense amplifier enable line SAEN, which enables the sense amplifiers SA₀0 . . . SA₀7.” *Id.* at 5:29–39. McClure further explains that the SAEN signal that the SD₀ circuit generates serves to ensure proper signal timing and to increase read cycle time of the memory device:

The second signal is generated after a sufficient time has elapsed to ensure that an adequate signal has developed on the read busses. If the sense amplifier SA₀0 associated with the memory cell being read is not enabled at the proper time the sense amplifier may not sense the amount of signal and the data conducted to the global data bus can be wrong, producing the wrong data at the output.

To ensure that the data conducted to the output is correct the sense amplifier SA₀ associated with the memory cell being read is enabled after a first delay period after the memory cell is accessed. If the sense amplifier is enabled too early the sense amplifier will conduct erroneous data. If the sense amplifier is enabled too late there is a delay in how fast all of the data can be accessed. This increases the read cycle time of the memory device, thus decreasing its speed.

Id. at 5:29–61.

Patent Owner argues that SAEN is merely a signal and, thus, cannot be a main amplifier strobe because it is not a circuit. Resp. 59. But Patent Owner's contention fails to account for the entirety of Petitioner's showing. The Petition identifies SAEN along with the circuit that generates SAEN, sense amplifier driver SD₀, as the recited main amplifier strobe. Pet. 67–68; Reply 28. As explained above, SD₀ is a circuit.

Patent Owner argues that Petitioner improperly changed its mapping to include SD₀. Sur-Reply 30. We disagree. The original Petition put a red box around both SAEN and SD₀ when identifying the alleged main amplifier strobe. Pet. 67–68. To the extent Petitioner clarified its position in the Reply brief, the clarification was appropriate. The original Petition asserted that McClure teaches a main amplifier strobe and cited evidentiary support, including the same evidence the Reply relies upon, to explain why McClure teaches a main amplifier strobe. The Reply brief properly reinforced the Petition rather than staking a new contention. *See, e.g., Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1368 (Fed. Cir. 2015) (“The Board must make judgments about whether a Petition identified the specific evidence relied on in a Reply and when a Reply contention crosses the line from the responsive to the new.”); *Ericsson Inc. v. Intellectual Ventures I*

LLC, 901 F.3d 1374, 1380–1381 (Fed. Cir. 2018) (reversing Board’s decision where Board erred by not considering arguments in reply that cited no new evidence and merely expanded on a previously argued rationale).

Patent Owner also argues that McClure cannot have a main amplifier strobe because McClure does not have a main amplifier. Resp. 59–60; Sur-Reply 30. This argument is unpersuasive for two reasons. First, the combined teachings of the references would have resulted in a circuit having a main amplifier as we explain above. *See* Reply 28. Second, McClure’s main amplifier strobe (SAEN along with SD₀) is “main” in the sense that it has a hierarchical relationship with local amplifiers (in other words, it is a circuit that generates a primary timing signal used to control a secondary device). Based on the claim construction of “main amplifier strobe” that we provide above, this is sufficient to satisfy the “main” requirement of claim 1’s main amplifier strobe.

For the reasons explained above, Petitioner has established by a preponderance of the evidence that each recitation of claim 1 is taught by the combination of McClure with Merritt, Issa, or Kawasumi. Petitioner has also established by a preponderance of the evidence that claim 1 as a whole would have been obvious over McClure in view of Merritt, Issa, or Kawasumi.

10. *Ground Twelve: Obviousness of Claims 1–3 over Merritt in view of Issa*

Petitioner asserts that claims 1–3 would have been obvious over Merritt in view of Issa. Pet. 7. As with Ground 2, Petitioner relies on Merritt for teaching local amplifiers that meet claim 1’s requirements of “local amplifiers each coupled to a pair of global read data lines” and “a main

amplifier strobe coupled to each of the plurality of local amplifiers.” Pet. 68–70. For the reasons we explain when addressing Ground 2 above, Petitioner fails to establish that Merritt has local amplifiers that meet these requirements. Petitioner, thus, fails to establish by a preponderance of the evidence that claims 1–3 would have been obvious over Merritt in view of Issa.

IV. CONCLUSION

Petitioner has established by a preponderance of the evidence that claim 1 of the ’429 patent is unpatentable. Petitioner has not established by a preponderance of the evidence that claims 2 and 3 of the ’429 patent are unpatentable.¹⁵

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	103	Winograd, Issa, Merritt		1–3
1–3	102	Merritt		1–3
1–3	103	Manning, Merritt		1–3
1	102	Issa		1
2	103	Issa, Winograd, Merritt, Monzel		2
3	103	Issa, Winograd, Merritt		3

¹⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. §§ 42.8(a)(3), (b)(2).

1	103	Winograd, Issa, Monzel		1
2	103	Winograd, Monzel		2
1	103	Merritt, Issa, Monzel		1
2	103	Merritt, Monzel		2
1	103	McClure, Winograd, Merritt, Issa, Kawasumi ¹⁶	1	
1–3	103	Merritt, Issa		1–3
Overall Outcome			1	2, 3

V. ORDER

It is

ORDERED that Petitioner has proven by a preponderance of the evidence that claim 1 of U.S. Patent No. 7,158,429 B1 is unpatentable;

FURTHER ORDERED that Petitioner has not proven by a preponderance of the evidence that claims 2 and 3 of U.S. Patent No. 7,158,429 B1 are unpatentable;

and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

¹⁶ We do not rely on Winograd with respect to this ground.

IPR2021-00170
Patent 7,158,429 B1

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