

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED SEMICONDUCTOR ENGINEERING, INC.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2021-00180
Patent 6,624,007 B2

Before MITCHELL G. WEATHERLY, JO-ANNE M. KOKOSKI, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318

I. INTRODUCTION

Advanced Semiconductor Engineering (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–8 of U.S. Patent No. 6,624,007 B2 (“the ’007 patent,” Ex. 1001). Paper 2 (“Pet.”). Bell Semiconductor, LLC (“Patent Owner”) filed a Patent Owner Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). Between the filings of the Petition and the Preliminary Response, Patent Owner filed a statutory disclaimer of claim 8. Ex. 2001.

On June 9, 2021, we instituted *inter partes* review of claims 1–7. Paper 8 (“Institution Decision” or “Inst. Dec.”). After institution, Patent Owner filed a Response to the Petition (Paper 15, “PO Resp.”), Petitioner filed a Reply to Patent Owner’s Response (Paper 26, “Reply”), and Patent Owner filed a Sur-reply (Paper 31, “Sur-reply”).

On March 17, 2022, the parties presented arguments at an oral hearing for this proceeding. We have entered a transcript of the hearing into the record. Paper 41 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Based on the record before us, we conclude that Petitioner has shown, by a preponderance of the evidence, that claims 1–7 of the ’007 patent are unpatentable.

II. BACKGROUND

A. *Related Matters*

The parties indicate that the ’007 patent is involved in the following proceedings: *Bell Semiconductor, LLC v. Microchip Technology, Inc.*, No.6:20-cv-00296 (W.D. Tex. Apr. 16, 2020); *Bell Semiconductor, LLC v. Integrated Device Technology Inc.*, No. 19-cv-2155 (D. Del. Nov. 18, 2019); *Bell Semiconductor, LLC v. NXP Semiconductors, N.V.*, No. 1:20-cv-00611

(W.D. Tex. Mar. 23, 2020), and *Bell Semiconductor, LLC v. Renesas Elecs. Corp.*, Civil Action 6-19-cv-02196 (M.D. Fla. Nov. 18, 2019). Pet. 85; Paper 4, 1.

B. The '007 Patent

The '007 patent, titled “Method of Making Leadframe by Mechanical Processing,” issued on September 23, 2003. Ex. 1001, codes (45), (54). The '007 patent discloses a method of making a leadframe and a method of making a semiconductor device using the leadframe. Ex. 1001, 1:6–9.

With regard to preparing the leadframe, the '007 patent describes processing an electroconductive material having a uniform thickness using a first punching step, a stamping step, and a second punching step. Ex. 1001, 2:54–59. According to the '007 patent,

The first punching may be performed for forming a patterned region in the electroconductive material, the stamping may be performed for compressing the patterned region to provide a stamped portion of a thickness smaller than the uniform thickness of the electroconductive material, and the second punching may be performed for removing an unnecessary part from the stamped portion.

Ex. 1001, 2:59–65.

With regard to preparing a semiconductor device using the leadframe, the '007 patent discloses a method comprising (1) mounting a semiconductor chip on the leadframe, (2) “producing an intermediate product by forming a packaging layer to enclose the chip, wherein the intermediate product includes the leadframe, the chip and the packaging layer,” and (3) cutting the intermediate product. Ex. 1001, 2:31–38.

The '007 patent explains that the cutting step is performed using multiple cutters, a first cutter for making a “full cut” in the leadframe, and a second cutter, having a thickness greater than the thickness of the first cutter, for

making a “partial cut” in the leadframe. Ex. 1001, 2:38–42. According to the ’007 patent, “[t]he determination of where the full cut and the partial cut are to be made is based on a common cut line, so that the full cut and the partial cut coact to prevent the formation of burrs at the cut site.” Ex. 1001, 2:48–51.

C. Challenged Claims

Petitioner challenges claims 1–7 of the ’007 patent.¹ Independent claim 1 is illustrative, and is reproduced below.

1. A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a leadframe;
producing an intermediate product by forming a packaging layer to enclose the chip, the intermediate product including the leadframe, the chip and the packaging layer; and
cutting the intermediate product;
wherein the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness greater than the first thickness, the first cutter being used for making a full cut in the leadframe, the second cutter being used for making a partial cut in the leadframe, the full cut and the partial cut corresponding in position to each other.

Ex. 1001, 8:50–65.

¹ As stated above, Patent Owner filed a statutory disclaimer of claim 8 of the ’007 patent. Ex. 2001.

D. Reviewed Challenges to Patentability

In view of Patent Owner’s disclaimer of claim 8, we review the following challenges remaining from the Petition (Pet. 4):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3	102 ²	Matsuo ³
2	103	Matsuo
2	103	Matsuo, Fukasawa ⁴
4	103	Matsuo, Shibata ⁵
4–7	103	Matsuo, Higuchi ⁶

Petitioner also relies on declarations from Jeffrey C. Suhling, Ph.D. Ex. 1003; Ex. 1031. Patent Owner deposed Dr. Suhling, and filed the transcript of the deposition as Exhibit 2004 in this proceeding.

Patent Owner relies on a declaration from Joseph Bernstein, Ph.D. Ex. 2002. Petitioner deposed Dr. Bernstein, and filed transcript of the deposition as Exhibit 1030.

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application from which the ’007 patent issued was filed before this date, the pre-AIA versions of these statutory sections apply.

³ P2001-77263A, published Mar. 23, 2001 (Ex. 1005 (original language), Ex. 1006 (translation)).

⁴ US 2001/0011772 A1, published Aug. 9, 2001 (Ex. 1009).

⁵ US 5,371,943, issued Dec. 13, 1994 (Ex. 1010).

⁶ H9-102573, published Apr. 15, 1997 (Ex. 1007 (original language), Ex. 1008 (translation)).

III. ANALYSIS

A. *Legal Standards*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, “a single prior art reference must expressly or inherently disclose each claim limitation”). Moreover, “[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he dispositive question

regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference.” (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))). Additionally, “[u]nder the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates.” *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art” to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when present, objective evidence of nonobviousness.⁷ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). “This is so because inventions in most, if not all, instances

⁷ The parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR*, 550 U.S. at 418–419.

On the other hand, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined or modified the prior art references. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination.”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014))).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art would have been a person having “a bachelor-level degree in mechanical engineering, materials science, electrical engineering, or a related field and at least 3–5 years of experience in the design/development of semiconductor packages.” Pet. 13. Petitioner also indicates that a person of ordinary skill in the art could have a higher level of education and less professional experience. Pet. 13.

Patent Owner contends a person of ordinary skill in the art ““would have had at least a bachelor’s degree in Mechanical Engineering, Materials Science or Electrical Engineering with at least two to three years of experience in the field of microelectronics or semiconductor materials processing’ or alternatively, advanced training in these technical areas in lieu of industrial experience.” PO Resp. 2–3 (quoting Ex. 2002 ¶ 29). Patent Owner acknowledges that its definition “varies slightly” from Petitioner’s, but states that “the difference does not affect Patent Owner’s analysis of the grounds asserted in the Petition.” PO Resp. 3.

The parties’ proposed definitions of a person of ordinary skill in the art are not materially different, and we agree with Patent Owner that any differences do not affect the analysis of the challenges presented in the Petition. PO Resp. 3; *see also* Ex. 1031 ¶ 8 (Petitioner’s declarant, Dr. Suhling, stating that his opinions would not change under Patent Owner’s definition).

In view of the foregoing, we adopt Petitioner’s definition of a person of ordinary skill in the art. The prior art of record reflects this level of ordinary skill. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). Under that standard, we construe claims “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Furthermore, we expressly construe the claims only to the extent necessary to resolve the unpatentability issues before us. *See Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

The parties dispute the meaning of the terms “an intermediate product,” “cutting the intermediate product,” and “packaging layer.” Pet. 13; PO Resp. 3–25; Reply 1–21; Sur-reply 1–22. We address each of these terms below.

1. “an intermediate product”

Claim 1 recites “[a] method of making a semiconductor device” comprising “mounting a semiconductor chip on a leadframe,” and “producing *an intermediate product* by forming a packaging layer to enclose the chip, the *intermediate product* including the leadframe, the chip and the packaging layer.” Ex. 1001 8:50–57 (emphasis added).

Patent Owner contends that “an intermediate product” should be construed as “a molded product consisting of multiple semiconductor devices.” PO Resp. 17. Petitioner contends that the term requires no express construction and should be given its plain and ordinary meaning,

and that Patent Owner’s attempt to restrict the term “intermediate product” to a product with multiple semiconductor devices contradicts the plain language of the claim and Specification. Pet. 13; Reply 2.

We begin our analysis by looking at the language of the claims. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (“First, we look to the words of the claims themselves . . . to define the scope of the patented invention.”). According to Patent Owner, the term “an intermediate product” does not have “an ordinary and accustomed meaning apart from the ’007 Patent as used by those of ordinary skill in the art of semiconductor packaging,” and the meaning of the term is not readily apparent from the words of the claim itself. PO Resp. 17. Patent Owner acknowledges the claim recites what the intermediate product must include, but argues

The term “including” is a term of art, meaning “that whatever element is . . . included, is not necessarily the only element encompassed by the subject of the clause that contains that verb.” *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1303 (Fed. Cir. 1999). Thus, the “intermediate product” must include the leadframe, the chip, and the packaging layer, but not to the exclusion of other elements.

PO Resp. 18.

Petitioner argues Patent Owner’s construction contradicts the language of the claim itself. Reply 2. According to Petitioner, claim 1 consistently, repeatedly, and unambiguously requires only one semiconductor chip in the intermediate product, and forming only a single semiconductor device. Reply 2–3. Specifically, Petitioner argues that claim 1 recites “mounting a semiconductor chip on a leadframe,” and recites “producing an intermediate product by forming a packaging layer to enclose *the chip*, the intermediate product including the leadframe, *the chip*

and the packaging layer.” Reply 2–3 (emphasis added by Petitioner). In view of this, Petitioner argues the language of claim 1 “reinforces that only a single chip is required.” Reply 2. Petitioner also argues claim 1 recites a “method for making a semiconductor device,” which indicates that the specified method steps need to be performed for only a single device, not multiple semiconductor devices. Reply 2. Accordingly, Petitioner asserts that Patent Owner should not be allowed to rewrite the claim to exclude embodiments with a single semiconductor chip. Reply 2–3 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) (“‘[A]’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’”)).

We find Petitioner’s arguments and evidence to be persuasive. Claim 1 itself expressly recites mounting a single chip on a leadframe and producing an intermediate product forming a packaging layer to enclose “the chip.” Ex. 1001, 8:50–55. Claim 1 also expressly refers to the intermediate product as including “the chip.” Ex. 1001, 8:55–57. In view of this, we agree with Petitioner that the language of claim 1 itself reinforces that claim 1 requires only a single chip. Reply 2–3. Accordingly, we find the plain language of claim 1 is clear in reciting “the intermediate product including the leadframe, the chip and the packaging layer,” and that this language does not require a product consisting of multiple semiconductor devices. Although we agree that the use of the term “including” does not exclude other elements from the intermediate product, we do not agree that “including” *requires* additional elements, as Patent Owner suggests.

We turn next to the Specification of the ’007 patent. *Vitronics*, 90 F.3d at 1582 (“[T]he specification ‘is always highly relevant to the claim

construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’’).

Patent Owner argues that the Specification consistently describes the intermediate product as “a molded product that is singulated into individual semiconductor devices from multiple semiconductor devices.” PO Resp. 19 (citing Ex. 1001, 6:43–46). Patent Owner asserts that the Specification never describes the intermediate product of its invention as something containing only a single semiconductor device. Sur-reply 3. Patent Owner directs us to the Abstract and other portions of the Specification that state multiple semiconductor chips are mounted on a leadframe, and the intermediate product is cut into finished devices. Sur-reply 3–4 (citing Ex. 1001, Abstract, 3:62–64, 8:3–11, Figs. 4, 15, 16). Patent Owner also argues that the Specification discusses the resin packaging step as encapsulating multiple semiconductor chips, which supports its argument that no intermediate products of the invention are described as containing solely one chip. Sur-reply 5 (citing Ex. 1001, 6:28–47). Additionally, Patent Owner criticizes Petitioner’s argument that the word “the” in claim 1 means “one,” because the Specification never shows or describes an intermediate product with only one chip, and such an understanding would be inconsistent with the written description. Sur-reply 3, 6–7.

Patent Owner further argues that Figures 16–18 of the ’007 patent constitute “[a]ll of the figures of the ’007 Patent that show an ‘intermediate product,’” and they all depict the intermediate product consisting of a molded product with multiple semiconductor devices prior to singulation. PO Resp. 19 (citing Ex. 2002 ¶ 58; Ex. 1001, 3:65–67, 4:1–3, 8:3–11, Figs. 16–18). Patent Owner contends that Figures 1–3 do not show an intermediate product, but rather depict a semiconductor device fabricated by

a method of the present invention. Sur-reply 6. According to Patent Owner, “[t]hese figures (and every other figure with only a single semiconductor chip) show the result of cutting an intermediate product, i.e., potential outputs resulting from the claimed method, not what the method itself entails or operates on.” Sur-reply 6 (emphasis omitted).

Additionally, Patent Owner argues that

given the detailed description and figures exclusively referring to an intermediate product with multiple chips from which an individual device is singulated . . . , the summary language in the “summary of the invention” that merely recapitulates the recitation of claim 1, [Ex. 1001,] 2:33–38, would not have led a [person of ordinary skill in the art] to the conclusion that the recited “intermediate product” could only contain one chip [Ex.] 2002, ¶¶ 54-67.

Sur-reply 3 n.2.

Petitioner argues that nothing in the Specification indicates that “intermediate product” requires multiple semiconductor devices, noting that the phrase “multiple semiconductor devices” does not appear in the Specification. Reply 4. Petitioner further argues that the language in the SUMMARY OF THE INVENTION portion of the Specification mirrors the claim language and only requires “a semiconductor device” and “a semiconductor chip.” Reply 4 (quoting Ex. 1001, 2:31–34).

Additionally, Petitioner asserts that the Specification explicitly refers to Figures 16–18 as preferred embodiments, and Petitioner directs us to Figures 1–3, arguing that each figure shows a single semiconductor device having a single chip. Reply 5. Petitioner also contends that both experts agree that the two-step cutting process described and claimed applies even if a single package is being cut from a leadframe. Reply 5 (citing Ex. 1030, 94:3–24; Ex. 1031 ¶ 12).

We find Petitioner’s arguments and evidence to be persuasive. It is undisputed that the Specification contains language that mirrors the claim, describing mounting “a semiconductor chip” on a leadframe, producing an intermediate product by enclosing “the chip” in a packaging layer, and that the intermediate product “include[es] the leadframe, the chip, and the packaging layer.” Ex. 1001, 2:31–37; Reply 4; Sur-reply 3 n.2 (acknowledging that this portion of the specification “recapitulates” the language in claim 1). The language in the Specification therefore supports an interpretation of the claim that does not require multiple semiconductor chips or devices. Furthermore, in view of this language in the Specification, we disagree with Patent Owner’s assertions that the Specification consistently describes the intermediate product as “a molded product that is singulated into individual semiconductor devices from multiple semiconductor devices” (PO Resp. 19) and never describes the intermediate product of its invention as something containing only a single semiconductor device (Sur-reply 3).

Further, we agree with Petitioner that the ’007 patent describes Figures 16–18 as preferred embodiments. Reply 4–5; Ex. 1001, 4:13–15; *see also* Ex. 1001, 8:44–49 (stating that “[t]he present invention . . . may be varied in many ways” and that “all such modifications as would be obvious to those skilled in the art are intended to be included within the scope of the following claims”). Therefore, even if, as Patent Owner suggests, Figures 16–18 constitute “[a]ll of the figures of the ’007 Patent that show an ‘intermediate product,’” and they all depict the intermediate product consisting of a molded product with multiple semiconductor devices prior to singulation (PO Resp. 19), we disagree that they support a construction that

requires an intermediate product having multiple semiconductor devices prior to singulation.⁸

Moreover, Patent Owner acknowledges that “figures [1–3] (and every other figure with only a single semiconductor chip) show the result of cutting an intermediate product, i.e., potential outputs resulting from the claimed method.” Sur-reply 6 (emphasis omitted). And Petitioner directs us to evidence showing that both declarants agree that the two-step cutting process described and claimed applies even if a single package is being cut from a leadframe. Reply 5 (citing Ex. 1030, 94:3–24; Ex. 1031 ¶ 12). This evidence is consistent with other portions of the Specification suggesting that intermediate products may include only a single semiconductor device.

For all of the foregoing reasons, the Specification does not support a construction of “intermediate product” that requires multiple semiconductor devices. Although the Specification discloses intermediate products that do contain multiple semiconductor devices, the Specification is clear that these are preferred embodiments. The Specification also expressly discloses that intermediate products can contain a single semiconductor chip, and that the claimed process can form a single semiconductor device. Ex. 1001, 2:31–37. These disclosures are consistent with the plain language in the claim, and support a finding that an intermediate product in claim 1 only requires at least one chip, and, therefore, a single semiconductor device. On the other hand, these disclosures are inconsistent with Patent Owner’s proposed construction requiring multiple semiconductor devices, and undermine

⁸ Indeed, during the Oral Hearing, counsel for Patent Owner acknowledged that the claims are not limited to the figures. *See* Tr 38:7–9 (“Q: So is it your position then that the claims are limited only to what's shown in figures 17, 18 and 19? A: We're not saying that these are picture claims, no . . .”).

Patent Owner’s argument that a person of ordinary skill in the art would not conclude that the intermediate product could contain only one chip. Sur-reply 3 n.2.

Finally, we turn to Patent Owner’s argument based on other intrinsic evidence. *V-Formation, Inc. v. Benetton Group SpA*, 401 F.3d 1307, 1310 (Fed. Cir. 2005) (stating that the intrinsic record “usually provides the technological and temporal context to enable the court to ascertain the meaning of the claim to one of ordinary skill in the art at the time of the invention”). Patent Owner argues that a person of ordinary skill in the art would have understood an intermediate product in the context of the ’007 patent to mean a molded product with multiple semiconductor devices based on prior art (Ex. 2012 (Shih)⁹) that describes “**molded array type**” leadframes comprising molding compound covering multiple semiconductor devices before being singulated. PO Resp. 21–22 (citing Ex. 2002 ¶¶ 59–61; Ex. 2012, Figs. 1, 3, 1:54–56, 1:60–62).

We do not find Patent Owner’s argument and evidence based on Shih to be persuasive because, as Petitioner points out and Patent Owner does not dispute, Shih does not use the term “intermediate product.” Reply 5–6. We, therefore, agree with Petitioner that Shih lacks any significant bearing on the construction of the claim term “intermediate product.” Reply 5–6. Patent Owner directs us to an embodiment in Shih with a single molded product having molding compound that covers multiple semiconductors, which is similar to the preferred embodiments disclosed in the ’007 patent. PO

⁹ US 6,424,024 B1, issued July 23, 2002. Patent Owner states that Shih is intrinsic evidence because the Examiner cited Shih during prosecution. PO Resp. 7. Petitioner does not dispute that Shih is intrinsic evidence. See Reply 5–6.

Resp. 21–22. Patent Owner, however, fails to explain sufficiently why a person of ordinary skill in the art would limit the construction of “intermediate product” in the context of the ’007 patent to the embodiment shown in Shih, when the ’007 patent itself is not limited to that embodiment, and expressly includes embodiments with only a single semiconductor.

For all of the foregoing reasons, we decline to adopt Patent Owner’s proposed construction of intermediate product. Instead, we defer to the language of the claim itself which recites “mounting a semiconductor chip on a leadframe,” and “producing an intermediate product by forming a packaging layer to enclose the chip, the intermediate product including the leadframe, the chip and the packaging layer.” Ex. 1001, 8:50–57. This language is unambiguous, and is consistent with the disclosure in the Specification indicating that an “intermediate product” does not require multiple semiconductor devices.

2. *“packaging layer”*

Claim 1 recites “mounting a semiconductor chip on a leadframe” and “forming a *packaging layer* to enclose the chip.” Ex. 1001, 8:53–55 (emphasis added). Although Patent Owner acknowledges that the term “packaging layer” appears in the Specification mirroring the language in claim 1, Patent Owner contends that “packaging layer” has a broader meaning, and should be construed as a “continuous resin layer on and between adjacent semiconductor devices.” PO Resp. 22.

In support of its proposed construction, Patent Owner directs us to Figure 16 and the corresponding discussion of Figure 16 in the Specification that states “[i]n this figure, **reference numeral 5’ refers to the resin layer formed in the package-forming operation.**” PO Resp. 23–24 (quoting Ex. 1001, 8:6–11 (emphasis added by Patent Owner)). Patent Owner refers to

resin layer 5' as “packaging layer 5' . . . which is formed as a continuous layer on and between adjacent semiconductor devices.” PO Resp. 24.

Patent Owner also argues “packaging layer” necessarily encloses more than just the semiconductor chip because the '007 patent describes the packaging layer as also covering, at a minimum, bonding wires. PO Resp. 23 (citing Ex. 1001, 4:54, Fig. 16; Ex. 2002 ¶¶ 77–79).

Additionally, Patent Owner argues that “packaging layer” was understood in the art to mean “a continuous resin layer on and between adjacent semiconductor devices.” PO Resp. 24 (citing Ex. 2002 ¶¶ 81–89; Ex. 2012, 5:13–16, Fig. 8). As an example, Patent Owner directs us to Figure 8 of Shih, purportedly showing a leadframe with an upper surface, wires, and leads encapsulated in a molding compound. PO Resp. 24–25.

Petitioner contends Patent Owner’s proposed construction improperly narrows the claimed method. Reply 6. Petitioner argues that claim 1 does not expressly require the packaging layer to be “continuous” or “between adjacent semiconductor devices.” Reply 6. Petitioner also argues the Specification does not limit “packaging layer” to Patent Owner’s construction, noting the term “packaging layer” appears in the SUMMARY OF THE INVENTION using language that mirrors the claim language. Reply 6–7. Additionally, Petitioner notes the SUMMARY OF THE INVENTION states that “[p]referably, the packaging layer may be formed in a manner such that it covers the stamped portions entirely *but allows part of the leadframe to be exposed.*” Reply 7 (quoting Ex. 1001, 3:5–7).

Petitioner argues an example of this embodiment is illustrated in Figures 14A–E showing the top portion of leads on either side exposed, contrary to Patent Owner’s proposed construction requiring a continuous resin on and between adjacent semiconductor devices. Reply 7. As to Patent Owner’s

reliance on Figure 16, Petitioner again asserts that Figure 16 is a preferred embodiment, and is not intended to be limiting. Reply 7.

Petitioner also argues that the Specification describes two alternative embodiments with respect to the formation of a packaging layer, one using a single molding cavity, and one using a plurality of separate molding cavities (referred to as the “individually-molded embodiment”). Reply 8. According to Petitioner, in the individually-molded embodiment, each chip is positioned in its own molding cavity, and the packaging layer is applied in each cavity, meaning it is not continuous or placed between each chip. Reply 8 (citing Ex. 1001, 6:35–37; Ex. 1031 ¶¶ 18–19). Petitioner states that Dr. Bernstein, Patent Owner’s declarant, agreed that the use of separate molding cavities was a well-established practice for making leadframe packages at the time of the ’007 patent. Reply 9 (citing Ex. 1030, 45:8–12, 71:5–13). Petitioner argues that adopting Patent Owner’s construction would omit this embodiment and import the single-molding cavity embodiment into the claim. Reply 8.

In its Sur-reply, Patent Owner emphasizes the difference between “resin packaging *layers*” in intermediate products and “*non-layer* ‘resin packages’ in finished semiconductor devices.” Sur-reply 7. According to Patent Owner, “the ’007 patent uses the term ‘layer’ carefully and consistently, to describe only the continuous and even sheet of resin that extends over and between semiconductor chips.” Sur-reply 7–8. Patent Owner argues the ’007 patent uses reference numeral 5’ to refer only to “the resin layer formed in the package-forming operation” depicted in Figure 16, and uses a different reference numeral—5—to refer to a non-layer “resin package” in individual devices once they have been singulated, as shown in Figures 1–3. Sur-reply 8. Additionally, Patent Owner asserts that when

describing the “resin packaging step,” the ’007 patent “deliberately eschews the term ‘layer,’ as it describes the broader concept of pouring of resin for packaging both a multi-chip cavity (which would constitute a layer) and individually-molded resin packages (which would not constitute a layer, lacking resin between devices).” Sur-reply 8.

Once again, we begin with the language of the claim. Claim 1 simply recites mounting a chip on a leadframe, and forming a packaging layer to enclose the chip. Ex. 1001, 8:53–55. The claim does not expressly require the packaging layer to be continuous or to exist between adjacent semiconductor devices. Reply 6. Thus, the language of claim 1 is clear, and does not support Patent Owner’s proposed narrow construction.

The Specification of the ’007 patent also does not support Patent Owner’s proposed construction. The term “packaging layer” itself appears twice in the Specification, both times in the SUMMARY OF INVENTION section. In the first instance, the Specification mirrors the language in the claim, reciting a method that comprises the steps of mounting a semiconductor chip on a leadframe and forming a packaging layer to enclose the chip. Ex. 1001, 2:33–35; PO Resp. 23. In the second instance, the Specification states “[p]referably, the packaging layer may be formed in a manner such that it covers the stamped portion entirely but allows part of the leadframe to be exposed.” Ex. 1001, 3:5–7. In both instances, the Specification does not expressly describe a packaging layer that is continuous or that exists between adjacent semiconductor devices.

Patent Owner directs us to Figure 16 in support of its proposed construction, and specifically to reference number 5’, which Patent Owner refers to as “packaging layer 5’.” PO Resp. 23–24. We note however, that the ’007 patent identifies 5’ as a “resin layer” not a “packaging layer.” Ex.

1001, 8:7–9. And, although Figure 16 does show resin layer 5' as a continuous layer that extends between adjacent semiconductor devices, as noted above, Figure 16 is only a preferred embodiment of the claimed invention. Accordingly, we disagree we should incorporate the characteristics of resin layer 5', shown in the preferred embodiment in Figure 16, into the construction of the term “packaging layer,” especially considering there is express language describing a “packaging layer” elsewhere in the Specification that indicates these characteristics (a continuous layer that extends between semiconductor devices) are not required.

Additionally, Patent Owner's arguments based on the assertion that Petitioner erroneously conflates “the intermediate product's recited ‘resin packaging *layer*’ with *non-layer* ‘resin packages,’” are unavailing. Sur-reply 7. Specifically, Patent Owner argues that that we should reject Petitioner's arguments because they are “inconsistent with the '007 patent's clear and consistent distinction between the two different elements, . . . [and] would also improperly render the term ‘layer’ mere surplusage.” Sur-reply 7. In support of its proposed construction, however, Patent Owner argues that “[t]he term ‘packaging layer’ as described in the '007 Patent necessarily encloses more than just the semiconductor chip, as at a minimum, the packaging layer also covers . . . the bonding wires.” PO Resp. 23 (citing Ex. 1001, 4:54, Fig. 16; Ex. 2002 ¶¶ 77–79). Column 4, line 54 of the '007 patent states that “[t]he *resin package* 5 encloses the chip 3 and the wires 4.” Ex. 1001, 4:54 (emphasis added). Thus, despite emphasizing the difference between “layer” and “package” in its Sur-reply to dispute Petitioner's arguments, Patent Owner itself relies on a portion of the Specification discussing properties of the *resin package* to support its

own arguments about the meaning of the term “packaging layer.” Patent Owner does not explain sufficiently why we should disregard Petitioner’s arguments that purportedly conflate resin packaging layers and resin packages, when Patent Owner relies on portions of the Specification describing resin packages to support its construction of packaging layer.

Additionally, Patent Owner acknowledges that the individually-molded resin packages disclosed in the Specification “lack[] resin between devices.” Sur-reply 8; *see also* Sur-reply 13 (stating that “[t]he ’007 patent does mention an ‘individually molded’ embodiment with each of the multiple semiconductor chips is sealed individually, such that resin may not cover the leadframe between the devices to be singulated”). This supports Petitioner assertion that the Specification discloses embodiments wherein resin is not continuous or between chips. Reply 8.

Furthermore, we do not find Patent Owner’s argument and evidence based on Shih to be persuasive because, as Petitioner points out and Patent Owner does not dispute, Shih does not use the term “packaging layer.” Reply 11. We, therefore, agree with Petitioner that Shih lacks any significant bearing on the construction of the claim term “packaging layer.” Reply 11. Patent Owner directs us to an embodiment in Shih showing various features encapsulated in a molding compound, which appears to be similar to the preferred embodiments disclosed in the ’007 patent. PO Resp. 24–25. Patent Owner, however, fails to explain sufficiently why a person of ordinary skill in the art would limit the construction of “packaging layer” in the context of the ’007 patent to the embodiment shown in Shih, when the ’007 patent itself is not limited to that embodiment, and expressly includes other embodiments.

For all of the foregoing reasons, we decline to adopt Patent Owner’s proposed construction of packaging layer. Instead, we defer to the language of the claim itself which recites a “packaging layer enclosing the chip.” This language is unambiguous, and is consistent with the disclosure in the Specification indicating that a “packaging layer” does not need to be continuous and extend between adjacent semiconductor devices.

3. *“cutting the intermediate product”*

After reciting the intermediate product includes “the leadframe, the chip and the packaging layer,” claim 1 recites:

cutting the intermediate product;

wherein the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness greater than the first thickness, the first cutter being used for making a full cut in the leadframe, the second cutter being used for making a partial cut in the leadframe, the full cut and the partial cut corresponding in position to each other.

Ex. 1001, 8:58–65.

Patent Owner contends that the term “cutting the intermediate product” should be construed as “cutting through the entire thickness of the intermediate product including the leadframe and the packaging layer.” PO Resp. 3. Petitioner argues this claim term requires no construction and is clearly defined by the claim language itself. Pet. 13; Reply 11.

We once again start our analysis with the language of the claims. Patent Owner contends that “[b]ased on the language of Claim 1, the cutting process is presumed to have two distinct and separate requirements: (1) the intermediate product itself must be cut; and (2) that cutting process must include a partial cut and a full cut to the leadframe using cutters with the

proscribed thicknesses.” PO Resp. 4. According to Patent Owner, finding otherwise would require rewriting the cutting step to read “cutting the leadframe” instead of “cutting the intermediate product.” PO Resp. 4.

Petitioner asserts that the plain language of the claim specifies “cutting the intermediate product,” not cutting the packaging layer. Reply 11. Petitioner also asserts that claim 1 further specifies the requirements of the cutting step by reciting “*the cutting step is performed by . . . making a full cut in the leadframe*” and “*making a partial cut in the leadframe*.” Reply 11–12 (quoting Ex. 1001, 8:59–65 (emphasis added by Petitioner)). According to Petitioner, “the claim language itself governs, and states that the cutting step is ‘performed by’ cutting the leadframe, which the claim defines as part of the intermediate product.” Reply 12.

We find Petitioner’s arguments to be persuasive. Claim 1 does not expressly recite cutting both the leadframe and packaging layer, as Patent Owner’s proposed construction requires. Ex. 1001, 8:58. Rather, claim 1 requires only cutting the intermediate product, and recites that the intermediate product includes the leadframe. Ex. 1001, 8:54–58. Additionally, claim 1 expressly recites that the cutting step is performed by making a “full cut in the leadframe,” and a “partial cut in the leadframe.” Ex. 1001, 8:62–65. Thus, the language of the claim itself focuses on cutting the leadframe, and there is no corresponding language regarding cutting the packaging layer. Furthermore, the phrase “wherein the cutting step” refers to the previous step of “cutting the intermediate product,” such that what follows—making a full cut and partial cut in the leadframe—specifies the requirements for cutting the intermediate product. Therefore, as written, this language of claim 1 does not present a requirement of the claim separate and

distinct from the step of cutting the intermediate product itself, as Patent Owner suggests. PO Resp. 4.

We turn next to the Specification. Patent Owner argues again that Figures 16–18 are the only figures in the '007 patent that show an intermediate product, with Figure 16 showing an intermediate product prior to the cutting step, and Figures 17 and 18 showing the two-step process of cutting the intermediate product. PO Resp. 4–6. Patent Owner argues that each of Figures 17A and 18B show a “full cut” made through both the leadframe and packaging layer of the intermediate product shown in Figure 16. PO Resp. 6–7. Patent Owner argues the Specification supports its proposed construction because it states that “as shown in FIG 17A, . . . *the cutter CB1 cuts through the entire thickness of the intermediate product* (‘full cut’ step).” PO Resp. 7 (quoting Ex. 1001, 8:15–19 (emphasis added by Patent Owner)); Sur-reply 9–11. Patent Owner thus concludes that the combination of the leadframe and the resin packaging layer comprise the “entire thickness of the intermediate product,” and asserts that “[t]he '007 patent does not depict, describe, or otherwise disclose cutting the intermediate product of claim 1 (shown in Fig. 16) without the required ‘full cut’ being made through *both* the entirety of the leadframe *and* the resin packaging layer.” Sur-reply 11; *see also* Sur-reply 9–10 (arguing that the '007 patent “unambiguously equates” the full cut step as being a cut through the leadframe and resin packaging layer).

Petitioner argues that nothing in the Specification limits the two-step cutting process to the preferred embodiment of Figure 16. Reply 13. By way of example, Petitioner directs us to Figures 14A–E. Reply 13–16. Petitioner also directs us to the portions of the Specification stating Figures 14A–E show “semiconductor devices (designated X11–X15) formed by

cutting an individually molded intermediate product,” and that “*the method of the present invention is applicable to* fabricating semiconductor device [X11] - X15 shown in *FIGS. . . 14A -14E.*” Reply 14 (quoting Ex. 1001, 6:57–59 (emphasis added by Petitioner)). According to Petitioner, Figures 14A–E depict devices formed by cutting through leadframe portions between individually-molded devices without the need to cut through resin or a packaging layer. Reply 16.

We find Petitioner’s arguments to be persuasive. Although Figures 16–18 of the ’007 patent show a packaging layer covering the entire leadframe and a blade cutting both the packaging layer and leadframe, these images show preferred embodiments of the invention, not requirements of the claims. *See* Ex. 1001, 4:13–15. Further, in the SUMMARY OF INVENTION section, the ’007 patent associates “cutting the intermediate product,” including making a “full cut” and “partial cut,” with cutting the leadframe:

The method comprises the steps of . . . cutting the intermediate product. The cutting step is performed by using a first cutter of a first thickness and a second cutter of a second thickness greater than the first thickness. The first cutter is used for making a “full cut” *in the leadframe*, while the second cutter is used for making a “partial cut” *in the leadframe*. In this specification, the “full cut” implies that *the leadframe is cut through* in its thickness direction. The “partial cut”, on the other hand, implies that the *leadframe is not cut through* in its thickness direction (nor in any other directions) and the depth of the cut is smaller than the thickness of the leadframe.

Ex. 1001, 2:32–48 (emphases added).

This language in the Specification is consistent with the language recited in claim 1. Ex. 1001, 8:58–65. Furthermore, contrary to Patent Owner’s assertions, this is an example of the Specification discussing cutting

the intermediate product without referring to Figures 16–18, and it does not mention the resin packaging layer. *See* PO Resp. 7; Sur-reply 9–11.

Therefore, we disagree that the '007 patent “unambiguously equates” the full cut step as being a cut through the leadframe and resin packaging layer. Sur-reply 9. Instead, the '007 patent repeatedly and consistently associates a full cut with cutting the leadframe.

The Specification also states that “[p]referably, the packaging layer may be formed in a manner such that it covers the stamped portion entirely but allows part of the leadframe to be exposed.” Ex. 1001, 3:5–7. In our Institution Decision, we stated that this language expressly allows for part of the leadframe in the intermediate product to be exposed, i.e., not covered by the packaging layer, which supports a determination that “cutting the intermediate product” in claim 1 does not require cutting the packaging layer. Inst. Dec. 18.

Patent Owner argues that we “misinterpreted” this language, and the corresponding language in claim 7 “because both of these citations instead refer to the leadframe being *exposed on the bottom surface* of the intermediate product as part of the step of forming the packaging layer, *not* that the packaging layer does not cover the top surface of the leadframe between devices.” PO Resp. 9. Patent Owner directs us to several instances in the Specification where the word “exposed” refers to the leadframe being exposed on the bottom surface, and asserts that “[n]owhere in the '007 Patent is ‘exposed’ used to refer to a top portion of a leadframe being exposed.” PO Resp. 9–15; Sur-reply 17–22. Patent Owner further argues that its proposed construction, which requires cutting through the packaging layer, is consistent with this language in the Specification, which purportedly describes only the bottom surface of the leadframe as being

exposed (i.e., having a packaging layer over the entire top surface of the leadframe).

As Petitioner points out, however, this language in the Specification, as well as the corresponding language in claim 7 (also stating that parts of the leadframe may be exposed), does not expressly limit the exposure to any particular surface (e.g., the bottom surface) of the leadframe. Reply 19. In contrast, when the inventors of the '007 patent intended to convey that a specific portion of the leadframe is exposed they expressly recited the location of such exposure, as evidenced by the numerous examples in the Specification. PO Resp. 10–15; *see also* Reply 19 (citing Ex. 1001 at 7:53–55 and 7:62–64 as examples of the inventors of the '007 patent explicitly referring to exposure at a side surface). Additionally, Petitioner notes that the Specification explicitly includes an individually-molded embodiment, and it is undisputed that this embodiment does not include resin between the individually-molded devices. Reply 18; Sur-reply 13.¹⁰ Petitioner also directs us to Figures 14A–E,¹¹ which show a semiconductor device with the

¹⁰ Patent Owner argues that the individually-molded embodiment is outside the scope of claim 1 based on its proposed constructions. Sur-reply 13. Specifically, Patent Owner contends that an individually-molded embodiment cannot constitute the intermediate product because it does not include a resin packaging layer. Sur-reply 13. Patent Owner also argues it cannot be cut by the full cut which requires that the cut be made through the leadframe and the resin packaging layer. Sur-reply 13. Because we decline to adopt Patent Owner's proposed constructions of "intermediate product" and "packaging layer," we disagree with the assertion that the individually-molded embodiment is outside the scope of claim 1.

¹¹ Patent Owner acknowledges that Figures 14A–E show semiconductor devices that "protrude sideways from the resin package," but asserts that that "Figures 14A–E were not subject to the cutting process claimed in Claim 1, because they do not have a 'step' on the bottom surface." PO Resp. 17. Patent Owner's "step" argument is not persuasive because, as Petitioner

top surface exposed. Reply 14; *see also* Ex. 1001, 6:57–59 (stating “[t]he method of the present invention is applicable to fabricating semiconductor device [X11] - X15 shown in FIGS. . . 14A–14E”).

Thus, the Specification as a whole does not support Patent Owner’s narrow view of “exposed,” limited to just the bottom surface of the leadframe being exposed. In view of this, we disagree that we misinterpreted the portion of the Specification stating that “[p]referably, the packaging layer may be formed in a manner such that it covers the stamped portion entirely but allows part of the leadframe to be exposed.” Ex. 1001, 3:5–7. This language permits, and other portions of the Specification confirm, that the exposed part of the leadframe can be the top surface of the leadframe. The disclosure of embodiments wherein the top surface of the leadframe is exposed (i.e., is not covered by the packaging layer) supports Petitioner’s arguments that “cutting the intermediate product” should not be construed to require cutting the packaging layer.

Patent Owner additionally argues that a person of ordinary skill in the art would have understood that “cutting the intermediate product” in the context of the art at the time of the ’007 patent would include cutting the leadframe and packaging layer because Shih shows cutting a purportedly similar intermediate product through both a leadframe and packaging layer. PO Resp. 7–8 (citing Ex. 2012, Fig. 8; Ex. 2002 ¶¶ 121–122). Patent Owner’s arguments based on Shih here are no more persuasive than those

points out, none of the exemplary semiconductor devices shown in Figures 9–14E (designated X2–X15) have a step on the bottom surface, including devices X2–X10 formed from an intermediate product with all devices molded together (as shown in Figure 16). Reply 17. Additionally, claim 1 does not require steps on the bottom surface. Ex. 1001, 8:51–65; Reply 17.

presented and considered in connection with Patent Owner’s proposed construction of “intermediate product” and “packaging layer.” PO Resp. 21–22, 24–25. We, therefore, find Patent Owner’s arguments based on Shih here to be unpersuasive for the same reasons discussed above.

For all of the foregoing reasons, we decline to adopt Patent Owner’s proposed construction of “cutting the intermediate product.” Instead, we defer to the language of the claim itself. This language is unambiguous, and is consistent with disclosures in the Specification indicating that “cutting the intermediate product” does not require cutting through the leadframe and packaging layer.

We determine that no other claim terms require an express construction. *See Realtime Data*, 912 F.3d at 1375.

D. Claims 1 and 3 – Anticipation by Matsuo

Petitioner contends claims 1 and 3 are unpatentable as anticipated by Matsuo. Pet. 14–37.

1. Matsuo (Ex. 1006)

Matsuo relates to the production of resin-sealed semiconductor devices, as depicted in Figure 2b, reproduced below. Ex. 1006 ¶¶ 1–17.

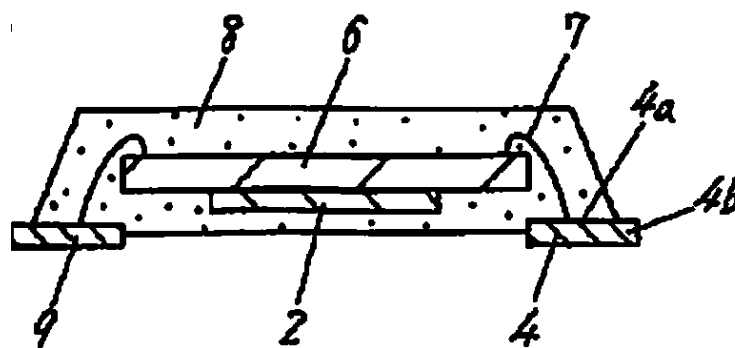


Figure 2(b) shows a cross sectional view of Matsuo's semiconductor device including semiconductor element 6 mounted on die pad part 2 of the leadframe. Ex. 1006 ¶ 45. Semiconductor element 6 is electrically connected to inner lead part 4a of lead part 4 by thin metal wire 7, and the outer perimeter is sealed by sealing resin 8. Ex. 1006 ¶ 45. The bottom surface of lead part 4 is exposed to form external terminal 9 and the outer lead part 4b is exposed from the side surface of sealing resin 8 to form a surface that is substantially flush with the side surface of the sealing resin 8. Ex. 1006 ¶ 45.

As part of the process of forming the semiconductor device, Matsuo describes using rotary blade 11 to cut lead part 4 on cutting section 5, as depicted in Figure 10. Ex. 1006 ¶ 53, Fig. 10. Matsuo explains that during this process, burrs may form on the surface of outer lead part 4b, as depicted in Figure 12, reproduced below.

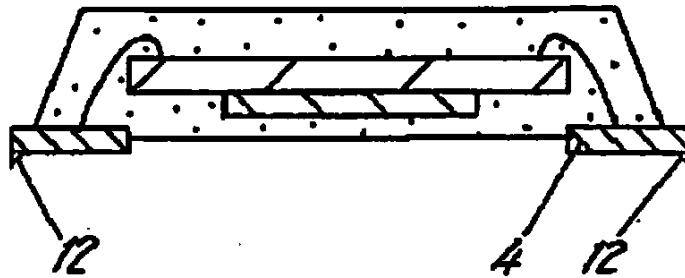


Figure 12 is a cross sectional view of the semiconductor device shown in Figure 2 that includes burrs 12 on lead part 4. Ex. 1006 ¶ 57. Matsuo explains that

Mounting failures may be produced when mounting the resin sealed semiconductor device on the substrate, or solder bridges may be produced when forming solder junctions, by the burr portions 12, so it is necessary to cut the leads so as to not produce burr portions 12, or necessary to remove burr portions 12 that have been produced. Note that in FIG. 12 the burr portion 12 is

shown on the bottom face side of the lead portion 4; however, it may be produced instead on the side face side of a lead portion 4, or the top face side of a lead portion 4.

Ex. 1006 ¶ 57.

To avoid the formation of burrs during cutting, Matsuo teaches forming cutting grooves in two or more stages. Ex. 1006 ¶ 67. According to Matsuo, this suppresses the generation of burrs because “gradually cutting the lead portions reduces the amount that is cut each time, reducing the amount of spring-back, due to cutting with the rotating blade, of the metal material that is the lead member material.” Ex. 1006 ¶ 67. Matsuo discloses one embodiment wherein the second blade used to form the second cutting groove has a narrower width than the blade used to form the first cutting groove. Ex. 1006 ¶¶ 87–88, 92, Figs. 27–29.

2. *Claim 1*

Claim 1 recites “[a] method of making a semiconductor device, the method comprising the steps of: mounting a semiconductor chip on a leadframe.” Ex. 1001, 8:51–53. Petitioner contends Matsuo teaches a method of making a semiconductor device that includes mounting a semiconductor chip (semiconductor element 6) on a leadframe (die pad part 2), according to the fourth embodiment in Matsuo. Pet. 19–22 (citing Ex. 1006 ¶¶ 36–38, 41, 47–49, 85–87).

Claim 1 next recites “producing an intermediate product by forming a packaging layer to enclose the chip, the intermediate product including the leadframe, the chip and the packaging layer.” Ex. 1001, 8:54–57. Petitioner contends Matsuo discloses producing an intermediate product “by forming a packaging layer (sealing resin 8) to enclose the chip (semiconductor element 6), the intermediate product including the leadframe (die portion 2

and lead portions 4 of lead frame), the chip (semiconductor element 6) and the packaging layer (sealing resin 8).” Pet. 22–24 (citing Ex. 1006 ¶¶ 51, 86, Fig. 27). To support its argument, Petitioner presents an annotated version of Matsuo’s Figure 27, reproduced below from the Petition.

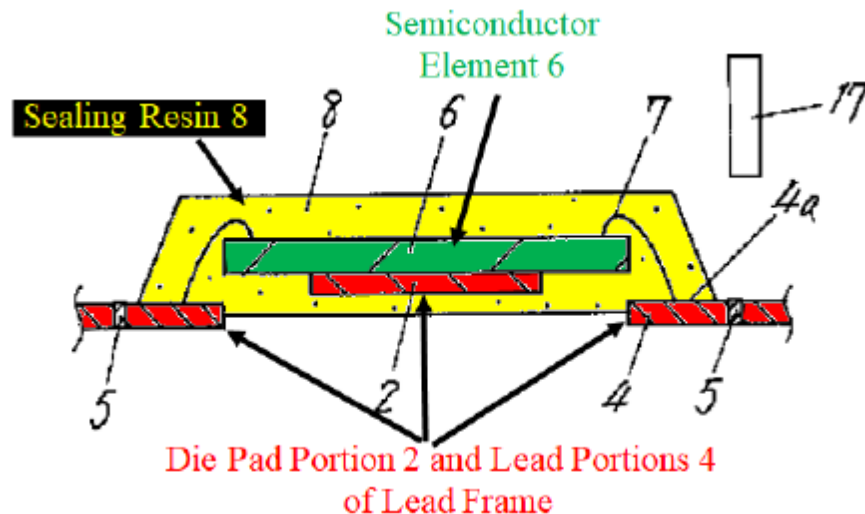


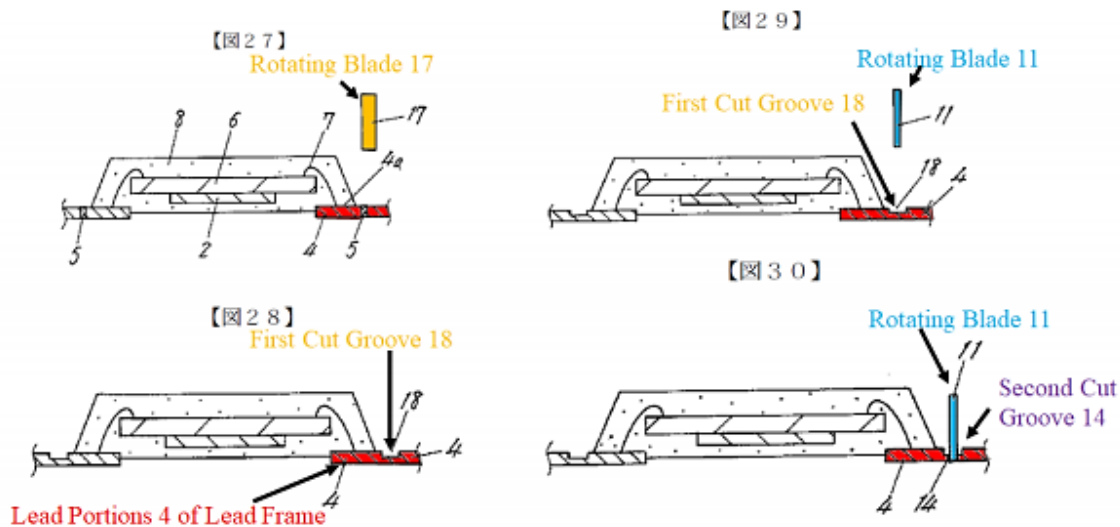
Figure 27 shows a cross-sectional view of one embodiment of Matsuo’s semiconductor with sealing resin 8 (highlighted in yellow by Petitioner), die pad part 2 and lead part 4 (highlighted in red by Petitioner) and semiconductor element 6 (highlighted in green by Petitioner). Pet. 23.

Claim 1 further requires “cutting the intermediate product.” Ex. 1001, 8:58. Petitioner contends Matsuo’s fourth embodiment involves a multistage lead cutting process as shown in Figures 27–31, with a first cut using rotary blade 17 and a second cut using rotating blade 11. Pet. 24 (citing Ex. 1006 ¶¶ 87–88). Petitioner notes that Matsuo explains the cutting results in the “resin sealed semiconductor devices hav[ing] been cut apart.” Pet. 24 (quoting Ex. 1006 ¶ 89).

Claim 1 additionally requires “the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness greater than the first thickness, the first cutter being used for

making a full cut in the leadframe, the second cutter being used for making a partial cut in the leadframe.” Ex. 1001, 8:59–64.

To support its assertions that Matsuo discloses the aforementioned cutting limitations in claim 1, Petitioner provides annotated versions of Matsuo Figures 27–30, reproduced below.



Petitioner’s annotated versions of Figures 27–30 depict cross-sectional views of Matsuo’s semiconductor package with Figure 27 showing rotating blade 17 (highlighted in yellow), Figure 28 showing first cut groove 18 in lead portion 4 (highlighted in red), Figure 29 showing rotating blade 11 (highlighted in blue), and Figure 30 showing rotating blade 11 forming second cut groove 14 within first cut groove 18 in lead portion 4. Pet. 36.

Petitioner argues rotating blade 11 corresponds to the first cutter and rotating blade 17 corresponds to the second cutter recited in claim 1. Pet. 25. According to Petitioner, Matsuo states rotating blade 11 is “narrower in width” than rotating blade 17. Pet. 31 (citing Ex. 1006 ¶¶ 87–88). Referring to Figures 29 and 30 of Matsuo, Petitioner contends rotating blade 11 (the first cutter) makes a full cut in the leadframe, noting

Matsuo states rotating blade 11 is used to form “a ‘second cut groove 14’ that comprises the entire vertical dimension of the lead portion 4 of the leadframe.” Pet. 26–28. Referring to Figures 27 and 28 of Matsuo, Petitioner contends rotating blade 17 (the second cutter) makes a partial cut in the leadframe, noting Matsuo states it “forms a ‘first cut groove 18’ that is only partially through the leadframe in the vertical dimension.” Pet. 28–30.

Finally, claim 1 requires “the full cut and the partial cut corresponding in position to each other.” Ex. 1001, 8:64–65. Petitioner contends Matsuo discloses that the full and partial cuts, shown by grooves 14 and 18, respectively, in Matsuo Figures 27–30, are performed on the same location of the leadframe. Pet. 35–36 (citing Ex. 1006 ¶¶ 87–88).

Patent Owner argues that Petitioner fails to show Matsuo discloses “an intermediate product,” “cutting the intermediate product,” and “a packaging layer,” as claim 1 requires. PO Resp. 27–41. Patent Owner’s arguments, however, are each based on its proposed construction of these terms. PO Resp. 29 (“As described in Section III.A above, ‘cutting the intermediate product’ should be construed as ‘cutting through the entire thickness of the intermediate product including the leadframe and the packaging layer.’”), 32–33 (“As described in Section III.B above, ‘an intermediate product’ is ‘a molded product consisting of multiple semiconductor devices.’”), 39 (“As described in Section III.C above, the ‘packaging layer’ is ‘a continuous resin layer on and between adjacent semiconductor devices.’”). For the reasons discussed above, we do not adopt Patent Owner’s constructions. Patent Owner does not present any arguments based on any other construction of the terms. *See* PO Resp. 27–41; Sur-reply 22–29.

We have reviewed the undisputed evidence and arguments Petitioner provides regarding Matsuo's disclosure of the limitations in claim 1 (Pet. 14–37), and agree, for the reasons set forth in the Petition, that Matsuo discloses these limitations of claim 1. As noted above, Patent Owner does not dispute Petitioner's contentions regarding Matsuo's disclosures based on the plain and ordinary meaning of the claim terms. Thus, after considering the parties' arguments and the evidence presented during the trial, we determine Petitioner has established by a preponderance of evidence that Matsuo anticipates claim 1.

3. *Claim 3*

Claim 3 depends from claim 1 and requires “the full cut is made after the partial cut is made.” Ex. 1001, 9:1–2. Petitioner directs us to portions of Matsuo disclosing the limitations recited in claim 3. Pet. 36–37 (citing Ex. 1006 ¶¶ 87–88 and Figures 27–30 describing and showing a first partial cut and followed by a second full cut). Patent Owner does not separately address claim 3.

We have reviewed the undisputed evidence and arguments Petitioner provides regarding Matsuo's disclosure of the limitations in claim 3, and agree, for the reasons set forth in the Petition, that Matsuo discloses these limitations of claim 3. As a result, we determine Petitioner has established by a preponderance of evidence that Matsuo anticipates claim 3.

E. Claims 4–7: Obviousness in view of Matsuo and Higuchi

Petitioner contends the subject matter of claims 4–7 would have been obvious in view of Matsuo and Higuchi. Pet. 71–81.

1. *Higuchi (Ex. 1008)*

Higuchi is directed to a method of manufacturing a highly accurate lead frame, in particular a lead frame having a thin-walled flat portion at a

tip of an inner lead. Ex. 1008 ¶¶ 1, 3. One embodiment of Higuchi's method includes (1) heat treating the lead frame material, (2) pressing the heat-treated material to form a lead frame having an intermediate shape having inner leads with a tip connected to a central connecting pad, outer leads connected to the inner leads, and a support lead connected to the connecting pad, (3) heat treating the lead frame having an intermediate shape to remove internal residual stress generated in the previous step, (4) carrying out a leveling process to form a through-hole and an element mounting portion defined by the through-hole at the center of the connecting pad, and then providing a thin-walled flat portion on the tip portion of the inner lead through a pressing process that releases stress through the through-hole, and (5) removing the connecting piece so as to leave the element mounting portion formed at the center of the connecting pad. Ex. 1008 ¶ 4. Higuchi provides detailed explanations of each step along with figures to illustrate its invention. *E.g.*, Ex. 1008 ¶¶ 8–15, Figs. 1–4.

2. *Analysis*

Claims 4–7 depend, directly or indirectly, from claim 1. Petitioner contends Matsuo discloses the method of claim 1 (as discussed above) and directs us to portions of Higuchi that disclose or suggest the additional limitations present in claims 4–7. Pet. 73–81; *see also* Pet. 48–70 (providing an analysis regarding Higuchi's disclosure of limitations in claim 8 corresponding to similar limitations in claims 4–7). In particular, Petitioner asserts Matsuo discloses preparing a leadframe, but does not provide the details of that process, whereas Higuchi does. Pet. 71. Petitioner contends that Higuchi discloses a five-step, mechanical process for preparing a lead frame. Pet. 71. According to Petitioner, these steps include leveling the leadframe material using a roller leveler, thereby providing a plate with

uniform thickness, as claim 4 requires. Pet. 73 (citing Ex. 1008 ¶ 9). Higuchi also discloses a first punching step to form a patterned region comprised of through holes and supplementary holes, a stamping step to compress the patterned region to a thickness smaller than the uniform thickness of the electroconductive material, and a second punching step to remove an unnecessary part from the stamped region, as claim 5 requires. Pet. 74–75 (citing Ex. 1008 ¶¶ 11–12). Petitioner also asserts that the first punching step forms tip portions of inner leads and connecting pieces that become regions for wire bond connections between the leads and the semiconductor device in the final leadframe (i.e., lands) that are adjacent to supplementary through holes (i.e., openings), and that the stamping step causes the lands to be spread out into the openings, as claim 6 requires. Pet. 75–78 (citing Ex. 1008 ¶¶ 10, 12). Finally, Petitioner contends the combined teachings of Matsuo and Higuchi disclose the packaging layer covering the stamped portion entirely, and allowing part of the leadframe to be exposed, as claim 7 requires. Pet. 78–81 (citing Ex. 1006 ¶¶ 47, 51, 95; Ex. 1008 ¶ 12).

Petitioner further argues a person of ordinary skill in the art would have recognized the benefits of using Higuchi’s process, and, therefore, would have been motivated to incorporate Higuchi’s leadframe processing steps into Matsuo’s manufacturing process. Pet. 72–73 (noting Higuchi’s benefits include “suppress[ing] the release of the internal residual stress that is present from slitting, and the like, and further carr[ying] out correction of the residual strain that is produced in the intermediate shape processing of the lead frame” (quoting Ex. 1008 ¶ 4)). Petitioner also contends that using Higuchi’s leadframe manufacturing process would have been a simple combination of prior art steps that would have yielded predictable results,

and that a person of ordinary skill in the art would have had a reasonable expectation of success in utilizing Higuchi's process because Higuchi's process is "well-suited for mass producing" the type of leadframe disclosed in Matsuo. Pet. 72–73 (citing Ex. 1003 ¶¶ 203–204).

Patent Owner does not dispute Petitioner's contentions that Higuchi teaches or suggests the additional limitations in claims 4–7, that a person of ordinary skill in the art would have had reason to combine the teachings of Matsuo and Higuchi, or that a person of ordinary skill in the art would have had a reasonable expectation of success. Instead, Patent Owner relies on the same arguments discussed above regarding Matsuo's failure to disclose all of the limitations in claim 1, based on Patent Owner's proposed construction of claim terms. For the reasons discussed above, we do not adopt Patent Owner's constructions, and we have determined Petitioner has established by a preponderance of evidence that Matsuo anticipates claim 1.

Petitioner has provided an undisputed analysis of the scope and content of Matsuo and Higuchi, explained where the prior art references teach or suggest each limitation in the challenged claims, and explained why a person of ordinary skill in the art would have had reason to combine the prior art references with a reasonable expectation of success. Pet. 71–81. We have reviewed the information and arguments Petitioner provides regarding claims 4–7, and we agree, for the reasons presented in the Petition, that Higuchi teaches or suggests all of the additional limitations of claims 4–7, that a person of ordinary skill in the art would have had reason to combine the teachings of Matsuo and Higuchi, and that a person of ordinary skill in the art would have had a reasonable expectation of success. Pet. 71–81. In view of this, we find Petitioner has established by a preponderance of

evidence that the subject matter of claims 4–7 would have been obvious based on the combined teachings of Matsuo and Higuchi.

F. Claim 2 — Obviousness in view of Matsuo

Petitioner contends the subject matter of claim 2 would have been obvious in view of Matsuo. Pet. 37–38. Claim 2 depends from claim 1 and requires “the partial cut is made after the full cut is made.” Ex. 1001, 8:66–67. As discussed above, Petitioner contends that Matsuo discloses a first, partial cut followed by a second, full cut. Pet. 36–37; Ex. 1006 ¶¶ 87–88, Figs. 27–30. Petitioner acknowledges that Matsuo does not expressly disclose reversing the order of the partial cut and full cut so that the partial cut is made after the full cut, but Petitioner contends that there are only two options for the cutting order, and a person of ordinary skill in the art would have recognized that the order of the partial cut and full cut is a design choice, as well as a simple substitution of one known technique for another to obtain predictable results. Pet. 37–38 (citing Ex. 1003 ¶¶ 131–132). Petitioner also argues that the ’007 patent does not explain that cutting order is critical to the claimed invention. Pet. 38 (citing Ex. 1003 ¶ 134).

Patent Owner does not address Petitioner’s arguments regarding making a partial cut after a full cut. Instead, Patent Owner relies on the same arguments discussed above regarding Petitioner’s failure to demonstrate Matsuo discloses all of the limitations in claim 1, based on Patent Owner’s proposed construction of claim terms. For the reasons discussed above, we do not adopt Patent Owner’s constructions, and we have determined Petitioner has established by a preponderance of evidence that Matsuo anticipates claim 1.

We have reviewed the undisputed information and arguments Petitioner provides regarding claim 2, and agree, for the reasons set forth in

the Petition, that it would have been obvious to a person of ordinary skill in the art to choose from one of two known options for the cutting order, including making a partial cut after a full cut, and that a person of ordinary skill in the art would have had a reasonable expectation of success. Pet. 37–38. As a result, we determine Petitioner has established by a preponderance of evidence that the subject matter of claim 2 would have been obvious in view of Matsuo.

G. Petitioner’s Remaining Patentability Challenges

Having determined that Petitioner establishes by a preponderance of the evidence that Matsuo anticipates claims 1 and 3, that claims 4–7 are unpatentable as obvious in view of Matsuo and Higuchi, and that claim 2 is unpatentable as obvious in view of Matsuo, we do not address Petitioner’s additional grounds challenging claims 2 and 4. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (nonprecedential) (“We agree that the Board need not address [alternative grounds] that are not necessary to the resolution of the proceeding.”).

IV. CONCLUSION

After reviewing the complete record developed during the course of the trial, we conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that claims 1–7 of the ’007 patent are unpatentable.¹²

¹² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or*

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that Petitioner established by a preponderance of evidence that claims 1–7 of the '007 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

In summary:

Claim(s)	35 U.S.C. §	References/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 3	102	Matsuo	1, 3	
2	103	Matsuo	2	
2	103	Matsuo, Fukasawa ¹³		
4	103	Matsuo, Shibata		
4–7	103	Matsuo, Higuchi	4–7	
Overall Outcome			1–7	

Reexamination During a Pending AIA Trial Proceeding. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

¹³ As explained above, we do not reach this ground, or the ground involving Shibata, in view of our determination that Petitioner has otherwise established claims 2 and 4 are unpatentable as obvious.

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