

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2021-00254
Patent 7,495,951 B1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background and Summary*

STMicroelectronics, Inc., (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–19 (“the challenged claims”) of U.S. Patent No. 7,495,951 B1 (Ex. 1001, “the ’951 patent”). Paper 1 (“Pet.”) 4. Monterey Research, LLC (“Patent Owner”) elected not to file a Preliminary Response. Upon consideration of the Petition, we instituted *inter partes* review of all challenged claims on all grounds raised. Paper 6 (“Dec. Inst.”), 32.

Patent Owner filed a corrected Response to the Petition (Paper 13, “PO Resp.”), Petitioner filed a Reply (Paper 15, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 18, “PO Sur-Reply”). An oral hearing was held on March 16, 2022, and the hearing transcript is included in the record. *See* Paper 29 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that claims 1–19 of the ’951 patent are unpatentable.

B. *Real Parties-in-Interest*

Petitioner identifies itself, STMicroelectronics N.V., and STMicroelectronics International N.V. as the real parties-in-interest. Pet. 2. Patent Owner identifies itself and IPValue Management as real parties-in-interest. Paper 4, 1.

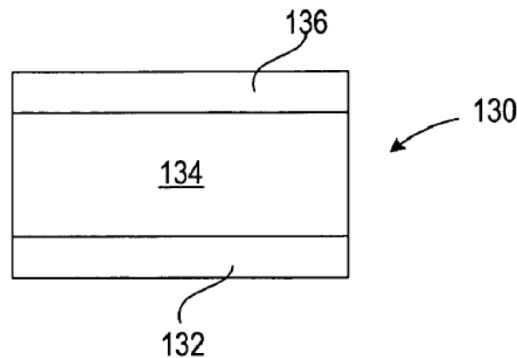
C. *Related Matters*

The parties identify *Monterey Research, LLC v. STMicroelectronics, Inc.*, No. 1:20-cv-0089 (D. Del.) as a matter that can affect or be affected by this proceeding. Pet. 2; Paper 4, 1.

D. The '951 Patent

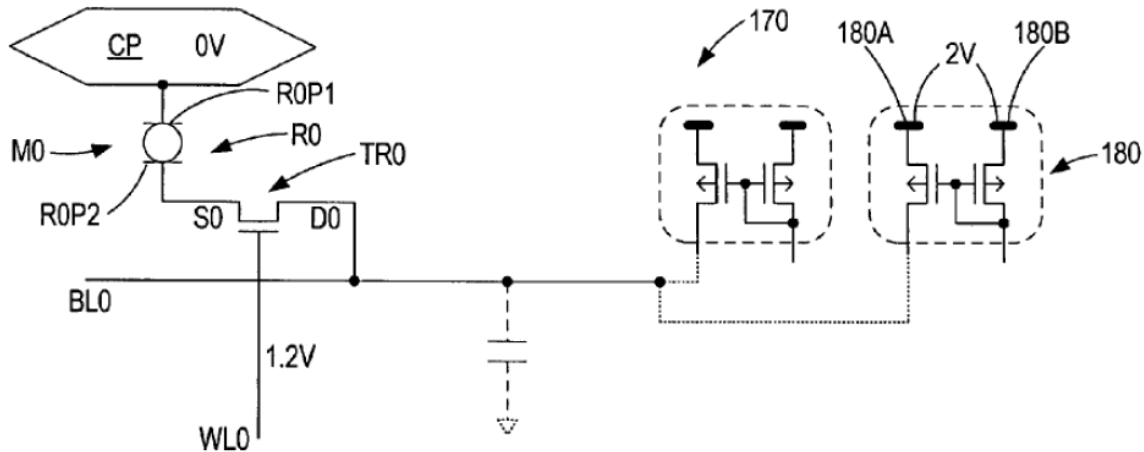
The '951 patent is directed to “a memory array which includes a plurality of resistive memory devices.” Ex. 1001, 1:7–9. A resistive memory device is a device that is “capable of adopting a low-resistance (‘programmed’) state and a high resistance (‘erased’) state by application of electrical potentials” across it. *Id.* at 1:42–44. Once programmed, applying an appropriate potential across the device allows “the level of current therethrough [to] be sensed, indicating whether the device is in its high or low resistance state (the ‘read’ step).” *Id.* at 1:45–48.

The resistive memory device described in the '951 patent is illustrated in Figure 9, which is reproduced below.



The figure above is Figure 9 of the '951 patent, which is a cross-sectional view of one embodiment of a resistive memory device. *Id.* at 2:51–53. Resistive memory device 130 includes active layer 134 (e.g., nickel oxide) sandwiched between two electrodes 132/136 (e.g., copper). *Id.* at 5:24–28.

Resistive memory device 130 is one component of a memory cell, such as the memory cell illustrated in Figure 11, which is reproduced below.



The figure above is Figure 11 of the '951 patent, which is a schematic illustration of a memory cell. *Id.* at 2:56–59. The memory cell includes resistive memory device R0 having electrode R0P1 connected to common plate CP and electrode R0P2 connected to bitline BL0 and wordline WL0 of a memory cell array through transistor TR0. *Id.* at 5:40–45, Fig. 11.

To program memory device R0, common plate CP is held at 0V, the terminals of current limiter 180 are held at 2V, and a 1.2V potential is applied to wordline WL0 to drive transistor TR0 into a conducting state. *Id.* at 5:48–52. This causes a 2V potential to appear across resistive memory device R0 from electrode R0P2 to electrode R0P1, driving R0 into a low-resistance (programmed) state. *Id.* at 5:52–60. Current limiter 180 limits the current flowing through transistor TR0 to approximately 20 μ A to avoid damaging R0. *Id.* at 5:60–63.

To erase memory device R0, common plate CP is held at 0V, the terminals of current limiter 170 are held at 1V, and a 2.5V potential is applied to wordline WL0. *Id.* at 5:64–6:4. This causes a 1V potential to appear across resistive memory device R0 from electrode R0P2 to electrode

R0P1, driving R0 into a high-resistance (erased) state. *Id.* at 5:64–6:6.¹ Current limiter 170 limits the current flowing through transistor TR0 to approximately 50 μ A to avoid damaging R0. *Id.* at 6:6–9.

E. Illustrative Claim

Claim 1 is illustrative of the challenged claims and is reproduced below.

1. A method of changing the state of a resistive memory device which is capable of adopting relatively higher and lower resistance states, the resistive memory device comprising first and second electrodes and an active layer between the first and second electrodes, the method comprising applying an electrical potential across the electrodes from higher to lower potential in a direction from one electrode to the other to change the state of the resistive memory device from one state to the other, said direction being the same as that in which said electrical potential would be applied across the electrodes to change the state of the resistive memory device from said other state to said one state.

Ex. 1001, 9:4–15.

Claims 8, 11, 14, and 17 are substantially similar to claim 1. *Id.* at 9:4–15, 9:35–48, 9:54–10:8, 10:14–29, 10:36–51. They differ from claim 1 by identifying the high/low resistance states as erased/programmed states and by reciting applying a potential to switch the memory device from (a) a programmed to an erased state (claim 8), (b) an erased to a programmed

¹ The '951 patent states that resistive memory device R0 is put into a low-resistance state when both programmed and erased. *Compare* Ex. 1001, 5:58–60 (indicating R0 is driven into a low-resistance state during programming), *with id.* at 6:4–6 (indicating R0 is driven into a low-resistance state during erasing). We interpret the column 6 disclosure to be a mistake, as does Dr. Anantram. *See* Ex. 1002 ¶ 40 n.2. Earlier, the '951 patent indicates resistive memory devices are two-state devices having “a low-resistance (‘programmed’) state and a high-resistance (‘erased’) state.” Ex. 1001, 1:42–43.

state (claim 11), and (c) an erased to a programmed and back to an erased state (claims 14 and 17). *Id.*

Claim 17 differs from claims 1, 8, 11, and 14 in two additional ways. First, claim 17 does not require a potential to be applied across the device in the same direction when switching from the erased-to-programmed and the programmed-to-erased states. *Id.* Second, claim 17 does require limiting current through the device when switching the device from the erased-to-programmed and programmed-to-erased states by means of first/second current limiting structures. *Id.*

F. Evidence²

Reference		Effective Date	Exhibit
I. G. Baek et al., <i>Highly Scalable Non-volatile Resistive Memory using Simply Binary Oxide Drive by Asymmetric Unipolar Voltage Pulses</i> , IEDM Technical Digest, IEEE International Electron Devices Meeting (Dec. 13–14, 2004) (“Baek Paper”)		Dec. 15, 2004	1003
Baek Application	US 2006/0054950 A1	Mar. 16, 2006	1004
Scheuerlein	US 2007/0008785 A1	Jan. 11, 2007	1005
Hyunjun Sim et al., <i>Resistance-Switching Characteristics of Polycrystalline Nb₂O₅ for Nonvolatile Memory Application</i> , IEEE Electron Device Letters, Vol. 26. Issue 5 (May 2, 2005) (“Sim”)		May 2, 2005	1006

G. Asserted Grounds

Petitioner asserts the challenged claims would have been unpatentable on the following grounds:

² Petitioner also relies on the Declarations of M. P. Anantram, Ph.D. (Exs. 1002, 1023) and Gerard P. Grenier (Exs. 1009, 1017). Patent Owner relies on the Declaration of Nader Bagherzadeh (Ex. 2003).

Claims	35 U.S.C. §	Reference(s)
1–16	102(b)/103(a)	Baek Paper
5, 6, 9, 10, 12, 13, 15, 16	103(a)	Baek Paper, Sim
1–16	102(e)/103(a)	Baek Application
5, 6, 9, 10, 12, 13, 15, 16	103(a)	Baek Application, Sim
17–19	102(e)/103(a)	Scheuerlein

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner identifies a person of ordinary skill in the art (“POSITA”) at the time of the invention as someone that would have had “at least a master’s degree in electrical engineering, as well as coursework in or experience with circuits and semiconductor devices, solid state physics, and materials science.” Pet. 10 (citing Ex. 1002 ¶ 30). Patent Owner adopts that definition. PO Resp. 18.

Previously, in our Institution Decision, we set forth a narrower definition for a person skilled in the art—one that required specific experience with resistive memory devices. Dec. Inst. 7. However, given the parties agreement, we adopt their agreed-to definition for purposes of this decision. In doing so, we note that our analysis below would not differ under either definition. *Id.*

B. Claim Construction

Claims in an *inter partes* review are interpreted “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2020). Under that standard, the “words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citation omitted). “There are only two

exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution.” *Hill-Rom Services, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014) (internal citation omitted). “The standards for finding lexicography and disavowal are exacting.” *Id.* Consequently, although we may “look to the specification and prosecution history to interpret what a patentee meant by a word or phrase in a claim,” we may not read “extraneous limitations . . . into the claims” absent an express definition or clear disavowal of claim scope. *Bayer AG v. Biovail Corp.*, 279 F.3d 1340, 1348 (Fed. Cir. 2002). Finally, only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

1. Selecting a level of current limit

In our Institution Decision, we preliminarily construed the term “selecting a level of current limit” to mean “selecting . . . one or more levels of current limit.” Dec. Inst. 8. This is the meaning Petitioner ascribed to the term in the Petition. Pet. 32. Patent Owner accepts our preliminary construction for purposes of this proceeding. PO Resp. 19. We maintain that construction here.

2. first/second current limiting structures

Claim 17 recites different limitations for programming [erasing] a resistive memory device by “limiting current through the resistive memory device by means of a first [second] current limiting structure to change the resistive memory device from the erased [programmed] . . . state to the programmed [erased] . . . state.” Ex. 1001, 10:41–51.

In our Institution Decision, we found these limitations were means-plus-function limitations requiring construction under 35 U.S.C. § 112 ¶ 6. Dec. Inst. 9–11. We did so because they recite the term “means” and do not recite sufficient structure to overcome the presumption that § 112 ¶ 6 applies because the structures they do recite (i.e., first/second “current limiting structures”) are nonce terms that do not correspond to definite structures. *Id.* at 9–10 (quoting *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348, 1350 (Fed. Cir. 2015)). We further found the Specification linked several structures to the function performed by the “means” recited in these limitations, including current mirrors 110/120 and 170/180 shown in Figures 5/6 and 11/12, respectively. *Id.* at 10 (citing Ex. 1001, 3:58–61, 4:6–11, 4:20–24, 5:45–48, 6:4–9, 6:14–20, Figs. 5, 6, 11, 12). Therefore, we preliminarily construed these limitations to require “first/second current mirrors (and equivalents thereof) that limit the current through the resistive memory device when a potential is applied to switch the device from its programmed-to-erased and erased-to-programmed states.” *Id.* at 10–11.

Our construction is consistent with Petitioner’s proposed construction of this term, and Petitioner does not dispute it. Pet. 10–12; Pet. Reply 1–31. For purposes of this proceeding, Patent Owner does not dispute that these limitations should be construed as means-plus-function limitations. PO Resp. 19–20. However, Patent Owner argues that because the Specification consistently identifies elements 110/120 and 170/180 as current sources/limiters and occasionally as current mirrors, we should construe them as current sources/limiters/mirrors rather than as current mirrors.³ *Id.*

³ Patent Owner includes current mirrors 160 (Fig. 8) and 220 (Fig. 14) in its analysis. PO Resp. 19. We exclude these structures, however, because they limit current to read the resistance state of the memory device rather than to

We disagree. The Specification discloses “current source/limiters” 110, 170, and 180 include “p channel transistors connected as a current mirror,” and “current source/limiter 120” includes “n channel transistors connected as a current mirror.” Ex. 1001, 3:58–61, 5:45–48, 6:14–20. Although the Specification later refers to each of these devices as simply “current source/limiters,” the only tangible “current source/limiters” disclosed in the Specification are current mirrors.

Accordingly, for the reasons discussed above, we maintain our preliminary construction of the first/second current limiting structure limitations to mean “first/second current mirrors (and equivalents thereof) that limit the current through the resistive memory device when a potential is applied to switch the device from its programmed-to-erased and erased-to-programmed states.”

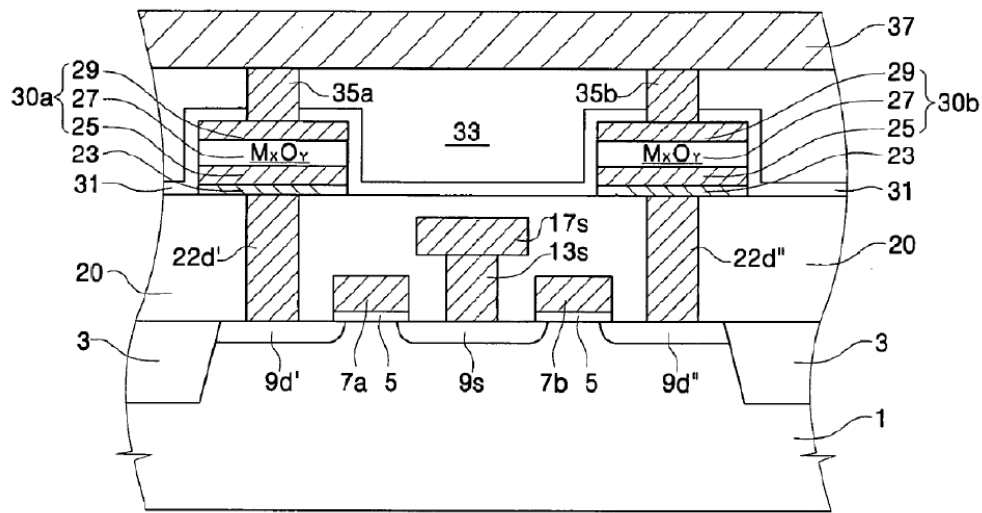
C. Challenges Based on the Baek Application

Petitioner argues claims 1–16 are unpatentable as anticipated by or obvious over the Baek Application. Pet. 44–60; Pet. Reply 19–26. Patent Owner disagrees. PO Resp. 47–57; PO Sur-Reply 17–20. For the reasons discussed below, we find Petitioner has shown by a preponderance of evidence that claims 1–16 are unpatentable over the Baek Application.

1. Baek Application

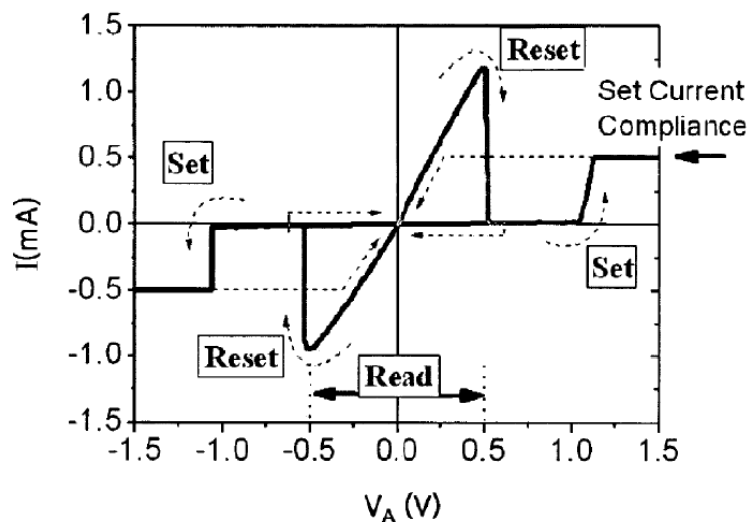
The Baek Application discloses a “non-volatile memory cell[] compris[ing] an insulating layer formed on a semiconductor substrate and lower and upper electrodes formed on the insulating layer.” Ex. 1004 ¶ 6. The memory cell is illustrated in Figure 1, which is reproduced below.

change it “from the erased [programmed] . . . state to the programmed [erased] . . . state” as required by claim 17. *Compare* Ex. 1001, 4:52–61 and 6:53–61, *with id.* at 10:41–51.



The figure above is Figure 1 of the Baek Application, which is a “cross-sectional view illustrating resistance RAM [random access memory] cells.” *Id.* ¶ 16. The RAM cells include first/second data storage elements 30a/30b that each include lower electrode 25, transition metal oxide 27, and upper electrode 29. *Id.* ¶ 27. The metal in the transition metal oxide can be nickel, cobalt, zinc, copper, hafnium, zirconium, titanium, or chromium. *Id.* ¶¶ 30–31.

The I-V or current-voltage characteristics of data storage elements 30a/30b are illustrated in Figure 9, which is reproduced below.



The figure above is Figure 9 of the Baek Application, which is a “graph illustrating a switching characteristic (I-V curve) of a data storage element that employs a nickel oxide layer.” *Id.* ¶ 64. The horizontal axis in Figure 9 “indicates a voltage V_A between the upper and lower electrodes of the data storage element,” and the vertical axis “indicates a current I that flows through the nickel oxide (Ni_xO_x) layer.” *Id.*

The Baek Application discloses that “when the voltage V_A between the upper and lower electrodes was about 0.5 V, the nickel oxide (Ni_xO_x) layer was switched to a reset state having a high resistance.” *Id.* ¶ 65. This reset state is depicted in Figure 9 as the horizontal line having a current of 0.0 mA. Conversely, “when the voltage V_A between the upper and lower electrodes was about 1.1 V, the nickel oxide (Ni_xO_x) layer was switched to a set state having a low resistance.” *Id.* The set state is depicted in Figure 9 as the tilted line with an approximate 45° slope between -0.5 V and + 0.5V. The Baek Application further discloses that “[a] maximum allowable current (current compliance) was set to about 0.5 mA during application of the voltage V_A in order to convert the nickel oxide (Ni_xO_x) layer to the set state.” *Id.* This was done “to prevent the nickel oxide (Ni_xO_x) layer from being damaged when a large amount of current flows through the nickel oxide (Ni_xO_x) layer.” *Id.*

2. Claims 1, 7, 8, 11, and 14

Claim 1 recites “[a] method of changing the state of a resistive memory device which is capable of adopting relatively higher and lower resistance states, the resistive memory device comprising first and second electrodes and an active layer between the first and second electrodes.” Ex. 1001, 9:4–8. Petitioner demonstrates how the Baek Application discloses these limitations. *See* Pet. 45–47 (quoting/citing Ex. 1004 ¶¶ 4, 6,

27, 41, Figs. 1, 9, 10). The Baek Application discloses a non-volatile memory cell having upper and lower electrodes and a “transition metal oxide layer . . . interposed between the lower and upper electrodes.” Ex. 1004 ¶¶ 6, 27, Fig. 1. The device can be in one of two resistance states, a “set state (low resistance)” and a “reset state (high resistance).” *Id.* ¶ 41. Patent Owner does not dispute this. PO Resp. 47–57; PO Sur-Reply 17–20.

Claim 1 further requires “applying an electrical potential across the electrodes from higher to lower potential in a direction from one electrode to the other to change the state of the resistive memory device from one state to the other.” Ex. 1001, 9:8–12. Petitioner demonstrates how the Baek Application discloses this limitation. *See* Pet. 47–49 (quoting/citing Ex. 1004 ¶¶ 4, 38–39, 64–65, Fig. 9; Ex. 1002 ¶¶ 153–156, 165). The Baek Application discloses that “when the voltage V_A between the upper and lower electrodes was about 0.5 V, the nickel oxide (Ni_xO_y) layer was switched to a reset state having a high resistance.” Ex. 1004 ¶ 65. Patent Owner does not dispute this. PO Resp. 47–57; PO Sur-Reply 17–20.

Lastly, claim 1 requires applying the electrical potential in the same direction across the electrodes “to change the state of the resistive memory device from said other state to said one state.” Ex. 1001, 9:12–15. Notwithstanding Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how the Baek Application discloses this limitation. *See* Pet. 49–52 (quoting/citing Ex. 1004 ¶ 65, Fig. 9; Ex. 1002 ¶ 157). The Baek Application discloses that “when the voltage V_A between the upper and lower electrodes was about 1.1 V, the nickel oxide (Ni_xO_y) layer was switched to a set state having a low resistance.” Ex. 1004 ¶ 65.

Patent Owner argues “Petitioner failed to show that the Baek Application discloses the claimed ‘said direction’ was the same direction, as

required by claim 1.” PO Resp. 48 (citing Ex. 2003 ¶ 132). That is, Patent Owner argues Petitioner has failed to show that the voltages applied in the set and reset operations have the same polarity so that they are applied “from higher to lower potential” across the same “one electrode to the other.” Ex. 1001, 9:8–15. Patent Owner argues “the Petition never identifies which of the two electrodes in the Baek Application represents a first electrode and which of the two electrodes represents a second electrode[]” and never identifies which of the two electrodes “receives an applied electrical potential.” PO Resp. 49. Therefore, Patent Owner contends, “Petitioner failed to show a direction of the first electrical potential, that such a direction was from a higher potential electrode to a lower potential electrode, or that the electrical potential is applied in the same direction from one electrode to the other.” *Id.* (citing Ex. 2003 ¶ 134) (emphasis omitted).

Petitioner replies that Figure 1 of the Baek Application discloses “a resistive memory device with an active layer between ‘upper’ and ‘lower’ electrodes.” Pet. Reply 19 (citing Ex. 1004 ¶ 6, Fig. 1). Petitioner argues these electrodes “suffice to disclose the claimed [first/second] electrodes” because claim 1 “make[s] no substantive distinction between the two.” *Id.* at 20–21. Petitioner further argues “there are only two ways that current can flow across [Baek’s] electrodes—either from the upper electrode to the lower electrode, or vice versa” and when current flows in either direction “the electrical potential would be applied from higher to lower potential” across the electrodes. *Id.* at 21 (citing Ex. 1023 ¶ 55). Petitioner further argues Figure 9 of the Baek Application teaches “applying current in the same direction—switching from set to reset, and from reset to set, both occurring with positive polarity of applied electrical potential.” *Id.* at 23 (citing Ex. 1023 ¶¶ 55–56, 59).

Patent Owner replies that, by failing to identify which of Baek's electrodes is the first or second electrode, Petitioner "essentially writes 'first and second electrodes' out of the claims." PO Sur-Reply 18. Patent Owner further argues that "the claimed starting point matters," "[t]he claimed direction matters," and "a starting point must be identified, in relation to a directionality, in order to show the claimed 'applying an electrical potential across the electrodes from higher to lower potential in a direction from one electrode to the other.'" *Id.* (emphasis omitted).

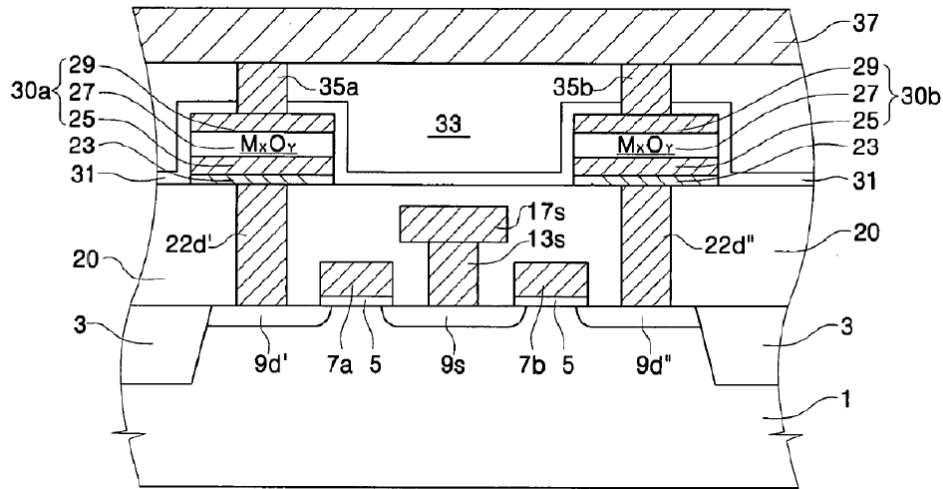
We find Petitioner has demonstrated the Baek Application discloses changing the state of a resistive memory device from one state to the other and back again by applying an electrical potential across two electrodes in the same direction for both changes-of-state. First, we note that claim 1 requires an active layer between first and second electrodes, but doesn't require any spatial relationship (e.g., above/below or left/right) between the first and second electrodes. Ex. 1001, 9:6–8. Thus, Petitioner's identification of the "upper" and "lower" electrodes in Figure 1 demonstrates that the Baek Application discloses the recited first and second electrodes. Pet. 46–47 (citing Ex. 1004 ¶ 6, Fig. 1).

Second, although claim 1 requires applying a potential "from higher to lower potential in a direction from one electrode to the other" to change the resistive state from "one state to another" and to apply a potential in the same direction to change the resistive state "from said other state to said one state," it doesn't require the "one electrode" to be either the first or second electrode. Ex. 1001, 9:8–15. Thus, the higher potential can be applied to either electrode, i.e., to either the upper or lower electrodes in the Baek Application. The only limitation required by claim 1 is that the higher

potential is applied to the same electrode when the device is switched from one state to another and back again.

Petitioner demonstrates how the Baek Application discloses these limitations by applying a higher potential to the upper electrode of a resistive memory device in order to switch the device from a low resistance set state (one state) to a high resistance reset state (another state) and to switch the device back to the set state. *See* Pet. 48–49 (citing Ex. 1004 ¶¶ 38, 65, Fig. 9; Ex. 1002 ¶¶ 156–157). The Baek Application discloses “when the voltage V_A between the upper and lower electrodes was about 0.5 V, the nickel oxide (Ni_xO_y) layer was switched to a reset state having a high resistance” and “when the voltage V_A between the upper and lower electrodes was about 1.1 V, the nickel oxide (Ni_xO_y) layer was switched to a set state having a low resistance.” Ex. 1004 ¶ 65. Thus, a higher positive potential of 1.1 V or 0.5 V is applied to the upper electrode (one electrode) than to the lower electrode (other electrode) to switch the resistive memory device to the low resistance state (one state) and to switch it back to the high resistance state (other state). As Dr. Anantram explains, the voltages applied in the set (1.1 V) and reset (0.5 V) operations are applied to the upper electrode of the Baek Application’s resistive memory device because they are “applied to the bit line 37 in Figure 1 (connected to the top electrode) while the bottom electrode is kept at a lower potential by turning on the first access transistor (by enabling first word line 7a) and grounding the source line 17s.” Ex. 1002 ¶ 156.

Figure 1 of the Baek Application is reproduced below.



The figure above is Figure 1 of the Baek Application, which is a cross-sectional illustration of “a pair of resistance RAM [memory] cells.”

Ex. 1004 ¶ 25, Fig. 1. The device includes a first access transistor consisting of drain 9d', source 9s, and gate 7a over a channel region, where gate 7a acts as a first word line. *Id.* Source 9s is connected to common source line 17s.

Id. ¶ 26. Drain 9d' is connected to contact 22d', which is connected to resistive storage element 30a via its lower electrode 25. *Id.* ¶¶ 26–27.

Storage element 30a is connected to bit line 37 via its upper electrode 29 and contact 35a. *Id.* ¶¶ 27, 37. To set or reset resistive storage element 30a, the Baek Application discloses “common source line 17s is grounded and the first access transistor is selectively turned on” by applying a word line voltage “to the first word line 7a” and “a reset voltage or a set voltage is applied to the bit line 37 while the first access transistor is turned on.” *Id.*

¶ 38. Thus, when the first access transistor is on, a set (1.1 V) or reset (0.5 V) voltage is applied to upper electrode 29 via bit line 37 and contact 35a, and 0 V is applied to lower electrode 25, which is grounded through the first access transistor to grounded source line 17s. We agree with and credit

Dr. Anantrum’s testimony that this means an electrical potential is “applied across the electrodes from higher potential (set/reset voltage) to lower potential (ground) in a direction from one electrode (the top electrode) to the other (bottom electrode).” Ex. 1002 ¶ 156.

Claim 7 depends from claim 1 and further requires the higher resistance state to be an erased state and the lower resistance state to be a programmed state. Ex. 1001, 9:32–34. Petitioner demonstrates how the Baek Application discloses this limitation. Pet. 56–58 (quoting/citing Ex. 1004 ¶¶ 39–40, 65; Ex. 1002 ¶ 166). The Baek Application teaches “a set state having a low resistance” and “a reset state having a high resistance.” Ex. 1004 ¶ 65. According to Dr. Anantram, a person skilled in the art would have known that the “set” or low resistance state was a “programmed” state corresponding to a logical value of “1” and the “reset” or high resistance state was an “erased” state corresponding to a logical value of “0.” Ex. 1002 ¶ 166 (citing Ex. 1005 ¶ 46). Dr. Anantram’s testimony is supported by the evidence of record. For example, Scheuerlein discloses that it is both “arbitrary which resistance state corresponds to a data 0 or a data 1” and convenient to say “a programmed memory cell has been ‘set’ to its low resistance state, and an erased memory cell has been ‘reset’ to its high-resistance state.” Ex. 1005 ¶ 46. Thus, Petitioner shows sufficiently that the Baek Application’s low resistance set state is a programmed state and its high resistance reset state is an erased state.

Claims 8, 11, and 14 are substantially similar to claim 1. *Compare* Ex. 1001, 9:4–15 (claim 1), *with id.* at 9:35–48 (claim 8), 9:54–10:8 (claim 11), *and* 10:14–29 (claim 14); *see also* § I.E., *supra*. Claims 8, 11, and 14 are even more similar to claim 7, which requires the high/low resistance states of claim 1 to be erased/programmed states. *Compare*

Ex. 1001, 9:4–15 (claim 1) and 9:32–34 (claim 7), *with id.* at 9:35–48 (claim 8), 9:54–10:8 (claim 11), and 10:14–29 (claim 14). As a result, Petitioner’s analyses of claims 8, 11, and 14 rely on and incorporate Petitioner’s analyses of claims 1 and 7. Pet. 58–59. Patent Owner does not specifically challenge Petitioner’s analyses of claims 8, 11, and 14. PO Resp. 47–53; PO Sur-Reply 17–18. We find Petitioner has demonstrated how the Baek Application discloses all of the limitations of claims 8, 11, and 14 for the reasons discussed above with respect to claims 1 and 7.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that the Baek Application discloses all of the limitations of claims 1, 7, 8, 11, and 14. Consequently, Petitioner demonstrates by a preponderance of evidence that claims 1, 7, 8, 11, and 14 are unpatentable as anticipated by the Baek Application. Moreover, because “a disclosure that anticipates under § 102 also renders the claim[s] [obvious] under § 103,” Petitioner demonstrates by a preponderance of evidence that these claims are unpatentable as obvious over the Baek Application.

Realtime Data, LLC v. Iancu, 912 F.3d 1368, 1373 (Fed. Cir. 2019).

3. Claims 2–4

Claim 2 depends from claim 1, and further requires the active layer to be “on and in contact with the first electrode” and the second electrode to be “on and in contact with the active layer.” Ex. 1001, 9:16–18. Claim 3 depends from claim 1, and further requires the active layer to comprise metal oxide. *Id.* at 9:19–20. Claim 4 depends from claim 1, and further requires the active layer to be “selected from the group consisting of nickel oxide, copper oxide, titanium oxide, tantalum oxide, aluminum-tantalum oxide, strontium-tantalum oxide, zirconium oxide, and cobalt oxide.” *Id.* at 9:21–25.

Petitioner demonstrates how the Baek Application discloses these limitations. Pet. 51–53 (citing Ex. 1004 ¶¶ 6, 27, 30–31, code (54), Fig. 1; Ex. 1002 ¶¶ 159–161). The Baek Application discloses resistive memory device 30a consists of “a lower electrode 25, a transition metal oxide layer pattern 27 and an upper electrode 29 . . . [that] are sequentially stacked.” Ex. 1004 ¶ 27, Fig. 1; *see also id.* ¶ 11 (“A transition metal oxide layer is formed on the lower electrode layer. . . . An upper electrode layer is formed on the transition metal oxide layer”). The Baek Application further discloses the TMO layer can be an oxide of nickel, copper, titanium, zirconium, or cobalt, any one of which is sufficient to meet the metal oxide limitation of claim 3 and the Markush group limitation of claim 4. *Id.* ¶¶ 30, 31. Patent Owner does not dispute this. PO Resp. 47–57; PO Sur-Reply 17–18.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that the Baek Application discloses all the limitation of claims 2–4. Petitioner, therefore, demonstrates by a preponderance of evidence that claims 2–4 are unpatentable as anticipated by the Baek Application as well as obvious over it. *See Realtime Data*, 912 F.3d at 1373 (“a disclosure that anticipates under § 102 also renders the claim[s] [obvious] under § 103”).

4. Claims 5, 6, 9, 10, 12, 13, 15, and 16

Claim 5 depends from claim 1, and further requires “selecting a level of current limit through the resistive memory device.” Ex. 1001, 9:26–28. As discussed in § II.B.1, *supra*, “selecting a level of current limit” requires selecting one or more levels of current limit, i.e., a current limit for erased-to-programmed switching, programmed-to-erased switching, or both.

Claim 6 depends from claim 5, and further requires “limiting current through the resistive memory device to the selected level.” *Id.* at 9:29–31.

Notwithstanding Patent Owner’s arguments to the contrary, Petitioner demonstrates how the Baek Application discloses the limitations of claims 5 and 6. Pet. 53–57 (citing Ex. 1004 ¶ 65, Fig. 9; Ex. 1002 ¶¶ 162, 165). The Baek Application discloses that when its resistive memory device is programmed to be in the “set” state, “[a] maximum allowable current (current compliance) was set to about 0.5 mA during application of the [set] voltage V_A .” Ex. 1004 ¶ 65. This is shown in Figure 9 of the Baek Application where the current is limited to the “set current compliance” limit of 0.5 mA when a “set” voltage of 1.1 V is applied to the resistive memory device. *Id.*, Fig. 9.

Patent Owner argues⁴ the Baek Application does not disclose “selecting a current limit” because “a current compliance is not a current limit.” PO Resp. 53–54 (citing Ex. 2003 ¶ 143); *see also id.* at 35 (citing Ex. 2003 ¶ 107) (“the Baek Paper never defines current compliance as a limit”), 43 (citing Ex. 2003 ¶ 120) (“A current compliance level is not a current limit.”); PO Sur-Reply 12, 19–20 (same). We disagree.

The Baek Application discloses that when the device is in the high resistance “reset” state and a sufficiently high voltage V_A (e.g., 1.1 V) is applied to switch it to the low resistance “set” state:

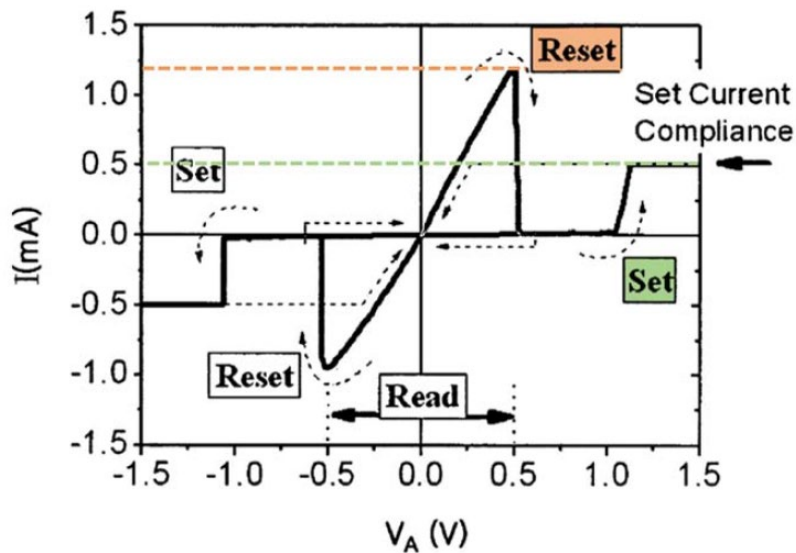
[a] maximum allowable current (current compliance) was set to about 0.5 mA during application of the voltage V_A in order to convert the nickel oxide (Ni_xO_y) layer to the set state. This

⁴ Although Patent Owner makes this argument against finding claims 5 and 6 obvious over the Baek Application, we consider it here because it is relevant to the issue of whether claims 5 and 6 are anticipated by the Baek Application.

limit is applied to prevent the nickel oxide (Ni_xO_y) layer from being damaged when a large amount of current flows through the nickel oxide (Ni_xO_y) layer having the set [low resistance] state.

Ex. 1004 ¶ 65 (emphasis added). Thus, contrary to Patent Owner’s contention, the Baek Application expressly identifies the current compliance value as a current limit or maximum allowable current. Indeed, the Baek Application sets and applies this current limit for the same reasons disclosed in the ’951 patent—to prevent damage to the resistive memory device. *See* Ex. 1001, 1:65–67 (“applying an electrical potential across the electrodes and limiting current through the resistive memory device”), 5:16–21 (“the applied voltages and current limits are carefully selected . . . with it being insured that there are no high currents which could cause damage to the memory cell”).

Petitioner illustrates how the Baek Application applies a “current limit” or “current compliance” in an annotated and colorized version of Figure 9, which is reproduced below. Pet. 54 (citing Ex. 1002 ¶ 162).



The figure above is a Petitioner annotated and colorized version of Figure 9 of the Baek Application. *Id.* It discloses the I-V or current-voltage characteristic of the disclosed resistive memory device. Ex. 1004 ¶ 64.

When the device is in the high resistance “reset” state (horizontal line at 0 mA current between -1 V and +1 V) and the voltage across the device is increased beyond about 1 V, the current begins to increase with increasing voltage. However, when the voltage across the device reaches and exceeds the 1.1 V “set” voltage (green), the current stops increasing with increasing voltage. Instead, it is limited to a “set current compliance” or maximum current of 0.5 mA (green dashed line). *See* Ex. 1002 ¶ 162 (Dr. Anantram explaining annotated and colorized Figure 9).

Patent Owner’s expert, Dr. Bagherzadeh, does not provide a credible alternative explanation for the I-V characteristic shown in Figure 9 of the Baek Application. Instead, Dr. Bagherzadeh declares, without supporting evidence or explanation, that “the Baek Paper never defines current compliance as a limit” and “[a] current compliance level is not a current limit.” Ex. 2002 ¶¶ 107, 120, 143. This testimony is not credible. It is contradicted by the express teachings of the Baek Application, which describes the current compliance as “[a] maximum allowable current” and a “limit [that] is applied” to prevent damage to the resistive memory device. Ex. 1004 ¶ 65.

Claims 9, 12, and 15 depend from claims 8, 11, and 14, respectively, and limit claims 8, 11, and 14 in the same way claim 5 limits claim 1, i.e., by requiring “selecting a level of current limit through the resistive memory device.” Ex. 1001, 9:49–50, 10:9–10, 10:30–32. Claims 10, 13, and 16 depend from claims 9, 12, and 15, respectively, and limit claims 9, 12, and 15 in the same way claim 6 limits claim 5, i.e., by “limiting current

through the resistive memory device to the selected level.” *Id.* at 9:51–53, 10:11–13, 10:33–35. Petitioner’s analyses of claims 9, 10, 12, 13, 15, and 16 rely on and incorporate Petitioner’s analyses of claims 1, 5, 6, 8, 11, and 14. Pet. 59–60. Patent Owner argues Petitioner fails to demonstrate the unpatentability of claims 9, 10, 12, 13, 15, and 16 for the reasons discussed above, i.e., that the Baek Application’s disclosure of selecting and applying a “set current compliance” fails to disclose selecting and applying a “level of current limit.” PO Resp. 35, 43, 53–54; PO Sur-Reply 12, 19–20. We disagree for the reasons discussed above with respect to claims 5 and 6.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that the Baek Application discloses all the limitations of claims 5, 6, 9, 10, 12, 13, 15, and 16, and therefore demonstrates by a preponderance of evidence that these claims are unpatentable as anticipated by the Baek Application as well as obvious over it. *See Realtime Data* 912 F.3d at 1373 (“a disclosure that anticipates under § 102 also renders the claim[s] [obvious] under § 103”).

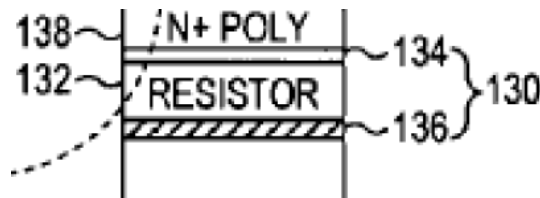
D. Challenges Based on Scheuerlein

Petitioner argues claims 17–19 are unpatentable as anticipated by or obvious over Scheuerlein. Pet. 63–73; Pet. Reply 28–31. Patent Owner disagrees. PO Resp. 61–66; PO Sur-Reply 23–26. For the reasons discussed below, we find Petitioner has demonstrated by a preponderance of evidence that claims 17–19 are unpatentable as anticipated by or obvious over Scheuerlein.

1. Scheuerlein

Scheuerlein discloses “a method for programming a memory array of nonvolatile memory cells having switchable resistor memory elements.”

Ex. 1005 ¶ 8. Scheuerlein's switchable resistor memory elements are shown in Figure 1, a portion of which is reproduced below.



The figure above shows the structure of Scheuerlein's resistor memory element 130, which "includes a chalcogenide layer 132 located between two electrodes 134, 136." *Id.* ¶¶ 37–38, Fig. 1.

The current-voltage or I-V characteristics of resistor memory element 130 is shown in Figure 3 of Scheuerlein, which is reproduced below.

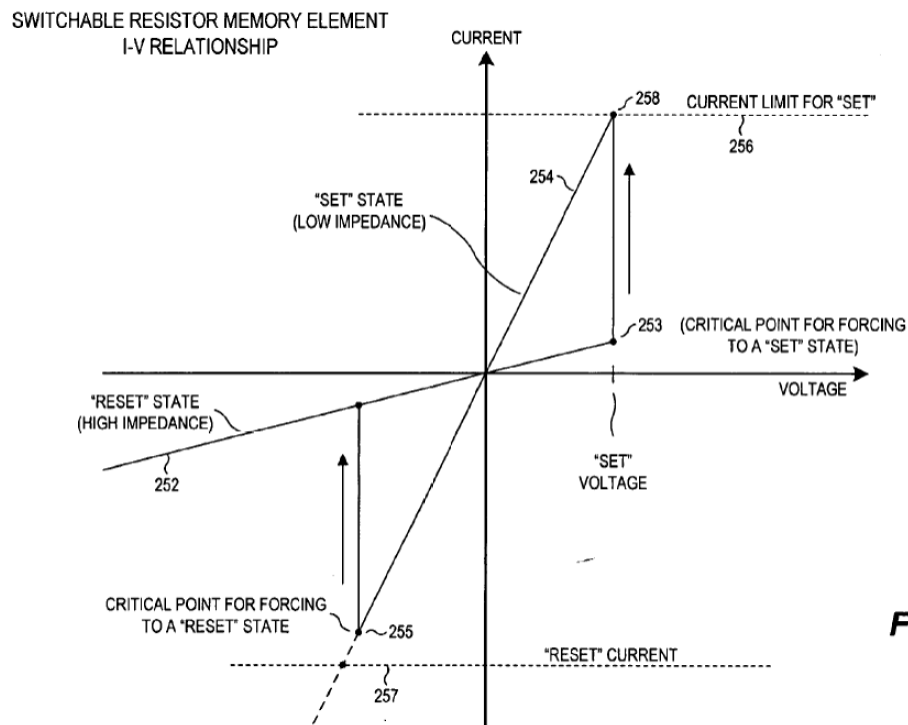
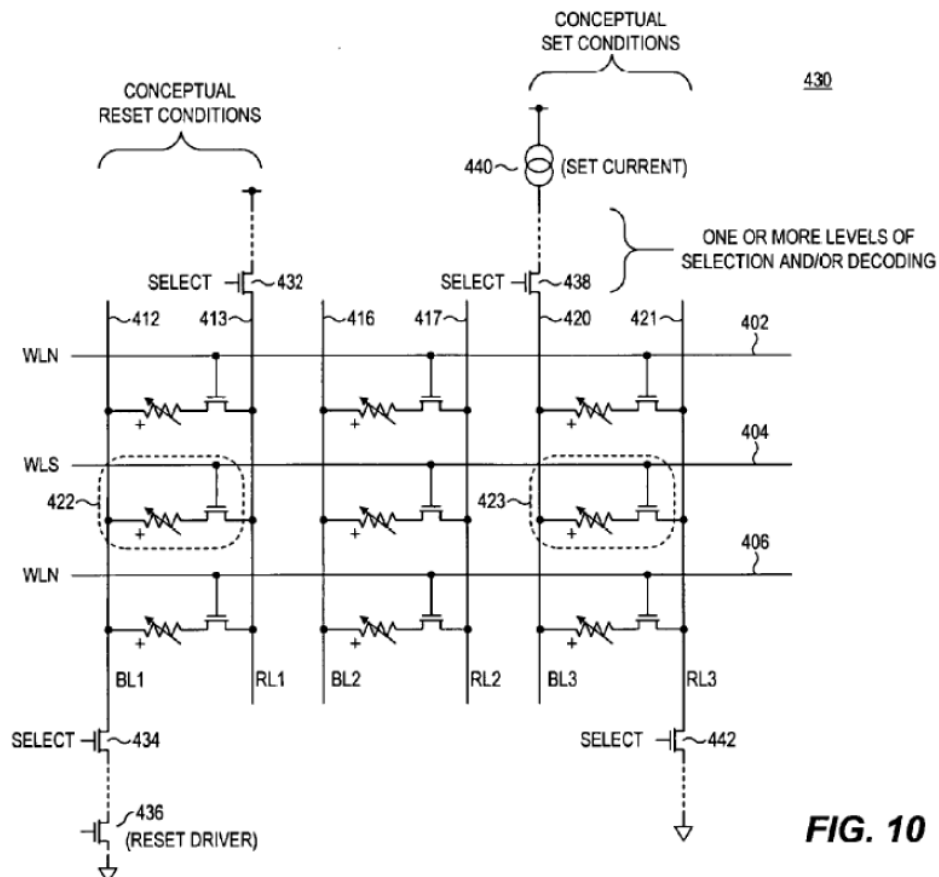


FIG. 3

The figure above shows the current-voltage relationship of Scheuerlein's resistor memory element 130. *Id.* ¶ 18, Fig. 3. Memory element 130 is in a high resistance state when its I-V characteristic follows (shallow slope) line 252 and is in a low resistance state when its I-V characteristic follows

(steep slope) line 254. *Id.* ¶ 43. To program memory element 130, Scheuerlein switches from high resistance state 252 to low-resistance state 254 by applying “set” voltage 253 while limiting the current flowing through memory element 130 to current limit 256. *Id.* ¶¶ 43, 48. To erase memory element 130, Scheuerlein switches from low-resistance state 254 to high resistance state 252 by applying “reset” voltage 255 while supplying sufficient (minimum) reset current 257. *Id.* ¶¶ 44, 49.

Circuits for switching Scheuerlein’s resistor memory elements between low and high resistance states are illustrated in various Figures, including Figure 10, which is reproduced below.



The figure above shows an array of resistor memory elements (e.g., elements 422, 423) and circuitry to program/erase (set/reset) them. *Id.* ¶ 84, Fig. 10.

For example, to “set” resistive memory element 423, Scheuerlein biases “data line 420 . . . at VDD through a current limiting circuit 440 (configured to limit current flow into the data line to the magnitude of the desired set current), while the reference line 421 is driven to ground through a select device 442.” *Id.* ¶ 86. To “reset” resistive memory element 422, Scheuerlein biases “data line 412 . . . at ground by a reset driver 436 . . . while the associated reference line 413 is driven to VDD through a select device 432” in order to supply “sufficient current to exceed the reset voltage across the resistor element.” *Id.* ¶ 87. Reset driver 436 is a “current providing circuit.” *Id.* ¶ 90. Scheuerlein describes the current sources and current limiting circuits that program/erase (set/reset) resistive memory elements 422/423 as circuits that provide “a constant current irrespective of the voltage impressed across the device. Examples include a current mirror circuit.” *Id.* ¶ 121.

2. Claim 17

Claim 17 recites “[a] method of changing the state of a resistive memory device which is capable of adopting an erased, relatively higher resistance state and a programmed, relatively lower resistance state, the resistive memory device comprising first and second electrodes and an active layer between the first and second electrodes.” Ex. 1001, 10:36–41.

Petitioner demonstrates how Scheuerlein discloses these limitations. Pet. 64–65 (quoting/citing Ex. 1005 ¶¶ 6, 33, 36, 38, 43–44, 46, Fig. 1); Pet. Reply 28–31. Scheuerlein discloses a “switchable resistor memory element 130 [that] includes a chalcogenide layer 132 located between two electrodes 134, 136.” Ex. 1005 ¶ 38, Fig. 1. A “set” voltage can be applied to “cause[] the switchable resistor memory element to change from a high resistance state . . . to a low-resistance state” and a “reset” voltage can be

applied to “change the switchable resistor memory element back to its high resistance state,” i.e., “to change it from the low resistance [state] to the high resistance [state].” *Id.* ¶¶ 43–44. Patent Owner does not dispute this. PO Resp. 61–66; PO Sur-Reply 23–26.

Claim 17 further requires “applying an electrical potential across the electrodes and limiting current through the resistive memory device by means of a first current limiting structure to change the resistive memory device from the erased, higher resistance state to the programmed, lower resistance state.” Ex. 1001, 10:41–46. As discussed above, this limitation requires a first current mirror (and equivalents thereof) that limits the current through the resistive memory device when the device is switched from its erased to its programmed state. *See* § II.B.2, *supra*. Petitioner demonstrates how Scheuerlein discloses this limitation by disclosing current limiting structures 306, 440, and 452. Pet. 65–68 (quoting/citing Ex. 1005 ¶¶ 32, 43, 46, 48, 53, 86, 97, 99, 121, Figs. 3, 4, 10, 11); Pet. Reply 28–31.

Scheuerlein discloses switching memory element 130 from high resistance state 252 to low-resistance state 254 by applying “set” voltage 253 while limiting the current flowing through memory element 130 to current limit 256. Ex. 1005 ¶¶ 43, 48, Fig. 3. Scheuerlein uses “current limiting circuits” 306, 440, and 452 to “set” memory devices to a high resistance state. *Id.* ¶¶ 53, 86, 97, Figs. 4, 10, 11. For example, to “set” memory element 423 in Figure 10, Scheuerlein biases “data line 420 . . . at VDD through a *current limiting circuit* 440 (configured to limit current flow into the data line to the magnitude of the desired set current), while the reference line 421 is driven to ground through a select device 442.” *Id.* ¶ 86, Fig. 10 (emphasis added). Scheuerlein discloses that “[a] ‘current limiting circuit’ may also be thought of as . . . a constant current source” and that examples

of constant current sources “include a current mirror circuit.” *Id.* ¶ 121. Thus, each of current limiting circuits 306, 440, and 452 is a “current mirror” that is “set to provide a current equal to the set current limit 256” when a potential is applied to switch the resistive memory device from its erased to its programmed state. *Id.* ¶ 53, Figs. 3, 4. Patent Owner does not dispute this. PO Resp. 61–66; PO Sur-Reply 23–26.

Lastly, claim 17 requires “applying an electrical potential across the electrodes and limiting current through the resistive memory device by means of a second current limiting structure to change the resistive memory device from the programmed, lower resistance state to the erased, higher resistance state.” Ex. 1001, 10:46–51. As discussed above, this limitation requires a second current mirror (and equivalents thereof) that limits the current through the resistive memory device when the device is switched from its programmed to its erased state. *See* § II.B.2, *supra*.

Petitioner asserts Scheuerlein teaches or discloses these limitations. Pet. 68–72 (quoting/citing Ex. 1005 ¶¶ 32, 44, 54, 87, 90, 97, 121, Figs. 3, 4, 10, 11; Ex. 1002 ¶¶ 214, 216–218, 220–222); Pet. Reply 28–31. Petitioner argues Scheuerlein’s reset drivers 308, 436, and 454⁵ are “current providing circuits” that supply current to cause a reset that is “equal to the reset current 257.” Pet. 68–69 (citing/quoting Ex. 1005 ¶¶ 54, 87, 90, 97, Figs. 4, 10, 11; Ex. 1002 ¶ 216); Pet. Reply 30. Petitioner argues the reset drivers are current limiting because “setting current equal to that [reset current] level provides an upper boundary on the current.” Pet. 69 (citing Ex. 1002 ¶ 217). Petitioner further argues the reset drivers are “current mirrors” because

⁵ Petitioner mistakenly identifies the reset driver in Figure 11 as element 452. However, the reset driver in that Figure is element 454. Ex. 1005 ¶ 97, Fig. 11. We correct that mistake here.

Scheuerlein teaches that current mirrors are constant current sources. *Id.* at 70–71 (citing Ex. 1005 ¶ 121; Ex. 1002 ¶ 218); Pet. Reply 30. Petitioner further argues that to the extent Scheuerlein does not describe reset drivers 308, 436, and 454 as current mirrors, a person skilled in the art would have found it obvious to implement them as current mirrors because “a current mirror provides a constant current” and “using a current mirror . . . for a reset operation would have facilitated setting the reset current to the desired level of reset current 257.” Pet. 71–72 (citing Ex. 1005 ¶¶ 54, 121; Ex. 1002 ¶¶ 220–222); Pet. Reply 30. Petitioner argues this modification would have been obvious because Scheuerlein teaches that “a current mirror was a known circuit for providing constant current at a specific level.” *Id.* at 72 (citing Ex. 1002 ¶ 222). Therefore, implementing the reset drivers as current mirrors “would have been a predictable application of a known structure and technique.” *Id.*

Patent Owner argues “Scheuerlein does not disclose a first current limiting structure and a second current limiting structure.” PO Resp. 63 (citing Ex. 2003 ¶ 165). Patent Owner argues Scheuerlein does not describe its reset drivers as “current limiting structures” or “current mirrors” and that Petitioner erred in arguing that reset drivers 308, 436, and 454 provide a current equal to reset current 257. *Id.*; PO Sur-Reply 24. Patent Owner further argues “[t]he only current limiting structures described in Scheuerlein are current limiting circuits 306, 440, and 452” and “the only figure in Scheuerlein that shows two such current limiting circuits is Figure 11, which includes two current limiting circuits 452.” PO Resp. 64 (citing Ex. 1005 ¶¶ 53, 61, 86, 89, 95, 97, 100, Fig. 11; Ex. 2003 ¶ 167). Patent Owner argues current limiting circuits 452 in Figure 11 cannot be first and second current limiting structures because they are attached to

separate bit lines and, therefore, do not set/reset the same memory device as required by claim 17. *Id.* at 64–65 (citing Ex. 2003 ¶ 168). Patent Owner similarly argues that Figure 10’s current limiting structure 440 and reset driver 436 cannot be first and second current limiting structures because “current limiting structure 440 can program memory cell 423, while reset driver 436 can erase a different memory cell 422 on a different bit line.” PO Sur-Reply 24–25 (citing Ex. 1005 ¶ 84, Fig. 10) (emphases omitted).

Upon considering all the evidence and argument raised by Petitioner and Patent Owner, we agree with Petitioner that reset drivers 308, 440, and 454 are second current limiting structures that limit current through the resistive memory device when it is switched from its low-resistance (programmed) state to its high-resistance (erased) state. Scheuerlein discloses switching a resistive memory device from low-resistance state 254 to high resistance state 252 by applying “reset” voltage 255 while supplying sufficient reset current 257. Ex. 1005 ¶¶ 44, 49. This can be done, for example, using reset driver 436, which is a “current providing circuit” that drives a memory cell “with sufficient current to exceed the reset voltage across the resistor element.” *Id.* ¶¶ 87, 90, Fig. 10. It can also be done using reset driver 308, which is also a “current providing circuit” that is “set to provide a current *equal* to the reset current 257.” *Id.* ¶ 54, Fig. 4 (emphasis added). Thus, Scheuerlein teaches or discloses that reset drivers 308, 440, and 454 are “current limiting circuits” that provide a current equal to reset current 257. *Id.* Scheuerlein also discloses that reset drivers are current mirrors or teaches they can be implemented as current mirrors because Scheuerlein discloses “a current source . . . may be viewed as a circuit providing generally a constant current” and that one example of a current source is “a current mirror circuit.” *Id.* ¶ 121. Thus, reset drivers 308, 440,

and 454 are “second current limiting structures” per our construction of that term. *See* § II.B.2, *supra* (finding a “second current limiting structure” is a “second current mirror[] (and equivalents thereof) that limit[s] the current through the resistive memory device when a potential is applied to switch the device from its programmed-to-erased . . . state[].”

We disagree with Patent Owner’s numerous arguments that Petitioner has failed to meet its burden with respect to demonstrating that claim 17 is anticipated by or obvious over Scheuerlein. For example, Patent Owner argues that claim 17 is only challenged as anticipated by Scheuerlein because Petitioner “does not propose combining Scheuerlein with any other reference.” PO Resp. 62, 65. We disagree. The Petition challenges claim 17 as both anticipated by and obvious over Scheuerlein. *See* Pet. 71 (“Although Scheuerlein expressly taught using a current mirror to limit reset current, it also would have been obvious to use that approach based solely on Scheuerlein.”). It is black letter law that a claim can be found obvious over a single reference. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (“[I]n appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention.”); *see also Game and Tech Co. v. Activision Blizzard Inc.*, 926 F.3d 1370, 1381 (Fed. Cir. 2019) (a patentee’s “assertion that ‘a single reference . . . cannot support obviousness’ . . . is wrong as a matter of law.”).

Patent Owner next argues that claim 17 cannot be found obviousness because Petitioner “does not propose modifying Scheuerlein in any particular way” and provides “no motivation or explanation as to why a [person skilled in the art] would modify Scheuerlein.” PO Resp. 62, 65–66; PO Sur-Reply 23. We again, disagree. Petitioner argued “Scheuerlein

disclosed making the reset current ‘equal to’ . . . reset current 257” and “using a current mirror to provide a constant current—such as desired reset current 257,” and a person skilled in the art “would have combined these teachings.” Pet. 71 (citing Ex. 1005 ¶¶ 48, 53–54, Fig. 3; Ex. 1002 ¶ 222). Petitioner also argued that “using a current mirror as the ‘current providing circuit’ for a reset operation would have facilitated setting the reset current to the desired level of reset current 257” and that “[i]t would have been a predictable application of a known structure and technique to use a current mirror to provide a specific level of current, reset current 257, to perform a reset operation.” *Id.* at 71–72 (citing Ex. 1005 ¶¶ 54, 121; Ex. 1002 ¶ 222). Thus, Petitioner has not only explained how Scheuerlein could be modified (if it needs modification), but why a person skilled in the art would have made the modification. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007) (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”).

Patent Owner also argues that Scheuerlein’s reset drivers do not provide a current equal to reset current 257. PO Resp. 63. We disagree. Reset driver 308 is shown in Figure 4 of Scheuerlein, and Scheuerlein discloses that “[t]he magnitude of this current providing circuit 308 is preferably set to provide a current *equal* to the reset current 257” and that the circuit is controlled “to avoid providing another current value into the [device] array.” Ex. 1005 ¶ 54, Fig. 4 (emphasis added).

Finally, Patent Owner argues that Figures 10 and 11 of Scheuerlein do not show first and second current limiting structures because the structures shown for “setting” and “resetting” resistive memory devices are only capable of “setting” and “resetting” different devices on different bitlines. PO Resp. 64–65; PO Sur-Reply 24–25. We disagree. When interpreting a

reference “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). Scheuerlein discloses applying “set” voltage 253 to switch a resistive memory device from its high-resistance state 252 to its low-resistance state 254 and applying “reset” voltage 255 “[t]o change the switchable resistor memory element back to its high resistance state 252.” Ex. 1005 ¶¶ 43–44. Thus, all of the resistive memory devices shown in Figure 10 can be “set” by a current limiting circuit 440 (not shown on BL1 or BL2) and “reset” by a reset driver 436 (not shown on BL2 or BL3). This is expressly shown in Figure 11, where memory element 422 on bit line BL1 and memory element 423 on bit line BL3 can be “set” via current limiting circuits 452 and “reset” via reset drivers 454. *Id.* ¶¶ 97, 99, Fig. 11.

We decline to adopt, as unreasonable, the narrow interpretation of Figures 10 and 11 proposed by Patent Owner. For example, under Patent Owner’s interpretation, the memory devices on BL1 in Figure 10 (e.g., 422) could only be “reset,” the memory devices on BL3 (e.g., 423) could only be “set,” and the memory devices on BL2 could be neither “set” nor “reset” because neither current limiting circuit 440 nor reset driver 436 is coupled to BL2. Ex. 1005, Fig. 10. The same would be true of the memory devices on BL2 in Figure 11; because BL2 is coupled to neither a current limiting circuit 452 nor a reset driver 454 it can neither be “set” nor “reset.” *Id.*, Fig. 11. We further note that Patent Owner’s interpretation of Figure 11 ignores its disclosure of reset driver 454 and Scheuerlein’s description of using reset driver 454 to “reset” memory devices. Under the proper interpretation of Figure 11, all of the memory devices on BL1, BL2, and BL3 can be “set” by a current limiting circuit 452 and “reset” by a reset

driver 454, even though these circuits are only shown as coupled to BL1 and BL3.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that Scheuerlein either discloses all of the limitations of claim 17 or suggests a modification that teaches all of the limitations of claim 17. In the latter case, Petitioner provides sufficient reasoning with rational underpinning to make the modification. Consequently, Petitioner demonstrates by a preponderance of evidence that claim 17 is unpatentable as anticipated by or obvious over Scheuerlein.

3. Claims 18 and 19

Claim 18 depends from claim 17, and further requires the current determined by the first current limiting structure to be “different from the current determined by the second current limiting structure.” Ex. 1001, 10:52–54. Claim 19 depends from claim 18, and further requires the current determined by the first current limiting structure to be “lower than the current determined by the second current limiting structure.” *Id.* at 10:55–57. The first current limiting structure limits current to switch the resistive memory device from its erased (high resistance) to its programmed (low resistance) state, and the second current limiting structure limits current to switch the resistive memory device from its programmed (low resistance) to its erased (high resistance) state. *See* Ex. 1001, 10:41–46, 10:46–51.

Petitioner demonstrates how Scheuerlein discloses these limitations. *See* Pet. 72–73 (quoting/citing Ex. 1005 ¶ 55). Scheuerlein discloses “the ‘set’ voltage . . . causes the switchable resistor memory element to change from a high resistance state . . . to a low resistance state,” and “the ‘reset’ voltage . . . causes the switchable resistor memory element to change from the low resistance [state] to the high resistance [state].” Ex. 1005 ¶¶ 43–44.

Scheuerlein further discloses “the SET current limit is substantially less than the minimum RESET current to ensure that memory cells do not get ‘stuck’ in the SET state. In other words, $I_{\text{SET}} < I_{\text{RESET}}$ for proper operation.” *Id.*

¶ 55. Thus, Scheuerlein discloses that the current of the first current limiting structure (I_{SET}) is both different from (claim 18) and lower than (claim 19) the current of the second current limiting structure (I_{RESET}) as required.

Patent Owner does not dispute this, but argues that Petitioner has not demonstrated the unpatentability of claims 18 and 19 for the same reasons as claim 17. *See* PO Resp. 61–66; PO Sur-Reply 23–26. We disagree for the reasons discussed in § II.D.2, *supra*.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that all the limitations of claims 18 and 19 are met. Therefore, Petitioner demonstrates by a preponderance of evidence that claims 18 and 19 are unpatentable as anticipated by or obvious over Scheuerlein.

E. Challenges Based on the Baek Paper, the Baek Paper and Sim, and the Baek Application and Sim

Petitioner also argues that claims 1–16 are unpatentable as anticipated by or obvious over the Baek Paper and that claims 5, 6, 9, 10, 12, 13, 15, and 16 are unpatentable as obvious over the Baek Paper and Sim and over the Baek Application and Sim. Pet. 22–44, 60–63; Pet. Reply 2–18, 26–28. Patent Owner disputes the unpatentability of these claims on these grounds. PO Resp. 20–47, 57–61; PO Sur-Reply 7–17, 20–23.

As discussed in § II.C, *supra*, Petitioner has demonstrated by a preponderance of evidence that claims 1–16 are unpatentable as anticipated by or obvious over the Baek Application. Therefore, we need not consider whether Petitioner has also demonstrated that claims 1–16 are unpatentable

as anticipated by or obvious over the Baek Paper, that claims 5, 6, 9, 10, 12, 13, 15, and 16 are unpatentable as obvious over the Baek Paper and Sim, or that claims 5, 6, 9, 10, 12, 13, 15, and 16 are unpatentable as obvious over the Baek Application and Sim. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (non-precedential) (agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

III. CONCLUSION

We have reviewed the Petition, Patent Owner Response, Petitioner Reply, and Patent Owner Sur-Reply. We have considered all of the evidence and arguments presented by Petitioner and Patent Owner. We find, on this record, Petitioner has demonstrated by a preponderance of the evidence that claims 1–19 of the ’951 patent are unpatentable.

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–16	102(e), 103(a)	Baek Application	1–16	
5, 6, 9, 10, 12, 13, 15, 16	103(a)	Baek Application, Sim ⁶		
1–16	102(b), 103(a)	Baek Paper ⁷		
5, 6, 9, 10,	103(a)	Baek Paper,		

⁶ As discussed in § II.E, we do not decide whether claims 5, 6, 9, 10, 12, 13, 15, and 16 are unpatentable as obvious over the Baek Application and Sim.

⁷ As discussed in § II.E, we do not decide whether claims 1–16 are unpatentable as anticipated by or obvious over the Baek Paper.

12, 13, 15, 16		Sim ⁸		
17–19	102(e), 103(a)	Scheuerlein	17–19	
Overall Outcome			1–19	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown on this record that claims 1–19 of the '951 patent are unpatentable; and⁹

FURTHER ORDERED that this Decision is final, and a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁸ As discussed in § II.E, we do not decide whether claims 5, 6, 9, 10, 12, 13, 15, and 16 are unpatentable as obvious over the Baek Paper and Sim.

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. §§ 42.8(a)(3), (b)(2).

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