

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ASTRONICS TEST SYSTEMS, INC.,
Petitioner,

v.

TERADYNE, INC.,
Patent Owner.

IPR2021-00350
Patent 7,395,479 B2

Before DEBRA K. STEPHENS, TREVOR M. JEFFERSON, and
NATHAN A. ENGELS, *Administrative Patent Judges*.

STEPHENS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Astronics Test Systems, Inc. (“Petitioner”) challenges the patentability of claims 1–8 of U.S. Patent No. 7,395,479 B2 (“the ’479 patent,” Ex. 1003), assigned to Teradyne Inc. (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–8 of the ’479 patent are unpatentable (*see* 35 U.S.C. § 316(e) (2018) (“In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”)).

A. Background and Summary

Astronics Test Systems, Inc. (“Petitioner”) filed a petition for *inter partes* review (Paper 1 (“Pet.” or “Petition”)) challenging claims 1–13 of U.S. Patent 7,395,479 B2 (Ex. 1003 (“’479 Patent”)). Teradyne, Inc. (“Patent Owner”) timely filed a Preliminary Response (Paper 6 (“Prelim. Resp.”)). Along with its Preliminary Response, Patent Owner filed a Disclaimer which disclaimed claims 9–13 of the ’479 Patent (Ex. 2002; Prelim. Resp. 10; PO Resp. 7, n.1). As such, claims 1–8 were the remaining challenged claims before us and we did not address Petitioner’s challenge to claims 9–13. We instituted on all grounds directed to claims 1–8, on unpatentability (Paper 8 (“Inst. Dec.”), 39–40).

During the trial, Patent Owner filed a Response (Paper 10 (“PO Resp.”)), Petitioner filed a Reply (Paper 13 (“Pet. Reply”)), and Patent Owner filed a Sur-reply (Paper 15 (“PO Sur-reply”)).

An oral hearing was held April 21, 2022, a transcript of which appears in the record (Paper 23 (“Tr.”)).

Petitioner challenges claims 1–8 as unpatentable under 35 U.S.C. § 103 (Pet. 4). Patent Owner disputes Petitioner’s challenges as presented in the Petition ((*see* PO Resp.).

B. Real Parties in Interest

Patent Owner states that Teradyne, Inc. is the real-party-in-interest (Paper 3, 1).

Petitioner states that Astronics Test Systems, Inc. and Astronics Corporation are the real-parties-in-interest (Paper 1, 2).¹

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify a related matter. More specifically, Petitioner and Patent Owner indicate the ’479 Patent was asserted in the following district court proceeding: *Teradyne, Inc. v. Astronics Test Systems, Inc.*, No. 2:20-cv-2713 (C.D. Cal.) (Pet. 2; Paper 3, 1).

¹ Petitioner notes the District Court in related proceeding *Teradyne, Inc. v. Astronics Test Systems, Inc.*, No. 2:20-cv-2713 (C.D. Cal.) (Pet. 2; Paper 3, 1), dismissed Astronics Corp. for lack of personal jurisdiction (Ex. 1019); however, Petitioner listed Astronics Corp. “out of [an] abundance of caution” (Pet. 2, n.2). Given that no dispute exists between the Parties as to the stated real parties in interest, the Board accepts the Parties’ representations and, accordingly, does not determine whether the proper entities have been named as real parties of interest in this proceeding.

D. The '479 Patent

The '479 Patent, titled “Over-Voltage Test for Automatic Test Equipment,” issued July 1, 2008 (Ex. 1003, codes (45), (54)). The '479 Patent describes a test system in which a digital test instrument, e.g., “Automatic Test Equipment (ATE),” is “used to verify the performance of electronic devices,” “(sometimes referred to as a Unit Under Test [(UUT)])” (Ex. 1003, 1:16–28). ATEs are “programmed to provide stimulus to a particular circuit or component in the UUT and then measure the output to determine if the UUT has performed to its specifications” (*id.* at 1:30–33). The ATE described by the '479 Patent “is constructed to allow verification of proper operation of a UUT within its intended operating environment” (*id.* at 3:22–24) and, in addition, is “designed to [also] detect over-voltage situations” (*id.* at 5:29–30). Figure 2A shows digital channel 211, a component of the '479 Patent’s ATE, and is reproduced below (*id.* at 2:62–64 (“FIG. 2A is a circuit diagram of a portion of a digital test instrument according to one embodiment of the invention connected to a UUT”, 5:47–48).

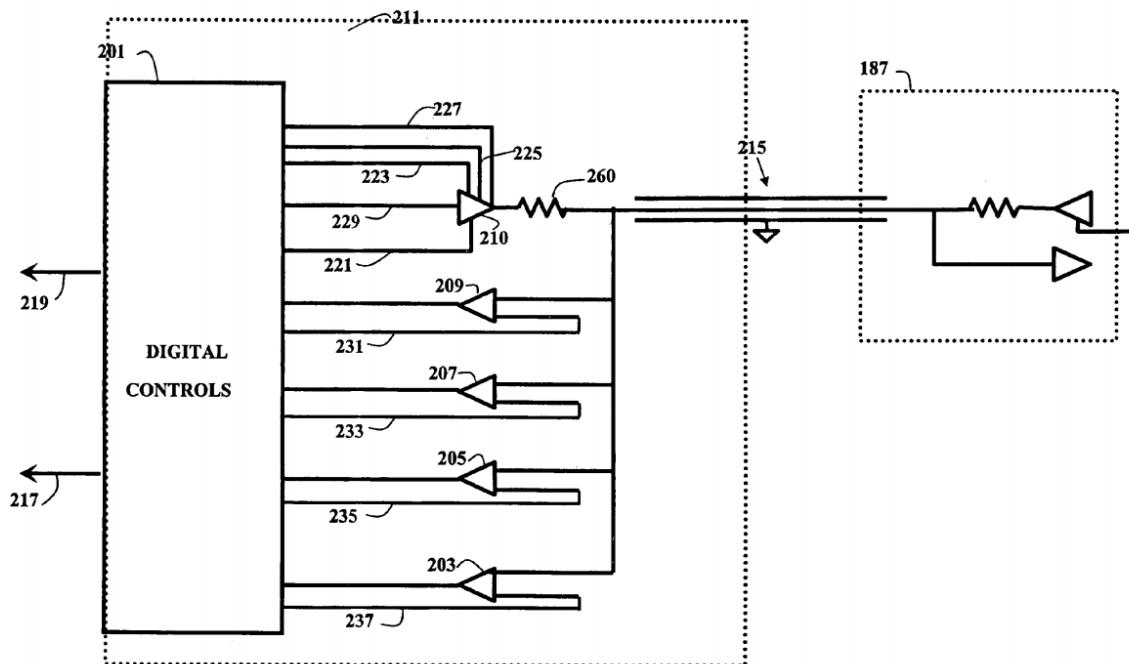


FIG. 2A

As shown in Figure 2A, digital channel 211 connects to interface 187 (of a UUT) via line 215 (*id.* at 4:16–18; *see id.* at 5:47–49, Fig. 1). Digital channel 211 senses and analyzes the value of a signal on line 215 to “determine whether there are faults within [the] system under test” (*id.* at 6:55–63). Specifically, “comparators 207 and 209 [are] coupled to the same signal connection point . . . so that they may receive as an input the signal on line 215” and “indicate whether the level of the signal on line 215 is above or below certain threshold levels that characterize normal operating conditions” (*id.* at 6:23–26, 6:64–66). Those threshold levels are “user programmable” (*id.* at 1:46–51). Then, “[d]igital control circuit 201 compares the outputs of comparators 207 and 209 to [a] programmed expected value. Based on the comparison, digital control circuit 201 places a value on pass/fail output 219,” which indicates “whether there are faults within the system under test” (*id.* at 6:45–54, 6:59–63).

In addition, as shown in Figure 2A, digital channel 211 includes comparators 203 and 205 to further “detect over-voltage conditions” on line 215 (*id.* at 7:7–8). In particular, “[w]hen the value on line 215 falls below [a] voltage specified by low over-voltage control input 235, comparator 205 asserts its output. Similarly, when the voltage on line 215 exceeds [a] value specified by high over voltage controlled input 237, comparator 203 asserts its output” (*id.* at 7:13–18). Like comparators 207 and 209, the thresholds comparators 203 and 205 analyze — over-voltage thresholds — may be user programmed (*id.* at 2:20–23, 3:43–51). Then, “outputs of comparators 203 and 205 are provided to digital control circuit 201” which “sets the value on safe/alarm output 217 based on the values output by comparators 203 and 205,” indicating whether or not “an over-voltage condition has occurred” (*id.* at 7:32–42).

The ’479 Patent states that an “over-voltage condition . . . may be used to protect the test equipment” (*id.* at 1:44–48), but that “[i]t is not, however, necessary that a voltage be so large as to cause physical damage in order to be considered over-voltage. Any voltage that is out of bounds or otherwise outside of the specified operating range may be considered ‘over voltage’” (*id.* at 5:15–19). Further, the ’479 Patent states that “over-voltage conditions may also be evaluated by the user program to determine whether the UUT is working properly” (*id.* at 3:49–51).

E. Illustrative Claims

Challenged claim 1 is the sole independent claimed.

1. Automatic test equipment adapted to execute a user program, the test equipment comprising

a channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value, the channel circuit comprising:

a) at least two comparison sub-circuits, each comparison sub-circuit having a signal input coupled to the signal connection point, a threshold input adapted to receive a threshold input signal having a value and a comparison output, and wherein each of the comparison sub-circuits is adapted to produce a comparison output signal at the comparison output having a value indicating the value of the input signal relative to the value of the threshold input signal; and

b) control circuitry having at least two measured value inputs, each measured value input coupled to the comparison output of one of the at least two comparison sub-circuits, a test output and an over-voltage output, the control circuitry adapted to generate a test output from a first subset of the comparison output signals produced by the at least two comparison sub-circuits and to generate the over-voltage output from a second subset of the comparison output signals produced by the at least two comparison sub-circuits; and

c) wherein the automatic test equipment is adapted to independently set the value of the threshold input signal for each of the at least two comparison sub-circuits based on the user program

(Ex. 1003, 13:57–14:17).

F. Evidence

Petitioner relies upon the following prior art references:

Reference	Exhibit
Miyamoto, US 6,292,342 B1, issued Sept. 18, 2001 (“Miyamoto”)	1006
Frame et al., US 6,856,158 B2, issued Feb. 15, 2005 (“Frame”)	1007

Schinabeck et al., US 4,635,259, issued Jan. 6, 1987 ("Schinabeck")	1008
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(Pet. 4–5).

Petitioner also relies on the Declaration of Stephen B. Wicker, Ph.D. for support of its contentions in the Petition (Ex. 1001) and Reply Declaration of Dr. Wicker (Ex. 1027).

Patent Owner relies on the Declaration of Mark H. Horenstein, PhD. for support of its contentions in the Patent Owner Response (Ex. 2005²).

G. Prior Art and Asserted Grounds

Petitioner initially challenged claims 1–13 of the '479 Patent (Pet. 4). Patent Owner disclaimed claims 9–13 in a disclaimer filed with and recorded by the Office (Prelim. Resp. 10 (citing Ex. 2002); Ex. 2002; PO Resp. 7, n.1). Accordingly, challenged claims 9–13 are deemed to no longer exist in the '479 Patent (*see General Electric Co. v. United Techs. Corp.*, Case IPR2017–00491, Paper 9 (July 6, 2017) (Paper 9) (Precedential); Prelim. Resp. 10 (citing *Dolby Labs., Inc., v. Intertrust Techs. Corp.*, IPR2020–01123, Paper 10 (Jan. 6, 2021); 35 U.S.C. § 253; *see also Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998)). Therefore, claims 1–8 remain. Petitioner asserts these claims, claims 1–8, would have been unpatentable on the following grounds:

² We note Patent Owner has submitted two Declarations of Dr. Mark Horenstein — Exhibit 2001 and Exhibit 2005 (*see* PO Resp. vii). Patent Owner does not indicate to which Exhibit they are referring when citing "Horenstein" in Patent Owner's Response (*see e.g.*, PO Resp. 4). Based on clarification from Patent Owner (Tr. 64, 3:10), we determine Patent Owner's arguments citing "Horenstein" refer to Exhibit 2005.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–8	103	Schinabeck
1–7	103	Miyamoto, Frame
8	103	Miyamoto, Frame, Schinabeck

(Pet. 5).

II. ANALYSIS

A. *Principles of Law*

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains (*KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007)). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence (*Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966)).

B. *Level of Ordinary Skill in the Art*

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis (*Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991))).

Petitioner asserts “a person having ordinary skill in the art (‘POSA’) at the time of the alleged invention would have had at least a bachelor’s

degree in electrical engineering, computer engineering, or a related field, and at least one year of experience with the testing of electronic equipment” (Pet. 20).

The prior art itself may demonstrate the level of ordinary skill in the art at the time of the invention (*see Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

In our Institution Decision, we adopted Petitioner’s definition of the level of ordinary skill in the art with minor modification (Dec. 8–9; *see* Pet. 20). In particular, we removed the qualifier “at least” from the education level and from the experience level, because the qualifier introduces ambiguity.

Patent Owner does not dispute this determination of the level of a person of ordinary skill in the art at the time of the invention (PO Resp. 8). Thus, we determine an ordinarily skilled artisan at the time of the invention would have had (i) a bachelor’s degree in electrical engineering, computer engineering, or a related field and (ii) one year of experience with testing of electronic equipment. We determine this asserted level of skill comports with the qualifications a person would have needed to understand and implement the teachings of the ’479 Patent and the prior art of record (*cf. Okajima*, 261 F.3d at 1355 (the prior art itself may reflect an appropriate level of skill in the art)).

C. Claim Construction

In interpreting the claims of the '063 patent, we “us[e] the same claim construction standard that would be used to construe the claim[s] in a civil action under 35 U.S.C. [§] 282(b)” (37 C.F.R. § 42.100(b) (2018)). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent (*see id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (*en banc*)).

“Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification” (*Phillips*, 415 F.3d at 1312). An inventor may rebut that presumption by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision (*In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994)). In the absence of such a definition, limitations are not to be read from the specification into the claims (*In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993)). Only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy (*Nidec Motor Corp.*, 868 F.3d at 1017 (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner states, “no terms require construction to resolve the grounds presented herein” (Pet. 5). Patent Owner addresses the “preamble” and the limitation “wherein the automatic test equipment is adapted to independently set the value of the threshold input signal for each of the at least two comparison sub-circuits based on the user program” (PO Resp. 8–13).

1. Preamble

Patent Owner contends that “[a]utomatic test equipment adapted to execute a user program, the test equipment comprising” is the preamble and that it is limiting (Ex. 1003, 13:57–58; PO Resp. 9). In particular, Patent Owner contends, “the preamble of claim 1 [is] limiting because it serves as antecedent basis for multiple terms in the body of the claim, and it supplies ‘essential structure’ of the claimed invention” (PO Resp. 9).

Petitioner does not address this contention (*see* Pet. Reply 4–5).

We agree with Patent Owner that the preamble is limiting because the body of the claim refers to the user program as well as the automatic test equipment (Ex. 1003, 13:57–58, 14:14–17; *see Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) ([D]ependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention’’)). Patent Owner asserts the following limitation, “a channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value” (Ex. 1003, 13:58–61), “although formatted within the same paragraph as the preamble[,], is not actually part of the preamble, but rather part of the body of the claim” (PO Resp. 10). However, further in its argument, Patent Owner flips its statement in arguing “input signal having a value” and contends this is a “requirement[] of the preamble” (*id.* at 11). Petitioner’s contentions are only directed to the limitation (Pet. Reply 4–5).

We determine the preamble is “[a]utomatic test equipment adapted to execute a user program, the test equipment comprising” and does not include the limitation that follows the “comprising” recitation: “a channel circuit having a signal connection point adapted to be coupled to a signal line of a

unit under test to receive an input signal having a value” (Ex. 1003, 13:58–61). We consider that limitation to be part of the body of the claim.

2. “*a channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value*”

Petitioner argues that although the claim recites an input signal, the claim does not recite that the “input signal having a value” is received from any particular component (Pet. Reply 4, 9). In particular, Petitioner argues, “the claim does not require *the single* input signal from the UUT [(Unit Under Test)]”; rather, “the words ‘a’ and ‘an’ . . . [mean] ‘one or more’” (*id.* at 9–10 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000); *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008))). Petitioner further contends, “[t]he specification contemplates providing the ATE over-voltage protection (OVP) as protection is ‘set based on the voltage levels that may cause damage to either the system under test 189 *or test system 139*’” (*id.* at 5 (citing Ex. 1003, 7:19–21, 3:47–48, 12:58–65)). Thus, according to Petitioner, Patent Owner’s construction excludes embodiments disclosed in the ’479 Patent (*id.*). More specifically, Petitioner argues the ’479 Patent “discloses testing in cycles, where comparators would receive and measure different values, not necessarily from the same signal or signal connection point” which Patent Owner does not address, instead “relying solely on one embodiment” (*id.* at 10 (citing Ex. 1003, 3:36–42, 6:23–26)).

Patent Owner contends “‘an input signal’ serves as antecedent basis for ‘*the* input signal’” and the “‘input signal having a value’ is received from a signal connection point coupled to a signal line of the UUT” (PO Resp.

10–11; PO Sur-reply 4). Patent Owner further responds Petitioner’s construction “ignores the claim as a whole, the specification, and the purpose of an automatic test equipment” (PO Sur-reply 2). More specifically, Patent Owner contends, “[a]n ATE tests a UUT by receiving an input signal from the UUT” (PO Sur-reply 2). Pointing to the ’479 Patent, Patent Owner argues, it discloses an “ATE . . . provide[s] stimulus to . . . the UUT and then measure[s] the output to determine if the UUT has performed to its specifications” (*id.* at 2–3 (citing Ex. 1003, 1:30–33)). According to Patent Owner, a channel circuit “interfaces to a signal connection point of the test instrument so that it can drive and *receive test signals at a test point in system under test 189*” (*id.* at 3 (quoting Ex. 1003, 3:65–4:3)).

Relying on Figure 1, Patent Owner argues, “the system under test (containing the UUT) from which the response signal is received is separate from ATE 139 and its channel circuits 211” (*id.* at 3 (quoting Ex. 1003, Fig. 1)). Patent Owner further argues the cited statements relied upon by Petitioner “explain *which portions of the system can be protected*, not *where the received input signal comes from*” (*id.* at 4 (citing Ex. 1003, 7:19–21, 3:47–48, 12:58–65)).

Initially, we note the claim recites “a channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value” (Ex. 1003, 13:58–61). Thus, due to the recitation, we determine the input signal could be either that the signal connection point receives an input signal or the channel circuit receives an input signal (*id.*).

The next limitation recites the comparison sub-circuit has “*a signal input . . . wherein each of the comparison sub-circuits is adapted to produce a comparison output signal at the comparison output having a value*

indicating the value of *the input signal* relative to the value of the threshold input signal” (*id.* at 13:62–14:3). The claim does not recite that the “signal input” receives “the input signal.” Nevertheless, in light of the claim language and the Specification and because Petitioner has contended both interpretations are shown, we interpret the recited “input signal” as the signal received from the UUT. The portion of the ’479 Patent describing, in part, Figure 1, cited by Patent Owner discloses

ATE 139 includes multiple instruments that may generate and measure signals. A host computer 120 executes a software program that controls operation of each of the instruments.

Host computer 120 may be programmed to analyze these outputs to determine whether the system under test 189 is operating properly. Such programming is traditionally a part of a user program and drives programmed values and compares measured values to expected values on one or more signal lines connected to the UUT. These steps may be programmed for multiple lines for multiple test cycles

(Ex. 1003, 3:32–51; PO Sur-reply 3). The ’479 Patent further describes an “ATE . . . provide[s] stimulus to . . . the UUT and then measure[s] the output to determine if the UUT has performed to its specifications” (Ex. 1003, 1:30–33; PO Sur-reply 3). Thus, these descriptions support both interpretations. Nevertheless, the ’479 Patent describes a signal being supplied and compared to expected values. Accordingly, we interpret “an input signal” as being the signal received from a unit under test (UUT).

3. *Remaining Terms*

Although Patent Owner argues the interpretation of the terms “based on a user program” and “independently set” (PO Resp. 5–6), for purposes of this Decision, we need not construe expressly any other claim terms (*see*

Nidec, 868 F.3d at 1017).

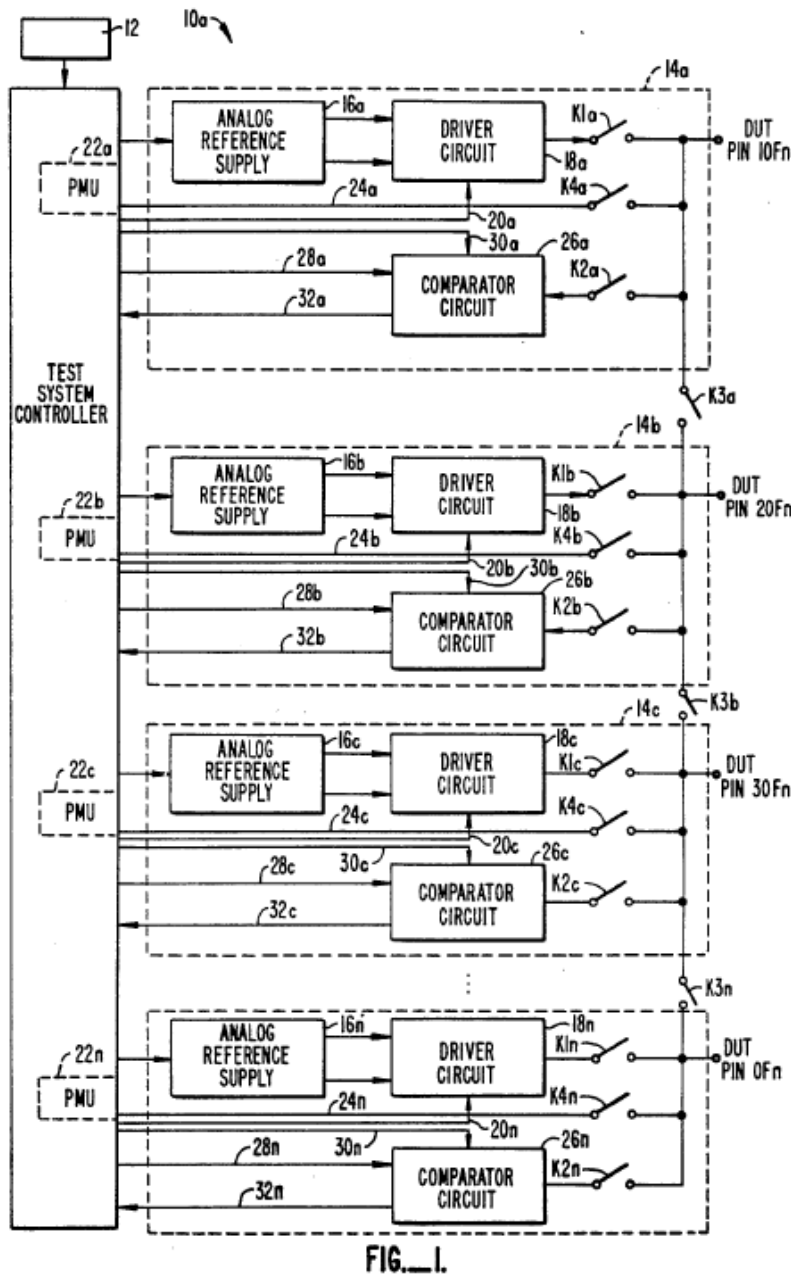
D. Ground 1: Asserted Obviousness over Schinabeck—Claims 1–8

Petitioner contends Schinabeck renders claims 1–8 obvious (Pet. 22–43).

1. Schinabeck (Ex. 1008)

Schinabeck is a patent titled “Method and Apparatus for Monitoring Response Signals During Automated Testing of Electronic Circuits,” issued January 6, 1987 (Ex. 1008, codes (45), (54)). Schinabeck describes a testing system “for automatically applying a test signal to and monitoring a response signal at a node of a device under test” (DUT) (*id.* at 3:30–33). Figure 1 of Schinabeck, reproduced below, is a block diagram showing a “test signal applying and response signal monitoring circuit” which

interfaces with and tests a “multi-terminal DUT” (*id.* at 5:67–68, 6:47–52, Fig. 1).



As shown in Figure 1, a block diagram of a testing circuit, test head controller 12 communicates with test signal applying and response signal monitoring circuit 10a control a programmed “pattern of test signals applied to the device under test (DUT) by the test signal applying and response

signal monitoring circuit 10a” (*id.* at 5:67–68, 6:25–28, 6:40–46, Fig. 1 (emphases omitted)). Schinabeck describes that the “test signal applying and response signal monitoring circuit 10a includes a plurality of pin electronics interface circuits 14a, 14b, 14c, . . . 14n connected to n pins of the DUT” and that, “[p]referably, one [of] pin electronics interface circuit 14 is connected to each terminal of the multi-terminal DUT” (*id.* at 6:47–52 (emphases omitted)). As an example, Schinabeck further describes “a DUT having sixteen terminals or pins is tested in a fixture containing sixteen identical pin electronics interface circuits 14” (*id.* at 6:58–62 (emphasis omitted)). The “single test head controller 12 contain[s] a stored program specifically written to test the particular DUT” (*id.* at 6:60–62 (emphasis omitted)). For example, to “test a signal input terminal of the DUT, the test head controller 12 closes a relay contact K1a . . . in the pin electronics interface circuit 14a to connect the test stimuli section of the test signal applying and response signal monitoring circuit 10a to pin 1 of the DUT” (*id.* at 6:63–7:1 (emphases omitted)).

The test signals applied to the DUT may be provided by driver circuits, e.g., driver circuit 18a, and by precision measurement units (PMUs), e.g., PMU 22a (*id.* at 7:6–19 (emphases omitted)). For example, PMU 22a “supplies desired voltages or currents to the appropriate pin of the DUT” (*id.* at 7:17–19 (emphasis omitted)). In this example, the test “closes only relay contact K4a . . . to enable coupling of pin 1 of the DUT to the PMU 22a via a line 24a. Similar PMUs 22b, 22c, . . . 22n can apply controlled test signals to corresponding other pins of the DUT, or one or more PMUs can be multiplexed to the pins” (*id.* at 7:20–26 (emphases omitted)). Ultimately, the “the output signals from the comparison means 26a can change in accordance with the test signal applied to the DUT” and

the “output signal from the comparison means 26a is returned to the test head controller 12 via a line 32a,” causing “the test head controller 12 to register either acceptance or rejection of the DUT, or to specify its quality” (*id.* at 7:37–50 (emphases omitted)).

2. *Analysis of Independent Claim 1*

Petitioner contends Schinabeck renders independent claim 1 obvious (Pet. 22–35).

a) *“input signal having a value”*

Petitioner relies on Schinabeck to teach

a channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value, the channel circuit comprising:

(Pet. 22–25 (citing Ex. 1008, 1:8–9, 1:50–55, 2:3–22, 2:58–62, 3:30–33, 3:53–63, 6:47–52, 7:59–60, Fig. 1, 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 88–91); Ex. 1003, 13:57–61). More specifically, Petitioner contends Schinabeck “is directed to a method and apparatus for automatically testing . . . electronic circuits by monitoring response signals during test of the electronic circuits in an automated electronic test system” (*id.* at 23 (quoting Ex. 1008, 1:8–9 (emphases added by Petitioner)). Petitioner further contends Schinabeck teaches “‘a stored program in the test system’ allowing ‘the ultimate user’ to select ‘whatever standard or specifications’ the user desires” providing a disclosed example that “the test rate is programmable” (*id.* (citing Ex. 1008, 2:3–22, 7:59–60; Ex. 1001 ¶ 88)). Petitioner asserts, Schinabeck discloses the recited “channel circuit” because “its ATE has ‘a plurality of pin electronics interface circuits . . . connected to n pins of the DUT” (Pet. 23 (citing Ex. 1008, 6:47–50, Fig. 1; Ex. 1001 ¶¶ 89–90)).

Petitioner additionally asserts an ordinarily skilled artisan “would have understood that switch K3a can be opened or closed depending upon the desired test set-up” (*id.* (citing Ex. 1008, 6:47–52; Ex. 1001 ¶¶ 89–90)). Petitioner further contends, “[e]ach channel ‘includes a node to be coupled to a pin of the [DUT] . . . and a comparison circuit connected to the node’ for receiving a ‘response signal’ (from the DUT) and comparing the response signal to a ‘programmed reference level’” (*id.* at 24–25 (citing Ex. 1008, code (57), 3:53–63, 6:47–50, Fig. 1, 11:43–68, 12:46–14:9)).

Patent Owner responds that “[t]he output of Schinabeck’s ‘driver circuit 18’ is . . . generated by the ATE itself and therefore cannot be the claimed ‘input signal’ received from the UUT” (PO Resp. 17–18 (citing Ex. 2005 ¶ 48)). Patent Owner argues, “the claim requires that the received ‘input signal having a value’ is a signal received from the UUT via the connection point” (*id.* (citing Ex. 2005 ¶ 49)). Patent Owner further contends Schinabeck’s driver circuit upon which Petitioner relies, “is *within* Schinabeck’s pin electronics interface circuit 14a, and therefore the driver’s generated output signal is not an input signal received from a UUT via a connection point to the UUT” (*id.* at 19 (citing Ex. 2005 ¶ 50)).

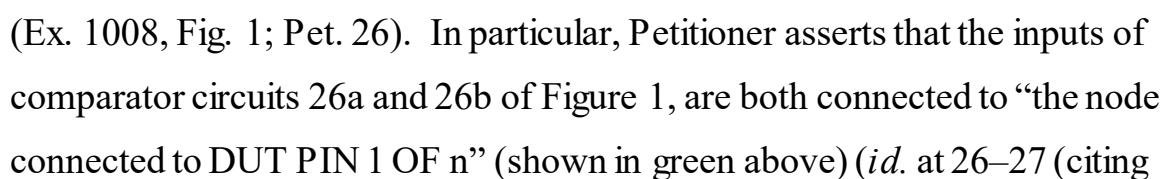
Petitioner responds, “Schinabeck’s input signal may come from a ‘signal line of a UUT,’ either through driver circuit 18a or through DUT PIN1OFn (a signal connection point) via switch K2a” as confirmed by both Patent Owner’s and Petitioner’s experts (Pet. Reply 7 (citing Pet. 24–25; Ex. 1026, 62:13–24, 67:1–22)).

As set forth *supra*, we interpret “input signal” as the signal supplied by the UUT. Schinabeck discloses the channel circuit receives a “response signal” (Ex. 1008, 11:49–53, 12:56–13:7; Pet. 24–25). In particular, Schinabeck teaches each of the comparison means indicates a value of the

response signal with respect to a programmed level (Ex. 1008, 11:49–53, 12:56–13:7; Pet. 24–25). Thus, we determine an ordinarily skilled artisan would understand that for Schinabeck’s comparison means to perform the comparison, the comparison means must receive the response signal which comes from the DUT (UUT), i.e., the input signal (*see* Ex. 1008, 11:49–53, 12:56–13:7; Pet. 24–25; Pet. Reply 7). Accordingly, we determine Petitioner has shown Schinabeck teaches the recited “channel circuit having a signal connection point adapted to be coupled to a signal line of a unit under test to receive an input signal having a value,” as recited in claim 1 (Ex. 1003, 13:58–61).

b) “at least two comparison sub-circuits, each comparison sub-circuit having a signal input . . . and a comparison output” – (limitation 1a)

Petitioner relies on Schinabeck to teach “at least two comparison sub-circuits, each comparison sub-circuit having a signal input coupled to the signal connection point” (Pet. 25–27 (citing Ex. 1008, 3:56–63, 4:43–66, 7:37–39, 8:6–18, 47–52, 11:43–68, 12:46–14:9, Figs. 1–2; Ex. 1001 ¶¶ 92–



Ex. 1008, 3:56–63, 4:43–66, 8:6–18, 11:43–68, Fig. 1; Ex. 1001 ¶ 92)).

Petitioner further asserts, “each comparator circuit receives a ‘programmed **reference level**’” and thus, Schinabeck teaches the “threshold input signal” (*id.* at 27 (citing Ex. 1003, 3:56–63, 4:43–66, 8:6–18, 9:16–35, 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 93–95)). Petitioner additionally asserts Schinabeck teaches “comparator circuits (26a and 26b) [shown in yellow] compare the response signal (the recited ‘input signal’) and programmed reference level (the recited ‘threshold input signal’), respectively, to produce a value based on the comparison” thus teaching the recited “comparison output” (*id.* at 27 (citing Ex. 1008, 3:56–63, 4:43–66, 8:6–18, 8:47–52, Figs. 1–2, 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 93–95)).

Patent Owner contends “grouping multiple comparison sub-circuits [in Schinabeck,] ignores the disclosed purpose of Schinabeck’s K3n switches” (PO Resp. 19). Patent Owner asserts, “Petitioner’s assertion that Schinabeck teaches or suggests ‘grouping’ multiple pin electronics interface circuits via switch K3a to receive the same signal at multiple comparators finds no support in the prior art” (*id.* at 20 (citing Pet. 23–24)). According to Patent Owner, “Schinabeck actually teaches using switches K3a only to drive controlled test signals to multiple input pins of a DUT [but] never teaches or suggest[s] using switch K3a . . . in the manner proposed by Petitioner to connect multiple receiver circuits to the same input signal” (*id.*). Patent Owner further contends, “Petitioner’s allegation that a [person of ordinary skill in the art] would use switch K3a [in the manner proposed] contradicts Schinabeck’s disclosure, and a [person of ordinary skill in the art] would have no reason to do so” but instead, is “hindsight reconstruction” (*id.* (citing Ex. 2005 ¶ 51)).

Patent Owner argues, “both comparison sub-circuits must receive the *same* input signal from the *same* connection point” of the unit under test (UUT) (PO Resp. 21). Patent Owner further contends, “each pin electronics interface circuit in Schinabeck (*e.g.*, 14a, 14b, . . . 14n) contains only a single comparison circuit (*e.g.*, 26a, 26b, . . . 26n) connected to one terminal of the DUT” (PO Resp. 23–24). According to Patent Owner, “Schinabeck’s switch K3a has a different purpose than the one contended by Petitioner [and, s]pecifically, switch K3a is used to multiplex control signals from one or more PMUs to the pins” as would be understood by an ordinarily skilled artisan (*id.* at 24 (citing Ex. 2005 ¶ 57), 26 (citing Ex. 1008, 7:17–26), 27–28 (citing Ex. 2005 ¶ 63)). Patent Owner contends Schinabeck’s “use of switch K3 (for multiplexing PMU control signals during parametric testing) does not . . . teach or suggest Petitioner’s grouping theory – *i.e.*, configuring multiple comparison means 26a and 26b to receive the same signal from the DUT” (*id.* at 26).

Patent Owner further contends, “Schinabeck does not disclose that a resulting signal from the DUT is received from that same ‘*input* terminal’ of the DUT that (as opposed to one of the DUT’s *output* terminals connected to a single pin electronic interface circuit having one comparator)” (*id.* (citing Ex. 2005 ¶ 60; *see* Ex. 1008, 6:55–57)). Patent Owner additionally asserts, “even if an input signal were received from the DUT at that same pin where switch K3a is closed, connecting two comparators (*e.g.*, comparator circuits 26a and 26b) would require additional configuration beyond merely closing switch K3a” (*id.* at 26–27 (citing Ex. 2005 ¶ 61)). Patent Owner contends, “Schinabeck says nothing about testing a signal or configuring the device to connect comparator circuit 26b to the same signal line as comparator circuit 26a. Indeed, there would be no need for a second comparator to perform the

two types of comparisons relied upon by Petitioner” (*id.* at 27). According to Patent Owner, “the go/no-go comparison would be done using the same comparator that is already in the first pin electronics interface circuit, and there is no need for a second comparator” (*id.* (citing Ex. 2005 ¶ 62). Patent Owner further contends Petitioner fails to explain why an ordinarily skilled artisan would have “configure[d] Schinabeck’s pin electronics interface circuits so that separate comparators in different interface circuits receive the same input signal from the same signal connection point” (PO Resp. 31 (citing Pet. 22–25)).

Petitioner responds that Schinabeck teaches this limitation, “by disclosing comparison sub-circuits grouped by closing switch K3n . . . [that] also receive a ‘programmed reference level’ and produce a value based on the comparison of the response signal and the programmed reference level” (Pet. Reply 8–9 (citing Pet. 25–27)). Petitioner further responds that “Schinabeck teaches sub-circuits producing comparison output signals based on the same input signal from the same connection point to the UUT” (*id.* at 9). Petitioner asserts Schinabeck discloses an “ATE has ‘a plurality of pin electronics interface circuits . . . connected to n pins of the DUT’ that can be grouped by closing switch K3n” (Pet. Reply 10 (citing Pet. 23–24), 11 (citing Ex. 1003, Fig. 1)). Petitioner additionally contends an ordinarily skilled artisan “‘would have understood that switch K3a can be opened or closed depending on the desired test set-up’ to create a channel circuit” (*id.* at 11 (citing Ex. 1001, 35–36; Ex. 1008, Fig. 1)). Petitioner thus asserts “[e]ach comparator circuit receives the response signal from the node connected to ‘DUT PIN 1 of n’” (*id.* (citing Ex. 1001, 39)). Petitioner argues because Patent Owner admits switch K3a “multiplex[es] control signals from one or more PMUS to the pins,” Patent Owner “admits

Schinabeck teaches ‘grouping’ multiple circuits” (*id.* at 12–13 (citing PO Resp. 24–25; Ex. 1008, 7:23–26)). Petitioner also asserts a PMU can both send signals to multiple pins and receive one pin’s signal through multiple comparators and an ordinarily skilled artisan would have understood if switches K3 are closed, they can receive or drive signals (*id.* at 13 (citing Ex. 1027 ¶¶ 7-11)). According to Petitioner, “[g]iven the simplicity of switches, a [person of ordinary skill in the art] would have understood when switch K3a is closed, Schinabeck’s comparator circuits become part of the same channel circuit . . . [otherwise,] Schinabeck’s Figure 1 could have omitted K3[] switches altogether” (*id.*). Petitioner additionally contends Schinabeck does not need to “explicitly describe using K3a for this purpose” because “switches are ‘fundamental’ and can be opened or closed for control signal purposes” (*id.* (citing Ex. 1003, 1:58–61, 8:43–54; Ex. 1026, 17:7–18:8, 39:8–44:1; MPEP § 2164.01)). Petitioner also disagrees that “additional configuration beyond closing switch K3a” would be necessary (*id.* at 14 (citing Ex. 1027 ¶ 11)).

Petitioner additionally contends Schinabeck’s “‘Go/No-go’ testing—based on an operating range—falls squarely within over-voltage testing” which is consistent with the ’479 Patent which discloses “multiple ways to respond, including *stopping the test* (*i.e.*, (‘Go-No-go testing’))” (*id.* (citing Ex. 1008, 5:17–20; Ex. 1003, 5:29–46)). Petitioner thus argues an ordinarily skilled artisan “would have understood that, besides ‘Go/No-go’ testing, Schinabeck discloses grouping comparators, and a [person of ordinary skill in the art] would have found it obvious to group comparators to run simultaneous and sequential tests” (*id.* (citing Ex. 1027 ¶¶ 12–14)).

In response, Patent Owner admits “switch K3n can be closed”; however, Patent Owner argues “the *only* use of switch K3n taught by

Schinabeck” is closing it to “multiplex control signals from one or more PMUs to the pins” (PO Sur-reply 10 (citing Ex. 1008, 7:17–26)). Patent Owner argues Schinabeck fails to teach a configuration in which “if switches K3 are closed, they can *receive* a signal just as they can be used to *drive* a signal (*id.* (citing Pet. Reply 13; Ex. 1027 ¶¶ 7–11)). Additionally, Patent Owner argues “what ‘*can*’ be done is not the proper test” and is “pure hindsight reconstruction” (*id.*).

We are persuaded by Petitioner’s contentions. In particular, we note claim 10 of Schinabeck recites:

Apparatus for repeatedly monitoring the response signal at a node of a device under test caused by a test signal applied to the node, comprising:

digitally programmed source means switchably connected by a first switch means to the node, the digitally programmed source means having a pre-selected programmed voltage-current characteristic defined by not-to-exceed voltage rail and current rail levels for supplying test signals to the node;

first comparison mean[s] switchably connected by a second switch means to the node for repetitively indicating the relative amplitude of the response signal voltage at the node with respect to a first programmed voltage level;

second comparison means switchably connected by the second switch means to the node for repetitively indicating the relative amplitude of the response signal voltage at the node with respect to a second programmed voltage level;

third comparison means switchably connected by the second switch means to the node for repetitively indicating the relative amplitude of the response signal current at the node with respect to a first programmed current level;

fourth comparison means switchably connected by the second switch means to the node for repetitively indicating

the relative amplitude of the response signal current at the node with respect to a second programmed current level;

control means connected to the digitally programmed source means and comparison means for continuing to cause the digitally programmed source means to apply the test signal to and the comparison means to monitor the response signal at the node in the event that the response signal voltage and current have a first predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively; and

means connected to the comparison means and control means for providing a fail signal in the event that the response signal voltage and current have a second predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively.

(Ex. 1008, 12:46–14:11; *see also* Ex. 1008, 4:40–5:13 (same language as claim 10); *see* Pet. 24–25). Each of the recited first, second, third, and fourth comparison means are “switchably connected . . . at the node”

(Ex. 1008, 12:56–13:7, 4:49–66; Pet. 27). Schinabeck’s node is described as “a node of a device under test” (Ex. 1008, 12:46–48; 4:40–43; *see also id.* at [57] (“a node to be coupled to a pin of the device under test”), 3:30–33 (“a method and apparatus for automatically applying a test signal to and monitoring a response signal at a node of a device under test”). Thus, Schinabeck teaches the recited signal connection point. Schinabeck further describes that each comparison means additionally measures the response signal at a node of the device under test (*id.* at 12:56–13:7, 4:49–66; Pet. 27). Accordingly, Schinabeck describes at least two comparison sub-circuits, each comparison sub-circuit having a signal input (response signal) coupled to the node (signal connection point). This contrasts with Patent

Owner’s assertion that Schinabeck fails to teach “‘grouping’ multiple pin electronics interface circuits via switch K3a to receive the same signal at multiple comparators” (PO Resp. 20). Indeed, Schinabeck teaches each of the four comparison means receiving the same response signal (*see* Ex. 1008, 12:56–13:7, 4:49–66). Therefore, Schinabeck also supports Petitioner’s assertion that an ordinarily skilled artisan would understand and use the switches in the manner proposed by the ’479 Patent claim 1 (Pet. 23–24) because Schinabeck describes use of the switches as recited in claim 1 of the ’479 Patent, in its (Schinabeck’s) claim 10—each comparison means switchably connected to a signal connection point. Although Patent Owner argues otherwise (*see* PO Resp. 21), we find that Schinabeck teaches “both comparison sub-circuits. . . receive the same input signal [(response signal)] from the same connection point [(node)]” (Ex. 1008, 12:56–13:7, 4:49–66; Pet. 27).

Petitioner’s annotated Figure 1 supports Petitioner’s contentions (Ex. 1008, Fig. 1; Pet. Reply 12). Each of the comparators 26a . . . 26n receives a signal from the DUT and a signal from the test head controller 12 via line 28a . . . 28n, respectively (*id.* at Fig. 1, 7:37–39, 11:43–68, 12:46–14:9; Pet. 26–27; *see also* 3:56–63, 4:43–66, 8:6–18, 11:43–68; Pet. 26–27). Schinabeck further teaches each of the comparator circuits receives a programmed reference level and, in particular, “comparison means . . . for indicating the relative magnitude of the response signal with respect to a programmed reference level” (Ex. 1008, 3:56–63, 4:43–66, 11:49–53, 12:56–13:7; Pet. 27). In performing these comparisons, Schinabeck teaches comparisons with programmed voltage levels (*id.* at 4:49–57, 11:43–68, 12:46–14:9; Pet. 27; Ex. 1001 ¶ 93–95) and programmed current levels (Ex. 1008, 4:57–66, 11:43–68, 12:46–14:9 Pet. 27; Ex. 1001 ¶ 93–95).

Schinabeck also teaches comparisons with minimum and maximum voltages (Ex. 1008, 8:6–18, 9:16–35 Pet. 27; Ex. 1001 ¶ 93–95). Schinabeck further teaches comparing the response signal with a programmed reference level (Ex. 1008, 3:56–63, 4:43–66, 8:6–18, 8:47–52, 11:43–68, 12:46–14:9, Figs. 1–2; Pet. 27; Ex. 1001 ¶¶ 93–95).

Patent Owner’s contention that “each pin electronics interface circuit in Schinabeck (*e.g.*, 14a, 14b, ... 14n) contains only a single comparison circuit (*e.g.*, 26a, 26b, ... 26n) connected to one terminal of the DUT” (PO Resp. 23) is inconsistent with the disclosure in Schinabeck (Ex. 1008, 12:56–13:7, 4:49–66). Indeed, Schinabeck discloses connecting four comparison circuits to *one* node and the comparison circuits receiving one response signal (*id.*).

Schinabeck also does not limit its invention to “multiplex control signals from one or more PMUs to the pins” (PO Resp. 24; *see* Ex. 1008, 12:56–13:7, 4:49–66). Again, Schinabeck’s claim 10 (and claim 3) discloses otherwise (Ex. 1008, 11:49–53, 12:56–13:7, 4:49–66).

Patent Owner admits comparators and switches were known but contends it is the particular combination of those components that require particular inputs and outputs as recited in the claims (Tr. 35:5–12). Schinabeck, however, teaches the particular combination of those components as discussed *supra* (*see* Ex. 1008, Fig. 1; Pet. 25–27).

Moreover, “apparatus claims cover what a device *is*, not what a device *does*” (*Hewlett-Packard Co. v. Bausch & Lomb, Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990); *see also Paragon Solutions, LLC v. Timex Corp.*, 566 F.3d 1075, 1091 (Fed. Cir. 2009) (“Absent an express limitation to the contrary, any use of a device that meets all of the limitations of an apparatus claim written in structural terms infringes that apparatus claim”) and *Roberts v.*

Ryer, 91 U.S. 150, 157 (1875) (“The inventor of a machine is entitled to the benefit of all the uses to which it can be put, no matter whether he had conceived the idea of the use or not”)).

We determine Schinabeck teaches the structure of the comparison sub-circuits recited in claim element 1a. Indeed, given that switches and comparators were known (Tr. 35:5–8; Ex. 1026, 17:17–18:8, 30:16–22), we determine switching certain switches on or off is a switch performing the same function it had been known to perform, yielding no more than one would expect from such an element (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007)). Thus, turning switches off or on in Schinabeck’s circuitry, would not have been “uniquely challenging or difficult for one of ordinary skill in the art” or “represented an unobvious step over the prior art” (see *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418-19)). A skilled artisan is “a person of ordinary creativity, not an automaton” (see *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420-21 (2007)). An ordinarily skilled artisan “must be presumed to know something” about the art “apart from what the references disclose” (*In re Jacoby*, 309 F.2d 513, 516 (CCPA 1962)). We further credit Dr. Wicker that an ordinarily skilled artisan “would have understood that switch K3a can be opened or closed depending upon the desired test set-up” and “by definition, switches are controlled to be open or closed” (Ex. 1001 ¶ 90). And again, Schinabeck contemplates use of the circuitry as recited, as described in claim 10 discussed *supra*. We thus are persuaded that Schinabeck teaches or at least suggests limitation 1a). We are also not persuaded Petitioner used impermissible hindsight reconstruction as the circuitry elements in Schinabeck are being used as was known to be used for the purpose of “monitoring response signals during automated testing of

electronic circuits” (Ex. 1008, [54]). Petitioner has not relied on addition of any other circuit elements — Petitioner is relying on closing switches in the disclosed circuitry of Schinabeck (Pet. 25–27). Additionally, Schinabeck discloses coupling comparison circuits to the same response signal (Ex. 1008, 11:49–53, 12:56–13:7, 4:49–66 and thus, Patent Owner’s contention that this grouping is “not any ‘desired’ configuration for functional or parametric testing” in Schinabeck is not supported by Schinabeck’s disclosure.

Patent Owner further contends Petitioner’s expert supports their assertions (PO Sur-reply 10–12). In particular, Patent Owner argues “Dr. Wicker [] has testified that ‘there would not have been a need for the comparison sub-circuits to receive the same input signal’” (*id.* at 10–11 (citing Ex. 1027 ¶ 8)); however, Dr. Wicker was referring to the recitation of claim 1 and that the same input signal would be split to be supplied to each sub-circuit (Ex. 1027 ¶ 8). Patent Owner additionally contends, “the proposed mapping would require more than simply closing K3a” and Petitioner failed to address this “complexity” (PO Sur-reply 11). Patent Owner again contends Dr. Wicker agreed (*id.*); however, again, Dr. Wicker’s testimony was taken out of context — Dr. Wicker stated “an input signal can travel from the UUT into multiple interface circuits (here 14a and 14b) through switch K3a when it is closed without additional configuration” (Ex. 1027 ¶ 11). Dr. Wicker additionally stated that additional switches would be closed to reach comparator circuits K2a and K2b (Ex. 2007, 31:14–32:15). We do not determine these to be “additional configurations” — no new elements were added. Rather, we consider these “configurations” to use an element as intended, *i.e.*, using switches as switches, in a manner contemplated by Schinabeck — testing of a device under test.

Patent Owner additionally argues Schinabeck's Go/No-go test, "relie[d] upon [by Petitioner,] is performed at a different time than, and thus would be performed using the same comparator as, the subsequent test" eliminating the "need for a second comparator" (PO Sur-reply 12–13 (citing PO Resp. 27, 33, 35–36; Ex. 2007, 37:13–38:19)). However, the VMAX and VMIN disclosed by Schinabeck is one example of a programmed reference level and used by Petitioner to show a programmed reference level could be set to a VMAX or VMIN value (*see* Pet. 27). Moreover, even considering Patent Owner's contention, Schinabeck's Go/No-go testing is provided as one embodiment of testing disclosed in which if the results (comparison of signals to limits) fail within a pass window, the test plan proceeds while if no pass result is found, a fail branch is undertaken (Ex. 1008, 10:61–64).

Accordingly, we determine Petitioner has shown Schinabeck teaches at least two comparison sub-circuits, each comparison sub-circuit having a signal input coupled to the signal connection point, a threshold input adapted to receive a threshold input signal having a value and a comparison output, and wherein each of the comparison sub-circuits is adapted to produce a comparison output signal at the comparison output having a value indicating the value of the input signal relative to the value of the threshold input signal,

as recited in claim 1.

- c) *"control circuitry adapted to generate . . . the over-voltage output . . . produced by the at least two comparison sub-circuits . . ."*
(limitation [1.b])

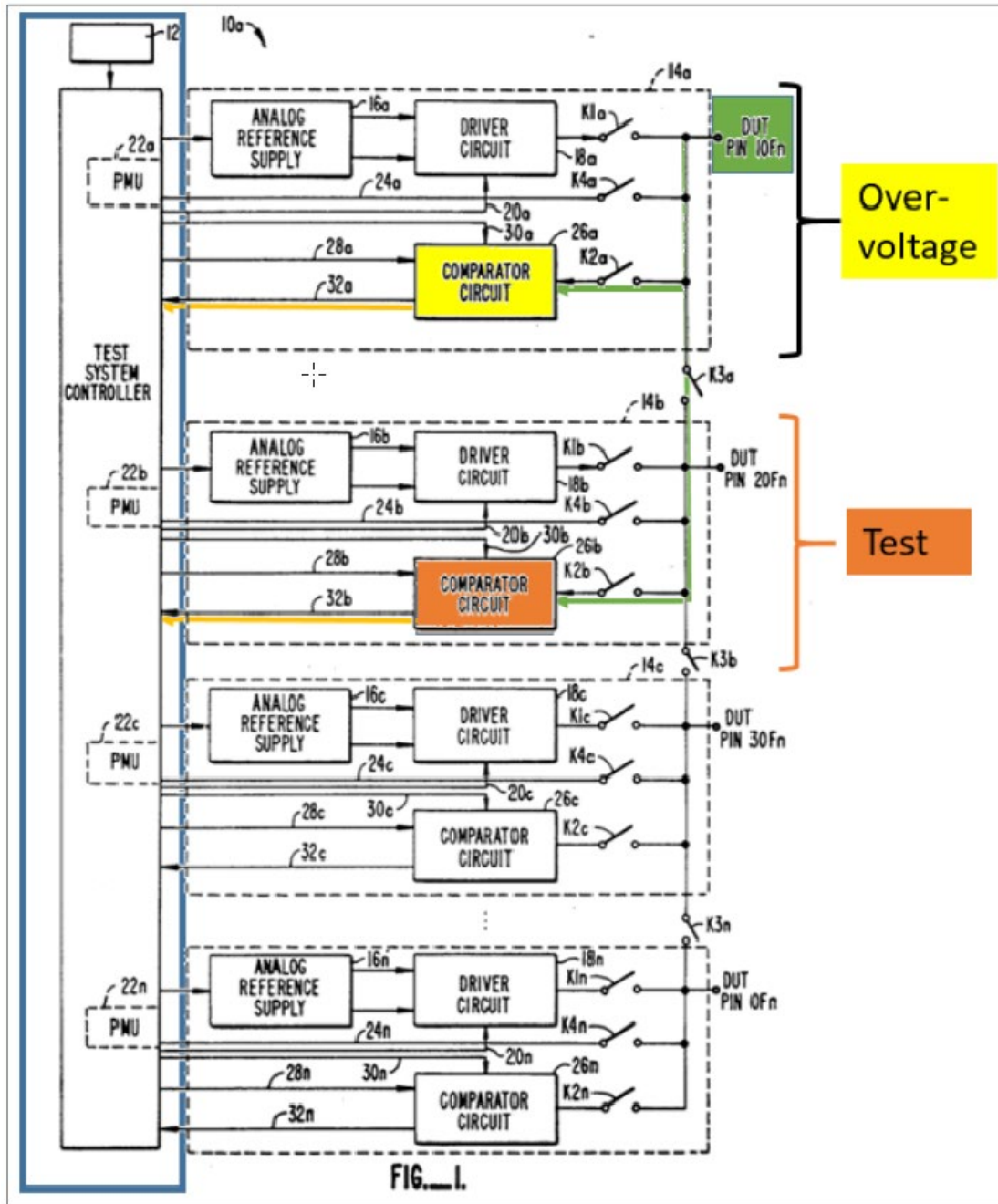
Petitioner relies on Schinabeck to teach

- b) control circuitry having at least two measured value inputs, each measured value input coupled to the comparison output of

one of the at least two comparison sub-circuits, a test output and an over-voltage output, the control circuitry adapted to generate a test output from a first subset of the comparison output signals produced by the at least two comparison sub-circuits and to generate the over-voltage output from a second subset of the comparison output signals produced by the at least two comparison sub-circuits

(Pet. 28–35 (citing Ex. 1008, 1:20–22, 1:54–57, 1:62–66, 2:37–41, 3:21–26, 3:63–4:3, 4:40–5:8, 5:50–52, 6:24–46, 6:64–7:6, 7:12–52, 7:56–60, 8:6–18, 8:26–52, 9:16–35, 10:6–8, 10:43–64, 11:43–68, 12:46–14:9, Figs. 1, 3; Ex. 1001 ¶¶ 96–108)). In particular, Petitioner asserts Schinabeck discloses “‘a test head controller,’ which is ‘implemented with a . . . microprocessor’” and “‘a test system controller’ comprising precision management units (‘PMUs’)” (*id.* at 28 (citing Ex. 1008, 6:25–46, 7:16–19, Fig. 1)).

Petitioner provides an annotated Figure 1 of Schinabeck (Pet. 29).



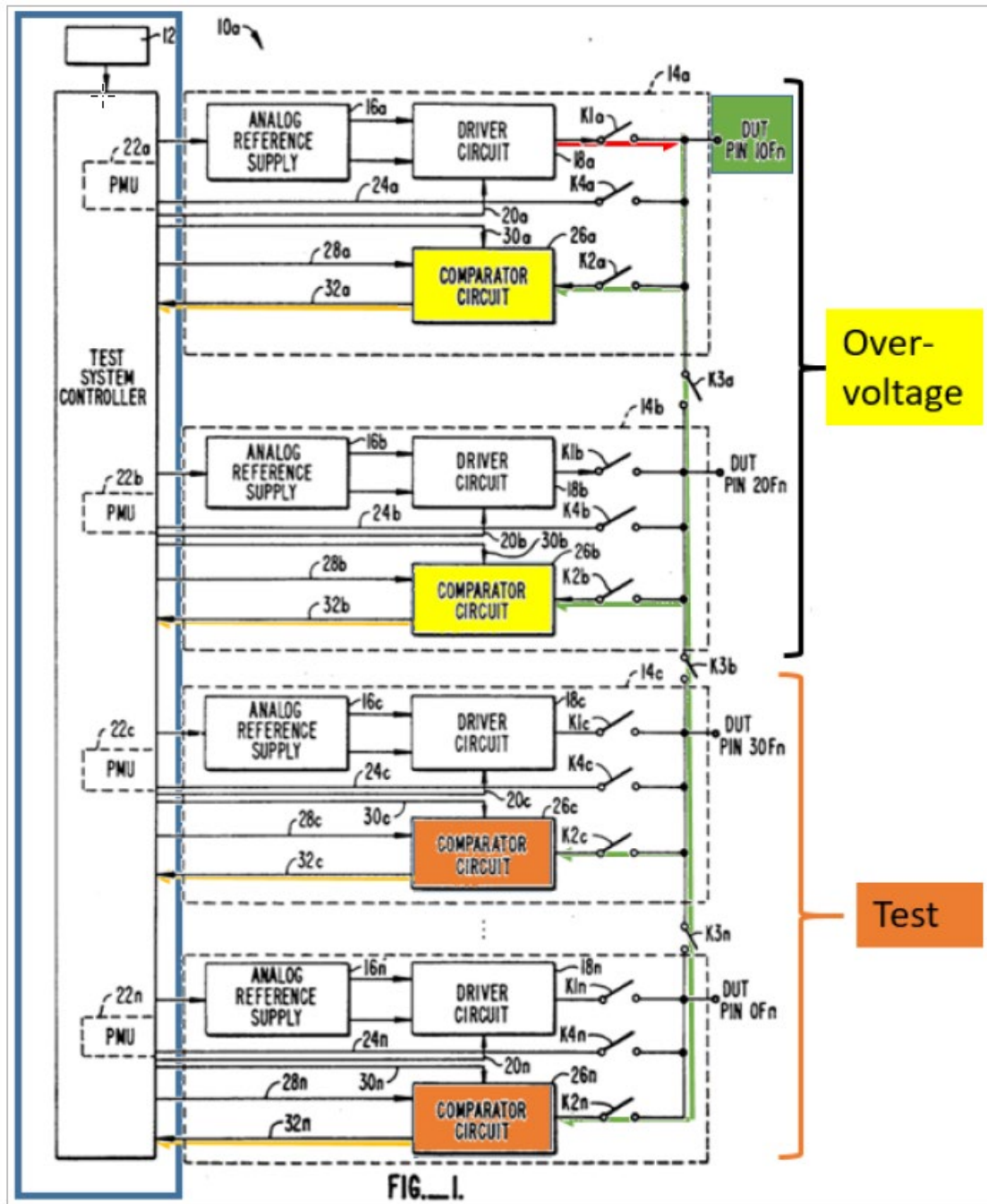
(*id.*; Ex. 1008, Fig. 1). Figure 1 of Schinabeck illustrates “a block diagram of a testing circuit fabricated according to” Schinabeck’s described invention (Ex. 1008, 5:67–68, Fig. 1). Petitioner has annotated Figure 1 to show comparator circuit 25a in yellow used in generating an over-voltage output; comparator circuit 25b in orange used in generating a test output; the DUT

and response signal in green; the comparator outputs in gold; and the control circuitry in blue (Pet. 29, 32–33; Ex. 1008, Fig. 1). Figure 1 of Schinabeck shows test head controller 12 connected to a test system controller (*id.* at Fig. 1). The test system controller provides input signals 30a and 30b to comparators 26a and 26b, respectively (*id.*). Comparators 26a and 26b provide signals 32a and 32b, respectively (*id.*). According to Petitioner, Schinabeck “describes a ‘test head controller’ . . . ‘implemented with a . . . microprocessor’ [that] transmits and receives test data, and controls the test signals applied to the DUT” (Pet. 28 (citing Ex. 1008, 6:25–46, Fig. 1)). Petitioner additionally asserts, “Schinabeck discloses a ‘test system controller’ comprising precision management units (‘PMUs’)” (*id.* at 29–30 (citing Ex. 1008, 7:12–52; Ex. 1001 ¶ 96)). Petitioner further contends Schinabeck teaches the “at least two measured value inputs” through lines 32a and 32b (*id.* at 30 (citing Ex. 1008, 7:56–60, 8:6–18, Figs. 1, 3; Ex. 1001 ¶ 97)).

Petitioner asserts each of these measured value inputs are coupled to “the comparison outputs . . . as each input to the control circuitry is coupled to the comparator circuit output signal” (*id.* (citing Ex. 1008, Fig. 1; Ex. 1001 ¶¶ 96–97)). According to Petitioner, Schinabeck discloses “control circuitry that generates the recited ‘test output’ as it provides a ‘fail signal’ if the comparator circuit output signal exceeds the ‘programmed reference level,’ which can include indicating whether the voltage level has exceeded the threshold” thus, disclosing a fail signal based on the output of each comparator (*id.* at 30–31 (citing Ex. 1008, 2:37–41, 3:63–4:3, 4:66–5:8, 8:26–52, 9:16–35, 10:6–8, 10:43–64; Ex. 1001 ¶ 98)).

Additionally, Petitioner argues, “Schinabeck discloses each comparator has a ‘reference level’ . . . [that] can be programmed to have

different values” which an ordinarily skilled artisan “would have understood . . . could be set to any desired level” (*id.* at 31–32 (citing Ex. 1008, 3:63–4:3, 4:43–66, 5:15–19, 8:6–18, 9:16–35; 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 98–100)). Petitioner asserts, “Schinabeck discloses using four total comparator circuits to generate an over-voltage output from outputs of a first two comparator circuits, and a test output from outputs of the second two comparator circuits,” as shown below in Figure 1 annotated by Petitioner (*id.* at 32 (citing Ex. 1008, 4:40–5:8, Fig. 1, 12:46–14:9)).



(*id.* at 33 (citing Ex. 1008, 4:40–5:8, 12:46–14:9, Fig. 1)). Figure 1 of Schinabeck illustrates “a block diagram of a testing circuit fabricated according to” Schinabeck’s described invention (Ex. 1008, 5:67–68, Fig. 1).

Referring to annotated Figure 1, Petitioner contends,

Schinabeck discloses a first and second “comparison means” can each compare a response signal to a first and second “programmed voltage level,” respectively [(as indicated by the yellow Over-voltage labels)]; a third and fourth “comparison means” can each compare a response signal to a first and second “programmed current level,” respectively [(as indicated by the orange Test labels)]; and “means for providing a fail signal in the event that the response signal voltage and current [exceed] the first and second programmed voltage levels and first and second programmed current levels, respectively

(Pet. 33–34 (emphases omitted) (citing Ex. 1008, 8:26–52, 9:16–35, 1043–64); Ex. 1008, Fig. 1). Annotated Figure 1 also illustrates the DUT and response signal in green, the comparator outputs in gold, the control circuitry in blue, and a signal from the driver 18a to the DUT in red (*id.*; Ex. 1008, Fig. 1).

In response, Patent Owner first argues Schinabeck fails to teach or suggest “a separate over-voltage output” (PO Resp. 34). More specifically, Patent Owner argues, “the test output and over-voltage output . . . are based on the same input signal from the DUT (but compared to different thresholds)” (*id.*). Patent Owner argues although “Schinabeck teaches settling a threshold reference level to generate a fail signal, so that its control circuitry can ‘register either acceptance or rejection of the DUT, or to specify its quality (*i.e.*, a test output) . . . Schinabeck does not teach or suggest an over-voltage output based on a separate comparison of the same input signal” (PO Resp. 34–35 (citing Ex. 1008, 7:49–50)). According to Patent Owner, “Schinabeck’s disclosure of ‘V-MAX’ and ‘V-MIN’” relied upon by Petitioner to teach the over-voltage threshold, “is instead used to determine whether testing of the DUT should start, and thus is comparing a different signal than the one that would later be used to generate a test output (should testing start)” (*id.* at 35; *see id.* at 36 (citing Ex. 2005 ¶ 78)). Patent

Owner asserts Go/No-go type testing is used for tests that “require unreasonably long times to settle to a stable operating point . . . and, the ‘test plan proceeds’ only if the comparison to the enabled limits (V-MAX and V-MIN) is within the window, and otherwise ‘a fail branch is undertaken’” (*id.* at 35–36 (Ex. 1008, 10:51-64; Ex. 2005 ¶ 77)). Thus, Patent Owner contends Schinabeck’s Go/No-go determination is made “to determine whether testing of the DUT should start”; therefore, “V-MAX and V-MIN are used at different times, and thus compare a different signal, than is subsequently compared when the test beings” (*id.* at 36 (citing Ex. 2005 ¶ 78)).

Patent Owner further contends, “Petitioner fails to show that Schinabeck discloses or renders obvious control circuitry that generates both a ‘test output’ and an ‘over-voltage output’ because Schinabeck’s controller outputs just a single ‘fails signal’ for a given pin of the DUT, regardless of how many comparisons are performed” (PO Resp. 36). Therefore, Patent Owner contends, “Schinabeck’s single ‘fail signal’ cannot be used to satisfy both of these two separate outputs in the claim” as Patent Owner argues Petitioner (*id.* (citing Ex. 2005 ¶ 79)). Patent Owner points to Schinabeck’s disclosure that “only a single fail signal is output for a given pin of the DUT” (*id.* at 37 (citing Ex. 1008, 4:43–66)).

Patent Owner additionally contends, “Petitioner provides no explanation” as to where Schinabeck “suggest[s] generating both a test output and an over-voltage output from the same input signal when Schinabeck’s approach to ‘voltage overshoot’ is to prevent testing from starting” (*id.* at 38). Patent Owner argues, “Petitioner has not explained why a POSITA would have modified Schinabeck to generate a test output **and** an over-voltage output **when performing DUT testing** when Schinabeck

already addresses voltage transient conditions from occurring during the time any test outputs are being generated” (*id.* (citing Ex. 2005 ¶ 82)).

Petitioner responds that “Schinabeck discloses a test output and over-voltage output based on a separate comparison of the same single input signal from a DUT (Pet. Reply 15 (citing Pet. 28–35)). In particular, Petitioner further contends, “Schinabeck discloses each comparator has a ‘programmed reference[] level’ and each [is] programmed to have different values” (*id.* (citing Ex. 1008, 4:43–66)). Thus, Petitioner asserts, “one comparator can employ a ‘programmed reference level’ indicating a test threshold and a second comparator circuit can employ a ‘programmed reference level’ indicating an over-voltage threshold and would thus, generate a test output and over-voltage output” (*id.*).

Claim 1 of the ’479 Patent recites:

control circuitry having at least two measured value inputs, each measured value input coupled to the comparison output of one of the at least two comparison sub-circuits, a test output and an over-voltage output, the control circuitry adapted to generate a test output³ from a first subset of the comparison output signals produced by the at least two comparison sub-circuits and to generate the over-voltage output from a second subset of the comparison output signals produced by the at least two comparison sub-circuits

(Ex. 1003, 14:4–13). The ’479 Patent discloses “[a]ny voltage that is out of bounds or otherwise outside of the specified operating range may be considered ‘over voltage’” (Ex. 1003, 4:17–19; *see also id.* at 7:1–6 (voltage above or below the rated operating voltage “are referred to generically as an over-voltage condition”)).

³ We interpret “a test output” as “the test output” to refer to the previously recited “a test output” in this limitation.

Claim 10 of Schinabeck recites:

control means connected to the digitally programmed source means and comparison means for continuing to cause the digitally programmed source means to apply the test signal to and the comparison means to monitor the response signal at the node in the event that the response signal voltage and current have a first predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively; and

means connected to the comparison means and control means for providing a fail signal in the event that the response signal voltage and current have a second predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively

(Ex. 1008, 13:8–14:9). The recited “control means” of Schinabeck are connected to comparison means, thus teaching the “at least two measured value inputs, each measure value input coupled to the comparison output of one of the at least two comparison sub-circuits,” as recited in claim 1 (*id.*; Pet. 30).

Schinabeck, in claim 10, additionally teaches the control means monitors “in the event that the response signal voltage and current have a first predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively” (Ex. 1003, 13:8–14:9; Pet. 31, 34). Further support is found in Schinabeck’s teaching that describes the PMU comprises two ADCs (analog to digital converters) (Ex. 1008, 8:1–5, 10:43–50; Pet. 34). Schinabeck teaches “measured value results are available by reading the ADC result,” each of which is “compared to enabled limits” (Ex. 1008, 10:49–50; Pet. 34). Thus, Schinabeck teaches a comparison of input from the comparator

measuring the signal's voltage and input from the comparator measuring the current's voltage, respectively, relative to enabled limits (Ex. 1008, 10:3–64; Pet. 34). Therefore, Schinabeck teaches “at least two measured value inputs, each measured value input coupled to the comparison output of one of the at least two comparison sub-circuits [(e.g., outputs of comparators 26a and 26b and outputs of comparators 26c and 26d)],” as recited in claim 1 of the '479 Patent.

As Schinabeck describes a programmed level for each comparator, we agree with Petitioner that “a first comparator circuit can be given a ‘reference level’ that indicate[s] a test threshold and a second comparator circuit can be given a ‘reference level’ that indicates an over-voltage threshold” (Pet. 31; Ex. 1008, 8:6–18, 9:18–35, 10:43–64, 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 98–99)). Additionally, despite Schinabeck's disclosure of a fail signal, Schinabeck teaches two different signals (voltage and current) are analyzed to provide that fail signal (Ex. 1008, 5:4–8, 14:3–9). Because Schinabeck teaches generating a comparison, we determine Schinabeck teaches generating an output—one a test output and one an over-voltage output.

Patent Owner's contentions directed toward Schinabeck's Go/No-go determination address only one embodiment of Schinabeck, but does not address Petitioner's assertions regarding Schinabeck's teachings and particularly, claim 10 and disclosure in column 4, line 66 through column 5, line 8 (PO Resp. 35–37).

Accordingly, we determine Petitioner has shown Schinabeck teaches “generat[ing] a test output from a first subset of the comparison output signals produced by the at least two comparison sub-circuits” and “generat[ing] the over-voltage output from a second subset of the

comparison output signals produced by the at least two comparison sub-circuits,” as recited in claim 1 of the ’479 Patent.

d) Remaining Limitation

Petitioner contends Schinabeck teaches the preamble (“[a]utomatic test equipment adapted to execute a user program, the test equipment comprising:” (Pet. 22–23 (citing Ex. 1008, 1:8–9, 50–55; 2:3–22, 7:59–60, 3:30–33; Ex. 1001 ¶ 88))).

Patent Owner does not dispute Petitioner’s contentions for the preamble of claim 1 (*see* PO Resp.). Based on Petitioner’s persuasive contentions and evidence, we determine Schinabeck teaches the preamble.

Petitioner contends Schinabeck teaches the remaining limitation — “wherein the automatic test equipment is adapted to independently set the value of the threshold input signal for each of the at least two comparison sub-circuits based on the user program” — recited in claim 1 (Pet. 35 (citing Ex. 1008, 3:56–63, 4:43–66, 8:6–18, 9:16–35, 11:43–68, 12:46–14:9; Ex. 1001 ¶¶ 109–110))).

Patent Owner does not dispute Petitioner’s contentions for this limitation of claim 1 (*see* PO Resp.). Based on Petitioner’s persuasive contentions and evidence, we determine Schinabeck teaches this limitation.

e) Conclusion

For the reasons explained above, we find Schinabeck teaches or suggests the subject matter of claim 1. Therefore, based on Petitioner’s persuasive evidence and argument, we conclude Petitioner has established by a preponderance of evidence that Schinabeck renders obvious the subject matter of claim 1.

3. *Analysis of Claim 2*

Petitioner contends Schinabeck teaches the limitations as recited in claim 2 (Pet. 35–36). In particular, Petitioner asserts Schinabeck teaches the limitations as recited, based on their contentions set forth with respect to claim 1 (*id.*).

Patent Owner contends, “Petitioner’s arguments for claim 2 fail for the same reasons as discussed with respect to claim 1” (PO Resp. 39). For the reasons set forth with respect to claim 1 and further based on Petitioner’s showings for claim 2, we determine Petitioner has shown that Schinabeck teaches the elements of claim 2. Therefore, based on Petitioner’s persuasive evidence and argument, we conclude that Petitioner has established by a preponderance of evidence that claim 2 is rendered obvious by Schinabeck.

4. *Analysis of Claims 3 and 4*

Petitioner asserts Schinabeck teaches the subject matter of claims 3 and 4 (Pet. 36–37). Claim 3 recites “[t]he automatic test equipment of claim 2 wherein the at least two comparison sub-circuits in each of the plurality of channel circuits comprises four comparison sub-circuits and each channel circuit additionally comprises a driver” (Ex. 1003:43–53). Claim 4 recites

[t]he automatic test equipment of claim 1 wherein the control circuitry comprises at least two threshold outputs, each coupled to the threshold input of one of the at least two comparison sub-circuits, and wherein the control circuitry is adapted to provide a signal having a programmable value at each of the threshold outputs

(*id.* at 4:54–68).

Patent Owner does not dispute these assertions, or raise arguments separate from those discussed above with respect to claim 1 from which each of claims 3 and 4 depend (*see generally* PO Resp.). For the reasons set forth with respect to claim 1 and further based on Petitioner’s showing for claims 3 and 4, we find Schinabeck teaches the subject matter of claims 3 and 4. Therefore, based on Petitioner’s persuasive evidence and argument, we conclude Petitioner has established by a preponderance of evidence that claims 3 and 4 are rendered obvious by Schinabeck.

5. *Analysis of Claim 5*

Petitioner argues Schinabeck discloses the limitation of claim 5 (Pet. 37–38). Claim 5 recites:

The automatic test equipment of claim 1 wherein
the test output of the control⁴ indicates the state of the
comparison output signal of at least one of the at least two
comparison sub-circuits relative to an expected state and
the over-voltage output indicates the state of the
comparison output signal of at least one of the at least two
comparison sub-circuits

(Ex. 1003, 14:49–54). Petitioner contends Schinabeck discloses “[t]he comparison means 26a can also receive a predicted signal from the test head controller.” (Pet. 38 (citing Ex. 1008, 7:34–50)). Petitioner further asserts, “[a]fter the comparison means compares the response signal and the predicted signal, ‘[t]he output signals from the comparator circuits are returned to the test system computer where they are checked in accordance with a stored program [(expected state)] from the proper responses’” (Pet. 38

⁴ We interpret this as “control circuitry” because claim 1 does not recite a “control” element (Ex. 1003, 13:57–14:17, 14:49–54).

(citing Ex. 1008, 2:14–22, 7:34–50; Ex. 1001 ¶¶ 120–23)). Thus, according to Petitioner, “because the output of the comparison means is next [compared] to the stored program by the control circuitry, Schinabeck discloses that the test output can be based on the recited ‘comparison output signal of at least one . . . comparison sub-circuit relative to an expected state’” (*id.* (citing Ex. 1001 ¶¶ 122–23)). Petitioner further asserts, Schinabeck discloses the “over-voltage output indicates the state of the comparison output signal of at least one of the . . . comparison sub-circuits,” as recited in claim 1 (*id.* (citing Ex. 1001 ¶¶ 124–25.))

Patent Owner argues, “... claim 5 requires that the *control circuitry*’s test output ‘indicates the state of the comparison output signal . . . relative to an expected state’” but, Petitioner “misapplies terms” and points to “Schinabeck’s *test system computer*—not Schinabeck’s purported control circuitry” (PO Resp. 39–40 (citing Ex. 1003, 14:49–54; Pet. 38)). According to Patent Owner, “Petitioner mapped Schinabeck’s ‘test head controller’ and ‘test system controller’ as the claimed ‘control circuitry’ . . .” (*id.* at 40). However, Patent Owner contends, “Petitioner now improperly points to a test system computer—an entirely different component in Schinabeck” (*id.* (citing Ex. 2001 ¶ 85; Pet. 28); PO Sur-reply 15).

Petitioner asserts, “the ’479 patent is clear: ‘*any* suitable control circuit’ may be used . . . (includ[ing] components such as ‘Schinabeck’s test system computer’” (Pet. Reply 17 (citing Ex. 1003, 6:3–6; Ex. 1027 ¶ 16)).

Schinabeck teaches

[t]he output signals from the comparator circuits are returned to the test system computer where they are checked in accordance with a stored program for the proper responses. In this manner, electronic components, for example, semiconductor memories or

other integrated circuits, can be individually tested to assure that they meet whatever standard or specification the ultimate user of the integrated circuit desires

(Ex. 1008, 2:14–22; *see* Pet. 38). Schinabeck also teaches “the switch means are controlled by a computer means” and “the computer means comprises a test system controller” (*id.* at 12:1–2, 5–6). Thus, we determine an ordinarily skilled artisan upon reading Schinabeck would have understood “test system computer” to include the test system controller.

Patent Owner further argues, “[c]laim 5 also requires that the control circuitry’s over-voltage output indicate the ‘state of the comparison output signal of at least one of the at least two comparison sub-circuits,’” but Petitioner provides no explanation as to what discloses this recited element (PO Resp. 40 (citing Pet. 22–35, 38; Ex. 2001 ¶ 86)). Patent Owner additionally maintains Petitioner pointed to a ‘fail signal’ provided by that circuitry as the claimed ‘test output’” (PO Sur-reply 15 (citing Pet. 28–32)).

Petitioner responds, “Schinabeck discloses control circuitry that may generate an over-voltage output if the comparator circuit output signal exceeds an over-voltage reference level” (Pet. Reply 17–18 (citing Pet. 28–32, 39–40)).

As set forth *supra*, Schinabeck teaches

[t]he output signals from the comparator circuits are returned to the test system computer where they are checked in accordance with a stored program for the proper responses. In this manner, electronic components, for example, semiconductor memories or other integrated circuits, can be individually tested to assure that they meet whatever standard or specification the ultimate user of the integrated circuit desires

(Ex. 1008, 2:14–22; *see* Pet. 38). Schinabeck also teaches controls means that receives data from the digitally programmed source means and

comparison means, that monitors the response signal, particularly, whether “the response signal voltage and current have a first predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively” and

means connected to the comparison means and control means for providing a fail signal in the event that the response signal voltage and current have a second predetermined relationship with respect to the first and second programmed voltage levels and first and second programmed current levels, respectively

(Ex. 1008, 14:2–14:9; *see also id.* at 11:42–68). Thus, Schinabeck teaches the “control means” monitors the relationship between the response signal and programmed levels (*id.*; Pet. 38; Ex. 1001 ¶¶ 122–23). We determine this monitoring by Schinabeck indicates the state of the comparison output signal and, further, the recited “means connected” teaches providing (“generating”) an output that indicates the state of the comparison output signal relative to an expected state (“relationship with respect to” programmed levels) (*see* Ex. 1008, 11:42–68, 13:8–14:9). As set forth *supra*, we find Schinabeck teaches generating “a test output” and “an over-voltage output.” We further find these signals indicate the state as recited. Accordingly, we find Schinabeck teaches

The automatic test equipment of claim 1 wherein

the test output of the control⁵ indicates the state of the comparison output signal of at least one of the at least two comparison sub-circuits relative to an expected state and
the over-voltage output indicates the state of the comparison output signal of at least one of the at least two comparison sub-circuits,

⁵ We interpret this as “control circuitry” because claim 1 does not recite a “control” element (Ex. 1003, 13:57–14:17, 14:49–54).

as recited in claim 5 (Ex. 1003, 14:49–54). Based on Petitioner’s persuasive evidence and argument, we conclude that Petitioner has established by a preponderance of evidence that claim 5 is rendered obvious by Schinabeck.

6. Analysis of Claim 6

Petitioner argues Schinabeck discloses the subject matter of claim 6 (Pet. 38–39). Claim 6 recites:

The automatic test equipment of claim 5 wherein the state of the over-voltage output is based on whether the signal at the signal input has a value between the values of the signals at the threshold inputs of two of the at least two comparison sub-circuits

(Ex. 1003, 14:55–59).

Patent Owner does not dispute these assertions, or raise arguments separate from those discussed above with respect to claims 1 and 5 from which claim 6 depends (*see generally* PO Resp.). For the reasons set forth with respect to claims 1 and 5, and further based on Petitioner’s showing for claim 6, we find Schinabeck teaches the subject matter of claim 6. Therefore, based on Petitioner’s persuasive evidence and argument, we conclude Petitioner has established by a preponderance of evidence that claim 6 is rendered obvious by Schinabeck.

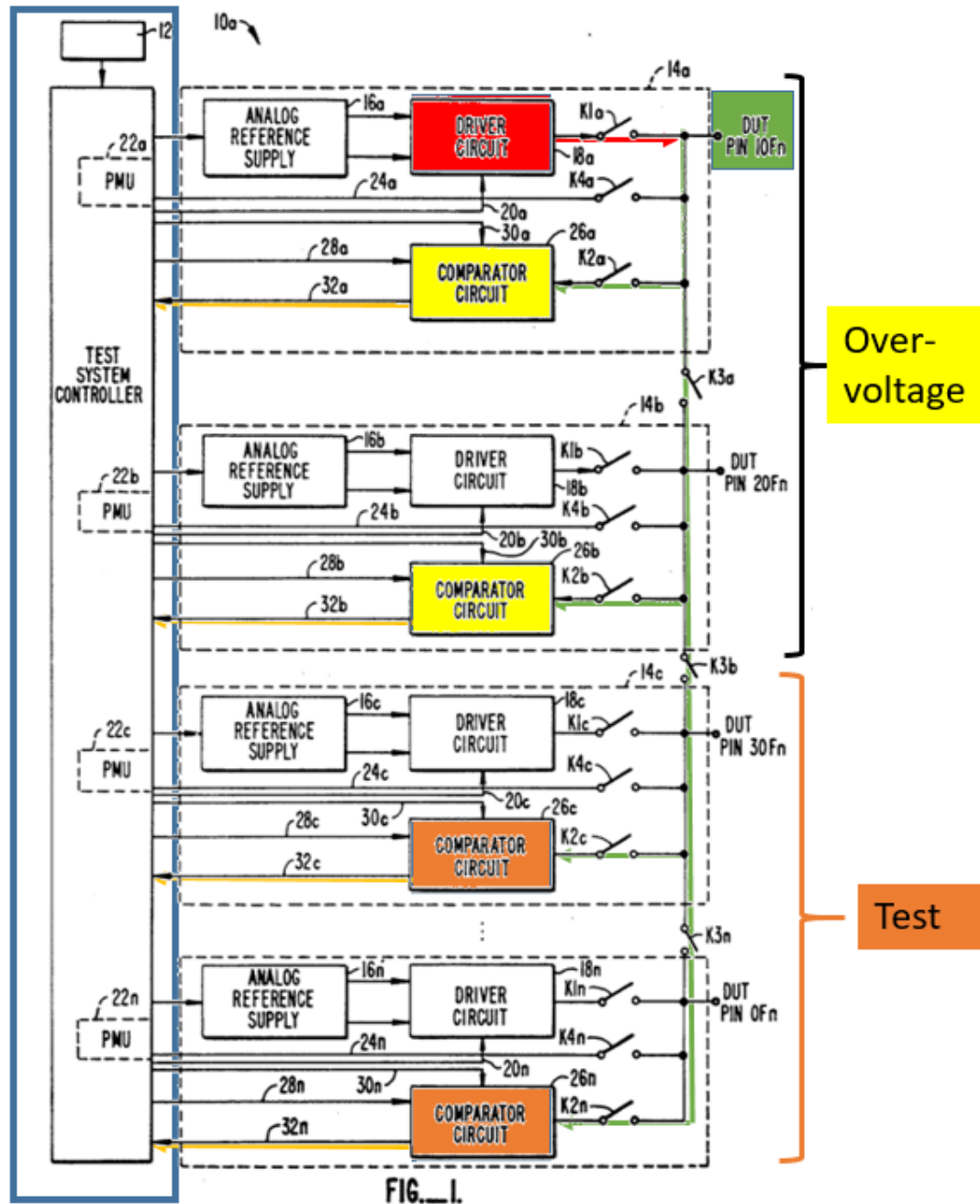
7. Analysis of Claim 7

Petitioner argues Schinabeck discloses the limitation of claim 7 (Pet. 39–42). Claim 7 recites:

The automatic test equipment of claim 6 additionally comprising
a driver coupled to the signal connection point and

disconnect circuitry connected between the output of the driver and the signal connection point, the disconnection circuitry having a control input coupled to the over-voltage output of the control circuitry

(Ex. 1003, 14:60–65). Petitioner contends, Schinabeck’s Figure 1 discloses “the recited ‘driver coupled to the signal connection point’ and ‘disconnect circuitry connected between’ the two” (Pet. 39–40 (citing Ex. 1003, 14:60–65; Ex. 1008, Fig. 1 (annotated))).



(Ex. 1008, Fig. 1 (annotated by Petitioner)). Petitioner has annotated Figure 1 to show comparator circuits 25a and 25b in yellow used in generating an over-voltage output; comparator circuits 26c and 26d in orange used in generating a test output; the DUT and response signal in green; the comparator outputs in gold; the control circuitry in blue; and the driver circuit 18a and signal connection point in red (Pet. 40–41; Ex. 1008, Fig. 1).

Petitioner asserts the driver circuit “switch[es] . . . signals onto . . . the pins of the [DUT]” when switch K1a is closed.” (Pet. 41 (citing Ex. 1008, 2:3–8, 6:63–7:11) (“test head controller . . . closes a relay contact K1a . . . to connect the test stimuli . . . to pin 1 of the DUT”), 11:43–68, 12:46–14:9)).

Petitioner continues, “Schinabeck also discloses that the PMU can ‘suppl[y] desired voltages or currents to the appropriate pin of the DUT’ by closing switch K4a ‘to enable coupling of pin 1 of the DUT to the PMU’ (*id.* (citing Ex. 1008, 7:17–26, 7:64–8:1)). Petitioner thus asserts, “in both instances, there is a switch between the driver and the signal connection point . . . both switches [being] controlled by the control circuitry” (*id.* (citing Ex. 1008, 6:63–7:26, 11:43–12:2, 12:46–14:9; Ex. 1001 ¶¶ 130–132)).

Petitioner further argues that “Schinabeck renders the recited “disconnect circuitry having a control input coupled to the output of the control circuitry” obvious as such circuitry was known in the prior art and it would have been apparent that it could activate the switch based on the over-voltage output.” (*id.* (citing Ex. 1003, 1:54–61); Ex. 1003, 1:54–61)). According to Petitioner, an ordinarily skilled artisan “would have understood that Schinabeck’s switches, which already are controlled by the control circuitry, could include a control input connected to the over-voltage output of the control circuitry” (*id.* at 41–42 (citing Ex. 1003, 1:54–61; Ex. 1001 ¶¶ 133–35)).

Petitioner contends an ordinarily skilled artisan “would be motivated and have the knowledge to modify Schinabeck to include this control input to prevent ‘voltage overshoot [that] can damage the [DUT],’ by adding a control line to open the switch in the event of such an ‘overshoot,’ thereby disconnecting the ATE from the DUT” (Pet. 42). According to Petitioner,

“[s]uch a modification would have been obvious to try as there already was an identified, predictable solution for disconnecting switches in response to an over-voltage output and, thus, would have a reasonable expectation of success and predictable results” (*id.* (citing Ex. 1008, 3:13–15; Ex. 1001 ¶¶ 133–135)).

Patent Owner argues, “Petitioner alternatively maps either (i) switch K1a and driver circuit 18a or (ii) switch K4a and PMU 22a as the recited ‘disconnect circuitry’, but Petitioner has failed to show that the switches are coupled to over-voltage output of the control circuitry” (PO Resp. 40–41 (citing Pet. 40–41)). Patent Owner alleges that contrary to it being “obvious to modify Schinabeck to ‘include a control input connected to the over-voltage output of the control circuitry’ to ‘prevent ‘voltage overshoot [that] can damage the [DUT]’, ... Schinabeck’s approach to ‘voltage overshoot’ is to prevent testing from ever occurring” (*id.* at 41 (citing Schinabeck, 3:13–15; Horenstein ¶ 87)).

Petitioner responds to Patent Owner’s contention by asserting an ordinarily skilled artisan “would have understood that Schinabeck’s ‘Go/No-go’ testing is but one embodiment for over-voltage testing [as] such a modification was well-known” (Pet. Reply 19 (citing PO Reply 39–42; Ex. 1003, 1:58–61, Ex. 1026, 18:20–24)).

Patent Owner replies that “Petitioner effectively concedes that Schinabeck does not disclose the disconnect circuitry of claim 7, and instead argues only that it would have been obvious to modify Schinabeck to include this feature to prevent voltage overshoot” (PO Sur-Reply 16 (citing Pet. 40–41; PO Reply 18–19)). Relying on its expert, Patent Owner argues, “Schinabeck’s approach to ‘voltage overshoot’ is Go/No-go testing to prevent testing from ever occurring, rather than disconnecting switch K1a”

(PO Sur-Reply 16 (citing Ex. 2005 ¶ 87)). Patent Owner argues that “Petitioner’s reply is just a vague, general assertion that Go/No-go testing is ‘but one embodiment’—ignoring that Go/No-go testing is the embodiment the Petition relied upon” (PO Sur-reply 16 (citing Pet. 31 (the V-MAX, V-MIN thresholds from Go/No-go testing))).

Petitioner has articulated reasoning as to why an ordinarily skilled artisan would have modified “Schinabeck to include this control input to prevent ‘voltage overshoot [that] can damage the [DUT],’ . . . by adding a control line to open the switch in the event of such an ‘overshoot,’” thereby disconnecting the ATE from the DUT” (Pet. 42). As previously discussed, Schinabeck discloses switches that can be closed or opened (*see* Ex. 1008, 2:3–8, 6:63–7:11, 11:43–12:2, 12:46–14:9, Fig. 1). In particular, Schinabeck describes closing a relay contact K1a to connect test stimuli to a pin of the DUT, i.e., Schinabeck describes its circuitry (“control circuitry”) controlling the relay contact K1a (*id.* at 6:63–7:11). Schinabeck additionally describes issues with voltage overshoot in testing and describes monitoring response signals to assure proper responses (Ex. 1008, 2:13–22, 3:13–15). Schinabeck further describes producing a signal which is then used to determine whether to proceed with the test plan or undertake a fail branch (*id.* at 10:60–64). We credit Dr. Wicker’s testimony that an ordinarily skilled artisan “would have understood that Schinabeck’s switches, which are already controlled by the control circuitry, could include a control input connected to the over-voltage output of the control circuitry” (Ex. 1001 ¶ 133). Indeed, Schinabeck discloses providing a signal in the case of a voltage overshoot (Ex. 1008, 11:54–12:2, 13:8–14:9). We further credit Dr. Wicker’s testimony that “[s]uch a modification would have been obvious to try as there already was an identified, predictable solution for

disconnecting switches in response to an over-voltage output and, thus, would have a reasonable expectation of success and predictable results” (Ex. 1001 ¶¶ 133–135 (citing Ex. 1003, 1:54–61)). The ’479 Patent supports Dr. Wicker’s testimony that disconnecting switches was known:

Some test instruments include protective circuitry that isolates circuitry in the test instrument from an input when the voltage and/or current applied at the input exceeds a rated value. Traditional and solid state fuses are used for this purpose. Also, switches have been used along with a voltage sensing circuit that activates the switch to disconnect the test instrument from an input when the voltage or current at the input exceeds a specific value

(Ex. 1003, 1:54–61). Dr. Horenstein additionally admitted in his testimony that “switches have been used along with voltage-sensing circuits to disconnect the test instrument from an input” (Ex. 1026, 18:20–24). Thus, because we determine Schinabeck teaches detecting an over-voltage; protecting a device from over-voltage during testing; and using switches connected to control circuitry, to close or open circuits to the device under test. We also find Dr. Wicker’s testimony articulates reasoning with a rational underpinning as to why an ordinarily skilled artisan would have modified Schinabeck in the manner recited and why such a modification would have been within the skill of an ordinarily skilled artisan (*see* Ex. 1001 ¶¶ 133–135). Accordingly, we determine Schinabeck teaches

a driver coupled to the signal connection point and

disconnect circuitry connected between the output of the driver and the signal connection point, the disconnection circuitry having a control input coupled to the over-voltage output of the control circuitry

as recited in claim 7 (Ex. 1002, 14:60–65).

For the reasons set forth with respect to claims 1, 5, and 6 and further based on Petitioner's showings for claim 7, we determine Petitioner has shown that Schinabeck renders the elements of claim 7 obvious. Therefore, based on Petitioner's persuasive evidence and argument, we conclude that Petitioner has established by a preponderance of evidence that claim 7 is rendered obvious by Schinabeck.

8. Analysis of Claim 8

Petitioner argues Schinabeck discloses the limitation of claim 8 (Pet. 41). Claim 8 recites:

The automatic test equipment of claim 7 wherein the control circuitry comprises at least one low pass filter and/or delay element coupled between the over-voltage output and the comparison outputs of the two of the at least two comparison sub-circuits.

(Ex. 1003, 14:66–15:3). In particular, Petitioner asserts that “[Schinabeck’s] PMUs have delays and ‘programmable filter settings’” where “the PMU is provided between the over-voltage output and the comparator” (Pet. 42–43 (citing Pet. 22–35; Ex. 1008, 8:53–9:15, 10:12–64, Fig. 1; Ex. 1001 ¶¶ 136–38)).

Patent Owner argues that the PMU “is not located in the claimed signal path between ‘the comparison output of the at least two comparison sub-circuits’ and the alleged ‘over-voltage output’” (PO Resp. 41).

Specifically, according to Patent Owner, Schinabeck’s PMU is not in the signal path between Schinabeck’s comparator output signal 32 (which Petitioner maps to the claimed comparison output) and the purported over-voltage output of the control circuitry (which Petitioner maps as ‘test head controller’) . . . [and] does not process that signal when it reaches the test

system controller” (*id.* (citing Pet. 43.)) Patent Owner points to Figure 1, “show[ing] that the PMU is not located on line 32 and does not process that signal when it reaches the test system controller” (*id.* (citing Pet. 26; Ex. 2005 ¶ 88)).

Petitioner responds that “Schinabeck discloses returning output signal from comparison means 26a to test head controller 12 via line 32, of which PMUs are a part” and “the PMU itself can be assigned as an output comparator” (Pet. Reply 19 (citing Ex. 1008, 7:42–50; Ex. 1026, 71:3–19)).

Patent Owner, however, disputes that Schinabeck’s PMU is on the signal line 32 and, further, that “the purported [low pass filter] or delay element within the PMU is coupled between the recited features, even though there are multiple paths through the PMU (PO Sur-reply 17 (citing Ex. 1008, 7:42–50, Fig. 2)). Patent Owner also argues Petitioner first argued “the PMU can be assigned as an output comparator” in the Reply while “the Petition mapped comparator 26a—*not* the PMU—as the comparison sub-circuit of claim [8]” (*id.* (citing Pet. Reply 19)).

Figure 1 of Schinabeck depicts a “Test System Controller” element receiving at least an “output signal from the comparison means 26a on the line 32a” and including multiple PMU 22a–n elements (Ex. 1008, 7:47–50, Fig. 1). Schinabeck further describes use of filters in the PMUs (*id.* at 10:12–64; Pet. 43). Thus, we determine the test head and test system controller (“control circuitry” as annotated by Petitioner in blue in Figure 1 of Schinabeck) comprises at least one low pass filter which is between the over-voltage output and the comparison outputs (lines 32a and 32b) of the comparison circuits 26a and 26b. While Figure 1 does not specifically show the line 32a abutting the PMU element bounded by dashed lines, Schinabeck describes that the PMU includes comparators that compare and monitor test

signals (*id.* at 8:1–5, 19–26, 10:56–61, Fig. 2), which as discussed *supra*, are used in generating the control circuitry outputs (Pet. 34–35; Ex. 1008, 13:8–14:9). Thus, we determine Schinabeck has description that supports Petitioner’s assertion despite Figure 1. Accordingly, we determine Schinabeck describes use of filters in the PMUs, which are part of the test system controller. We therefore determine Petitioner has shown Schinabeck teaches “the control circuitry comprises at least one low pass filter and/or delay element coupled between the over-voltage output and the comparison outputs of the two of the at least two comparison sub-circuits,” as recited in claim 8.

For the reasons set forth with respect to claims 1 and 5–7 and further based on Petitioner’s showings for claim 8, we determine Petitioner has shown that Schinabeck teaches the elements of claim 8. Therefore, based on Petitioner’s persuasive evidence and argument, we conclude that Petitioner has established by a preponderance of evidence that claim 8 is rendered obvious by Schinabeck.

9. Determination of Unpatentability

For the reasons discussed above and based on the full trial record, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the subject matter recited in claims 1–8 would have been obvious over the teachings of Schinabeck.

E. Grounds 2 and 3: Alleged Obviousness over Miyamoto and Frame – Claims 1–7 and over Miyamoto, Frame and Schinabeck – Claim 8

Petitioner contends the combination of Miyamoto and Frame renders independent claims 1–7 obvious (Pet. 49–69) and the combination of

Miyamoto, Frame, and Schinabeck renders claim 8 obvious (*id.* at 75). Because Ground 1 is dispositive as to all challenged claims, we need not reach Grounds 2 and 3 (*see SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding that a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (non-precedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding” and, thus, agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”)). In light of our determination that Petitioner has established by a preponderance of the evidence that Schinabeck renders claims 1–8 obvious, we take no position on whether the same claims are also obvious over the combination of the teachings and suggestions of Miyamoto and Frame and Miyamoto, Frame, and Schinabeck.

III. CONCLUSION⁶

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that the challenged claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–8	103	Schinabeck	1–8	
1–7	103 ⁷	Miyamoto, Frame		
8	103 ⁸	Miyamoto, Frame, Schinabeck		
Overall Outcome			1–8	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–8 of the '995 patent have been shown to be unpatentable; and

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding* (see 84 Fed. Reg. 16,654 (Apr. 22, 2019)). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices (see 37 C.F.R. § 42.8(a)(3), (b)(2)).

⁷ As explained above, we do not reach this rejection, as we determine the issue is not necessary to the resolution of the proceeding.

⁸ As explained above, we do not reach this rejection, as we determine the issue is not necessary to the resolution of the proceeding.

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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