

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
STMICROELECTRONICS, INC.,
Petitioners,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-00985¹
Patent 6,651,134 B1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ STMicroelectronics, Inc., which filed a petition in IPR2021-00355, has been joined as a party to this proceeding.

I. INTRODUCTION

A. BACKGROUND

Advanced Micro Devices, Inc., (“AMD”) filed a Petition (Paper 1, “Pet.”) requesting institution of *inter partes* review of claims 1–21 (“the challenged claims”) of U.S. Patent No. 6,651,134 B1 (Ex. 1001, “the ’134 patent”). Monterey Research, LLC, (“Patent Owner”) filed a Preliminary Response. Paper 9. After our email authorization, Petitioner filed a Preliminary Reply (Paper 10) and Patent Owner filed a Preliminary Sur-Reply (Paper 11). We instituted review. Paper 13 (“Institution Decision” or “Inst.”).

After we instituted review, STMicroelectronics, Inc. (“STM”) was joined as a Petitioner to this proceeding. Paper 23. Thus, AMD and STM are, collectively, the “Petitioner.” Patent Owner filed a Response. Paper 19 (“PO Resp.”). Petitioner filed a Reply. Paper 21 (“Pet. Reply”). Patent Owner filed a Sur-Reply. Paper 22 (“PO Sur-Reply”). We held a hearing on September 1, 2021, and a transcript appears in the record. Paper 30 (“Tr.”).

This is a final written decision as to the patentability of the challenged claims. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–21 of the ’134 patent are unpatentable.

B. REAL PARTIES IN INTEREST

AMD identifies itself and ATI Technologies ULC as the real parties in interest. Pet. 3. STM identifies itself, a related company under common ownership, STMicroelectronics International N.V., and their parent company, STMicroelectronics N.V., as real parties in interest. IPR2021-

00355, Paper 1, 3. Patent Owner identifies itself and IPValue Management as real parties in interest. Paper 5, 1.

C. RELATED MATTERS

The parties identify the following matters related to the '134 patent: *Monterey Research, LLC v. Qualcomm Inc.*, No. 1:19-cv-02083-NIQA-LAS (D. Del.); *Monterey Research, LLC v. Nanya Tech. Corp.*, No. 1:19-cv-02090-NIQA-LAS (D. Del.); *Monterey Research, LLC v. Advanced Micro Devices Inc.*, No. 1:19-cv02149-NIQA-LAS (D. Del.); *Monterey Research, LLC v. STMicroelectronics N.V.*, No. 1:20-cv-00089-NIQA-LAS (D. Del.); *Monterey Research, LLC v. Marvell Tech. Grp. Ltd.*, No. 1:20-cv-00158-NIQA-LAS (D. Del.); and *Marvell Semiconductor, Inc. v. Monterey Research, LLC*, No. 3:20-cv-03296 (N.D. Cal.). Pet. 3; Paper 5, 1.

The parties identify two additional adjudications, now complete, which involved the '134 patent: *In the matter of: Certain Static Random Access Memories and Products Containing Same*, Inv. No. 337-TA-792 (ITC); and *Cypress Semiconductor Corp. v. GSI Tech., Inc.*, No. 3:13-cv-02013-JST and No. 3:13-cv-03757-JST (N.D. Cal.). Pet. 3; Paper 5, 1–2.

D. THE '134 PATENT

The '134 patent is titled Memory Device with a Fixed Length Non Interruptible Burst. Ex. 1001, code (54). The patent discloses that “the data burst transfers of conventional memories can be interrupted and single access made,” and proposes a memory device “that has a fixed burst length.” *Id.* at 1:37–45.

Figure 1 is reproduced below:

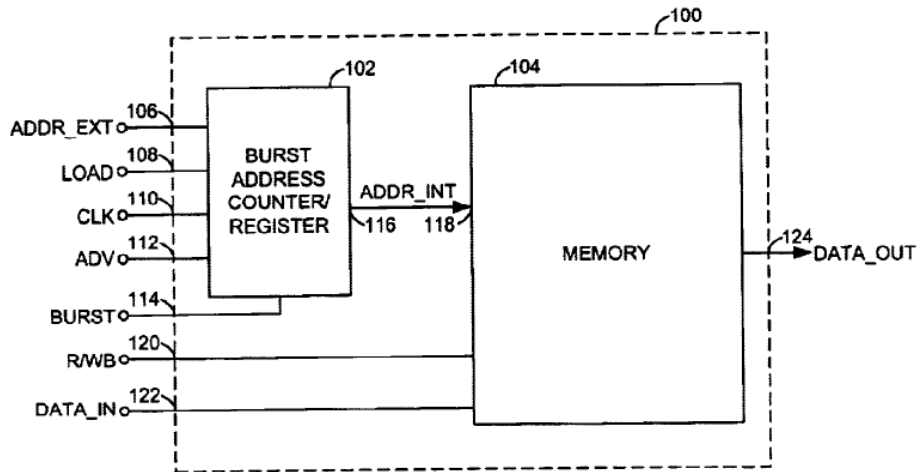


FIG. 1

Ex. 1001, Fig. 1. Figure 1 depicts circuit 100 configured as a fixed burst memory, in which circuit 102 accepts external signals including external address signal ADDR_EXT, and “generate[s] the signal ADDR_INT as a fixed number of addresses in response to the signal CLK.” *Id.* at 3:21–22. The ’134 patent states that “[o]nce the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).” *Id.* at 3:25–28.

The ’134 patent depicts two embodiments for circuit 102, in Figures 2 and 3. Figure 2 is reproduced below:

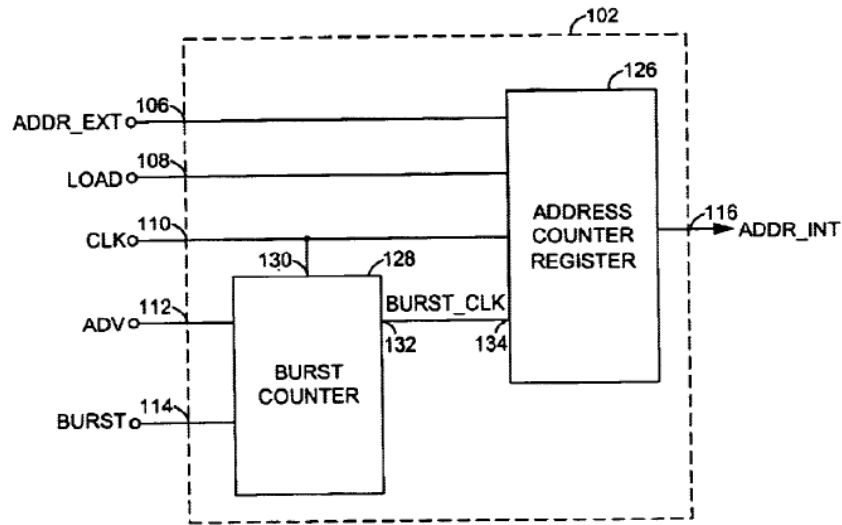


FIG. 2

Id. Fig. 2. Figure 2 shows burst counter 128 receiving signal CLK (a clock signal), signal ADV, and signal BURST, and providing signal BURST_CLK. “When the signal ADV is asserted, the burst counter 128 will generally present the signal BURST_CLK in response to the signal CLK. The signal BURST_CLK generally contains a number of pulses that has been programmed by the signal BURST.” *Id.* at 4:10–14. Figure 3 and the associated description disclose an alternative circuit, in which “counter 138 may be configured to generate a number of addresses in response to the signals CLK, BURST[,], and ADV” and where “[t]he number of addresses generated by the counter 138 may be programmed by the signal BURST.” *Id.* at 4:29–31. The ’134 patent describes more generally that, “[w]hen the signal ADV is asserted, the circuit 100 will generally generate a number of address signals” and that “[t]he address signals will generally continue to be generated until the Nth address signal is generated.” *Id.* at 4:42–48.

E. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. A circuit comprising:
 - a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and
 - a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

Ex. 1001, 5:22–32. Independent claim 16 recites limitations similar to those of claim 1, expressed as means-plus-function elements. *Id.* at 6:20–30.

Independent claim 17 recites limitations similar to those of claim 1, expressed as a “method of providing a fixed burst length data transfer.” *Id.* at 6:31–39. Claims 2–15 depend, directly or indirectly, from claim 1. *Id.* at 5:33–6:19. Claims 18–21 depend, directly or indirectly, from claim 17. *Id.* at 6:40–48.

F. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1–3, 8, 12, 13, 16, 17	102	Wada ²
1–4, 8, 12–14, 16, 17	103	Wada
1–4, 8, 12–14, 16, 17	103	Wada, Barrett ³

² U.S. Patent No. 6,115,280 (Ex. 1005).

³ U.S. Patent No. 5,584,033 (Ex. 1010).

Claim(s) Challenged	35 U.S.C. §	References/Basis
4–7, 18–20	103	Wada, Fujioka ⁴
4–7, 18–20	103	Wada, Barrett, Fujioka
9–10, 14, 21	103	Wada, Reeves ⁵
9–10, 14, 21	103	Wada, Barrett, Reeves
11, 15	103	Wada, Lysinger ⁶
11, 15	103	Wada, Barrett, Lysinger

Pet. i–iii, 5. Petitioner relies also on the Declaration of R. Jacob Baker, Ph.D., P.E. Ex. 1002.

II. ANALYSIS

A. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner proposes that a person of ordinary skill “would have had a bachelor’s degree in electrical or computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 11 (citing Ex. 1002 ¶ 43). Patent Owner does not dispute this definition of a person of ordinary skill. *See generally* PO Resp. We adopt Petitioner’s proposed level of ordinary skill as it is consistent with the level of skill reflected in the specification and in the asserted prior art references.

⁴ U.S. Patent No. 6,185,149 (Ex. 1006).

⁵ U.S. Patent No. 6,226,755 (Ex. 1008).

⁶ U.S. Patent No. 5,748,331 (Ex. 1009).

B. CLAIM CONSTRUCTION

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Under this standard, a claim is construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* Only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

I. “non-interruptible”

As to “non-interruptible,” Petitioner submits that the prior art discloses the claim elements under the following construction adopted by the parties in an International Trade Commission (ITC) investigation—“cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated.” Pet. 12 (citing Ex. 1011, 12–13). We adopted that construction in the Institution Decision. Inst. 8–9. Patent Owner agrees with that construction (PO Resp. 21), and we apply it here.

One dispute in this proceeding relates to whether the prior art discloses a non-interruptible burst; specifically, whether the need to maintain an external control signal prevents a burst from being “non-interruptible.” We stated in the Institution Decision that the agreed construction would not encompass “a circuit in which burst operation depends on external control.” Inst. 18. Patent Owner relies on that view of the claim scope to argue that the claim excludes a system in which an external signal must be maintained in a certain state for a burst to be completed. PO Resp. 28.

We note that the claim itself requires certain external signals for the claimed address generation. Claim 1 recites a logic circuit configured to generate address signals “in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals.” Ex. 1001, 5:22–32. Those three recited external signals may influence the circuit’s ability to generate internal addresses as claimed. For example, stopping the clock signal or removing power from the circuit would prevent (or interrupt) address generation. *See* Pet. Reply 12; Tr. 19:17–22. Doing so, however, would prevent all operation by the circuit. This, in our view, would not represent an interrupted burst, which we determine requires interruption during continued circuit operation, such as interruption to generate a new burst or to accept another command. Thus, as a matter of logic, the need to maintain the clock signal does not render address generation interruptible.

Further, we agree with Patent Owner that the claimed “external address signal” need only be provided at the beginning of the process, not maintained throughout, for the circuit to generate a burst of address signals. *See* Tr. 54:11–13. As the specification instructs, that external address signal provides an “initial address” to “determine the initial location where data transfers to and from the memory 104 will generally begin.” Ex. 1001, 2:66–3:4.

The parties agree that the “one or more control signals” term relates to the ADV signal described in the specification. *See, e.g.*, Tr. 12:19–23, 54:15–18; Ex. 1001, 3:5–6 (“The signal ADV may be, in one example, used as a control signal.”). The corresponding signal in the prior art lies at the core of the parties’ dispute regarding using control signals to generate address signals without interruption.

The specification describes that “[w]hen the signal ADV is asserted, the circuit 100 will generally begin transferring a predetermined number of words.” Ex. 1001, 3:8–10. It states that the “[t]he transfer is generally non-interruptible.” *Id.* at 3:10–11. The specification describes also that the ADV signal may be combined with a LOAD signal, which loads the initial address, as the combined ADV/LDb signal. *Id.* at 3:14–15. It states that “[w]hen the signal ADV/LDb is in the first state, the circuit 102 will generally load an address presented by the signal ADDR_EXT as an initial address” and that “[w]hen the signal ADV/LDb is in the second state, the circuit 102 may be configured to generate the signal ADDR_INT as a fixed number of addresses in response to the signal CLK.” *Id.* at 3:17–22. Just like the standalone ADV signal, the specification states that, for the combined ADV/LDb signal, “[o]nce the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (e.g., a non-interruptible burst).” *Id.* at 3:25–28.

Ultimately, we conclude that we need not resolve whether the need to hold the ADV line high to complete a burst renders the burst interruptible and, therefore, is outside the claim scope. As discussed below, Petitioner’s assertions regarding Wada and Barrett render the subject matter of the challenged claims obvious even under Patent Owner’s view of the claim scope. Accordingly, for purposes of this Decision, we apply Patent Owner’s view—that a non-interruptible burst does not require the control signals be maintained in a particular state once a burst begins.

2. “predetermined number of internal address signals”

Petitioner states that the ITC expressly construed the term as “a fixed number of internal address signals for a burst access.” Pet. 16. Petitioner submits that the ITC further applied the term in a narrower manner, such that it did not read on prior art “fixing the burst length before a data transfer by using a mode register” because that burst length “could be programmed.” Pet. 16 (citing Ex. 1013, 24–25). Thus, Petitioner submits that a “predetermined number” under the ITC’s construction must be a number determined at manufacture time. *Id.* Thus, Petitioner maps the claims to the prior art asserted here using what it views as the ITC’s implied construction—“fixed or programmable at manufacture time using bond options or voltage levels.” Pet. 16.

We do not understand any dispute raised by the parties to turn on whether we adopt Petitioner’s view that the predetermined number must be fixed at manufacture time. Moreover, such a construction would not appear to be consistent with dependent claim 5, which recites that the “fixed burst length is programmable.” Ex. 1001, 5:40–41. Thus, we do not adopt Petitioner’s proposed construction and proceed with no express construction for “predetermined number.”

3. “means for reading data . . . / means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals”

The parties agree that the structure corresponding to the means for reading data is “memory array 104.” Pet. 13; PO Resp. 21.

The parties appear to agree that the structure corresponding to the means for generating a predetermined number of internal address signals is

“burst address counter/register 102,” which may take the form shown in either Figure 2 or Figure 3. Pet. 14–15; PO Resp. 21.

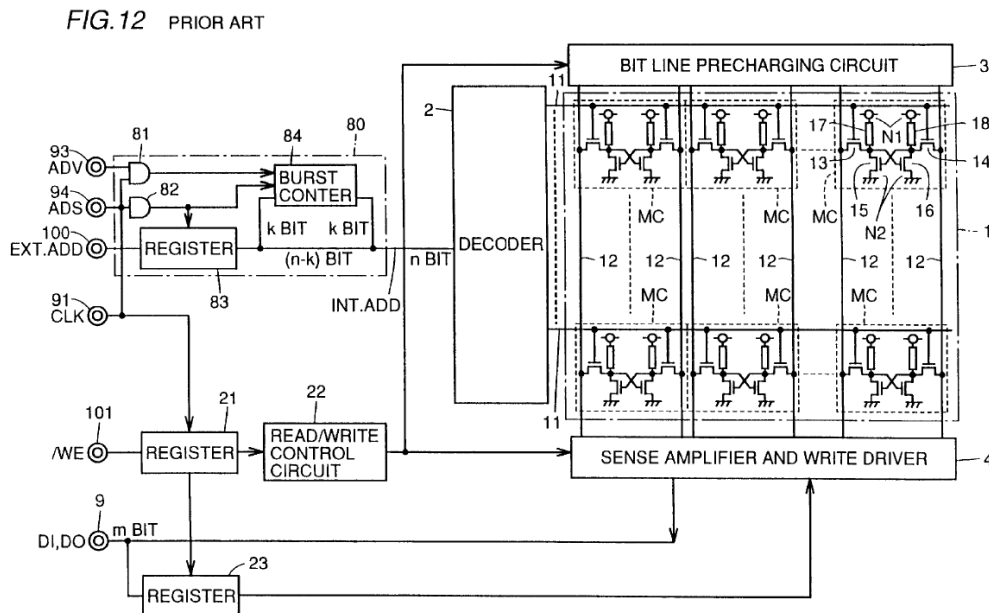
We proceed with both proposed constructions.

C. OBVIOUSNESS OVER WADA AND BARRETT

Wada discloses a “semiconductor memory for operating in burst mode.” Ex. 1005, code (57). Petitioner relies on two aspects of Wada—its description of a first “conventional SRAM” and its “Second Embodiment.” *See, e.g.*, Pet. 24–30 (identifying, for each challenged limitation, Wada’s disclosures of a “Conventional Embodiment” and “Second Embodiment”). Petitioner submits that it would have been obvious to a skilled artisan “to apply the teachings of Barrett to achieve an uninterruptible data transmission stream.” Pet. 52–53 (emphasis omitted).

1. Wada’s disclosures

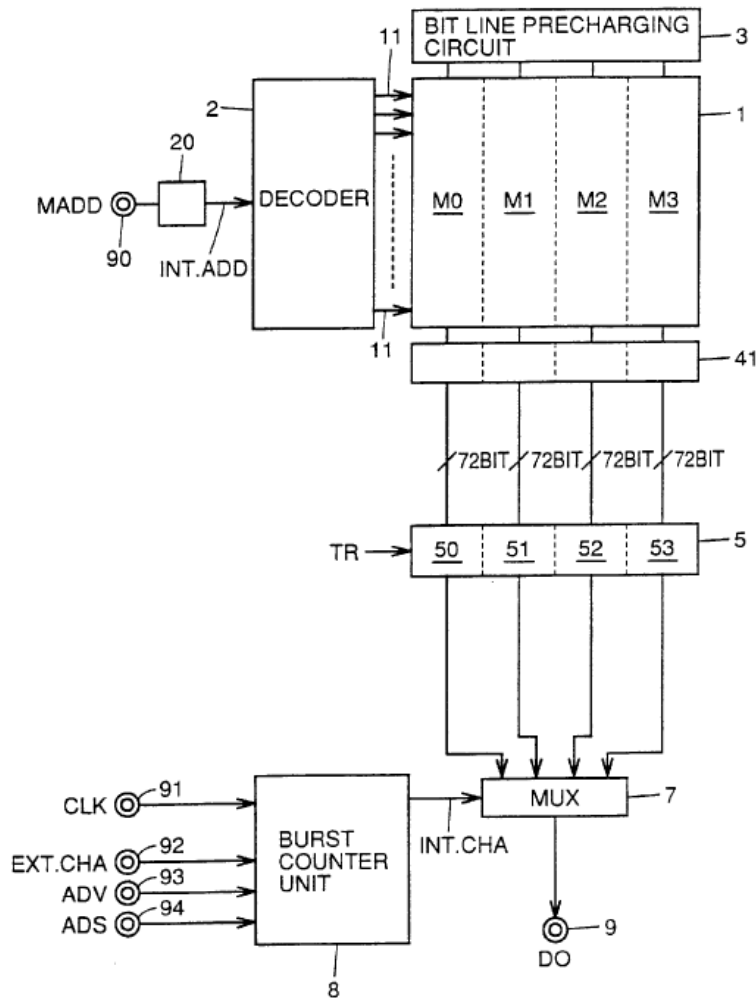
Wada’s first conventional embodiment is depicted in Figure 12, reproduced below:



Ex. 1005, Fig. 12. Figure 12 depicts burst counter unit 80 that starts with external address signal EXT.ADD and increments the address to create internal address signal INT.ADD, which is provided to decoder 2 to select word line 11 in memory cell array 1 for reading or writing data. *Id.* at 1:22–2:33, 3:5–32. Wada discloses that “every time the clock signal CLK is at a leading edge and the advance signal ADV is High,” the internal address “is incremented by the burst counter.” *Id.* at 3:5–9. Wada notes that speed improvement in the conventional embodiment described above is limited by the “operative delays resulting from the parts of the memory cell array” such as “delay times in the operations of the word lines.” *Id.* at 5:26–42.

Wada discloses a second conventional SRAM embodiment, depicted in Figure 15, reproduced below:

FIG. 15 PRIOR ART



Id. Fig. 15. Figure 15 depicts memory cell array 1 where the word line 11 selected for reading or writing is determined by memory address input signal MADD, which is sent to the decoder as internal address signal INT.ADD.

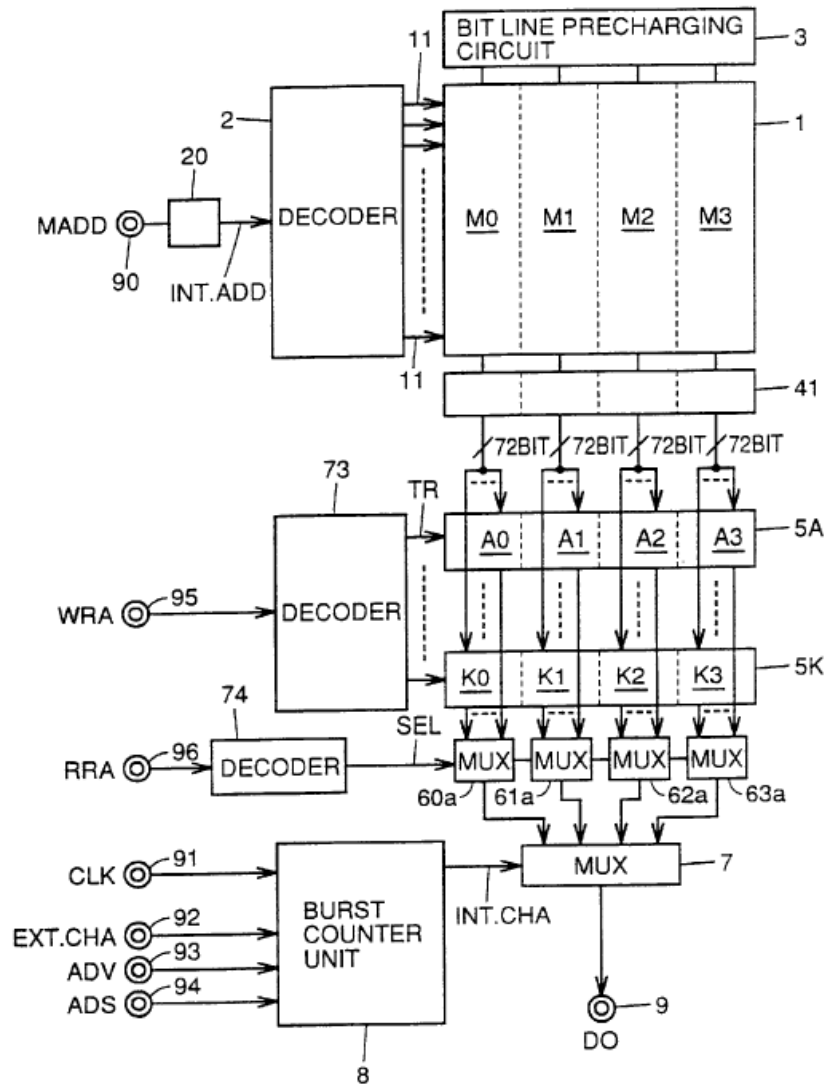
Id. at 3:33–62. Figure 15 depicts output register 5, which retains data received from memory cell array 1 through sense amplifier 41. *Id.* at 3:42–4:13. Rather than using a burst counter to increment the address identifying a memory word line as in the first conventional embodiment, the second

conventional embodiment uses burst counter 8 to accept external chunk address signal EXT.CHA and increment it, producing internal chunk address signal INT.CHA, which allows multiplexer 7 to select from one of four blocks, 50 through 53, in output register 5, to provide to data input/output pin 9. *Id.* at 4:6–40.

Wada indicates its second conventional embodiment avoids the operative delays involved in its first conventional embodiment. *Id.* at 5:43–45. Wada notes that the second conventional embodiment has the disadvantage of one clock-cycle delay between two burst outputs relating to two memory addresses. *Id.* at 5:50–53. That delay arises because data must be retained in the output register until output, preventing new data from being captured from the memory cell array. *Id.* at 5:11–24. Thus, Wada proposes an improved approach using burst mode that does not suffer from the operative delays of the conventional embodiment described above or the additional conventional embodiment with “data output interruptions” between bursts associated with different addresses. *Id.* at 5:66–6:7. Wada describes six enumerated embodiments that purport to address deficiencies of the prior art. *Id.* at 12:28–14:52 (First Embodiment), 14:53–16:50 (Second Embodiment), 16:51–18:48 (Third Embodiment), 18:49–19:34 (Fourth Embodiment), 19:35–20:60 (Fifth Embodiment), 20:61–38 (Sixth Embodiment).

Wada's Second Embodiment is depicted in Figure 3, reproduced below:

FIG.3



Id. Fig. 3. Figure 3 depicts a system sharing most components with Figure 15 (the second conventional embodiment) described above, but using multiple output registers 5A through 5K in place of single output register 5, and using additional multiplexers 60a through 63a to select among the multiple output registers. *See id.* at 14:63–15:2 (describing differences

between the First Embodiment and Second Embodiment), 12:36–13:13 (describing differences between the second conventional embodiment and the First Embodiment). As with Wada’s second conventional embodiment, its Second Embodiment uses burst counter unit 8 to convert external chunk address signal EXT.CHA into internal chunk address signal INT.CHA, which controls which block of the selected output register is transferred to output pin 9. *Id.* at 15:66–16:3.

Because the Second Embodiment uses multiple output registers, it can “execute data burst output in uninterrupted fashion.” *Id.* at 16:12–15. That is, it avoids the one clock-cycle delay associated with the single output register used in the second conventional embodiment. *See id.* at 5:50–53 (describing that “a data-free period (an interruption in the flow of data output) is bound to occur between two burst outputs”), 14:28–33 (describing that using two output registers as in the First Embodiment “permit[s] uninterrupted burst output of data), 16:12–15 (describing that the Second Embodiment “provides one advantage identical to that of the first embodiment, i.e., the ability to execute data burst output in uninterrupted fashion”).

2. Barrett’s disclosures

Barrett discloses “a burst transfer protocol [that] allows pausing only at pre-determined, fixed intervals of n data words.” Ex. 1010, code (57). Barrett’s protocol allows sender or receiver devices to “cause transmission to pause” only after each burst of data. *Id.* It notes that “[t]he essential feature of burst communication is that the data transfer takes place at high speed and without interruption.” *Id.* at 1:64–66. Barrett also discloses that, “[i]n effect, allowing a pause at any point defeats the purpose of burst

transmission, which is to send data a[s] rapidly as possible in an uninterrupted stream.” *Id.* at 2:39–41.

Petitioner asserts that Barrett’s teachings are applicable to Wada because both are directed to high-speed data exchange. Pet. 51–52. Petitioner asserts that “applying Barrett’s teachings to Wada to render bursts uninterruptible would result in improved transmission efficiency by minimizing overhead associated with terminating and initiating packets.” *Id.* at 52.

3. Unpatentability disputes

Petitioner contends that both the first conventional embodiment and the Second Embodiment of Wada disclose the elements of claim 1. Pet. 24–30. As to the claimed “logic circuit configured to generate a predetermined number of said internal address signals,” Petitioner identifies burst counter unit 80 in Wada’s first conventional embodiment (Pet. 26) and burst counter unit 8 in Wada’s Second Embodiment (Pet. 28). As described above, Wada teaches that those two circuits are “identical in structure” other than being provided with different external address signals. *See* Ex. 1005, 4:18–21 (describing differences between the burst counter unit 80 and burst counter unit 8), 12:36–39 (describing differences between the second conventional embodiment and the First Embodiment, not including any difference in burst counter unit 8), 14:63–15:5 (same, as between the First Embodiment and Second Embodiment), Figs. 1, 2 (showing the First Embodiment and Second Embodiment contain the same burst counter unit 8). Thus, Wada’s two embodiments identified by Petitioner for the claimed logic circuit offer no functional difference for our analysis.

a. Non-interruptible address generation

Patent Owner argues that the identified circuits in Wada do not satisfy the limitation “wherein said generation of said predetermined number of internal address signals is non-interruptible” appearing in each independent claim.⁷ PO Resp. 27–33. In each circuit Wada describes, if the ADV signal is not maintained in a high state throughout a burst, the circuit will not continue generating addresses for the burst. *See* Ex. 1005, 2:55–59, 3:5–9. Petitioner, however, asserts a combination in which Wada’s system is modified in light of Barrett’s teachings to render Wada’s system non-interruptible. Pet. 50–53.

Patent Owner challenges whether the combination of Wada and Barrett would result in non-interruptible address generation, arguing that Barrett lacks any disclosure “for preventing the burst transmission from being interrupted by external signals.” PO Resp. 35. We do not agree. Barrett discloses that “allowing a pause at any point defeats the purpose of burst transmission, which is to send data a[s] rapidly as possible in an uninterrupted stream.” Ex. 1010, 2:39–41. Barrett thus discloses a system in which a device transfers data “in successive cycles, without interruption.” *Id.* at 6:8–10; *accord id.* at 3:14–16 (“Once burst transfer is initialized, the sending device transmits an uninterrupted stream of n data transfer cycles over the communications bus.”). As to the controlling device’s ability to interrupt a burst, Barrett provides that transmission may be paused only “[a]fter a predetermined number of n data transfer cycles, where n is greater

⁷ Patent Owner argues also that Wada fails to disclose a “predetermined number” of generated addresses. PO Resp. 24–27. We address that argument below in the context of obviousness. *See infra* at 22.

than one.” *Id.* at 3:16–19. Patent Owner points to Barrett’s discussion of allowing a pause after a burst, before completing a “data transmission,” but the claim language here does not exclude such an approach. Rather, as long as a burst of predetermined length cannot be stopped, the claim is satisfied. We find that, in the above disclosures, Barrett teaches a non-interruptible burst.

b. Combining Barrett and Wada

Patent Owner argues that skilled artisans would have had no reason to combine Barrett’s teachings with Wada to result in the asserted combination. PO Resp. 36–48. Petitioner’s case in this regard relies on Barrett’s teaching that “allowing a pause at any point defeats the purpose of burst transmission, which is to send data a[s] rapidly as possible in an uninterrupted stream.” Ex. 1010, 2:39–41; *see* Pet. 52–53. Petitioner further reasons that “applying Barrett’s teachings to Wada to render bursts uninterruptible would result in improved transmission efficiency by minimizing overhead associated with terminating and initiating packets.” Pet. 52.

Patent Owner argues that because “Wada is directed to memory burst operation and Barrett is directed to burst data transfers between I/O devices,” there would have been no reason to combine their teachings. PO Resp. 37. While Patent Owner identifies differences in the data-transfer rates between the two types of devices, we do not agree those differences overcome Barrett’s disclosure of the desirability of precluding burst interruptions. Rather, Barrett’s teaching explains an aspect of burst data transfer that Wada leaves silent. Although Wada does not disclose any burst interruption, Wada also does not disclose the desirability of prohibiting burst interruptions. Barrett does. Barrett discloses that allowing burst

interruptions is undesirable, thus motivating a skilled artisan to modify Wada's circuit to prohibit such interruptions.

According to Patent Owner, Petitioner's stated motivation does not justify a device that "relinquishes control of the burst output." PO Sur-Reply 12–13. We do not agree. Petitioner explains that there would be a benefit to "minimizing overhead associated with terminating and initiating packets." Pet. 52. Relinquishing control of the burst output, as the consequence of the asserted combination, logically reduces overhead in the overall system—if a burst cannot be stopped, then there is no requirement to determine whether to stop it. Petitioner's stated rationale has a logical basis and would have motivated skilled artisans to modify Wada's circuit to render it non-interruptible.

While Patent Owner complains that Petitioner has not sufficiently explained "how Wada's control circuit would have been modified" (PO Sur-Reply 13; *accord* PO Resp. 48–50 (regarding reasonable expectation of success)), the '134 patent contains no detail about how its circuit renders a burst non-interruptible (*see* Ex. 1001, 3:5–4:48, Figs. 1–3). By treating such details as within the ordinary skill in the art, the '134 patent precludes Patent Owner's argument that Petitioner needed to show additional detail regarding how to implement the asserted combination. Indeed, Patent Owner's declarant agreed that "the reader would understand" the "pulse circuit design" required to generate a certain number of pulses. Ex. 1015, 153:24–159:2. Thus, regardless of the '134 patent's disclosures, the record supports, and we find that the required modification would have been well within the ordinary skill in the art.

Patent Owner submits further that Barrett operates using asynchronous data transfer whereas Wada uses synchronous, clock-driven transfer. PO Resp. 43–46. Because Barrett’s approach allows pauses between successive bursts, Patent Owner contends it is not compatible with Wada’s approach of eliminating delay between bursts. *Id.* The claims here do not relate to multiple successive bursts, and Barrett’s behavior in that regard is not relevant to whether the prior art discloses the claimed limitations. While it is possible that Barrett’s approach would create a problem if implemented in Wada’s system, Petitioner’s proposed combination does not include Barrett’s full approach to controlling data flow, including data flow between bursts. Rather, Petitioner’s proposed combination includes only the particular desire to prohibit interruptions within Wada’s bursts. *See* Pet. 50–53. Thus, we do not agree that Barrett’s teachings that allow for inter-burst pauses would apply in the asserted combination and defeat Wada’s ability to permit successive, uninterrupted bursts. *See* PO Resp. 46.

Having reviewed the full record and considered the parties’ contentions, we find that skilled artisans would have had reason to modify Wada’s circuit in light of Barrett’s teachings to render Wada’s burst-address generation non-interruptible.

c. Predetermined number of internal address signals

For Wada’s first conventional embodiment, Petitioner asserts that incrementing a k-bit portion of the EXT.ADD provided to burst counter unit 80 means that 2^k addresses are generated for INT.ADD, a number predefined by the number of bits separated from an n-bit EXT.ADD for incrementing. Pet. 26–27.

For Wada's Second Embodiment, Petitioner asserts that "the burst length is fixed by the choice of a four-input multiplexer and the choice of dividing the memory into four blocks (M0-M3)." Pet. 29. Petitioner points out that Wada's Figure 4 shows that the internal chunk address INT.CHA takes on four successive values in response to incrementing the address Ac received as external chunk address signal EXT.CHA. *Id.* (citing Ex. 1005, Fig. 4).

Patent Owner argues that neither of Wada's asserted embodiments discloses generating a predetermined number of internal addresses. PO Resp. 23–27. As to Wada's conventional embodiment, Patent Owner submits that, while it is limited to 2^k unique addresses for a given external address, external signals may cause it to stop short of that number, or cause it to generate additional, duplicate, addresses. *Id.* at 24–25; PO Sur-Reply 7. Petitioner points out that Patent Owner's declarant agrees that Wada discloses a burst counter that can generate 2^k addresses. Pet. Reply 7 (citing Ex. 1015, 193:16–194:5).

As to Wada's Second Embodiment, Patent Owner argues that "[n]either the number of memory blocks nor the number of multiplexer inputs has any bearing whatsoever on how many INT.CHA signals are generated." PO Resp. 26. Patent Owner relies in part on deposition testimony from Petitioner's declarant. *Id.* (citing Ex. 2006, 91:10–92:1). But that testimony relates to a statement the declarant, Dr. Baker, had written about "burst of data to or from the memory [that] comes from a single bank." Ex. 2006, 90:22–24. That is not the case in Wada, which describes four multiplexers used to transfer data to another multiplexer for a burst output. Ex. 1005, 15:66–16:3. Wada does not describe an arbitrary burst

length but instead describes that a burst involves successively transferring data from four multiplexers. *Id.* (“Given the internal chunk address signal INT.CHA sent from the burst counter unit 8, the multiplexer 7 successively transfers to the data input/output pin 9 the data fed from the multiplexers 60a through 63a.”). Thus, at least in Wada’s Second Embodiment, the circuit is designed to generate a predetermined number of internal addresses, corresponding to the multiplexers 60a through 63a that provide data to multiplexer 7 for input/output.

While we agree with Patent Owner that generating the expected number of addresses in Wada depends on completing an uninterrupted burst, that is exactly the case in the asserted combination. As discussed above, when Wada is modified in light of Barrett, the result is a system in which a burst cannot be stopped once started. In that system, the burst counter generates the expected number of addresses—one for each multiplexer 60a through 63a.

d. Objective indicia of nonobviousness

Patent Owner argues that objective indicia of nonobviousness show that the subject matter of the claimed invention would not have been obvious. PO Resp. 53–66. Specifically, Patent Owner asserts that “there was a long-felt but unmet need for an SDRAM⁸ that could transfer data quickly and efficiently using predetermined, non-interruptible bursts.” *Id.* at 54.

According to Patent Owner, before the ’134 patent, “burst accesses of JEDEC-compliant SDRAM memories were interruptible.” *Id.* As support,

⁸ Synchronous dynamic random access memory (SDRAM). *See* PO Resp. 1, 4.

Patent Owner points to a standard—JESD79F (Ex. 2010)—that it asserts was “first published in 2000” and includes a “BURST TERMINATE” command to truncate read bursts. *Id.* at 54–55 (citing Ex. 2010, 23, 27)⁹. The exhibit, however, bears a date of February 2008, and indicates it is a revision of a document published May 2005. Ex. 2010, 1. Nowhere does Patent Owner explain the discrepancy, or attempt to show that any revisions following the purported initial publication in 2000 were unrelated to the asserted burst terminate disclosures. That is, Patent Owner fails to demonstrate that the burst terminate command was part of the standard that was published in 2000 as opposed to the revised standard that was published in 2008. For that simple reason, we conclude Patent Owner has failed to meet its burden of showing that memory burst access prior to the ’134 patent was interruptible.

Further, even if we were to accept that the burst terminate disclosures in the 2008 publication were also disclosed in the 2000 publication, the document does not support Patent Owner’s substantive assertion. It notes that the “BURST TERMINATE” command “[a]pplies only to read bursts with autoprecharge disabled” and that “this command is undefined (and should not be used) for read bursts with autoprecharge enabled.” Ex. 2010, 16 n.8.¹⁰ Thus, even if the revised JESD79F standard had predated the ’134 patent, it shows that non-interruptible bursts (which, in Patent Owner’s

⁹ Citations to the Joint Electron Device Engineering Council (JEDEC) standards (Exs. 2010–2018) refer to the page numbers added to the bottom of each page for this proceeding.

¹⁰ The JESD79F standard provides auto precharge is an “option for each burst access” “to provide a self-timed row precharge that is initiated at the end of the burst access.” Ex. 2010, 5.

view, are those with no option to terminate) were known and used before the '134 patent. The JESD79F standard discloses a logic circuit that can be configured to generate bursts with no option to terminate them—such as any write burst and any read burst with autoprecharge enabled. Thus, the standard contradicts Patent Owner's assertion that "[b]efore the invention of the '134 Patent, which issued on November 18, 2003, burst accesses of JEDEC-compliant SDRAM memories were interruptible." *See* PO Resp. 54. *Cf. ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018) (holding that a reference discloses a device as claimed when it discloses a device that may operate as claimed at least in some configurations).

Moreover, Patent Owner's entire theory that the '134 patent met a long-felt need is unsupported and illogical. Patent Owner contends that prior to the '134 patent's invention, in DRAM¹¹ and SDRAM, "longer, more efficient bursts were not possible given the need to regularly refresh the DRAM cells." PO Resp. 64. In Patent Owner's view, that establishes "a long-felt need in the industry for a memory that could provide predetermined, non-interruptible burst operations." *Id.* at 65.

As explained above, the JESD79F standard already allowed predetermined non-interruptible bursts—i.e., bursts that could not be terminated with the burst terminate command. Moreover, the need to refresh DRAM cells could not have been solved by making bursts non-interruptible, because simply preventing interruption does not itself refresh the memory. Indeed, Patent Owner's declarant agreed that the '134 patent does not teach

¹¹ Dynamic Random Access Memory (DRAM). *See* PO Resp. 1, 4.

eliminating DRAM refreshes. *See id.* at 14 (citing Ex. 1015, 27:12–19). Rather, the patent discusses hiding refreshes by performing internal actions. Ex. 1001, 5:6–10, Fig. 6. As Petitioner explains, work prior to the ’134 patent disclosed partitioning memory such that one portion may be refreshed while another is accessed—an approach termed “hiding” the refresh. *See* Pet. Reply 14–15 (citing Ex. 1008, code (57)); Pet. 60–65. Patent Owner has not sufficiently explained how the challenged claims addressed the need for memory refresh. We therefore find that Patent Owner has not demonstrated that the invention claimed in the ’134 patent addressed a long-felt but unmet need.¹²

Finally, we note that Patent Owner’s theory based on the JEDEC standards contradicts its claim-construction position. As evidence that later JEDEC standards (e.g., DDR3, DDR4) produced “non-interruptible” bursts, Patent Owner points to the standards removing the “BURST TERMINATE” command (Ex. 2011, 44, 92) or expressly stating that “[b]urst interrupts are not allowed” (Ex. 2012, 31). PO Resp. 55–56; *accord id.* at 57 (citing Ex. 2014, 34 n.5 (“Burst reads or writes cannot be terminated or interrupted.”)). Indeed, Patent Owner draws a parallel between the burst terminate command in the early JEDEC standards (e.g., DDR) and “the falling of the advance signal” in Wada, which would “terminate the burst”

¹² Moreover, only claims 9 and 10 require the memory to be DRAM, and only claim 10 requires a burst sufficiently long to provide time for a DRAM refresh cycle (i.e., time for a hidden refresh). *See* Ex. 1001, 5:21–6:48. Thus, Patent Owner’s evidence could at most show a nexus between claim 10 and the JEDEC standard. But as explained, Patent Owner has not established that non-interruptible bursts themselves addressed the need for DRAM refresh, or that non-interruptible bursts were required for other mechanisms to address DRAM refresh.

according to Patent Owner. Tr. 60:5–13. But the later JEDEC standards that eliminate the burst terminate command nonetheless require control signals that must be maintained high during read and write burst access, just as Wada requires the ADV signal must be maintained high during read and write burst access. *See, e.g.*, Ex. 2014, 27 (§ 2.1, “CKE must be maintained high throughout read and write access.”). Thus, the later JEDEC standards that Patent Owner identifies as showing non-interruptible bursts describe circuits that depend on maintaining external signals in a particular way—which, according to Patent Owner, would make their bursts interruptible rather than non-interruptible.^{13, 14} Accordingly, even if we were to accept Patent Owner’s contention that there was a long-felt but unmet need for non-

¹³ We note that accepting Patent Owner’s assertions regarding the later JEDEC standards would require a finding that Wada anticipates the challenged claims. That is because the JEDEC standards, like Wada, describe interactions between external control devices and memory circuits to maintain certain control signals. *See, e.g.*, Ex. 2012, 12 (§ 2.4, describing functionality for external connections). If a circuit requires external devices to maintain control signals for non-interruptible address generation, then Wada discloses non-interruptible address generation.

¹⁴ Even ignoring the dependence on external signals, we question Patent Owner’s reliance on the DDR2 specification, which expressly allows for burst interruption for 8-bit bursts. Ex. 2011, 29–30 (§ 2.6 “However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively.”). Patent Owner has not addressed how the claims, which require the bursts to be non-interruptible, are consistent with making bursts interruptible only in certain conditions. As for the standards that Patent Owner asserts “explicitly made bursts non-interruptible,” the significantly later dates on those standards raise questions regarding their connection with the ’134 patent. *See* Ex. 2012, 1 (May 2012); Ex. 2013, 1 (Aug. 2014); Ex. 2014, 1 (July 2012); Ex. 2015, 1 (June 2017); Ex. 2016, 1 (Feb. 2016).

interruptible bursts, we would find that Patent Owner has not shown the required nexus between the claimed invention and the later JEDEC standards because those standards do not generate non-interruptible bursts per Patent Owner's own interpretation of what that means. *See WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1359 (Fed. Cir. 1999) ("The patentee bears the burden of showing that a nexus exists between the claimed features of the invention and the objective evidence offered to show non-obviousness.").

e. Conclusion

As discussed, we find that a person of ordinary skill in the art had reason to modify Wada's system in light of Barrett, and that the combined teachings disclose all of claim 1's limitations. We have considered Patent Owner's assertions regarding objective indicia of nonobviousness together with Petitioner's proofs regarding the combined teachings of Wada and Barrett and find the subject matter of claim 1 would have been obvious over Wada and Barrett.

For claims 2–4, 8, 12–14, 16, and 17, Petitioner provides contentions showing how the same combination of Wada and Barrett teach each of the elements recited in these claims. Pet. 17–53. Other than as addressed above regarding claim 1, Patent Owner does not challenge Petitioner's contentions regarding Wada's and Barrett's disclosures with respect to claims 2–4, 8, 12–14, 16, and 17. *See* PO Resp. 22–50. We determine Patent Owner has waived any such argument regarding these claims. *See* Paper 14, 8 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."); *In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016); Consolidated Trial Practice Guide 52 (Nov. 2019). We have reviewed

the parties' contentions and the evidence presented, including objective evidence of nonobviousness, and conclude that Petitioner has shown by a preponderance of the evidence that the subject matter of each of claims 2–4, 8, 12–14, 16, and 17 would have been obvious over Wada and Barrett.

D. ADDITIONAL OBVIOUSNESS GROUNDS BASED ON WADA AND BARRETT

Petitioner asserts further that Fujioka, Reeves, and Lysinger, each disclose the limitations of challenged dependent claims and that skilled artisans had reasons to combine teachings from Fujioka, Reeves, or Lysinger with Wada and Barrett to arrive at those dependent claims. Pet. 53–72. Other than as discussed regarding claim 1, Patent Owner does not challenge Petitioner's contentions regarding combinations including Fujioka, Reeves, or Lysinger. *See* PO Resp. 50–53. We determine Patent Owner has waived any such argument. *See* Paper 14, 8; *In re NuVasive, Inc.*, 842 F.3d at 1380–81; Consolidated Trial Practice Guide 52.

We have reviewed the parties' contentions and evidence, including objective evidence of nonobviousness, and conclude that Petitioner has shown by a preponderance of the evidence: that the subject matter of each of claims 4–7 and 18–20 would have been obvious over Wada, Barrett, and Fujioka; that the subject matter of each of claims 9, 10, 14, and 21 would have been obvious over Wada, Barrett, and Reeves; and that the subject matter of each of claims 11 and 15 would have been obvious over Wada, Barrett, and Lysinger. *See* Pet. 53–72.

E. GROUNDS BASED ON WADA WITHOUT BARRETT

Petitioner also challenges claims 1–21 as anticipated or rendered obvious over Wada alone or in combination with Fujioka, Reeves, or

Lysinger. *See* Pet. 17–71. We need not determine the merits of these challenges because, as explained above, Petitioner has demonstrated the unpatentability of claims 1–21 over the combination of Wada and Barrett, alone or in further combination with Fujioka, Reeves, or Lysinger. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but can “greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

III. CONCLUSION¹⁵

For the reasons discussed, we conclude:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–3, 8, 12, 13, 16, 17	102	Wada	Not decided	Not decided

¹⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–3, 8, 12, 13, 16, 17	103	Wada	Not decided	Not decided
1–3, 8, 12, 13, 16, 17	103	Wada, Barrett	1–3, 8, 12, 13, 16, 17	
4–7, 18– 20	103	Wada, Fujioka	Not decided	Not decided
4–7, 18– 20	103	Wada, Barrett, Fujioka	4–7, 18–20	
9, 10, 14, 21	103	Wada, Reeves	Not decided	Not decided
9, 10, 14, 21	103	Wada, Barrett, Reeves	9, 10, 14, 21	
11, 15	103	Wada, Lysinger	Not decided	Not decided
11, 15	103	Wada, Barrett, Lysinger	11, 15	
Overall Outcome			1–21	

IV. ORDER

It is

ORDERED that Petitioner has proven that claims 1–21 of the '134 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Xin-Yi Zhou
Ryan K. Yagura
Nicholas J. Whilt
Brian M. Cook
O'MELVENY & MYERS LLP
vzhou@omm.com
ryagura@omm.com
nwhilt@omm.com
bcook@omm.com

PETITIONER:

Tyler R. Bowen
Roque Thuo
PERKINS COIE LLP
bowen-ptab@perkinscoie.com
thuo-ptab@perkinscoie.com

PATENT OWNER:

Theodoros Konstantakopoulos
Kevin McNish
DESMARAIS LLP
tkonstantakopoulos@desmaraisllp.com
kkm-ptab@desmaraisllp.com