

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC. and
STMICROELECTRONICS, INC.,¹
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-00990
Patent 6,534,805 C1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

JUDGMENT
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ STMicroelectronics, Inc., which filed a petition in IPR2021-00356, has been joined as a petitioner in this proceeding.

I. INTRODUCTION

A. *Background and Summary*

Advanced Micro Devices, Inc. (“AMD”) filed a Petition requesting *inter partes* review of claims 8, 10, 12, 16, 18, 22, and 23 (“the challenged claims”) of U.S. Patent No. 6,534,805 C1 (Ex. 1001, “the ’805 patent”). Paper 1 (“Pet.”), 5. Monterey Research, LLC (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). Upon consideration of the Petition and Preliminary Response, we instituted *inter partes* review of all challenged claims on all grounds raised. Paper 12 (“Dec. Inst.”).

Subsequent to our Institution Decision, STMicroelectronics, Inc. (“STM”) was joined as a petitioner to this proceeding. Paper 33. Thus, all references to Petitioner below are references to AMD and STM. Patent Owner filed a Response to the Petition (Paper 25, “PO Resp.”), Petitioner filed a Reply (Paper 27, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 35, “PO Sur-Reply”). An oral hearing was held on September 1, 2021, and the hearing transcript is included in the record. *See* Paper 44 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that claims 8, 10, 12, 16, 18, 22, and 23 of the ’805 patent are unpatentable on the grounds raised in the Petition.

B. *Real Parties-in-Interest*

AMD identifies itself, ATI Technologies ULC, Globalfoundries Inc., and Globalfoundries U.S. Inc. as real parties-in-interest. Pet. 3. STM identifies itself and STMicroelectronics International N.V. as real parties-in-

interest. Paper 33, 2. Patent Owner identifies itself and IPValue Management as real parties-in-interest. Paper 6, 1.

C. Related Matters

AMD and Patent Owner identify the following as matters that can affect or be affected by this proceeding: *Monterey Research, LLC v. Advanced Micro Devices, Inc.*, No. 1:19-cv-02149 (D. Del.); *Monterey Research, LLC v. Qualcomm Inc.*, No. 1:19-cv-02083 (D. Del.); *Monterey Research, LLC v. STMicroelectronics N.V.*, No. 1:20-cv-00089 (D. Del.); *Monterey Research, LLC v. Marvell Tech. Grp. Ltd.*, No. 1:20-cv-00158 (D. Del.); and *Marvell Semiconductor, Inc. v. Monterey Research, LLC*, No. 3:20-cv-03296 (N.D. Cal.). Pet. 3; Paper 6, 1. AMD further identifies *Monterey Research, LLC v. Nanya Tech. Corp.*, No. 1:19-cv-02090 (D. Del.) as a matter that can affect or be affected by this proceeding. Pet. 3. STM further identifies *Qualcomm, Inc. v. Monterey Research, LLC*, IPR2020-01491 (PTAB Mar. 8, 2021) as a matter that can affect or be affected by this proceeding. Paper 33, 3.

D. Evidence Relied Upon²

Reference		Effective Date	Exhibit
Oh	US 6,417,549 B1	July 9, 2002	1004
R. Jacob Baker et al., <i>CMOS Circuit Design, Layout and Simulation</i> , (2011) (“Baker”)		1998	1005

E. Instituted Grounds of Unpatentability

We instituted review on the following grounds:

² Petitioner also relies upon the Declarations of Dr. Miltiadis Hatalis (Exs. 1002, 1039), Dr. Jacob Baker (Exs. 1011, 1038), Dr. Gretchen Hoffman, (Exs. 1013, 1037), Debra L. Tasker (Ex. 1023), Rebecca McKay Johnson (Ex. 1024), Nathan Rupp (Ex. 1027), and Rachel J. Watters (Ex. 1036).

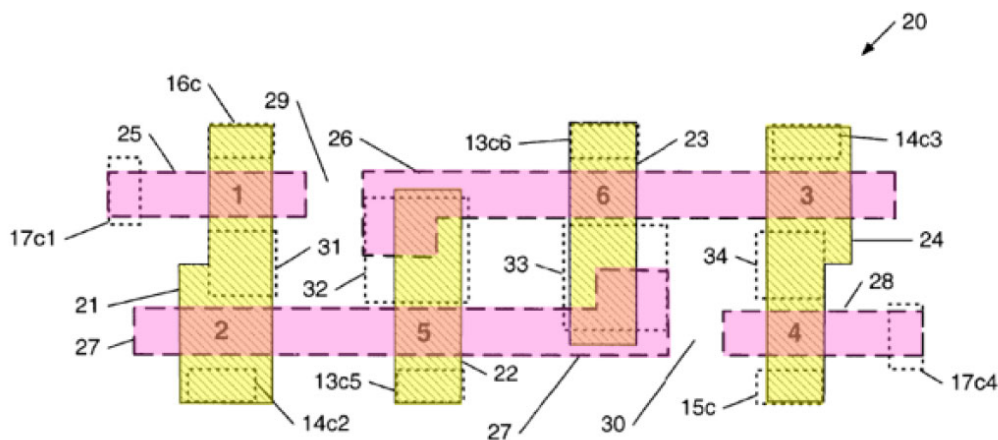
Ground	Claims	35 U.S.C. §	References
1	8, 10, 12, 16, 18, 22, 23	103(a)	Oh
2	8, 10, 12, 16, 18, 22, 23	103(a)	Oh, Baker

II. ANALYSIS

A. The '805 Patent

The '805 patent is directed to “an improved Static Random Access Memory (SRAM) cell design and method of manufacture.” Ex. 1001, 1:7–10. Figure 1 of the '805 patent illustrates “the transistor configuration of an embodiment of an improved SRAM memory cell.” *Id.* at 4:61–62. The cell includes circuit components formed in silicon, a polysilicon layer, an interconnect layer, a first metal layer containing bitlines, and a second metal layer containing a wordline. *Id.* at 6:17–19, 10:30–43, 11:50–51, 13:19–30.

Figure 2 of the '805 patent illustrates “a layout 20 that may be used to form in silicon the memory cell 10 represented in FIG. 1.” *Id.* at 6:17–19. A modified version of Figure 2, colorized by Petitioner, is reproduced below.



The figure is a Petitioner-colored version of Figure 2 of the '805 patent, illustrating the layout of the active regions (yellow) and gates (pink) of an

SRAM memory cell 10. Pet. 6. Illustrated in the layout are “NMOS³ transistors 1–4 . . . formed within [outer] active regions 21 and 24, and PMOS⁴ transistors 5 and 6 . . . formed within [inner] active regions 22 and 23. Ex. 1001, 6:26–29.

Active regions 21–24 (yellow) “are arranged side-by-side and substantially parallel to each other.” *Id.* at 6:38–40. They are “substantially oblong, and . . . may be substantially rectangular as well.” *Id.* at 6:65–67. For example, “PMOS active regions . . . 22 or 23 . . . may have a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region.” *Id.* at 6:67–7:4. NMOS active regions 21 and 24 are “substantially oblong if the length of the region is substantially constant and the width of the region . . . varies only with the respective widths of the access and latch transistors.” *Id.* at 7:24–28.

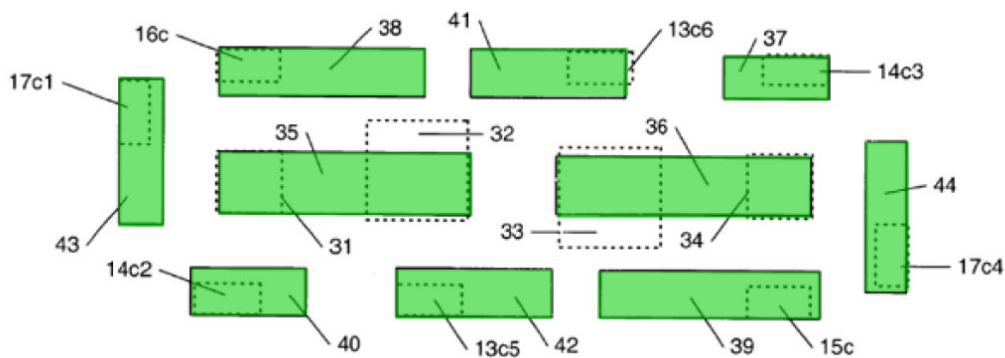
Polysilicon structures 25–28 (pink) are formed above and substantially perpendicular to active regions 21–24 (yellow). *Id.*, Fig. 2. Polysilicon structures 25 and 27 “are arranged above active region 21 to form gates of pass transistor 1 and latch transistor 2, respectively.” *Id.* at 6:55–57. Polysilicon structures 26 and 28 are arranged above active region 24 “to form gates of pass transistor 4 and latch transistor 3, respectively.” *Id.* at 6:58–60. “[P]olysilicon structures 26 and 27 each include two gates.” *Id.* at 11:37–38. For example, polysilicon structure 26 “form[s] gates of PMOS latch transistor 6 and NMOS latch transistor 3,” and polysilicon structure 27 “form[s] gates of NMOS latch transistor 2 and PMOS latch

³ N-type metal-oxide-semiconductor.

⁴ P-type metal-oxide-semiconductor.

transistor 5.” *Id.* at 11:32–37. Thus, “polysilicon structures 26 and 27 . . . each perform a local interconnecting function because they each connect two separate gate conductors together.” *Id.* at 11:38–41.

Figure 3 of the ’805 patent “illustrates a local interconnect layer which may be used in conjunction with the layout shown in FIG. 2.” *Id.* at 11:50–51. A modified version of Figure 3, colored by Petitioner, is reproduced below. Pet. 9.



The figure is a Petitioner-colored version of Figure 3 of the ’805 patent, which consists entirely of interconnects 35–43 that connect various components of transistors 1–6 (Fig. 2) to various structures in first and second metal layers (not shown) that are disposed above the interconnect layer. Ex. 1001, 10:30–42, 11:67–12:8, 13:10–32.

Interconnect 35 “connects the source of transistor 1 to the drains of transistors 2 and 5 and the gates of transistors 3 and 6” via contacts 31 and 32. *Id.* at 11:67–12:4, Figs. 2, 3. Interconnect 36, similarly, connects the source of transistor 4 to the drains of transistors 3 and 6 and the gates of transistors 2 and 5 via contacts 33 and 34. *Id.* at 12:6–8, Figs. 2, 3. Interconnects 37 and 40, respectively, couple ground line V_{SS} in the first metal layer (not shown) to the sources of transistors 2 and 3 through contacts 14c2 and 14c3 and vias in a first dielectric layer (not shown) between the

interconnect and first metal layers. *Id.* at 10:32–43, 13:16–27, Figs. 2, 3. Interconnects 38 and 39, respectively, couple bitlines in the first metal layer (not shown) to the drains of transistors 1 and 4 through contacts 16c and 15c and vias through the first dielectric layer (not shown). *Id.* at 10:30–43, 13:12–27, Figs. 2, 3. Interconnects 41 and 42, respectively, couple power line V_{CC} in the first metal layer (not shown) to the sources of transistors 5 and 6 through contacts 13c5 and 13c6 and vias in the first dielectric layer (not shown). *Id.* at 10:34–43, 13:18–27, Figs. 2, 3. Interconnects 43 and 44, respectively, couple global wordline 17 in the second metal layer (not shown) to gates 25 and 28 of transistors 1 and 4 through contacts 17c1 and 17c4 and vias in the first dielectric layer (not shown), and a second dielectric layer (not shown) between the first and second metal layers (not shown). *Id.* at 9:11–14, 13:27–32, Figs. 2, 3.

B. Illustrative Claim

Claims 8 and 16 are independent claims. Ex. 1001, Reexam. Cert. 1:25–35, 1:64–2:9. Claims 10 and 12 depend from claim 8. Ex. 1001, 14:40–45; Reexam. Cert. 1:19–20, 1:39–41. Claims 18, 22, and 23 depend from claim 16. Ex. 1001, Reexam. Cert. 2:13–15, 2:37–46. Claim 8 is illustrative of the challenged claims and is reproduced below.

8. A memory cell comprising

a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another, and

a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions; and

a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.

Ex. 1001, Reexam. Cert. 1:25–35.

C. Level of Ordinary Skill in the Art

Petitioner identifies a person of skill in the art (“POSITA”) at the time of the invention as someone that would have had “a bachelor’s degree in electrical engineering, computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent.” Pet. 16 (citing Ex. 1002 ¶¶ 25–40). In our Institution Decision, we adopted this description as our own. *See* Dec. Inst. 11–12. Neither party disputes that preliminary finding, which we maintain for purposes of this decision. *See* PO Resp. 14; Pet. Reply 1–33.

D. Claim Construction

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Under this standard, a claim is construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* Only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

At the institution phase of this proceeding, both parties agreed that “[t]o resolve the particular grounds presented in this Petition, no claim requires explicit construction.” Pet. 16; Prelim. Resp. 11. Therefore, we did

not offer any preliminary constructions for any claim terms. *See* Dec. Inst. 12. The parties now dispute construction of the term “a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline” (“the local interconnect layer” limitation). *See* PO Resp. 14–18; Pet. Reply 6–10.

*A Single Local Interconnect Layer Comprising Local Interconnects
Corresponding to Bitlines and a Global Wordline*

Patent Owner argues “[t]his limitation means ‘one local interconnect layer that includes short connections that route bitline signals and a global wordline signal along that same layer.’” PO Resp. 14–15. Patent Owner further argues this means routing “both bitline and wordline signals for connection to *laterally-displaced* components on” the local interconnect layer. *Id.* at 15 (emphasis added). Patent Owner argues the Specification supports its construction by disclosing that local interconnects (a) provide “short runs relative to much longer metal conductors used for global connections” and (b) perform “the function of connecting features within a circuit.” *Id.* (citing quoting Ex. 1001, 11:18–23). Patent Owner further argues the prosecution history supports its construction and “should be dispositive because this language was added to distinguish claim 8 from Osada⁵ . . . the examiner allowed claim 8 over Osada,” and this panel found Oh’s disclosures to be substantially similar to Osada’s. *Id.* at 17, 17 n.2 (citing Dec. Inst. 12).

Petitioner argues “[t]he meaning of this term is plain; no construction is needed.” Pet. Reply 6. Petitioner further argues that because Patent Owner’s construction “does not support [its] attempt to distinguish prior art,

⁵ US 6,677,649 B2 issued to Osada et al.

[Patent Owner] further interprets its construction to require connecting ‘laterally-displaced components,’” which finds no support in the Specification. *Id.* at 7–8. Petitioner argues that although Figure 3 of the ’805 patent shows interconnects 35 and 36 connecting laterally displaced components, it does not show bitline interconnects 38 and 39 or wordline interconnects 43 and 44 connecting laterally displaced components. *Id.* at 9.

We agree with Petitioner that the local interconnect layer limitation should be construed to have its plain and ordinary meaning in view of the Specification. The Specification discloses that local interconnects are short conductors that “connect[] features within a circuit” rather than “much longer metal conductors used for global connections.” Ex. 1001, 11:18–21. The Specification discloses that a local interconnect layer is a deposited conducting layer that is “patterned and etched” and “a distinct process layer that *exclusively* performs such short [local] connections.” *Id.* at 11:22–23, 12:39–49 (emphasis added). This last disclosure distinguishes a local interconnect layer from other layers that may perform the interconnect function. For example, a polysilicon layer that “partially provide[s] local interconnect” functions but also “provid[es] transistor gate[]” functions is not a local interconnect layer because it does not *exclusively* perform the interconnect function. *Id.* at 11:23–27. Likewise, a dielectric layer having contacts or vias that connect structures in layers above and below it is not a local interconnect layer because it is not a conducting layer. *Id.* at 8:52–64 (disclosing a dielectric layer opening used to contact underlying layers is a “contact opening,” “contact hole,” or “via” rather than an “interconnect”). Moreover, although the Specification discloses an interconnect layer containing interconnects, a first metal layer containing bitlines, and a second metal layer containing a wordline, it fails to disclose how the bitlines and

wordline are laid out in the first and second metal layer, i.e., it fails to show whether they require “laterally displacing” interconnects in the interconnect layer. *Id.* at 13:19–32.

Given the Specification’s disclosures, we construe “a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline” to mean “one conductive layer containing non-global interconnects, including interconnects for bitlines and a global wordline, that exclusively perform the function of connecting features within a circuit.” *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (“[T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.”).

We disagree with Patent Owner’s contention that the prosecution history requires a different construction. When claim 8 was initially rejected, Patent Owner amended it to recite “a local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.” Ex. 1007, 488. Patent Owner argued this distinguished claim 8 over Osada because it recited “the *single* [interconnect] layer of Fig. 3,” which has “all the runs for the bitlines, V_{CC}, V_{SS} and the wordline,” whereas Osada has “*multiple* layers for its runs.” *Id.* at 502. The Examiner suggested Patent Owner amend claim 8 to recite a *single* local interconnect layer, and when Patent Owner did, allowed claim 8. *Id.* at 1039, 1057–1058.

In our view, the Examiner erred in finding claim 8’s recitation of a *single* local interconnect layer distinguished that claim over Osada. As we stated in our Institution Decision, we “do not see a meaningfully claimed distinction between the disclosures of the ’805 patent, Osada, and Oh, all of which disclose an SRAM having three metal layers, including a first metal

layer having interconnects for upper layer bitlines and a wordline.” Dec. Inst. 10. It is this first metal layer that is the *single* local interconnect layer because it is the only conductive layer in the ’805 patent, Osada, and Oh that *exclusively* performs the interconnect function.

As discussed in § II.A, *supra*, the ’805 patent discloses an SRAM cell having transistors formed in a silicon layer, gates formed in a polysilicon layer, interconnects formed in a local interconnect layer, bitlines formed in a first metal layer, and a wordline formed in a second metal layer. Ex. 1001, 6:17–19, 10:30–43, 11:50–51, 13:19–30. The ’805 patent identifies the local interconnect layer as the first conducting layer deposited over the polysilicon gate layer, and indicates that it “*may be* made from a material having higher resistivity than [] metals or conducting materials,” for example, it may be made of polysilicon. *Id.* at 11:50–54, 12:42–45, Figs. 2–3 (emphasis added). The ’805 patent identifies the first metal layer as “the first conductive layer above the local interconnect layer,” but recognizes this “*may be a misnomer* in those cases where the local interconnect layer utilizes a metal.” *Id.* at 10:40–43, 12:40–42. Thus, the ’805 patent’s single local interconnect layer can be a first metal layer, the ’805 patent’s first metal layer containing bit lines can be a misnamed second metal layer, and the ’805 patent’s second metal layer containing a word line can be a misnamed third metal layer.

Oh discloses an SRAM cell with a similar structure, discussed in § II.E.2, *infra*, having transistors in a semiconductor substrate, polysilicon gates in a first conductive (polysilicon) layer, interconnects in a second conductive (first metal) layer, a wordline in a third conductive (second metal) layer, and bitlines in a fourth conductive (third metal) layer. *See* Ex. 1004, 3:40–4:10, Figs. 3, 5, 7, 9.

Osada discloses an SRAM cell having a similar structure to Oh's.
Figure 4 of Osada is reproduced below.

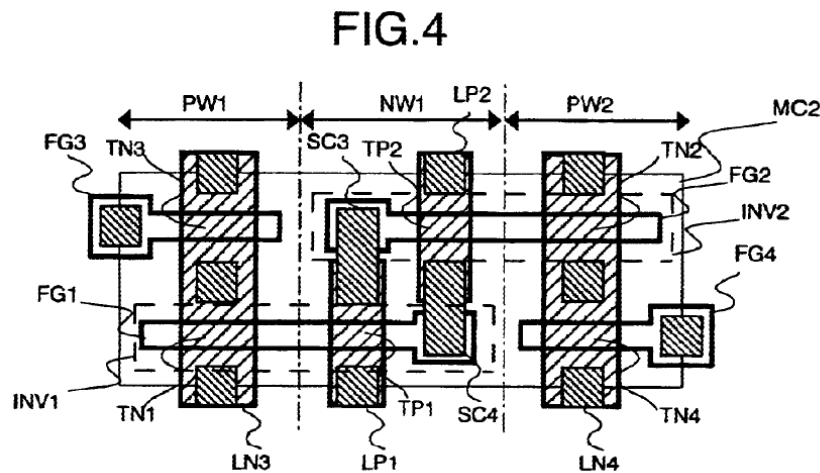


Figure 4 illustrates “an SRAM cell in accordance with Embodiment 3” of Osada. Ex. 1009, 4:10–11. The symbols in Figure 4 “are the same as those in FIG. 2.” *Id.* at 7:22–25. They include transistors TN1–TN4 and TP1–TP2 formed in a semiconductor substrate and polysilicon gates FG1–FG4 formed in a polysilicon layer. *Id.* at 5:27–45, 5:61–6:7. The remaining layers of Osada—the interconnect, first metal, and second metal layers—are shown in Figure 5, which is reproduced below.

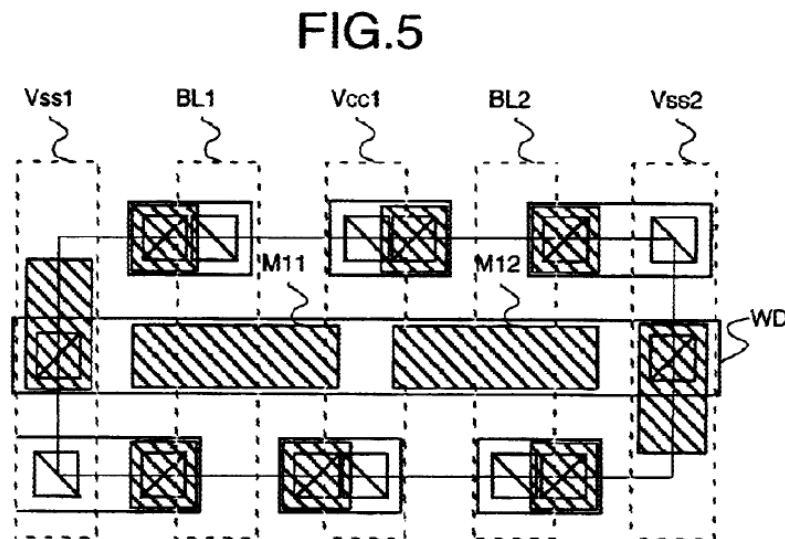


Figure 5 of Osada “is a diagram showing a layout of via holes of SRAM cells for connection between multilayered metal leads in accordance with Embodiment 3.” *Id.* at 4:15–17. As before, the symbols used in Figure 5 “are the same as those in FIG. 2.” *Id.* at 7:21–23. Figure 5 discloses interconnects in a first metal layer (structures with a hashed fill, such as M11/M12), interconnects and a wordline (WD) in a second metal layer (structures with a solid outline and no fill), and bitlines (BL1/BL2), power line (V_{cc1}), and ground lines (V_{ss1}/V_{ss2}) in a third metal layer (structures with a dashed outline and no fill). *Id.* at 5:65–67, 6:8–20, 7:58–61. Thus, the only conductive layer in Osada’s third embodiment that *exclusively* performs the interconnect function is Osada’s first metal layer, just like the “single local interconnect layer” shown in Figure 3 of the ’805 patent. For this reason, the Examiner erred in finding Osada lacked a “single local interconnect layer.”

E. Obviousness Over Oh

Petitioner argues claims 8, 10, 12, 16, 18, 22, and 23 are unpatentable as obvious over Oh. Pet. 36–70. Patent Owner disagrees. PO Resp. 18–35. For the reasons discussed below, we find Petitioner has demonstrated by a preponderance of evidence that claims 8, 10, 12, 16, 18, 22, and 23 are unpatentable over Oh.

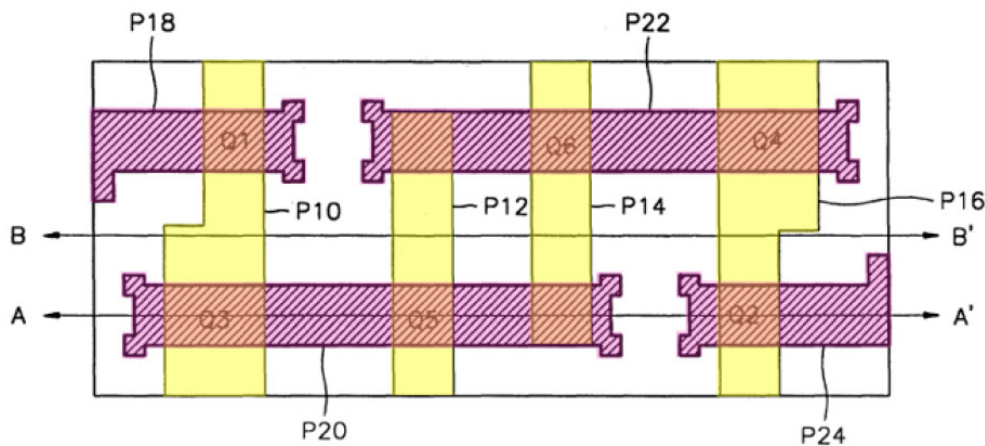
1. Oh

Oh discloses “a static random access memory device (SRAM) which can be manufactured by a CMOS⁶ standard logic manufacturing process and a method for manufacturing the same.” Ex. 1004, 1:7–12. “The SRAM device comprises a semiconductor substrate in which parallel first and

⁶ Complementary Metal-Oxide-Semiconductor.

second active regions of a first conductive type are arranged and third and fourth active regions of a second conductive type are arranged between the first and second active regions.” *Id.* at 3:42–47.

Figures 3–9 of Oh are “layouts of the exemplary mask patterns used for manufacturing [the] SRAM device,” while Figures 10 and 11 show “the SRAM device . . . manufactured using the mask patterns of FIGS. 3 through 9.” *Id.* at 8:9–10, 12:21–24. A Petitioner-colored version of Figure 3 of Oh is reproduced below. Pet. 20.



The figure is a Petitioner-colored version of Figure 3 of Oh illustrating “the layout of mask patterns for use in forming active regions and gates” of Oh’s SRAM cell. Ex. 1004, 8:45–47. Outer masks P10/P16 (yellow) are used to form first/second active regions and inner masks P12/P14 (yellow) are used to form third/fourth active regions. *Id.* at 8:47–53. The first through fourth active regions have the same “shapes and arrangements” as masks P10–P16. *Id.* at 12:30–36, 14:49–51. The first/second active regions P10/P16 “form[] NMOS transistors . . . parallel to each other in a bar shape” and the third/fourth active regions P12/P14 “form[] PMOS transistors . . . parallel to each other between the first and second active regions P10 and P16.” *Id.* at 8:62–67. NMOS transistors Q1 and Q3 “are formed in the first

active region,” NMOS transistors Q2 and Q4 “are formed in the second active region,” and PMOS transistors Q5/Q6 are formed in the third/fourth active regions, respectively. *Id.* at 12:37–53.

Masks P18/P24 (pink) are used to form the gates of the first/second access transistors Q1/Q2, and masks P20/P22 (pink) are used to form the gates of the first/second drive transistors Q3/Q4 and the first/second load transistors Q5/Q6. *Id.* at 8:53–61. “The gate P20 . . . [is] arranged perpendicular to the first active region P10, and . . . to the third active region P12,” and the “gate P22 . . . [is] arranged perpendicular to the second active region P16, and . . . to the fourth active region P14.” *Id.* at 9:4–12.

Oh’s SRAM device includes “a first metal layer . . . , a second metal layer which forms the word line, and a third metal layer which forms bit lines.” *Id.* at 3:29–32. Figure 5 of Oh, reproduced below, illustrates the masks used to form structures on the first metal layer.

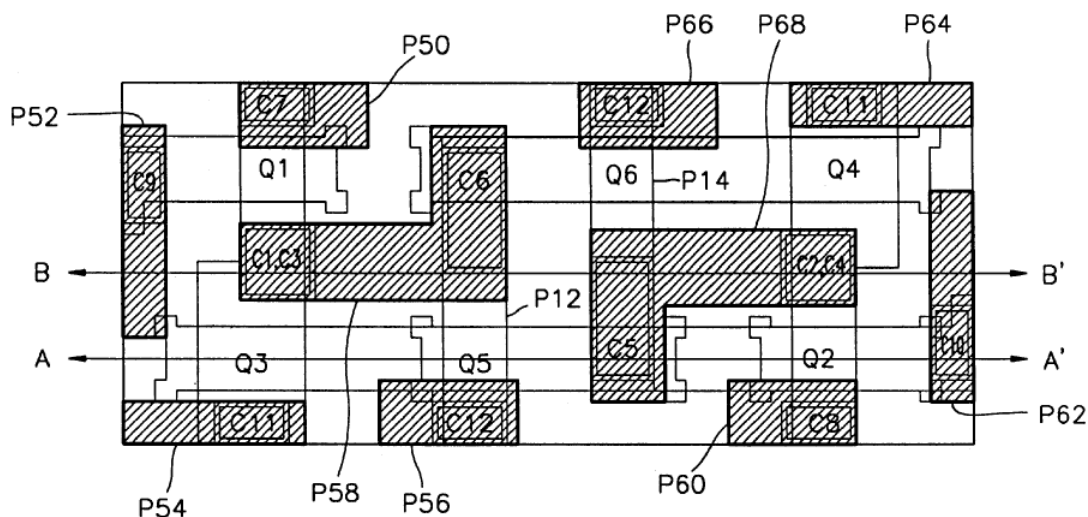


Figure 5 of Oh is a “layout of mask patterns for forming a first connection line, a second connection line and a plurality of first pad layers.” *Id.* at 10:7–9. Mask P50 “form[s] a first pad layer C7” that connects to the source of transistor Q1, mask P60 “form[s] a first pad layer C8” that

connects to the source of transistor Q2, mask P52 “form[s] a first pad layer C9” that connects to the gate of transistor Q1, and mask P62 “form[s] a first pad layer C10” that connects to the gate of transistor Q2. *Id.* at 10:9–15, 10:28–34. The sources of transistors Q1/Q2 connect through first pads C7/C8 to bitlines in the third metal layer via second pads C7/C8 formed in the second metal layer and vias C7/C8 formed in the two dielectric layers separating the three metal layers. *Id.* at 11:4–6, 11:13–15, 11:25–28, 11:35–38, 11:52–54, 11:60–62, 12:6–9, 12:14–17, Figs. 6–9. The gates of transistors Q1/Q2 connect through first pads C9/C10 to a wordline in the second metal layer through vias C9/C10 formed in the dielectric layer separating the first and second metal layers. *Id.* at 11:6–8, 11:15–17, 11:45–48, Figs. 6–7.

2. *Claim 8*

a) *memory cell*

Claim 8 recites a memory cell. Reexam. Cert. 1:25. Petitioner argues that Oh teaches or suggests this limitation. *See* Pet. 36 (citing Ex. 1004, 1:6–13, 3:3–4:10, Figs. 3–25). Patent Owner disagrees, arguing that Oh instead is directed to “improvements to photolithography masks used to manufacture memory” cells and that Oh’s figures “do not show memory cell structures themselves.” PO Resp. 10–11 (emphasis omitted).

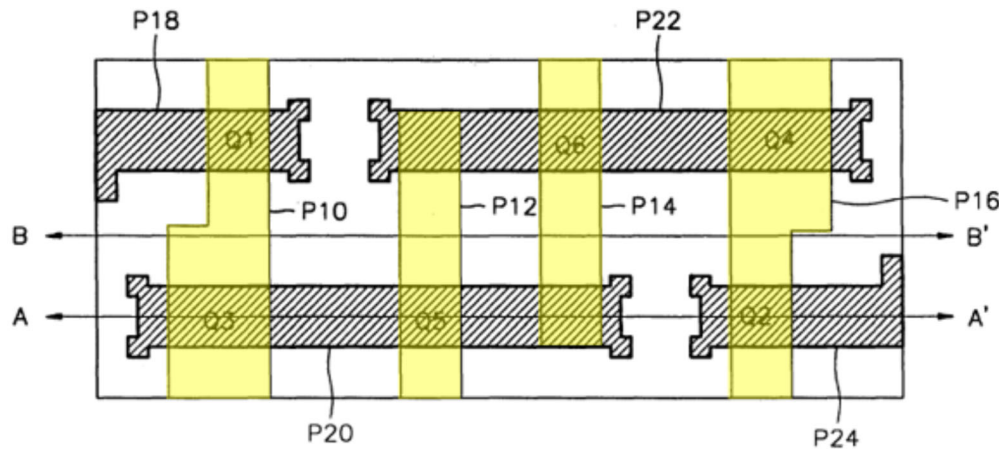
We agree with Petitioner that Oh teaches or suggests a memory cell. Oh discloses “a static random access memory (SRAM) device which can be manufactured by standard CMOS logic manufacturing processes.” Ex. 1004, 3:3–5. Figures 3 through 9 of Oh are “exemplary mask patterns used for manufacturing [the] SRAM device.” *Id.* at 8:9–11. Figures 10 through 25 are cross-sectional views of Oh’s SRAM device made using the photolithographic masks shown in Figures 3 through 9. *Id.* at 8:15–27. For

example, Oh discloses the first through fourth active regions shown in Figures 10 and 11 are formed using masks P10 through P16 and have “shapes and arrangements . . . [that] are the same as shown in the mask patterns P10, P12, P14, and P16 in FIG. 3.” *Id.* at 12:25–36, 14:49–51.

b) substantially oblong active regions

Claim 8 further requires the memory cell to include a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another. Reexam. Cert. 1:25–27.

Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. See Pet. 36–38. Petitioner illustrates Oh’s teachings with a colorized version of Figure 3 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Oh’s Figure 3 showing the mask patterns (yellow) used to make four active regions in a semiconductor substrate. Pet. 37. Petitioner demonstrates how Oh teaches the active regions formed by masks P10–P16 are substantially oblong and parallel based on Figure 3 and the express teachings in Oh. *Id.* at 36–38 (citing Ex. 1004, 3:40–47, 4:11–21, 7:9–15, 8:62–67, 12:66–13:6, Fig. 3).

Oh teaches “the first and second active regions P10 and P16 . . . are arranged parallel to each other *in a bar shape*, and the third and fourth active regions P12 and P14 . . . are also arranged parallel to each other.” Ex. 1004, 8:62–67 (emphasis added). Oh also teaches “*the shapes* and arrangements of the first through fourth active regions are the same as shown in mask patterns P10, P12, P14, and P16 in FIG. 3.” *Id.* at 14:49–51 (emphasis added). Thus, Oh’s third/fourth active regions have the same shapes as masks P12/P14, i.e., they are “rectangular in shape and ha[ve] length and width dimensions that are substantially constant” as Petitioner contends. *See* Pet. 37 (citing Ex. 1004, Fig. 3). The ’805 patent describes inner active regions, such as Oh’s active regions P12/P14, as “substantially oblong” if they have “a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region.” Ex. 1001, 6:65–7:4.

Oh describes the first/second active regions as having the same shapes as masks P10/P16, i.e., “the first [second] active region can have a wider width at regions overlapped by the gate of the first [second] drive transistor than at regions overlapped by the gate of the first [second] access transistor.” Ex.1004, 4:11–21, 7:9–15, 14:49–51. As Petitioner contends, the ’805 patent describes this as one way outer active regions, such as Oh’s active regions P10/P16, are “substantially oblong.” *See* Pet 37–38; *see also* Ex. 1001, 7:24–28 (describing NMOS outer active regions as substantially oblong if “the length of the region is substantially constant and the width of the region . . . varies only with the respective widths of the access and latch transistors”).

We note that claim 8 only requires a plurality of substantially oblong active regions. *See* Reissue Cert. 1:25–26. Thus, Petitioner demonstrates

this limitation is met by demonstrating active regions P10/P16 are substantially oblong, active regions P12/P14 are substantially oblong, or all of these regions are substantially oblong. Petitioner demonstrates that all of active regions P10–P16 are substantially oblong.

Patent Owner makes numerous arguments that Petitioner has failed to show Oh's active regions are substantially oblong. *See* PO Resp. 19–21, 25–29; PO Sur-Reply 8–10. Patent Owner first argues that because “mask patterns used to form structures on a wafer are different—and, indeed, must be different—from the patterns of the structures formed by those masks,” Petitioner “cannot establish that the mask patterns illustrated in Oh's drawings . . . are the same as the patterns of the resulting memory cell structures.” PO Resp. 27–28 (emphasis omitted). Patent Owner next argues that even if Oh's mask patterns did show the shapes of Oh's active regions, Petitioner cannot rely on those shapes to show the active regions are substantially oblong because (a) Oh's drawings are not to scale, (b) Oh's specification contradicts what is shown in Figure 3, and (c) patent drawings cannot be relied on to demonstrate sizes or proportions. *Id.* at 19–21, 25–27 (citing Ex. 1004, 8:2–4, 9:22–29; quoting *Nystrom v. Trex Co., Inc.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005)). Patent Owner also argues that Petitioner cannot show that Oh's active regions are substantially oblong because (a) Oh's drawings do not show the lengths of the active regions, (b) Petitioner and Dr. Hatalis admit that Oh's drawings don't allow the lengths, distances between, or shapes of structures to be determined, and (c) Petitioner stated that it relied on more than Oh to show the shapes of Oh's active regions. *See* PO Sur-Reply 8–10 (citing/quoting Pet. Reply 12, 16, 18, 29; Ex. 1039 ¶¶ 23, 25, 33, 40, 49, 67, 69, 75). We disagree with each of Patent Owner's contentions for the reasons that follow.

Figures 3 through 9 of Oh disclose “mask patterns used for manufacturing an SRAM” and Figures 10 and 11 disclose cross-sectional views of “the SRAM . . . manufactured using the mask patterns of FIGS. 3 through 9.” Ex. 1004, 8:9–18. Oh discloses that these Figures “are *not necessarily* drawn to scale,” not that they are *not* drawn to scale. *Id.* at 8:2–4 (emphasis added). Moreover, Oh expressly discloses that the active regions formed in its SRAM device have the same shapes as the mask patterns shown in Figure 3, and expressly describes these active regions as being bar-shaped. *See id.* at 12:30–36 (disclosing the first through fourth active regions of Oh’s SRAM device correspond to masks P10–P16), 14:49–51 (disclosing “[t]he *shapes and arrangements* of the first through fourth active regions *are the same* as shown in the mask patterns P10, P12, P14, and P16 in FIG. 3”), 8:62–64 (disclosing “active regions P10 and P16 . . . are . . . in a bar shape”) (emphases added). Thus, regardless of whether Oh’s figures are drawn to scale and regardless of whether the shapes of the structures formed by the masks differ in some respects from the shapes of the masks themselves, Oh expressly discloses that the active regions formed in its SRAM device have the same substantially oblong bar shape as the mask patterns shown in Figure 3 that are used to form those active regions.

Patent Owner relies on Oh’s description of the shapes of masks (active regions) P10/P16 in column 9 to support its argument that Oh describes these shapes differently than the shapes shown in Figure 3. *See* PO Resp. 21 (citing Ex. 1004, 9:22–29). Oh’s column 9 description, however, is inconsistent not only with the shapes shown in Figure 3, but with every other description in Oh of the shapes of active regions P10/P16, all of which describe shapes that are consistent with the shapes shown in Figure 3. *Compare* Ex. 1004, 9:22–29, *with id.* at 4:11–21, 7:9–15, 12:66–

13:6, 20:59–65, 23:30–36, Fig. 3. Consequently, we agree with Petitioner that Oh’s column 9 description is simply a typographical error. *See* Pet. Reply 15 n.7.

Patent Owner relies on cases like *Nystrom* and *Hockerson-Halberstadt* for the proposition that Petitioner cannot rely on Oh’s unscaled drawings to show the shape of masks (active regions) P10–P16. But these cases stand for a different proposition—that unscaled drawings cannot be relied on to show the *precise sizes or dimensions* of objects when the specification is silent on the issue. *See Nystrom v. Trex Co., Inc.*, 424 F.3d 1136, 1148–49 (Fed. Cir. 2005) (finding drawings could not be relied on to show deck board features in a precisely claimed 1:40 ratio because “patent drawings cannot be the basis for challenging the validity of claims reciting *specific dimensions* not disclosed directly in such prior art”) (emphasis added); *see also Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 953, 956 (affirming a claim construction disavowing a wide shoe heel groove despite drawings showing a wide groove because “patent drawings do not define the *precise proportions* of the elements and may not be relied on to show *particular sizes* if the specification is completely silent on the issue”) (emphases added); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977) (finding drawings could not be relied on to demonstrate a whiskey barrel chime “approximately 5/8 in length” because “[a]bsent any written description in the specification of *quantitative* values, arguments based on *measurement of a drawing* are of little value”) (emphases added).

Petitioner does not rely on Figure 3 to demonstrate the precise dimensions of Oh’s active regions. Instead, Petitioner relies on Figure 3 to show the active regions have a “substantially oblong” shape. *See* Pet. 36–37 (citing Ex. 8:62–67, Fig. 3). Moreover, Oh is not completely silent on the

shapes of the active regions shown in Figure 3. Oh discloses “the first and second active regions P10 and P16 . . . [are] in a bar shape.” Ex. 1004, 8:62–64. Oh also discloses the first through fourth active regions have “shapes and arrangements . . . [that] are the same as shown in the mask patterns P10, P12, P14 and P16 in FIG. 3.” *Id.* at 14:49–51. Thus, if the first and second active regions P10 and P16 have a “bar shape,” the third and fourth active regions P12 and P16 also have a “bar shape” as shown in Figure 3.

The lengths of Oh’s active regions are immaterial to whether they are substantially oblong. Per the ’805 patent, an active region is substantially oblong if (a) it has “a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region” or (b) “the length of the region is substantially constant and [] the width of the region varies by approximately 1/3 or less along the length of the region.” Ex. 1001, 6:65–7:4, 7:20–24. Neither of these descriptions requires any particular length, or any particular length-to-width ratio.

The statements made in Petitioner’s Reply or in Dr. Hatalis’ reply declaration regarding the inability to determine lengths, distances between, or shapes of the structures shown in Oh’s drawings do not detract from our finding that Petitioner has demonstrated that Oh’s active regions are “substantially oblong.” Petitioner’s statements that the lengths of Oh’s active regions cannot be determined from Figure 3 or that interconnect P50 can be extended rightward because the distance between it and interconnect P58 cannot be determined from Figure 5 are little more than correct statements of the law regarding ascertaining precise dimensions from unscaled drawings and were made to rebut an argument regarding obviousness over the combination of Oh and Baker, not obviousness over

Oh alone. *See* Pet. Reply 12, 18; Ex. 1039 ¶¶ 23, 49, 69; *see also* *Nystrom*, 424 F.3d at 1148–49; *Hockerson-Halberstadt*, 222 F.3d at 956 *Wright*, 569 F.2d at 1127. Likewise, Dr. Hatalis’ statements that structural sizes can’t be “derive[d] . . . solely from patent drawings” and that “patent drawings do not define the precise proportions of the elements” are simply correct statements of law. Ex. 1039 ¶¶ 33, 40.

Petitioner’s statement that it does not rely on Oh alone to demonstrate the substantially oblong shape of Oh’s inner active regions P12/P14 is factually incorrect. *See* Pet. Reply 16; *see also* Pet. 36–38 (relying on Oh alone to demonstrate active regions P10–P16 are substantially oblong). Moreover, Petitioner need not demonstrate Oh’s inner active regions P12/P14 are substantially oblong to demonstrate Oh discloses a plurality of substantially oblong active regions because Petitioner demonstrates outer active regions P10/P16 (a plurality) are substantially oblong based on Oh’s description of their shape. *See* Pet. 36–38; *see also* Ex. 1004, 12:66–13:6.

Finally, any statements made in Petitioner’s Reply and Dr. Hatalis’ reply declaration that the shapes of contacts cannot be determined from Figure 5 are irrelevant because they do not pertain to the shapes of Oh’s active regions and were made to rebut an argument regarding obviousness over the combination of Oh and Baker, not obviousness over Oh alone. *See* Pet. Reply 29–30; Ex. 1039 ¶¶ 67, 75. Furthermore, Petitioner cites *Hockerson-Halberstadt* for the proposition that Patent Owner “cannot rely on Oh’s unscaled figures to argue the contacts shown are non-square.” Pet. Reply 29. We disagree. As discussed above, *Hockerson-Halberstadt* stands for the proposition that unscaled drawings cannot be relied on to show the *precise sizes or dimensions* of objects when the specification is silent on the issue. *See Hockerson-Halberstadt*, 222 F.3d at 956. Oh is not silent on the

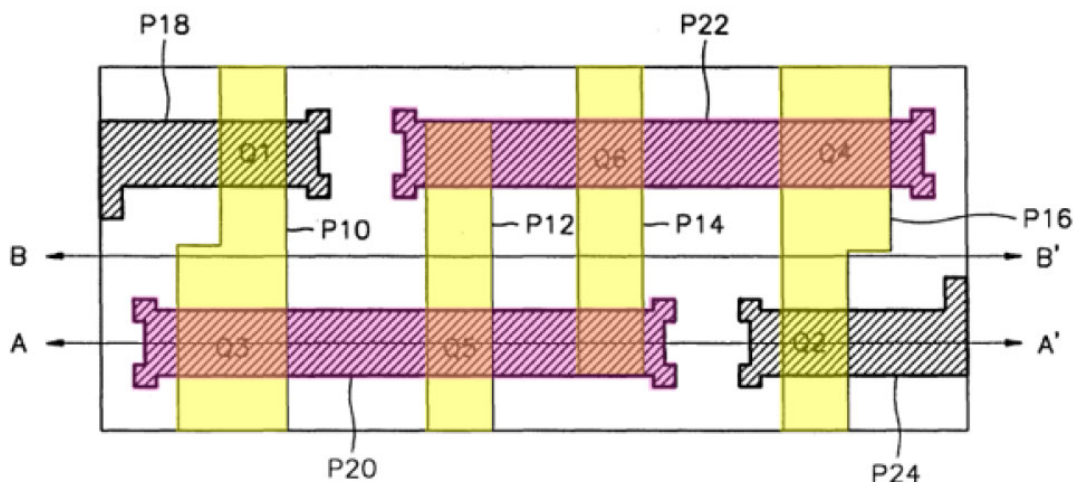
shape of the active regions in its SRAM device. They are described as having “a bar shape” and the same shape as masks P10–P16 in Figure 3. Ex. 1004, 4:11–21, 8:62–67, 14:49–51.

For the reasons discussed above, we find Petitioner has demonstrated that Oh discloses a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially parallel with one another as recited in claim 8.

c) substantially oblong local interconnects

Claim 8 requires a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions. Reexam. Cert. 1:25–27.

Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. See Pet. 40–44. Petitioner illustrates Oh’s teachings with a colorized version of Figure 3 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Figure 3 of Oh showing mask patterns P20/P22 (pink) used to make the gates of transistors Q3–Q6 in a

semiconductor substrate. Pet. 41. Petitioner demonstrates how Oh teaches the gates formed by masks P20/P22 are (a) above the semiconductor substrate, (b) partially extended across the memory cell, (c) substantially parallel with one another and substantially perpendicular to active regions (yellow) in the semiconductor substrate, and (d) substantially oblong. *Id.* at 40–44 (citing Ex. 1004, 3:3–13, 8:53–61, 9:4–21, 9:30–63, 12:64–65, Figs. 3–11, 26–29; Ex. 1002 ¶¶ 59–68, 82–86).

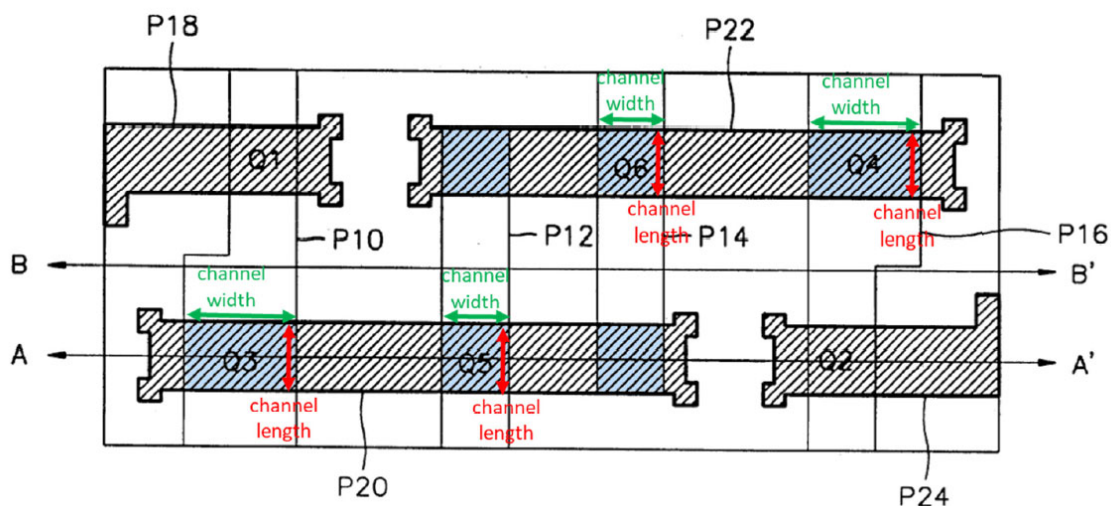
Oh teaches forming gate oxide layer 56 over semiconductor substrate 50, and depositing a first conductive layer to form gates for the transistors in the semiconductor substrate. Ex. 1004, 14:55–58, Fig. 10. Oh teaches mask P20 forms gates for “the first drive transistor Q3 and the first load transistor Q5,” and mask P22 forms gates for the second drive/load transistors Q4/Q6. *Id.* at 14:64–15:1. Oh further teaches “[t]he gate P20 of the first drive transistor Q3 . . . and the gate P20 of the first load transistor Q5 . . . are laterally connected,” as are the gates P22 of the second drive/load transistors Q4/Q6. Ex. 1004, 9:4–12. Thus, gates P20/P22 are local interconnects according to the ’805 patent. *See* Ex. 1001, 11:26–29 (identifying “a local interconnect” as a structure “configured such that multiple gates are connected”).

Oh teaches gate P20 for transistors Q3/Q5 partially extends over the memory cell because it “crosses the first, third and fourth active regions” but not the second, and gate P22 for transistors Q4/Q6 partially extends over the memory cell because it “crosses the second, fourth and third active regions” but not the first. Ex. 1004, 12:56–58, 12:60–62, 14:54–15:1, Figs. 3, 10. Oh further teaches gate P20 is perpendicular to “the first active region P10” and “the third active region P12,” and gate P22 is perpendicular to “the second active region P16” and “the fourth active region P14.” *Id.* at 9:4–12, Fig. 3.

Oh also teaches that gates P20/P22 are substantially parallel because gate P20 is located on a “line parallel to the gate P18 . . . and the gate P22”. *Id.* at 9:17–20, Fig. 3.

Oh teaches gates P20/P22 extend length-wise across the widths of three active regions and width-wise across the channel lengths of transistors Q3–Q6. Ex. 1004, Fig. 3. According to the unrebutted testimony of Dr. Hatalis, “the width of polysilicon structures P20 and P22 define the channel length of transistors Q3–Q6,” which a person skilled in the art would know should be “minimized to improve [transistor] performance and decrease SRAM cell size.” Ex. 1002 ¶ 82. Thus, “[b]ecause the length[s] of polysilicon structures P20 and P22 span[] three active regions that are spaced apart,” a person of ordinary skill in the art would have known that each polysilicon structure P20/P22 must have a length that is “greater than or equal to approximately three times its width under any reasonable design rules.” *Id.* ¶ 83.

Dr. Hatalis’ opinion is further explained in Petitioner’s Reply via a second annotated version of Figure 3 of Oh, which is reproduced below.



The figure is a Petitioner-annotated version of Figure 3 of Oh labelling the widths and lengths of the channel regions in transistors Q3–Q6. Pet.

Reply 15. Each of the channels of transistors Q3–Q6 (blue) has a width (green) that contributes to the length of gates P20/P22 and a length (red) that is less than or equal to the channel width. Thus, because each gate P20/P22 extends across three active regions, each gate has a length-to-width ratio that must be greater than three times the width-to-length ratio of the channels of transistors Q3–Q6, i.e., each gate must have a length-to-width ratio that is greater than three. This is explained in Dr. Hatalis’ opening declaration as follows: “the aspect ratio of polysilicon structures P20 and P22 must be greater than 3:1” because “[e]ach active region should have a minimum [channel] width on par with or greater than the minimum polysilicon width [channel length].” *Id.* ¶ 83.

Dr. Hatalis’ opinion regarding the width-to-length ratios of transistor channels was confirmed by Patent Owner’s declarant, Dr. Bagherzadeh. Upon being questioned about the size of transistors made using Intel’s 0.18 μm manufacturing process in 1999, Dr. Bagherzadeh testified as follows:

Q. And do you have any understanding as to what Lg of 130 nanometer refers to?

A. Lg is corresponding to -- to length of the gate probably.

Q. Got it. Did you finish your answer or –

A. Yeah because we have Ws and Ls. So W and L are standard transistor sizes, W/L, so it refers to the length.

Q. And the length of the gate is the area where the polysilicon[] crosses over the active region to form a transistor; is that right?

A. Yes, yes. It's a square with W on one side -- it's actually rectangular -- well, it could be the same. It -- and it has a W and L definition, yes.

Q. And if it is a rectangular -- if the channel region is rectangular, L_g refers to the shorter region, right? The shorter dimension in the rectangle; is that right?

A. The width would be longer, that's where the transistor -- that's where electrons cross, so the wider the W, the more stronger the -- the transistor in terms of gate.

Q. And L_g would be the gate length which is the shorter dimension in -- in the transistor?

A. It was -- it was -- yes, it would be the shorter of the two, most of the time, yes. Most of the time, yes.

Ex. 1040, 179:17–181:4. A polysilicon gate having a 3:1 aspect ratio is “substantially oblong.” *See* Ex. 1001, 7:28–31 (identifying “any region or structure having a length that is greater than or equal to approximately three times its maximum width” as a “substantially oblong” structure).

Patent Owner argues that Petitioner has failed to show Oh's polysilicon gate interconnects are substantially oblong for the same reasons discussed above with respect to Oh's active regions—i.e., because Figure 3 of Oh depicts masks P20/P22 rather than gates, masks have different shapes than the structures they are used to make, and even if Figure 3 showed gates having the same shape as masks P20/P22, Petitioner cannot rely on those shapes because Oh's figures are not drawn to scale. *See* PO Resp. 30–31; PO Sur-Reply 11–12.

We disagree with Patent Owner's contentions for the reasons discussed in § II.E.2.b, *supra*. We further note that Oh refers to P20/P22 as both the mask patterns for gates and the gates themselves. *Compare* Ex. 1004, 8:55–57 (“reference symbol P20 represents the mask pattern for

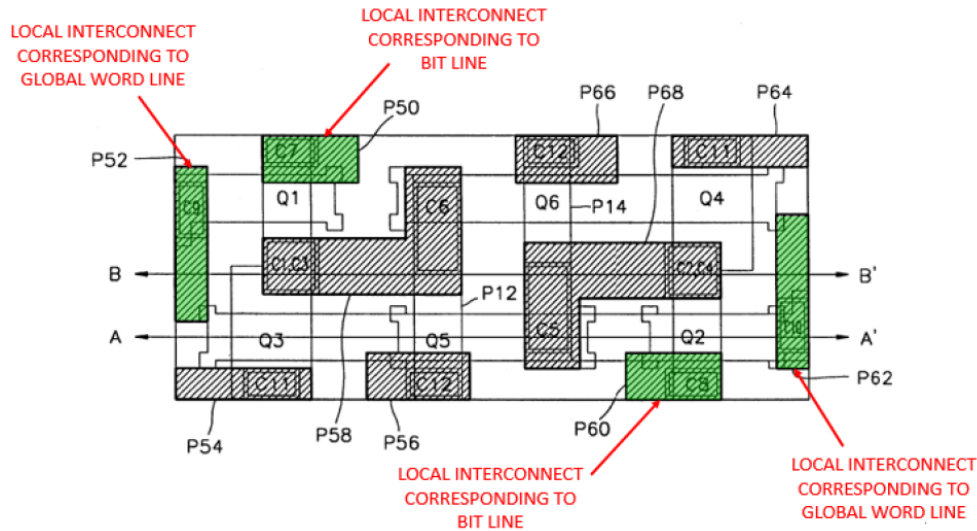
forming the gate of the first drive transistor Q3”), *with id.* at 9:4–5 (“The gate P20 of the first drive transistor Q3 . . .”). In describing the SRAM cell in Figure 10, Oh discloses “the gate (not shown correspond[s] to the mask pattern P18 of FIG. 3),” “the gate 58 (correspond[s] to the mask pattern P20 of FIG. 3),” “the gate (not shown correspond[s] to the mask pattern P22 of FIG. 3),” and “the gate 60 (correspond[s] to the mask pattern P24 of FIG.3).” *Id.* at 14:62–15:2. Oh equates the shapes of these gates to the shapes of mask patterns P18–P24. *See id.* at 15:3–5 (“For ease of understanding about the shape and arrangement of the gates, reference is made to FIGS. 3, 10, and 11 and the description thereof.”).

For the reasons discussed above, we find Petitioner has demonstrated that Oh discloses a plurality of substantially oblong local interconnects above the semiconductor substrate and arranged substantially parallel with one another and substantially perpendicular to the active regions in the semiconductor substrate as recited in claim 8.

d) single local interconnect layer

Claim 8 further requires a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline. Reexam. Cert. 1:25–27.

Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. *See* Pet. 45–47, 50–52, 58–60. Petitioner illustrates Oh’s teachings with an annotated version of Figure 5 of Oh, which is reproduced below.



The figure is a Petitioner-annotated version of Figure 5 of Oh showing masks for pads P50, P52, P60, and P62 (green) in Oh's second conduction layer, which is the first metal layer after Oh's polysilicon gate layer. *Id.* at 51. Petitioner demonstrates how Oh teaches the pads in this layer are local interconnects in a single local interconnect layer that includes interconnects for bitlines and wordlines. *Id.* at 45–47, 50–52, 58–60 (citing Ex. 1004, 3:29–33, 4:66–5:34, 10:7–12:21, 13:7–41, 16:24–67, Figs. 3–9, 21; Ex. 1002 ¶¶ 87–89, 95–96, 105–107).

First, Oh teaches its SRAM device consists of “multiple metal layers [that] include a first metal layer which forms the first and second connection lines, a second metal layer which forms the word line, and a third metal layer which forms bit lines.” Ex. 1004, 3:29–33. Figure 5 illustrates Oh's first metal layer because it has masks “for forming a first connection line, a second connection line and a plurality of first pad layers.” *Id.* at 10:7–9. Figure 7 illustrates Oh's second metal layer because it has masks “for forming a word line and a plurality of second pad layers.” *Id.* at 11:23–24. And Figure 9 illustrates Oh's third metal layer because it has masks “for forming power supply lines and bit lines.” *Id.* at 12:1–2.

First pads C9/C10 (P52/P62) in Oh's first metal layer are connected to the gates of first/second access transistors Q1/Q2 by contacts C9/C10. *Id.* at 10:12–15, 10:31–34; *see also id.* at 16:31–33, 16:48–50 (indicating first pads C9/C10 are designated P52/P62 in Figure 5). First pads C9/C10 (P52/P62) are connected to word line P98 (mask P98 in Figure 7) in Oh's second metal layer by first vias C9/C10. *Id.* at 11:45–48; *see also id.* at 11:48–50 (“The *word line P98*, which extends across the cell in a bar shape, is arranged parallel to the gates of the transistors.”) (emphasis added). Thus, first pads C9/C10 (P52/P62) in Oh's first metal layer are local interconnects “corresponding to” word line P98.

First pads C7/C8 (P50/P60) in Oh's first metal layer are connected to the sources of first/second access transistors Q1/Q2 by contacts C7/C8. *Id.* at 10:9–12, 10:28–31; *see also id.* at 16:29–30, 16:45–47 (indicating first pads C7/C8 are designated P50/P60 in Figure 5). First pads C7/C8 (P50/P60) are connected to second pads C7/C8 (P86/P92) in Oh's second metal layer by first vias C7/C8. *Id.* at 11:25–28, 11:35–38; *see also id.* at 17:40–41, 17:50–51 (indicating second pads C7/C8 are designated P86/P92 in Figure 7). Second pads C7/C8 (P86/P92) are connected to first/second bit lines 102/106 (P114/P118) in Oh's third metal layer by second vias C7/C8. *Id.* at 12:6–9, 12:14–17; *see also id.* at 17:32–33, 17:40–41 (indicating first/second bit lines 102/106 are designated P114/P118 in Figure 9). Thus, first pads C7/C8 (P50/P60) in Oh's first metal layer are local interconnects “corresponding to” bit lines 102/106 (P114/P118).

Mask P58 in Figure 5 of Oh forms a first connection line that connects the drains of first access/drive transistors Q1/Q3 with the gates of second drive/load transistors Q4/Q6 and the source of first load transistor Q5 via

contacts C1/C3 and C6. *Id.* at 10:22–28; *see also id.* at 16:40–41 (indicating the first connection line is designated P58 in Figure 5). Likewise, mask P68 forms a second connection line that connects the drains of second access/drive transistors Q2/Q4 with the gates of first drive/load transistors Q3/Q5 and the source of second load transistor Q6 via contacts C2/C4 and C5. *Id.* at 10:41–47; *see also id.* at 16:61 (indicating the second connection line is designated P68 in Figure 5). Thus, first/second connection lines (P58/P68) in Oh’s first metal layer are local interconnects that connect various sources, drains, and gates of transistors Q1–Q6. *See* Pet. 45–48 (explaining how P58/P68 in Oh’s first metal layer are local interconnects).

Lastly, as explained in § II.E.4, *infra*, masks P54, P56, P64, and P66 form pads in Oh’s first metal layer that interconnect transistors Q1–Q6 with power and ground lines in Oh’s third metal layer. Consequently, Oh’s first metal layer is a single local interconnect layer because it is the only deposited metal layer in Oh whose structures exclusively perform the interconnect function.

Patent Owner argues “Oh does not teach a single local interconnect layer that includes short connections that both route bitline signals and route a global wordline signal along that same layer.” PO Resp. 32. In doing so, Patent Owner admits that “Oh discloses ‘local interconnects corresponding to . . . a global wordline’ on [Oh’s] metal 1 layer” because “Oh’s global wordline signal . . . is routed from via P72 . . . along local interconnect P52 to contact C9, and eventually down to the gate of transistor Q1.” *Id.* at 32 (emphases omitted). However, Patent Owner denies that Oh teaches a local interconnect corresponding to bitlines for “rout[ing] the bitline and bitline-bar signals along that same layer” because Oh “rout[es] the bitline signal

vertically downward from via P70 through (rather than along) pad layer P50 to contact C7.” *Id.* at 33 (emphases omitted).

Patent Owner’s argument is based entirely on its proposed construction of the single local interconnect layer limitation and its interpretation of that construction to require interconnects that connect “*laterally-displaced components* on [the interconnect] layer.” *Id.* at 15 (emphasis added). We reject that construction for the reasons discussed above. *See* § II.D.1, *supra*. Nothing in the ’805 patent or its prosecution history narrows the plain and ordinary meaning of the single local interconnect layer limitation to require interconnects that connect laterally displaced components. *Id.* Indeed, although the ’805 patent discloses a single local interconnect layer having a plurality of interconnects, it fails to disclose the arrangement of bitlines in a first metal layer or a global wordline in a second metal layer or how the local interconnects connect the bitlines and global wordline to transistors in the semiconductor substrate. *See* Ex. 1001, 11:66–12:17, 13:10–32, Fig. 3. Thus, the ’805 patent fails to disclose that the local interconnects shown in Figure 3 must connect “laterally-displaced” components as Patent Owner contends.

e) Conclusions regarding claim 8

For the reasons discussed in §§ II.E.2.a through II.E.2.d, *supra*, Petitioner has demonstrated by a preponderance of evidence that Oh teaches or suggests all the limitations of claim 8. Accordingly, Petitioner has demonstrated that claim 8 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

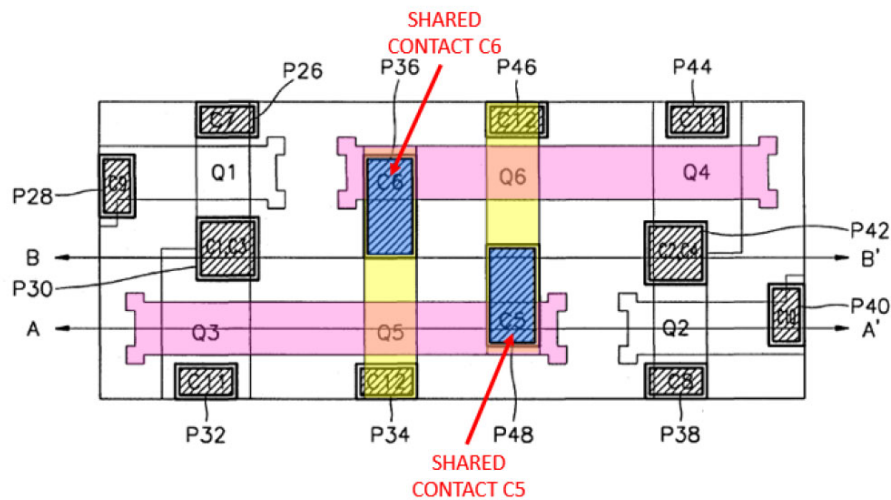
3. Claim 10

Claim 10 depends from claim 8 and requires the memory cell to include a shared contact to one of the active regions and a polysilicon

structure that is arranged substantially perpendicular to the active region and has a portion that abuts a portion of the active region. Ex. 1001, 14:40–45.

Petitioner argues that Oh teaches or suggests this limitation. *See* Pet. 54–58. Patent Owner argues that Petitioner has failed to demonstrate that claim 10 is unpatentable over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 18–35. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2, *supra*, and find Petitioner has demonstrated that Oh teaches the limitation recited in claim 10.

Petitioner illustrates Oh’s teachings with an annotated version of Figure 4 of Oh, which is reproduced below.



The figure is a Petitioner-annotated version of Figure 4 of Oh showing mask patterns P12/P14 (yellow) for making inner active regions in a semiconductor substrate, mask patterns P20/P22 (pink) for making polysilicon gates over the substrate, and mask patterns P36/P48 (blue) for making contacts C5/C6. Pet. 55. Petitioner demonstrates how Oh teaches each of contacts C5/C6 contact an active region P14/P12 and a polysilicon gate P20/P22, i.e., how each is a shared contact for an active region and a

polysilicon structure, and how polysilicon gates P20/P22 are substantially perpendicular to and abut a portion of active regions P12/P14. *Id.* at 54–56 (citing Ex. 1004, 7:56–58, 9:43–47, 9:61–63, 10:1–6, 16:4–23, Figs. 3–25).

Oh discloses P36 is the mask for forming a hole for contact C6 to the gates of transistors Q6/Q4 and the source of transistor Q5, and P48 is the mask for forming a hole for contact C5 to the gates of transistors Q5/Q3 and the source of transistor Q6. Ex. 1004, 9:44–47, 9:60–63, Fig. 4. Oh teaches filling the holes for contacts C5/C6 with tungsten to form plugs. *Id.* at 7:56–58, 16:4–8, Figs. 4, 21. Thus, C5 is a shared contact that contacts an active region (source of transistor Q6) and a polysilicon structure (gates for transistors Q5/Q3), and C6 is a shared contact that contacts an active region (source of transistor Q5) and a polysilicon structure (gates for transistors Q6/Q4).

As discussed in § II.E.2.b, *supra*, Oh teaches gates P20/P22 are substantially perpendicular to active regions P10–P16 as shown in Figures 3 and 4. *See, e.g.*, Ex. 1004, 14:49–51 (teaching “[t]he shapes and arrangements of the first through fourth active regions are the same as shown in the mask patterns P10, P12, P14, and P16 in FIG. 3”), 15:3–5 (referencing Figure 3 for “understanding about the shape and arrangement of the gates”). Thus, as shown in Figures 3 and 4, contact C5 is shared by active region P14 and gate P20, which is substantially perpendicular to and has a portion that abuts a portion of active region P14, and contact C6 is shared by active region P12 and gate P22, which is substantially perpendicular to and has a portion that abuts a portion of active region P12. *Id.* at Figs. 3, 4.

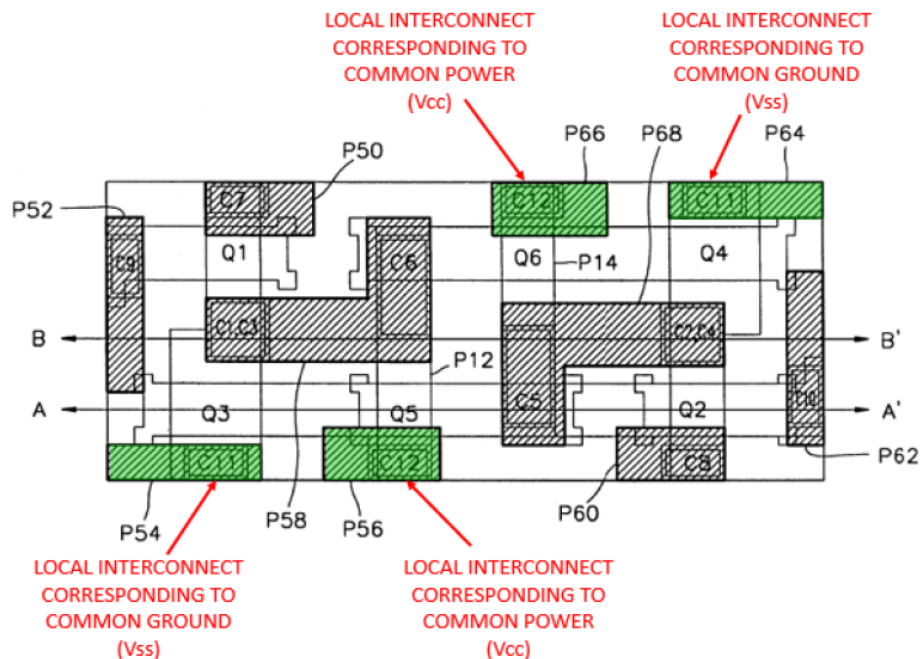
For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that claim 10 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

4. Claim 12

Claim 12 depends from claim 8, and requires the single local interconnect layer to include local interconnects corresponding to common power and common ground. Reexam. Cert. 1:39–41.

Petitioner argues that Oh teaches or suggests this limitation. See Pet. 58–60. Patent Owner argues that Petitioner has failed to demonstrate that claim 12 is unpatentable over Oh for the same reasons discussed above with respect to claim 8. See PO Resp. 18–35. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2, *supra*, and find Petitioner has demonstrated that Oh teaches the limitation recited in claim 12.

Petitioner illustrates Oh’s teachings with an annotated version of Figure 5 of Oh, which is reproduced below.



The figure is a Petitioner-annotated version of Figure 5 of Oh showing the mask patterns P54/P56/P64/P66 used to make pads C11/C12 (green) on Oh's first metal layer. Pet. 59. As discussed in § II.E.2.d, *supra*, Petitioner demonstrates how Oh's first metal layer is a single local interconnect layer. Petitioner further demonstrates how pad C12 connects transistors Q5/Q6 to a common power line formed by mask P116 in Oh's third metal layer, and how pad C11 connects transistors Q3/Q4 to common ground lines formed by masks P112/P120 in Oh's third metal layer. *Id.* at 58–60 (citing Ex. 1004, 5:13–25, 10:15–22, 10:34–41, 11:8–13, 11:17–22, 11:28–35, 11:38–45, 11:55–67, 12:3–6, 12:3–14, 12:18–21, 13:55–64, Figs. 3–9).

Oh teaches P54/P64 are masks for forming first pad C11 in Oh's first metal layer that contacts transistors Q3/Q4 via first contact hole C11. Ex. 1004, 10:15–18, 10:34–37, Fig. 5. First pad C11 contacts power supply lines V_{SS} (ground) formed by masks P112/P120 in Oh's third metal layer through first via C11, second pad C11 in Oh's second metal layer, and second via C11. *Id.* at 11:8–11, 11:17–19, 11:31–35, 11:41–45. 11:62–67, 12:2–6, 12:17–21, Figs. 6–9. Similarly, Oh teaches P56/P66 are masks for forming first pad C12 in Oh's first metal layer that contacts transistors Q5/Q6 via contact C12. *Id.* at 10:18–22, 10:37–41, Fig. 5. First pad C12 contacts power supply lines V_{CC} (ground) formed by mask P116 in Oh's third metal layer through first via C12, second pad C12 in Oh's second metal layer, and second via C12. *Id.* at 11:11–13, 11:20–22, 11:28–31, 11:38–41, 11:55–60, 12:9–14, Figs. 6–9. Thus, masks P54/P56/P64/P66 (pads C11/C12 in Oh's first metal layer) are local interconnects corresponding to common power and common ground in Oh's first metal layer (single local interconnect layer).

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that claim 12 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

5. *Claim 16*

Claim 16 is an independent claim that is substantially similar to claim 8. Both claims recite a memory cell having a plurality (e.g., 4) of substantially oblong and substantially parallel active regions formed in a semiconductor substrate and both recite a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline. *Compare* Reexam. Cert. 1:25–35, *with id.* at 1:64–2:9.

Claim 16 differs from claim 8 in three ways. First, it requires the two inner active regions to have source/drain regions for p-channel transistors. *Id.* Second, it requires the two outer active regions to have source/drain regions for n-channel transistors. *Id.* Third, it does not require a plurality of substantially oblong and substantially parallel local interconnects above the semiconductor substrate that are substantially perpendicular to the active regions. *Id.* Given the substantial similarity between claims 8 and 16, Petitioner relies largely on its analysis of claim 8 to demonstrate how Oh discloses the limitations of claim 16. *See* Pet. 60–61, 66. Petitioner further argues that Oh teaches its inner active regions P12/P14 have source/drain regions for p-channel transistors and its outer active regions P10/P16 have source/drain regions for n-channel transistors. *See* Pet. 61–66 (citing Ex. 1004, 8:62–67, 9:30–63, 12:37–51, Fig. 3).

Patent Owner argues that Petitioner has failed to demonstrate that claim 16 is unpatentable over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 18–35. We disagree with Patent Owner's

arguments for the reasons discussed in § II.E.2, *supra*, and find Petitioner has demonstrated that Oh teaches the limitations recited in claim 16.

First, Oh teaches a series of four substantially oblong active regions P10–16 formed in a semiconductor substrate and arranged side-by-side with long axes substantially parallel, as well as a single local interconnect layer having local interconnects corresponding to bitlines and a global wordline, for the reasons discussed in §§ II.E.2.a, II.E.2.b, and II.E.2.d, *supra*. Second, Oh teaches “the first and second [outer] active regions P10 and P16 [are] for forming NMOS transistors” and “the third and fourth [inner] active regions P12 and P14 [are] for forming PMOS transistors.” Ex. 1004, 8:62–65, Fig. 3. Oh further teaches forming sources/drains for (a) NMOS transistors Q1 and Q3 “in the first active region” P10, (b) NMOS transistors Q2 and Q4 “in the second active region” P16, (c) PMOS transistor Q5 “in the third active region” P12, and (d) PMOS transistor Q6 “in the fourth active region” P14. *Id.* at 12:30–53, Figs. 3, 11. Thus, Oh teaches each inner active region P12/P14 comprises a pair of source/drain regions for p-channel transistors Q5/Q6 and each outer active region P10/P16 comprises a pair of source/drain regions for n-channel transistors Q1–Q4.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that claim 16 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

6. Claim 18

Claim 18 depends from claim 16 and requires the single local interconnect layer to include local interconnects corresponding to common power and common ground. Reexam. Cert. 2:13–15. Claim 18, therefore, adds to claim 16 the same limitation that claim 12 adds to claim 8. *Compare id.* at 1:39–41, *with id.* at 2:13–15.

Given the substantial similarity between claims 8/16 and 12/18, Petitioner relies on its analysis of claim 12 to demonstrate how Oh discloses the limitations of claim 18. *See* Pet. 66–67. Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 18 over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 18–35. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2, *supra*. Moreover, we agree with Petitioner that Oh discloses a single local interconnect layer that includes local interconnects corresponding to common power and common ground for the reasons discussed in § II.E.4, *supra*.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that claim 18 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

7. *Claim 22*

Claim 22 depends from claim 16 and requires a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions. *Reexam. Cert.* 2:37–40.

As discussed in § II.E.2.c, Petitioner maps Oh’s polysilicon gates, formed by masks P20/P22 and having their same shapes and arrangements, to the claim 8 limitation requiring a plurality of substantially oblong local interconnects above said substrate and substantially perpendicular to the active regions in the substrate. Petitioner relies on these same polysilicon gates to meet the claim 22 limitation requiring a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions. *See* Pet. 67.

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 22 over Oh for the same reasons discussed above

with respect to claim 8. *See* PO Resp. 18–35. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2, *supra*. Moreover, we agree with Petitioner that Oh’s polysilicon gates formed by masks P20/P22 are a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions of Oh’s semiconductor substrate for the reasons discussed in § II.E.2.c, *supra*.

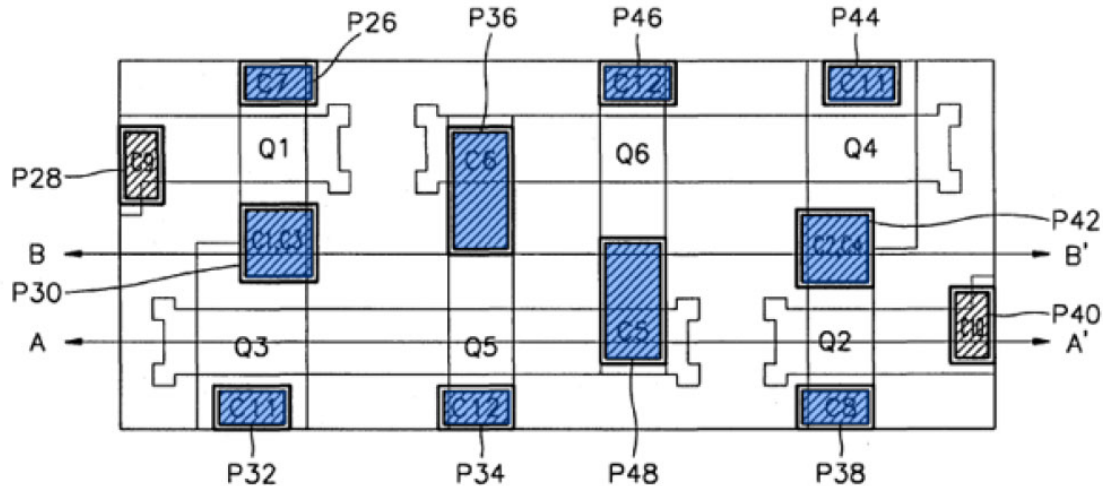
Accordingly, for the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that claim 22 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

8. *Claim 23*

Claim 23 depends from claim 16 and requires source/drain contacts to the source/drain regions of transistors, wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures. Reexam. Cert. 2:41–46.

Petitioner argues Oh teaches these limitations. *See* Pet. 54–55, 68–70. Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 23 over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 18–35. We disagree with these arguments for the reasons discussed in § II.E.2, *supra*, and find Petitioner demonstrates that Oh teaches the limitations of claim 23.

Petitioner illustrates Oh’s teachings with a colorized version of Figure 4 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Figure 4 of Oh showing masks for contacts C1–C8, C11, and C12 (blue). Pet. 68. Petitioner demonstrates how Oh teaches contacts C1–C8, C11 and C12 connect the sources/drains of transistors Q1–Q6 formed in active regions P10–P16. *Id.* at 68–70 (citing/quoting Ex. 1004, 7:56–58, 9:30–63, 12:37–53, 16:4–23, Figs. 4–25).

Oh teaches contact holes C1/C3 are formed on the drains of transistors Q1/Q3, contact holes C2/C4 are formed on the drains of transistors Q2/Q4, contact hole C5 is formed on the gates of transistors Q3/Q5 and the source of transistor Q6, contact hole C6 is formed on the gates of transistors Q4/Q6 and the source of transistor Q5, contact hole C7 is formed on the source of transistor Q1, contact hole C8 is formed on the source of transistor Q2, contact holes C11 are formed on the sources of transistors Q3/Q4, and contact holes C12 are formed on the drains of transistors Q5/Q6. *Id.* at 9:30–63, Fig. 4. Oh further teaches these contact holes are filled with tungsten to form contact plugs. *Id.* at 7:56–58, 16:4–23, Figs. 13, 14, 20, 21.

Contact plugs C5/C6 are each shared contacts to a polysilicon structure and inner active region because C5 contacts the polysilicon gates of transistors Q3/Q5 and the source of transistor Q6 formed in inner active

region P14, and C6 contacts the polysilicon gates of transistors Q4/Q6 and the source of transistor Q5 formed in inner active region P12. *Id.* at 9:44–47, 9:60–63, Figs. 14, 21.

For the reasons discussed above, Petitioner has demonstrated by a preponderance of evidence that claim 23 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

F. Obviousness Over Oh and Baker

As discussed in §§ II.E.2–II.E.8, *supra*, Petitioner has shown by a preponderance of evidence that claims 8, 10, 12, 16, 18, 22, and 23 of the '805 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Oh. This finding is dispositive of Petitioner's challenge to the patentability of all of the challenged claims. Accordingly, we need not address whether Petitioner has further shown, by a preponderance of evidence, that these claims are also unpatentable as obvious over the combination of Oh and Baker. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but also can “greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

III. CONCLUSION

We have reviewed the Petition, Patent Owner Response, Petitioner Reply, and Patent Owner Sur-Reply. We have considered all of the evidence and arguments presented by Petitioner and Patent Owner. We find, on this record, Petitioner has demonstrated by a preponderance of evidence

that claims 8, 10, 12, 16, 18, 22, and 23 of the '805 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.⁷

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
8, 10, 12, 16, 18, 22, 23	103(a)	Oh	8, 10, 12, 16, 18, 22, 23	
8, 10, 12, 16, 18, 22, 23	103(a)	Oh, Baker	Not Decided	Not Decided
Overall Outcome			8, 10, 12, 16, 18, 22, 23	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown on this record that claims 8, 10, 12, 16, 18, 22, and 23 of the '805 patent are unpatentable under 35 U.S.C. § 103(a) over Oh; and

FURTHER ORDERED that this Decision is final, and a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. §§ 42.8(a)(3), (b)(2).

IPR2020-00990
Patent 6,534,805 C1

FOR PETITIONER:

Xin-Yi Zhou
Ryan Yagura
Nicholas J. Whilt
Benjamin M. Haber
O'MELVENY & MYERS LLP
vzhou@omm.com
ryagura@omm.com
nwhilt@omm.com
bhaber@omm.com

Tyler R. Bowen
Philip A. Morin
PERKINS COIE LLP
bowen-ptab@perkinscoie.com
morin-ptab@perkinscoie.com

FOR PATENT OWNER:

Theodoros Konstantakopoulos, Ph.D.
Jordan N. Malz
Ryan G. Thorne
DESMARAIS LLP
tkonstantakopoulos@desmaraisllp.com
jmalz@desmaraisllp.com
rthorne@desmaraisllp.com