

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

SOLAS OLED LTD.,
Patent Owner.

IPR2021-00591
Patent 7,868,880 B2

Before SALLY C. MEDLEY, JO-ANNE M. KOKOSKI, and
JULIA HEANEY, *Administrative Patent Judges*.

HEANEY, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Display Co., Ltd., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively, “Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–40 of U.S. Patent No. 7,868,880 B2 (Ex. 1001, “the ’880 patent”). Paper 4 (“Petition” or “Pet.”). Solas OLED Ltd. (“Patent Owner”) did not file a Preliminary Response.

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Upon consideration of the Petition and the evidence of record, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing the unpatentability of at least one claim challenged in the Petition. Accordingly, we institute an *inter partes* review of all claims and all grounds asserted in the Petition.¹

A. *Related Proceedings*

Petitioner identifies the following litigation involving the ’880 patent: *Solas OLED Ltd. v. Samsung Electronics Co., Ltd. et al.*, Case No. 2:20-cv-00307 (E.D. Tex.) (the “Texas Action”); and *In the matter of Certain Active Matrix OLED Display Devices And Components Thereof*, Complaint

¹ *Guidance on the Impact of SAS on AIA Trial Proceedings* (Apr. 26, 2018), <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>; *see also SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS Guidance”).

No. 337-TA-1243² (U.S. International Trade Commission) (the “ITC Action”). Pet. 1–2.

B. The '880 Patent

The '880 patent, titled “Display Apparatus and Drive Control Method Thereof,” describes a display apparatus having an active matrix type display panel that includes a plurality of current control type optical elements, the apparatus being “capable of displaying moving images with a favorable display quality while being capable of displaying image information at an appropriate gradation corresponding to the display data.” Ex. 1001, at [54], 1:18–21, 3:32–38. The '880 patent describes four embodiments of a display apparatus having different display panels and peripheral circuits for the display panels. *Id.* at 4:14–5:35. Figures 9–11 of the '880 patent illustrate a second embodiment of the display apparatus. *Id.* at 4:40–49. Figure 9 is reproduced below.

² Petitioner refers to the “Complaint No.” (Pet. 2), but the ITC website indicates that 337-TA-1243 is the Investigation Number (Inv. No.). *See* https://usitc.gov/secretary/fed_reg_notices/337/337_1243_notice_01272021s-gl.pdf.

FIG.9

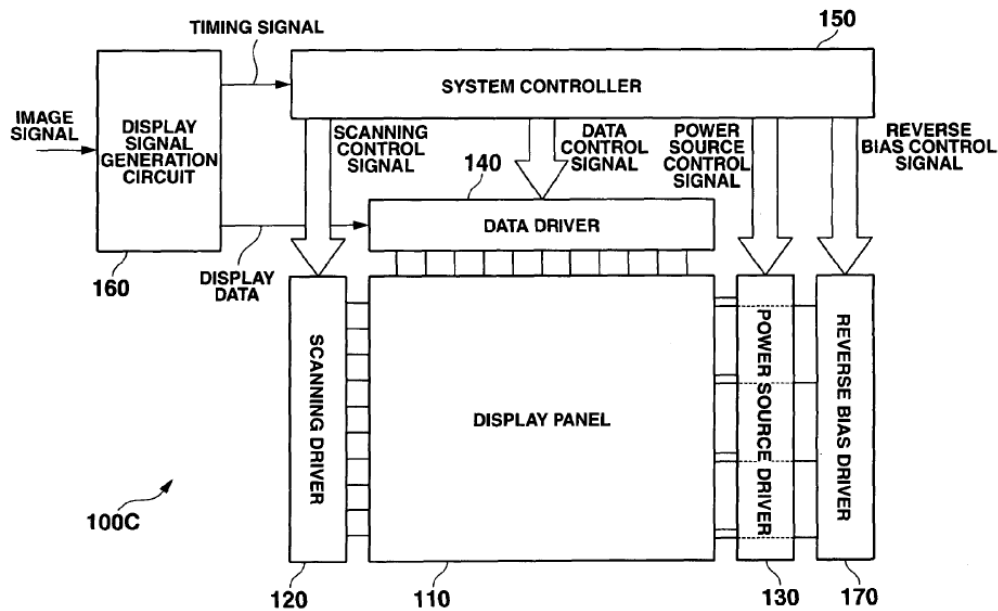


Figure 9 depicts display apparatus 100C, including display panel 110, scanning driver/scanning drive unit 120, power source driver/power source drive unit 130, data driver/data drive unit 140, system controller/drive control unit 150, display signal generation circuit 160, and reverse bias driver/state setting unit 170. *Id.* at 4:40–42, 18:11–18, 18:35–37.

Figure 10, reproduced below, depicts a display panel for the display apparatus of Figure 9. *Id.* at 17:33–35.

FIG.10

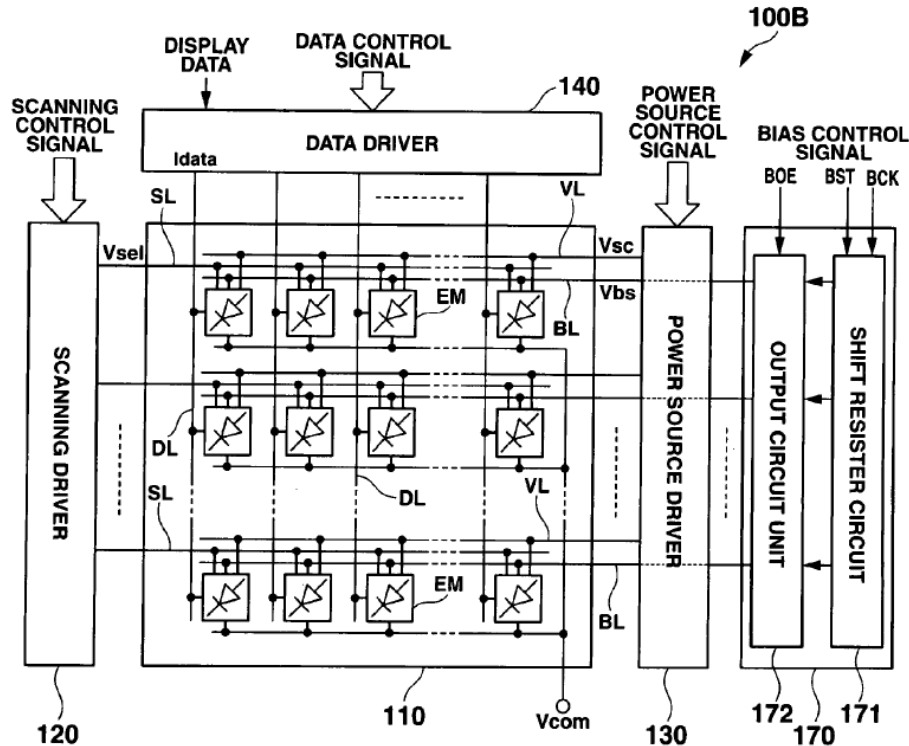


Figure 10 depicts display panel 110 having a plurality of display pixels EM arranged in two dimensions in row and column directions. *Id.* at 18:17–20. Scanning driver 120 sequentially applies selection level scanning signal V_{sel} to scanning lines SL of display panel 110 to set display pixels EM for each row to a selection state. *Id.* at 18:20–45. Power source driver 130 sequentially applies drive voltage V_{sc} to power source lines VL arranged in parallel to scanning lines SL in each row. *Id.* Data driver 140 supplies a gradation signal (gradation current I_{data}) corresponding to display data, to display pixels EM via data lines DL. *Id.* System controller 150 generates and outputs a scanning control signal, a power source control signal, a reverse bias control signal and a data control signal for performing a predetermined image display operation in display panel 110. *Id.* Display signal generation circuit 160 generates display data (luminance gradation

data) and supplies the data to data driver 140 on the basis of a picture image supplied from the outside. *Id.* Reverse bias driver 170 applies bias signal V_{bs} (a set signal) having a predetermined voltage level to display pixels EM in each row. *Id.* Display signal generation circuit 160 generates display data (luminance gradation data) and outputs the display data to data driver 140, and also supplies to system controller 150 a timing signal for displaying predetermined image information to display panel 110. *Id.*

Figure 11, reproduced below, illustrates in more detail display pixel EM and its display drive circuit DC2. *Id.* at 17:37–40, 19:18–23.

FIG.11

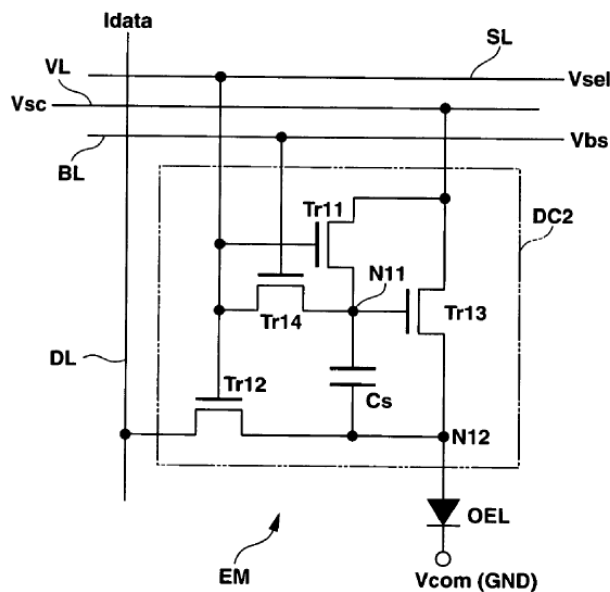


Figure 11 depicts display pixel EM of display panel 110, including display drive circuit DC2 and organic EL element (a light emitting element) OEL. *Id.* at 19:18–39. Display drive circuit DC2 fetches a gradation signal (gradation current I_{data}) corresponding to display data and generates a display drive current. *Id.* OEL performs a light emitting operation with a predetermined luminance gradation on the basis of the display drive current.

Id. Display drive circuit DC2 includes: thin film transistor (writing control circuit) Tr11; thin film transistor (writing control circuit) Tr12; thin film transistor (a control circuit) Tr13; thin film transistor (a bias control circuit) Tr14; and capacitor Cs (electric charge accumulation circuit). *Id.* at 7:32–40, 19:28–39. Thin film transistor Tr14 has a gate terminal (a control terminal) connected with bias line BL and a drain terminal and a source terminal (one and the other end of the conduction channel) respectively connected with scanning line SL and contact point N11. *Id.* at 19:34–39.

The display apparatus embodiment of Figures 9–11 addresses a problem of a change in threshold voltage (V_{th} shift, resulting from a drive history) that may be generated in amorphous silicon thin film transistors. *Id.* at 17:52–55. This problem occurs

in the case where an amorphous silicon thin film transistor is applied as a switching element (thin film transistor Tr13) for display drive, the current value of the display drive current I_b which is supplied to the organic EL element OEL owing to the change in threshold voltage does not correspond to display data, and the light emitting operation (the display operation) cannot be performed with an appropriate luminance gradation. Consequently, there is a possibility that the deterioration of the display image quality is invited.

Id. at 17:55–65. To address this problem, the voltage between the gate and the source (potential V_c between the ends of capacitor Cs illustrated in Figure 11) of the display drive switching element (thin film transistor Tr13, illustrated in Figure 11) of each display pixel EM is set to 0V (no voltage) or a negative voltage (a reverse bias voltage) in the non-light emitting operation period (the non-display operation period) except for the time of the light emitting operation (the display operation), resulting in a change in threshold

voltage in a frame period to suppress a change in threshold voltage of the switching element. *Id.* at 17:66–18:10.

Reverse bias driver 170 shown in Figure 10 includes a shift register 171 and an output circuit unit 172, with (i) shift register 171 sequentially outputting a shift signal corresponding to the bias line BL in each row on the basis of the clock signal BCK and the start signal BST supplied from the system controller 150 (illustrated in Figure 9), and (ii) output circuit unit 172 converting the shift signal to a predetermined voltage level to output the shift signal to each bias line BL as the bias signal Vbs on the basis of the output control signal BOE supplied as a bias control signal. *Id.* at 18:56–67. System controller 150 generates and outputs the bias control signal to reverse bias driver 170 as a timing control signal for controlling the operation state of reverse bias driver 170 in addition to scanning driver 120, power source driver 130 and data driver 140. *Id.* at 19:1–17. Consequently, a control is performed for (i) generating a scanning signal Vsel and a drive voltage Vsc having a predetermined voltage level, a gradation signal (a gradation current Idata) corresponding to the display data and a bias signal Vbs to output them to display panel 110, and (ii) continuously performing a drive control operation (a non-light emitting operation, a reverse bias setting operation, a writing operation, and a light emitting operation) in each display pixel EM to display predetermined image information based on an image signal on display panel 110. *Id.*

C. The Challenged Claims

Petitioner challenges claims 1–40 of the '880 patent. Pet. 1. Claims 1, 2, 3, and 25 are independent, claims 4–24 depend from claim 3, and

claims 26–40 depend from claim 25. Claim 25, reproduced below, is illustrative of the subject matter of the challenged claims:³

25. [25P] A drive control method of controlling a display apparatus to display image information corresponding to display data, wherein the display apparatus comprises a display panel including a plurality of display pixels arranged thereon in vicinities of intersections of a plurality of scanning lines arranged in a row direction and a plurality of data lines arranged in a column direction, and wherein each of the plurality of display pixels has an optical element and a display drive circuit which controls an operation of the optical element, the display drive circuit having a first switch circuit including a control terminal and a conduction channel having a first end and a second end, a drive voltage being applied to the first end of the conduction channel, a first end of the optical element being connected to the second end of the conduction channel, and a second end of the optical element being set to a given potential, the method comprising:

[25.1] sequentially setting the display pixels to a selection state, row by row;

[25.2] sequentially supplying a gradation signal corresponding to the display data to the display pixels in each row set to the selection state;

[25.3] in a display period, supplying as the drive voltage a voltage which sets each of the display pixels to a display operation state, and setting the display drive circuit of each of the display pixels to the display operation state in a bias state corresponding to the gradation signal; and

[25.4] in a non-display period including a period in which the display pixels are set to the selection state, supplying as the drive voltage a voltage which sets each of the display pixels to a non-display operation state, and setting each of the display pixels to the non-display operation state in which the display data is not displayed.

³ We reference Petitioner’s labels in claim 25. *See* Ex. 1002, 8; Pet. 71–72.

Ex. 1001, 42:38–43:2.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Challenged Claims	35 U.S.C. ⁴	Reference(s)/Basis
1–9, 11–14, 25–32	§ 102	Miyazawa ⁵
1–9, 11–14, 25–32	§ 103	Miyazawa
1–14, 25–33	§ 102	Morosawa ⁶
1–14, 25–33	§ 103	Morosawa
18–24, 34–40	§ 103	Morosawa and Shirasaki ⁷
24, 40	§ 103	Morosawa, Shirasaki, and Koyama ⁸
15–17	§ 103	Morosawa and Hector ⁹

Pet. 3. Petitioner relies on the Declaration of Miltiadis Hatalis, Ph.D.
(Ex. 1003) (“Hatalis Declaration”).

We note that Petitioner did not submit copies of the full text of
Morosawa (Ex. 1008) and Shirasaki (Ex. 1009). Instead, Morosawa and

⁴ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the ’880 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

⁵ US Patent Application Publication No. 2005/0083270 A1 to Miyazawa, published April 21, 2005 (Ex. 1006).

⁶ International Publication WO 2004/040543 A3 to Morosawa, published May 13, 2004 (Ex. 1008). Exhibit 1008 as submitted includes only the cover page of Morosawa and its International Search Report.

⁷ International Publication WO 2004/086347 A3 to Shirasaki, published October 7, 2004 (Ex. 1009). Exhibit 1009 as submitted includes only the cover page of Shirasaki and its International Search Report.

⁸ US Patent Application Publication No. 2003/0197664 A1 to Koyama, published October 23, 2003 (Ex. 1011).

⁹ US Patent No. 7,564,433 B2 to Hector et al., issued July 21, 2009 (Ex. 1010).

Shirasaki as submitted include only the cover page and a copy of its respective International Search Report. Because Petitioner cites to the text of both Morosawa and Shirasaki in the Petition (*see, e.g.*, Pet. 77 (citing Ex. 1008, 60:18–20; Ex. 1009, 54:16–23, 55:22–26), we consider Petitioner’s failure to submit the full text as a clerical error. Accordingly, Exhibits 1008 and 1009 will be expunged, and Petitioner is directed to file a replacement copy of each exhibit within ten business days of this Decision.

II. ANALYSIS

A. Claim Construction

Petitioner does not propose construction of any claim term. Pet. 11–12.

We determine we need not explicitly construe any claim terms at this stage of the proceeding. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed.

Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.*

Petitioner argues a person of ordinary skill in the art at the time of the invention

would have had at least a bachelor's degree in electrical engineering (or equivalent) and at least two years' industry experience, or equivalent experience in circuit design or related fields. Alternatively, a POSA could substitute directly relevant additional education for experience, e.g., an advanced degree relating to the design of electroluminescent devices, drive circuits, or other circuit design or an advanced degree in electrical engineering (or equivalent), with at least one year of industry experience in a related field.

Pet. 11 (citing Ex. 1003 ¶¶ 35–37).

For purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art. Based on our review of the '880 patent and the asserted prior art, we determine that Petitioner's definition comports with the qualifications a person would have needed to understand and implement the teachings of the '880 patent and prior art.

C. Principles of Law

“Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference,” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989), and that the claim limitations be “arranged or combined in the same way as recited in the claim[],” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008). However, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when available, evidence such as commercial success, long felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *see KSR*, 550 U.S. at 407 (“While the sequence of these questions might be reordered in any particular case, the [Graham] factors continue to define the inquiry that controls.”).

The Supreme Court made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. Reaching this conclusion, however, requires more than merely showing that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness additionally requires that a person of ordinary skill at the time of the invention “would have selected and combined those prior art elements in the

normal course of research and development to yield the claimed invention.”
Id.

D. Alleged Anticipation by Miyazawa

Petitioner contends Miyazawa anticipates claims 1–9, 11–14, and 25–32 of the ’880 patent. Pet. 14–49.

1. Miyazawa (Ex. 1006)

Miyazawa is titled “Electronic Circuit, Method of Driving the Same, Electronic Device, Electro-Optical Device, Electronic Apparatus, and Method of Driving the Electronic Device,” and “relates to an electronic circuit suitable for driving a driven element such as an electro-optical element.” Ex. 1006, at [54], [57], ¶ 2. Figure 1 of Miyazawa, reproduced below, illustrates a configuration of an electro-optical device. *Id.* ¶¶ 77, 88.

FIG. 1

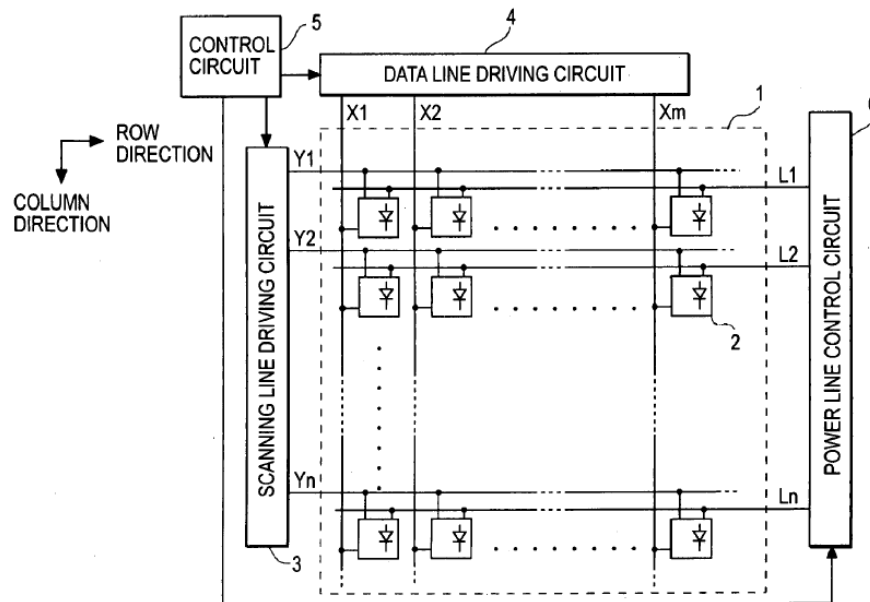


Figure 1 depicts display unit 1, an active matrix type display panel, in which the electro-optical elements are driven by thin film transistors (TFTs). *Id.* ¶ 88. In display unit 1, m dots by n lines of a group of pixels are arranged in a matrix, in a two-dimensional plan view. *Id.* A group of scanning lines Y1 to Yn each extending in a horizontal direction, and a group of data lines X1 to Xm each extending in a vertical direction, are provided, and pixels 2 (pixel circuits) are arranged corresponding to intersections of the scanning lines and the data lines. *Id.* Power lines L1 to Ln are provided in correspondence with scanning lines Y1 to Yn, and extend in a direction intersecting data lines X1 to Xm (a direction in which the scanning lines Y1 to Yn extend). *Id.* To the respective power lines L1 to Ln, a row of pixels (m dots) along a direction in which one scanning line Y extend are commonly coupled. *Id.* Pixel 2 may be a minimum unit for image display, or in the case of a color panel, pixel 2 may comprise three sub-pixels of R, G, and B. *Id.* Control circuit 5 synchronously controls scanning line driving circuit 3, data line driving circuit 4, and power line control circuit 6, based on vertical synchronizing signal Vs, horizontal synchronizing signal Hs, dot clock signal DCLK, and grayscale data D, which are inputted from devices. *Id.* ¶ 90. Under synchronous control, scanning line driving circuit 3, data line driving circuit 4, and power line control circuit 6 cooperate with each other to control display unit 1. *Id.*

Scanning line driving circuit 3 includes shift registers and output circuits, and outputs scanning signal SEL to scanning lines Y1 to Yn to perform line sequential scanning. *Id.* ¶ 91. Scanning signal SEL is a two-level signal of a high potential level (an “H level”) and a low potential level (an “L level”). *Id.* A scanning line corresponding to a row of pixels to

which data is written is set to the H level, and other scanning lines are set to the L level. *Id.* Scanning line driving circuit 3 performs sequential scanning for selecting each scanning line Y in a predetermined order (e.g., from top to bottom) for every period (1F) in which images of one frame are displayed. *Id.* In any horizontal scanning period (1H), m data items corresponding to the number of data lines X are sequentially latched. *Id.* Then, in next one horizontal scanning period (1H), the latched m data voltages Vdata are simultaneously outputted to the corresponding data lines X1 to Xm. *Id.*

¶ 92. Power line control circuit 6 variably sets voltages of the power lines L1 to Ln in units of rows of pixels, in synchronization with the line sequential scanning by scanning line driving circuit 3. *Id.* ¶ 93.

Miyazawa discloses five embodiments of pixel circuits (pixels 2). *Id.* ¶¶ 78–87. Figure 9 of Miyazawa, reproduced below, illustrates a pixel circuit according to a fourth embodiment of Miyazawa. *Id.* ¶ 85.

FIG. 9

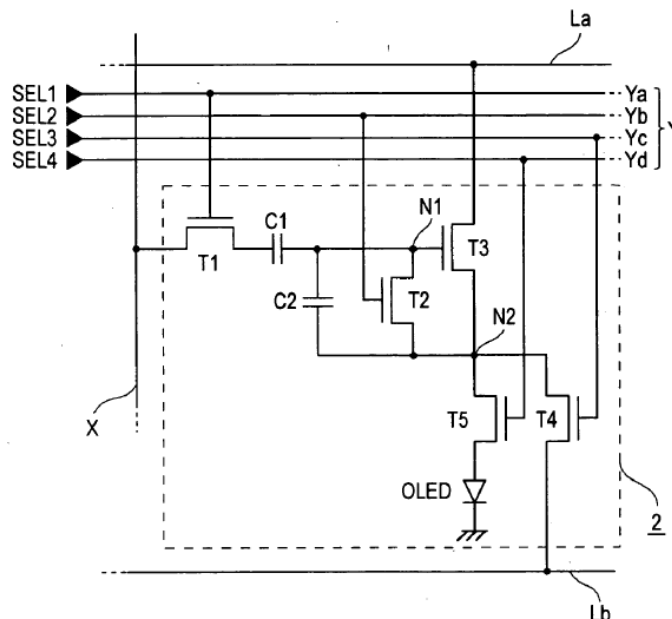


Figure 9 depicts a voltage follower type voltage-programmed mode pixel circuit. *Id.* ¶ 123. Scanning line Y includes four scanning lines Ya to Yd, to which scanning signals SEL1 to SEL4 are respectively supplied, and Figure 9 also includes two power lines La and Lb. *Id.* The pixel circuit has an organic EL element OLED, five n-channel type transistors T1 to T5, and two capacitors C1 and C2 each storing data. *Id.*

The gate of first switching transistor T1 in Figure 9 is coupled to the first scanning line Ya to which the first scanning signal SEL1 is supplied. *Id.* ¶ 124. One terminal of transistor T1 is coupled to data line X, and the other terminal is coupled to one electrode of first capacitor C1. *Id.* The other electrode of capacitor C1 is coupled to node N1. *Id.* The gate of driving transistor T3, one terminal of second switching transistor T2, and one electrode of second capacitor C2 are also coupled to node N1. *Id.* One terminal of driving transistor T3 is coupled to first power line La, and the other terminal of driving transistor T3 is coupled to node N2, to which the other terminal of second switching transistor T2, the other electrode of second capacitor C2, one terminal of a third switching transistor T4, and the anode of the organic EL element OLED via a fourth switching transistor T5, are also coupled. *Id.* Reference voltage Vss is applied to the cathode of the organic EL element OLED. *Id.* Second capacitor C2 is provided between the gate of driving transistor T3 and node N2, forming a voltage follower type circuit. *Id.* Second switching transistor T2 is provided in parallel to second capacitor C2, whose gate is coupled to second scanning line Yb to which second scanning signal SEL2 is supplied. *Id.* The other terminal of third switching transistor T4 is coupled to second power line Lb, and a gate of third switching transistor T4 is coupled to third scanning line Yc to which

third scanning signal SEL3 is supplied. *Id.* Further, a gate of fourth switching transistor T5 is coupled to fourth scanning line Yd to which fourth scanning signal SEL4 is supplied. *Id.*

Figure 10 of Miyazawa, reproduced below, is a timing chart for the operation of the pixel circuit shown in Figure 9. *Id.* ¶¶ 86, 125.

FIG. 10

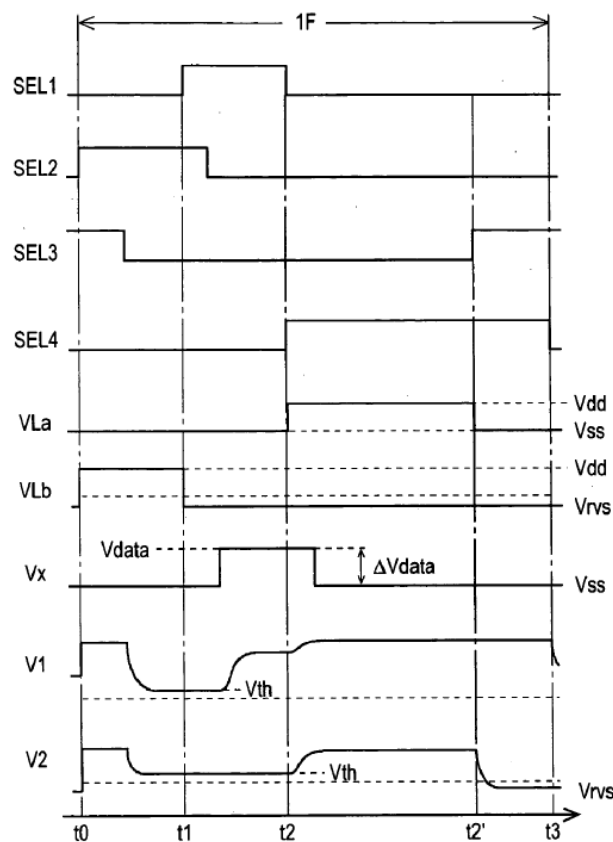


Figure 10 depicts periods t_0 to t_3 corresponding to one frame period $1F$, and including reverse bias period t_2' to t_3 during which a reverse bias is applied to element OLED, in addition to an initial period t_0 to t_1 , a data writing period t_1 to t_2 , and a driving period t_2 to t_2' . *Id.* ¶ 125. In Figure 10, V_{dd} is a power voltage, voltage V_{La} is the voltage of first power line La,

voltage VLb is the voltage of second power line Lb, voltage V1 is the voltage of node N1 directly coupled to node N2, voltage V2 is the voltage of node N2, and voltage Vx is the voltage of data line X. *Id.* ¶¶ 126–129. The operation of the pixel circuit shown in Figure 10 enables Vth compensation and suppression of Vth shift in the same operation process (the initializing period t0 to t1). *Id.* ¶ 130. Further, during the reverse bias period t2' to t3, since the reverse bias is applied to the organic EL element OLED, it is possible to lengthen the life span of the organic EL element OLED. *Id.*

2. Analysis

Independent Claim 25

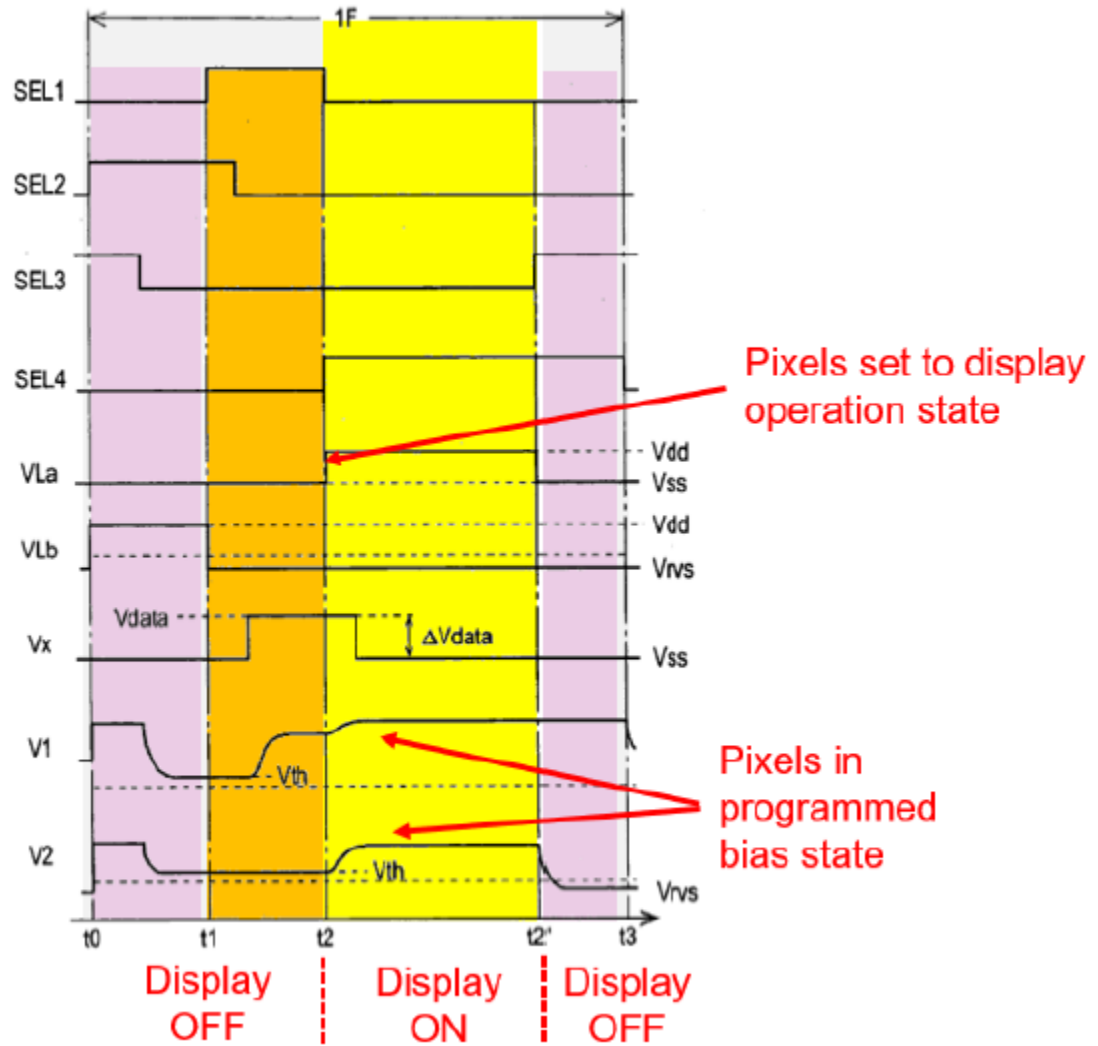
As to the preamble of claim 25, Petitioner contends Miyazawa discloses an active matrix type display panel in which electro-optical elements are driven by thin film transistors (TFTS) to display image data (recited “display apparatus”). Pet. 18, 44 (citing Ex. 1006 ¶¶ 88, 92, 128). Petitioner further contends Miyazawa’s display apparatus includes a display panel with pixels (2)/pixel circuits (recited “plurality of display pixels”) arranged in vicinities of intersections of scanning lines Y1 to Yn (recited “plurality of scanning lines”) arranged in a row direction and data lines X1 to Xm (recited “plurality of data lines”) arranged in a column direction, each of Miyazawa’s pixels 2 having an organic EL element OLED (recited “optical element”), and a pixel circuit illustrated in Miyazawa’s Figure 9 (recited “display drive circuit which controls an operation of the optical element”) including a driving transistor T3 (recited “first switch circuit” of the “display drive circuit”). Pet. 18–22, 25–26, 34–35, 44 (citing Ex. 1006 ¶¶ 88, 127–128, Figs. 1 and 9).

Claim 25 further recites “sequentially setting the display pixels to a selection state, row by row” (limitation [25.1]). Ex. 1001, 42:38–43:2. Petitioner contends Miyazawa discloses this limitation because Miyazawa discloses a scanning line driving circuit 3 which performs sequential scanning for selecting each scanning line Y in a predetermined order (e.g., from top to bottom) for every period in which images of one frame are displayed. Pet. 28, 44 (citing Ex. 1006 ¶¶ 91, 127).

Claim 25 further recites “sequentially supplying a gradation signal corresponding to the display data to the display pixels in each row set to the selection state” (limitation [25.2]). Ex. 1001, 42:38–43:2. Petitioner contends Miyazawa discloses this limitation because Miyazawa’s Figure 9 shows that, as each row is selected in sequence, gradation data is supplied from each data line in the selected row as the scan line turns on switching transistor T1. Pet. 28–29, 44 (citing Ex. 1006 ¶¶ 92, 127, Fig. 9).

Claim 25 further recites “in a display period, supplying as the drive voltage a voltage which sets each of the display pixels to a display operation state, and setting the display drive circuit of each of the display pixels to the display operation state in a bias state corresponding to the gradation signal” (limitation [25.3]). Ex. 1001, 42:38–43:2. Petitioner contends Miyazawa discloses this limitation because Miyazawa discloses that VLa rises to Vdd at time t2 to turn the pixels on, causing current to flow through the OLED according to a programmed bias state, such that during the prior selection/writing period, “the voltage V1 of node N1 are written in the capacitors C1 and C2” and “[t]his voltage stored on C1 and C2 sets drive transistor to the specific bias state that corresponds to that gradation signal, thus setting the OLED to the programmed brightness.” Pet. 45–46 (citing

Ex. 1006 ¶¶ 127–128, Fig. 10). Petitioner provides an annotated version of Miyazawa’s Figure 10, reproduced below:



Miyazawa Figure 10

Id. at 46. In the annotated version of Miyazawa’s Figure 10 above, Petitioner shades periods t_0 to t_1 , t_1 to t_2 , and t_2' to t_3 and labels them as “Display OFF” and shades period t_2 to t_2' as “Display ON.” *Id.* Petitioner also labels the rise of V_{La} to V_{dd} at time t_2 as “Pixels set to display operation state.” *Id.*

Claim 25 further recites “in a non-display period including a period in which the display pixels are set to the selection state, supplying as the drive voltage a voltage which sets each of the display pixels to a non-display operation state” and “setting each of the display pixels to the non-display operation state in which the display data is not displayed” (limitation [25.4]). Ex. 1001, 42:38–43:2. Petitioner contends Miyazawa discloses this limitation because Miyazawa discloses that drive voltage V_{La} drops to V_{ss} to turn off the pixels, and this off period includes the writing period t_1 to t_2 during which pixels are selected. Pet. 46 (citing Ex. 1006 ¶¶ 115, 127, Fig. 10).

After reviewing the evidence and arguments in the Petition regarding claim 25, which are unrebutted on this record, including the relevant portions of the supporting Hatalis Declaration, we are persuaded that Petitioner’s discussion of the particular structures in Miyazawa, and the explanations in the Petition and the Hatalis Declaration, are sufficient to establish a reasonable likelihood that Miyazawa anticipates claim 25. Accordingly, we determine Petitioner has established a reasonable likelihood of prevailing on its anticipation challenge with respect to claim 25.

Claims 26–32

Claims 26–32 depend directly or indirectly from claim 25. Petitioner directs us to portions of Miyazawa that disclose the additional limitations of these claims. Pet. 47–49. After reviewing the evidence and arguments Petitioner presents in the Petition regarding claims 26–32, which are unrebutted on this record, including the relevant portions of the supporting Hatalis Declaration, we are persuaded Petitioner has established a reasonable

likelihood of prevailing on its anticipation challenge with respect to claims 26–32.

Claims 1–3

Petitioner contends Miyazawa discloses each of the limitations of independent claims 1–3. Pet. 14–35. These claims contain limitations similar to those in claim 25, and Petitioner relies on the same arguments for those limitations in claims 1–3 as it does for claim 25. *Id.* Petitioner also directs us to portions of Miyazawa that disclose the additional limitations of claims 1–3. *Id.* Accordingly, for the reasons discussed above, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 1–3 as anticipated by Miyazawa.

3. Conclusion

Because we determine Petitioner has demonstrated a reasonable likelihood of prevailing with respect to its anticipation challenge as to at least one claim of the '880 patent, we need not address Petitioner's contentions as to Miyazawa's disclosures with respect to every challenged claim. *See SAS* Guidance (“[T]he PTAB will institute as to all claims or none. If the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition.”). For the foregoing reasons, we determine Petitioner has demonstrated a reasonable likelihood of prevailing with respect to its argument that Miyazawa anticipates claims 1–40.

III. CONCLUSION

Because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the '880 patent is unpatentable over the prior art of record, we institute an *inter partes* review as to all the challenged

claims on all the grounds asserted in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1353 (2018) (“The agency cannot curate the claims at issue but must decide them all.”).

Our factual findings, conclusions of law, and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of all challenged claims of the ’880 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the ’880 patent is hereby instituted commencing on the entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

FURTHER ORDERED that Petitioner shall file a replacement copy of Exhibits 1008 and 1009 within ten business days of this Decision.

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PETITIONER:

Nicholas Whilt
Ryan Yagura
Brian Cook
Ben Haber
Mark Liang
O'MELVENY & MYERS LLP
nwhilt@omm.com
ryagura@omm.com
bcook@omm.com
bhaber@omm.com
mliang@omm.com

PATENT OWNER:

Neil Rubin
Philip Wang
RUSS AUGUST & KABAT
nrubin@raklaw.com
pwang@raklaw.com