

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
ADVANCED MICRO DEVICES, INC.¹ and
STMICROELECTRONICS, INC.,²
Petitioner,

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

IPR2020-01491
Patent 6,534,805 C1

Before KRISTEN L. DROESCH, JOHN F. HORVATH, and
JASON W. MELVIN, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Advanced Micro Devices, Inc., which filed a petition in IPR2021-00776, has been joined as a party to this proceeding. *See* Paper 25.

² STMicroelectronics, Inc., which filed a petition in IPR2021-00704, has been joined as a party to this proceeding. *See* Paper 22.

I. INTRODUCTION

A. *Background and Summary*

Qualcomm Incorporated (“Qualcomm”) filed a Petition requesting *inter partes* review of claims 7–32 and 53–61 (“the challenged claims”) of U.S. Patent No. 6,534,805 C1 (Ex. 1001, “the ’805 patent”). Paper 1 (“Pet.”), 5–6. Monterey Research, LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). Upon consideration of the Petition and Preliminary Response, we instituted *inter partes* review of all challenged claims on all grounds raised. Paper 10 (“Dec. Inst.”).

Subsequent to our Institution Decision, Advanced Micro Devices, Inc. (“AMD”) and STMicroelectronics, Inc. (“STM”) were joined as parties to this proceeding. *See* Papers 22, 25. Moreover, in *Advanced Micro Devices, Inc. v. Monterey Research, LLC*, IPR2020-00990, Paper 45 (PTAB, Nov. 23, 2021), we determined AMD and STM showed by a preponderance of evidence that claims 8, 10, 12, 16, 18, 22, and 23 of the ’805 patent are unpatentable. Thus, AMD and STM are estopped from challenging the patentability of those claims in this proceeding. *See* 35 U.S.C. § 315(e)(1) (2018). Nonetheless, to challenge the patentability of claims 9, 11, 13–15, 17, 19–21, and 24–26, AMD and STM must demonstrate in this proceeding how the prior art maps to the limitations of claims 8, 10, 12, 16, 18, 22, and 23, from which these claims depend. Unless noted otherwise, we collectively refer to Qualcomm, AMD, and STM as “Petitioner.”

Patent Owner filed a Response to the Petition (Paper 18, “PO Resp.”), Petitioner filed a Reply (Paper 23, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 26, “PO Sur-Reply”). An oral hearing was held on December 7, 2021, and the hearing transcript is included in the record. *See* Paper 33 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Qualcomm has demonstrated by a preponderance of evidence that claims 7–32 and 53–61 of the '805 patent are unpatentable and AMD, and STM have demonstrated by a preponderance of evidence that claims 7, 9, 11, 13–15, 17, 19–21, 24–32 and 53–61 of the '805 patent are unpatentable.

B. Real Parties-in-Interest

Qualcomm identifies itself, Qualcomm Technologies, Inc., and Qualcomm CDMA Technologies Asia-Pacific Pte Ltd. as real parties-in-interest. Pet. 2. AMD identifies itself, ATI Technologies ULC, Globalfoundries Inc., and Globalfoundries U.S. Inc. as real parties-in-interest. Paper 25, 3. STM identifies itself, STMicroelectronics N.V., and STMicroelectronics International N.V. as real parties-in-interest. Paper 22, 2. Patent Owner identifies itself and IPValue Management as real parties-in-interest. Paper 3, 1.

C. Related Matters

The parties identify the following as matters that can affect or be affected by this proceeding: *Monterey Research, LLC v. Advanced Micro Devices, Inc.*, No. 1:19-cv-02149 (D. Del.); *Monterey Research, LLC v. Qualcomm Inc.*, No. 1:19-cv-02083 (D. Del.); *Monterey Research, LLC v. STMicroelectronics N.V.*, No. 1:20-cv-00089 (D. Del.); *Monterey Research, LLC v. Marvell Tech. Grp. Ltd.*, No. 1:20-cv-00158 (D. Del.); and *Marvell Semiconductor, Inc. v. Monterey Research, LLC*, No. 3:20-cv-03296 (N.D. Cal.). Pet. 2; Paper 3, 1. The parties identify the following as an administrative matter that can affect or be affected by this proceeding:

Advanced Micro Devices, Inc. v. Monterey Research, LLC, IPR2020-00990 (PTAB). Pet. 3; Paper 3, 2.

*D. Evidence Relied Upon*³

Reference		Effective Date	Exhibit
Oh	US 6,417,549 B1	July 9, 2002	1004
R. Jacob Baker et al., <i>CMOS Circuit Design, Layout and Simulation</i> , (2011) (“Baker”)		1998	1005
Lee	US 5,702,982	Dec. 30, 1997	1020
Nii	US 6,347,062 B2	Apr. 3, 2001 ⁴	1021
Hara	US 5,930,163	July 27, 1999	1023

E. Asserted Grounds

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1A	8–14, 16–20, 22–25, 27, 28, 30–32	103(a)	Oh
1B	8–14, 16–20, 22–25, 27, 28, 30–32	103(a)	Oh, Baker
2A	7, 15, 21, 26, 29 ⁵	103(a)	Oh, Lee
2B	7, 15, 21, 26,	103(a)	Oh, Baker, Lee

³ Petitioner also relies upon the Declarations of Jack C. Lee, Ph.D. (Ex. 1019), Sylvia Hall-Ellis, Ph.D. (Exs. 1028, 1039), and Michael J. Collins (Ex. 1037). Patent Owner also relies upon the Declaration of Nader Bagherzadeh, Ph.D. (Ex. 2015).

⁴ Petitioner relies on the filing date of Nii for its prior art status under 35 U.S.C. § 102(e). *See* Pet. 5.

⁵ Petitioner lists claim 58 under grounds 2A/2B, however, provides no analysis for claim 58 under either ground. *Compare* Pet. 5, *with id.* at 77–92. Therefore, we do not list claim 58 under these grounds.

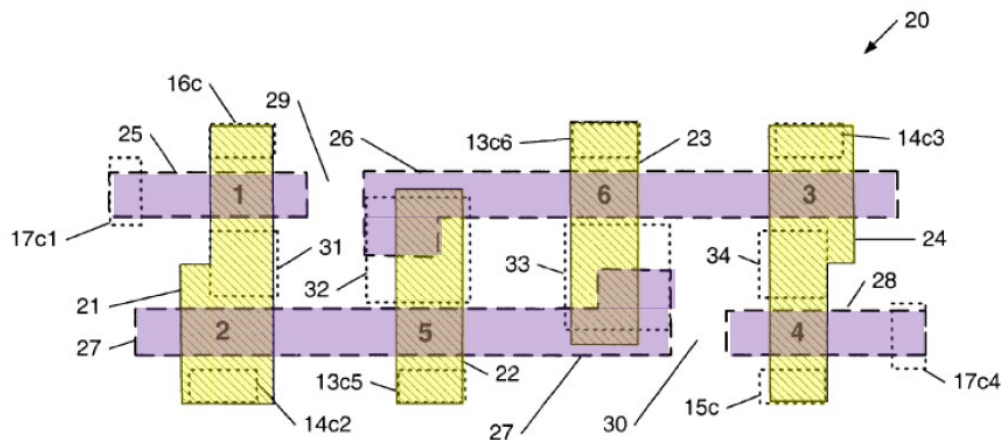
Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
	29		
3A	53–57, 59–61	103(a)	Oh, Nii
3B	53–57, 59–61	103(a)	Oh, Baker, Nii
4A	58	103(a)	Oh, Nii, Lee
4B	58	103(a)	Oh, Baker, Nii, Lee
5A	53–57, 59–61	103(a)	Oh, Hara
5B	53–57, 59–61	103(a)	Oh, Baker, Hara
6A	58	103(a)	Oh, Hara, Lee
6B	58	103(a)	Oh, Baker, Hara, Lee

II. ANALYSIS

A. The '805 Patent

The '805 patent is directed to “an improved Static Random Access Memory (SRAM) cell design and method of manufacture.” Ex. 1001, 1:7–10. Figure 1 of the '805 patent illustrates “the transistor configuration of an embodiment of an improved SRAM memory cell.” *Id.* at 4:61–62. The cell includes circuit components formed in silicon, a polysilicon layer, an interconnect layer, a first metal layer containing bitlines, and a second metal layer containing a wordline. *Id.* at 6:17–19, 10:30–43, 11:50–51, 13:19–30.

A modified version of Figure 2 of the '805 patent, colorized by Petitioner, is reproduced below. Pet. 8.



The figure is a Petitioner-colored version of Figure 2 of the '805 patent, illustrating the layout of the active regions (yellow) and gates (purple) of an SRAM memory cell 10. Pet. 8. Illustrated in the layout are “NMOS⁶ transistors 1–4 . . . formed within [outer] active regions 21 and 24, and PMOS⁷ transistors 5 and 6 . . . formed within [inner] active regions 22 and 23. Ex. 1001, 6:26–29.

Active regions 21–24 (yellow) “are arranged side-by-side and substantially parallel to each other.” *Id.* at 6:38–40. They are “substantially oblong, and . . . may be substantially rectangular as well.” *Id.* at 6:65–67. For example, “PMOS active regions . . . 22 or 23 . . . may have a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region.” *Id.* at 6:67–7:4. NMOS active regions 21 and 24 may be “substantially oblong if the length of the region is substantially constant and the width of the region . . . varies only with the respective widths of the access and latch transistors.” *Id.* at 7:24–28.

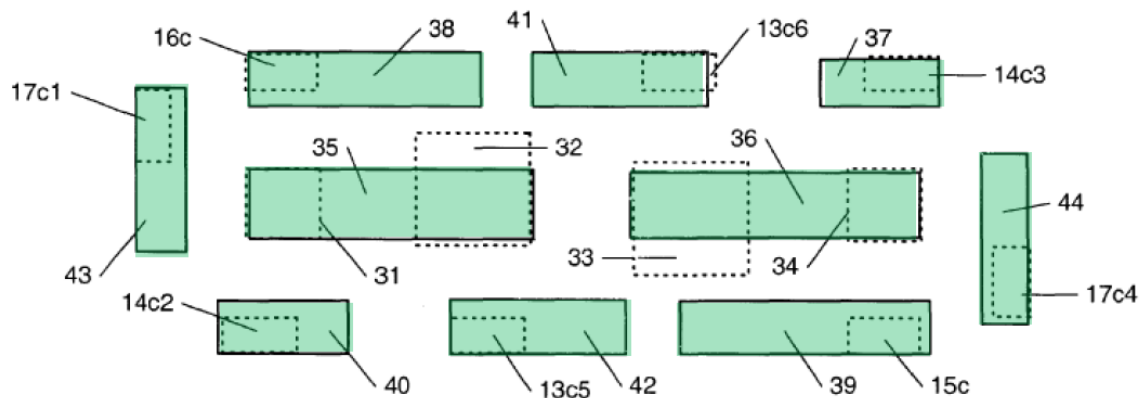
Polysilicon structures 25–28 (purple) are formed above and substantially perpendicular to active regions 21–24 (yellow). *Id.* at Fig. 2. Polysilicon structures 25 and 27 “are arranged above active region 21 to form gates of pass transistor 1 and latch transistor 2, respectively.” *Id.* at 6:55–57. Polysilicon structures 26 and 28 are arranged above active region 24 “to form gates of pass transistor 4 and latch transistor 3, respectively.” *Id.* at 6:58–60. “[P]olysilicon structures 26 and 27 each include two gates.” *Id.* at 11:37–38. For example, polysilicon structure 26 “form[s] gates of

⁶ N-type metal-oxide-semiconductor.

⁷ P-type metal-oxide-semiconductor.

PMOS latch transistor 6 and NMOS latch transistor 3,” and polysilicon structure 27 “form[s] gates of NMOS latch transistor 2 and PMOS latch transistor 5.” *Id.* at 11:32–37. Thus, “polysilicon structures 26 and 27 . . . each perform a local interconnecting function because they each connect two separate gate conductors together.” *Id.* at 11:38–41.

Figure 3 of the ’805 patent “illustrates a local interconnect layer which may be used in conjunction with the layout shown in FIG. 2.” *Id.* at 11:50–51. A modified version of Figure 3, colored by Petitioner, is reproduced below. Pet. 10.



The figure is a Petitioner-colored version of Figure 3 of the ’805 patent, which consists entirely of interconnects 35–43 that connect various components of transistors 1–6 (Fig. 2) to various structures in first and second metal layers (not shown) disposed above the interconnect layer. Ex. 1001, 10:30–42, 11:67–12:8, 13:10–32.

Interconnect 35 “connects the source of transistor 1 to the drains of transistors 2 and 5 and the gates of transistors 3 and 6” via contacts 31 and 32. *Id.* at 11:67–12:4, Figs. 2, 3. Interconnect 36, similarly, connects the source of transistor 4 to the drains of transistors 3 and 6 and the gates of transistors 2 and 5 via contacts 33 and 34. *Id.* at 12:6–8, Figs. 2, 3.

Interconnects 37 and 40, respectively, couple ground line V_{SS} in the first metal layer (not shown) to the sources of transistors 2 and 3 through contacts 14c2 and 14c3 and vias in a first dielectric layer (not shown) between the interconnect and first metal layers. *Id.* at 10:32–43, 13:16–27, Figs. 2, 3. Interconnects 38 and 39, respectively, couple bitlines in the first metal layer (not shown) to the drains of transistors 1 and 4 through contacts 16c and 15c and vias through the first dielectric layer (not shown). *Id.* at 10:30–43, 13:12–27, Figs. 2, 3. Interconnects 41 and 42, respectively, couple power line V_{CC} in the first metal layer (not shown) to the sources of transistors 5 and 6 through contacts 13c5 and 13c6 and vias in the first dielectric layer (not shown). *Id.* at 10:34–43, 13:18–27, Figs. 2, 3. Interconnects 43 and 44, respectively, couple global wordline 17 in the second metal layer (not shown) to gates 25 and 28 of transistors 1 and 4 through contacts 17c1 and 17c4 and vias in the first dielectric layer (not shown), and a second dielectric layer (not shown) between the first and second metal layers (not shown). *Id.* at 9:11–14, 13:27–32, Figs. 2, 3.

B. Illustrative Claim

Claims 8, 16, 27, 29, 30, 53, and 59 are independent claims. Ex. 1001, Reexam. Cert. 1:25–35, 1:64–2:9, 2:61–3:11, 3:15–56, 5:60–6:10, 6:36–52. Claims 9–15 depend directly or indirectly from claim 8. Ex. 1001, 14:36–45; Reexam. Cert. 1:19–20, 1:36–63. Claims 17–26 depend directly or indirectly from claim 16. *Id.* at Reexam. Cert. 2:10–60. Claim 28 depends directly from claim 27. *Id.* at 3:12–14. Claims 31–32 depend directly from claim 30. *Id.* at 3:57–67. Claims 54–58 depend directly or indirectly from claim 53. *Id.* at 6:11–35. Claim 60 depends directly from claim 59. *Id.* at 6:53–57.

Claim 8 is illustrative of the challenged claims and is reproduced below.

8. A memory cell comprising

a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another, and

a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions; and

a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.

Ex. 1001, Reexam. Cert. 1:25–35.

C. Level of Ordinary Skill in the Art

Petitioner identifies a person of skill in the art (“POSITA”) at the time of the invention as someone that would have had “a bachelor’s degree in electrical engineering, computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent.”

Pet. 12 (citing Ex. 1019 ¶¶ 50–53). In our Institution Decision, we adopted this description as our own. *See* Dec. Inst. 15–16. Neither party disputes that preliminary finding, which we maintain for purposes of this decision. *See* PO Resp. 14; Pet. Reply 1–29.

D. Claim Construction

In *inter partes* reviews, we interpret a claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019). Under that

standard, the “words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Moreover, that meaning applies “unless the patentee demonstrated an intent to deviate from [it] . . . by redefining the term or by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Teleflex, Inc. v. Ficoso N. America Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002); *see also Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). Only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

The parties dispute the meanings of the terms “substantially oblong active regions,” “substantially oblong local interconnects,” “substantially oblong polysilicon structures,” and “a single local interconnect layer.” *See* Pet. 13–15; Pet. Reply 1–10; PO Resp. 14–18; PO Sur-Reply 2–13. We construe these terms below.

1. Substantially Oblong Limitations

Petitioner argues all the “substantially oblong” terms—active regions, polysilicon structures, and interconnects—should be construed to have their plain and ordinary meaning of elongated, rectangular structures, which is how the Examiner construed them during reexamination of the ’805 patent. *See* Pet. 13 (citing Ex. 1007, 1015). Petitioner further argues that a person of ordinary skill in the art would have also considered the non-limiting shapes of the structures described in the Specification to be “substantially oblong.” *Id.* at 13–14 (citing Ex. 1001, 6:65–7:4, 7:20–31, 9:49–61, 11:1–10, 12:8–14).

In our Institution Decision, we preliminarily found a substantially oblong local interconnect was one that had a substantially rectangular shape, a substantially oblong active region was one that had one of the shapes described in column 7, lines 20–34 of the Specification, and a substantially oblong polysilicon structure was one that had one of the shapes described in column 11, lines 4–10 of the Specification. Dec. Inst. 18–22. Patent Owner does not dispute these preliminary constructions. *See* PO Resp. 14. Petitioner does not dispute our preliminary constructions of substantially oblong local interconnects and active regions, but does dispute and asks us to reconsider our preliminary construction of substantially oblong polysilicon structures. *See* Pet. Reply 2–3.

a) Active Regions

The Specification provides several non-limiting descriptions of substantially oblong active regions. *See, e.g.*, Ex. 1001, 6:65–67 (disclosing PMOS active regions “*may be substantially rectangular*”) (emphasis added); 7:20–24 (disclosing NMOS active regions “*may be considered to be substantially oblong if the length of the region is substantially constant and if the width of the region varies by approximately 1/3 or less along the length of the region*”) (emphasis added).

During prosecution, the patentee quoted several non-limiting descriptions of substantially oblong active regions to distinguish pending claim 1 over Kim,⁸ arguing the quoted descriptions “*define what is meant by an oblong shape as it pertains to an active region.*” Ex. 1006, 59–60 (quoting Ex. 1001, 7:20–34)⁹ (emphasis added). The patentee then argued

⁸ Japanese Patent JP 11-195716A.

⁹ Corresponding to page 11, line 29 to page 12, line 8 of the application.

that Kim’s active regions were not substantially oblong because they “illustrate[] the markedly dissimilar L-shaped active regions where the width of the active regions vary greater than 1/3 along the length of the active regions.” *Id.* at 60.

In our Institution Decision, we preliminarily found the patentee had disavowed “substantially oblong active regions” that did not have one of the shapes described in column 7, lines 20–34 of the Specification by claiming that portion of the Specification *defined* substantially oblong active regions. *See* Dec. Inst. 19. Petitioner disagrees, and contends that because the patentee’s arguments were “focused on Kim’s L-shaped regions” and “which L-shaped regions are properly considered ‘substantially oblong,’” the patentee “did not clearly and unmistakably disavow any claim scope regarding rectangles” or rectangularly shaped active regions. Pet. Reply 6 (citing *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1342 (Fed. Cir. 2009)).

Although claim terms are usually given their ordinary and customary meaning, that meaning may not apply “when a patent applicant surrender[s] claim scope during prosecution.” *Elbex Video, Ltd. v. Sensormatic Electronics Corp.*, 508 F.3d 1366, 1371 (Fed. Cir. 2007). The doctrine of prosecution history disclaimer ensures that “[a] patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement.” *Springs Window Fashions LP v. Novo Industries, L.P.*, 323 F.3d 989, 995–96 (Fed. Cir. 2003). Importantly, however, this doctrine does not apply when “the alleged disavowal is ambiguous” to one of ordinary skill in the art. *Omega Eng’g Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003). This can happen, for example, when the patentee makes a statement during prosecution that is clearly erroneous. *See Biotec*

Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc., 249 F.3d 1341, 1348 (Fed. Cir. 2001) (finding no estoppel when “a person of reasonable intelligence would not be misled into relying on the erroneous statement, for it [was] contrary not only to the plain language of the claims and the specification, but also to other statements in the same prosecution document.”).

The patentee’s claim that the quoted passage from the Specification *define* the shapes of “substantially oblong active regions” was clearly erroneous. First, the quoted passage uses permissive rather than definitional language. *See, e.g.*, Ex. 1001, 7:18–21 (“in an embodiment” and “an NMOS active region *may be considered* to be substantially oblong if . . .”) (emphasis added). Second, the quoted passage only describes the shapes of NMOS active regions. Elsewhere, the Specification discloses that PMOS active regions may be substantially oblong if they are “substantially rectangular,” i.e., if they “have a length that is substantially constant across the width . . . [and] a width that is substantially constant across the length.” *Compare id.* at 6:65–7:4, *with id.* at 7:20–34. Third, rather than limiting the plain and ordinary meaning of “substantially oblong,” the quoted passage describes NMOS active regions that can be considered “substantially oblong” even though they are non-rectangular. *See id.* at 7:4–6 (“an NMOS active region . . . may have some variation in width”), 7:20–24 (“an NMOS active region *may be considered to be* substantially oblong . . . if the width of the region varies by approximately 1/3 or less along the length”) (emphasis added), 7:24–28 (“an NMOS active region *may be considered* substantially oblong . . . if the width of the region by design varies only with the respective widths of the access and latch transistors”) (emphasis added), 7:28–30 (disclosing “‘substantially oblong’ may refer to any structure

having a length that is greater than or equal to . . . three times its *maximum* width,” implying a variable width having a maximum) (emphasis added).

For the reasons discussed above, we find a person of ordinary skill in the art would have known the quoted passage of the Specification does not *define* the shape of substantially oblong active regions. Therefore, the patentee’s prosecution history statement to that effect did not disavow the plain and ordinary meaning of that term, which includes substantially rectangular active regions. *See Biotec*, 249 F.3d at 1348. Instead, because the quoted passage describes active regions that can be considered “substantially oblong” even though they are not rectangular and the patentee argued that Kim’s L-shaped active regions *could not* be considered “substantially oblong,” the patentee’s statement was a disavowal of non-rectangular active regions that do not have one of the shapes described at column 7, lines 20–34 of the Specification.

For the reasons discussed above, we construe a “substantially oblong active region” to mean “(1) a substantially rectangular active region or (2) a non-rectangular active region that has (a) a substantially constant length and a width that varies by approximately 1/3 or less along its length, (b) a substantially constant length and a width that varies only by the widths of the access and latch transistors, or (c) a length that is greater than or equal to approximately three times its maximum width.”

b) Polysilicon Structure

The Specification provides the following non-limiting example of a substantially oblong polysilicon structure:

A polysilicon structure *may* be considered to be substantially oblong if the length of the polysilicon structure is greater than about three times the width of the polysilicon structure. Furthermore, a polysilicon structure *may* be considered to be substantially oblong despite having a substantially wider region if the wider region solely accommodates a contact region.

Ex. 1001, 11:4–10 (emphases added). During prosecution, to distinguish pending claim 1 over Kim, the patentee argued this passage “*defines* what is meant by oblong polysilicon structures.” Ex. 1006, 59–60 (quoting Ex. 1001, 11:4–10)¹⁰ (emphasis added). The patentee then argued that Kim’s polysilicon structures were not substantially oblong because they “form the characteristic L-shaped region which is contrary to the defined oblong characteristic shape, and the ‘boot’ of the L-shape is not used ‘solely to accommodate a contact’ as in the presently claimed polysilicon structures.” *Id.* at 60.

In our Institution Decision, we preliminarily found the patentee had disavowed “substantially oblong polysilicon structures” that did not have one of the shapes described in column 11, lines 4–10 of the Specification by claiming that that passage *defined* “substantially oblong polysilicon structures.” *See* Dec. Inst. 20. Petitioner disagrees, and contends that because the patentee’s arguments were focused on whether Kim’s L-shaped polysilicon structures could be considered substantially oblong, the patentee did not clearly and unmistakably disavow rectangularly shaped polysilicon structures. *See* Pet. Reply 6 (citing *Ecolab*, 569 F.3d at 1342).

¹⁰ Corresponding to page 18, lines 5–9 of the application.

The patentee's claim that the quoted passage from the Specification *defines* the shapes of "substantially oblong polysilicon structures" was clearly erroneous. First, the quoted passage uses permissive rather than definitional language. *See, e.g.*, Ex. 1001, 11:4–5 ("A polysilicon structure *may be considered* to be substantially oblong if . . .") (emphasis added). Second, rather than limiting the plain and ordinary meaning of "substantially oblong," the quoted passage describes polysilicon structures that can be considered "substantially oblong" even though they are not rectangular. *See id.* at 11:1–2 ("a portion of polysilicon structure 26 . . . may be wider than the remainder of polysilicon structure 26").

For the reasons discussed above, we find a person of ordinary skill in the art would have understood the quoted passage of the Specification does not *define* the shape of substantially oblong polysilicon structures. Therefore, the patentee's prosecution history statement to that effect did not disavow the plain and ordinary meaning of that term, which includes substantially rectangular polysilicon structures. *See Biotec*, 249 F.3d at 1348. Instead, because the quoted passage describes how non-rectangular polysilicon structures can still be considered "substantially oblong" and the patentee argued that Kim's L-shaped polysilicon structures could not be considered "substantially oblong," the patentee's statement was a disavowal of non-rectangular polysilicon structures that do not have one of the shapes described at column 11, lines 4–10 of the Specification.

For the reasons discussed above, we construe a "substantially oblong polysilicon structure" to mean "(1) a substantially rectangular polysilicon structure or (2) a non-rectangular polysilicon structure having a wider region that solely accommodates a contact region."

c) Local Interconnect

Petitioner argues a “substantially oblong local interconnect” is one that is rectangular or that otherwise meets “the non-limiting specification passages describing exemplary dimensional and functional criteria under which a structure is substantially oblong.” Pet. 13. In our Institution Decision, we construed this term to mean an interconnect “having a substantially rectangular shape” because the Specification describes local interconnects having a “substantially rectangular” shape. *See* Dec. Inst. 21–22 (citing Ex. 1001, 12:9–12).

We maintain our preliminary construction of a substantially oblong local interconnect, and note that the Specification distinguishes between the “substantially rectangular” interconnects shown in Figure 3, which “require connection to the structures of the previous layers in only two areas,” and prior art “multi-limbed, non-oblong interconnect structures” that require “three connections to the structures of previous layers.” Ex. 1001, 12:8–14.

2. A Single Local Interconnect Layer Comprising Local Interconnects Corresponding to Bitlines and a Global Wordline

Patent Owner argues “[t]his limitation means ‘one local interconnect layer that includes short connections that route bitline signals and a global wordline signal along that same layer.’” PO Resp. 15. Patent Owner argues its proposed construction is supported by the Specification, which discloses that the term local interconnect “may refer to the function of connecting features within a circuit” and “local interconnects provide ‘short runs relative to much longer metal conductors used for global connections.’” *Id.* (quoting Ex. 1001, 11:18–23). Patent Owner argues Figure 3 illustrates a local interconnect layer having interconnects 38/39 that route bitline signals horizontally along the local interconnect layer and interconnects 43/44 that

route a global wordline signal vertically. *Id.* at 15–16. Patent Owner further argues that a person of ordinary skill in the art “would have understood that in the context of a ‘single local interconnect layer’ connecting two features on the single layer would refer to routing a signal along the layer.” *Id.* (citing Ex. 2015 ¶ 92). Patent Owner also argues that its construction is supported by the prosecution history because the patentee added the single local interconnect layer limitation to distinguish claim 8 from Osada,¹¹ the examiner recognized the distinction, and “[i]t would violate the rules of claim construction for the Board to adopt a construction of this claim language that does not distinguish claim 8 from Osada.” *Id.* at 16–17.

Petitioner argues the single local interconnect layer limitation means “one local interconnect layer that includes local interconnects corresponding to bitlines and local interconnects corresponding to a global wordline.” Pet. Reply 7. Petitioner argues neither the claim language nor the Specification support Patent Owner’s proposed construction because neither uses the word “routing.” *Id.* at 8. Petitioner further argues Figure 3 does not “illustrate any routing along the local interconnect layer” because the ’805 patent does not “illustrate any contacts atop the local interconnect layer, let alone specific positions that would demonstrate routing.” *Id.* (citing Ex. 1001, Fig. 3).

The claims of a patent “must be read in view of the specification, of which they are a part.” *Markman v. Westview Inst., Inc.*, 52 F. 3d 967, 979 (Fed. Cir. 1995). Indeed, “the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic*,

¹¹ US 6,677,649 B2 issued to Osada et al. (Ex. 1009).

Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). The Specification discloses that local interconnects are short conductors that “connect[] features within a circuit” rather than “much longer metal conductors used for global connections.” Ex. 1001, 11:18–21. The Specification describes a local interconnect layer as a deposited layer of conducting material that is “patterned and etched” and “a distinct process layer that *exclusively* performs . . . short [inter] connections.” *Id.* at 11:22–23, 12:39–49 (emphasis added). Thus, a polysilicon layer that “provide[s] local interconnect” functions and also “provid[es] transistor gate[]” functions is not a local interconnect layer because it does not *exclusively* perform the interconnect function. *Id.* at 11:23–27. Likewise, a dielectric layer containing vias connecting structures in layers above and below it is not a local interconnect layer because it is not a deposited layer of conducting material. *Id.* at 8:52–64, 13:19–22 (disclosing forming “contacts” rather than “interconnects” in a deposited dielectric material layer). Given these disclosures, we construe a “single local interconnect layer” to mean “one conductive layer containing non-global interconnects, including interconnects for bitlines and a global wordline, that exclusively performs the function of connecting features within a circuit.”

We disagree with Patent Owner’s contention that the Specification or prosecution history require a different construction. Although the Specification discloses an interconnect layer, a first metal layer containing bitlines, and a second metal layer containing a wordline, it does not disclose how the bitlines and wordline are laid out with respect to the interconnects in the interconnect layer. *Id.* at 13:19–32. Thus, although Figure 3 shows bitline signals *can* be routed horizontally and a global wordline signal *can* be routed vertically, neither the Specification nor claims require such routing.

Indeed, the Specification expressly discloses that the embodiments shown in the Figures are “by way of example” only, and that the claimed invention is “susceptible to various modifications and alternative forms” and not limited to the embodiments shown. *Id.* at 5:1–10.

Moreover, the prosecution history, like the Specification, does not limit the single local interconnect layer limitation in the manner Patent Owner contends. During prosecution, claim 8 was amended to recite “a local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline” in order to overcome a pending rejection. Ex. 1007, 488 (emphasis omitted). The patentee argued amended claim 8 was patentable over Osada because it recited “the *single* [interconnect] layer of Fig. 3,” which has “all the runs for the bitlines, V_{CC} , V_{SS} and the wordline,” whereas Osada has “*multiple* layers for its runs.” *Id.* at 502. The Examiner suggested the patentee further amend claim 8 to recite a *single* local interconnect layer, and allowed claim 8 when the patentee did so. *Id.* at 1039, 1057–58.

In our view, the Examiner erred in finding claim 8’s recitation of a *single* local interconnect layer distinguished that claim over Osada. Like the ’805 patent, Osada discloses an SRAM having three metal layers: a first metal layer containing interconnects, a second metal layer containing a wordline (or bitlines), and a third metal layer containing bitlines (or a wordline). It is the first metal layer in both the ’805 patent and Osada that is the *single* local interconnect layer because that layer is the only deposited conductive layer that *exclusively* performs the interconnect function.

As discussed in § II.A, *supra*, the SRAM cell disclosed in the ’805 patent contains transistors in a silicon substrate, gates in a polysilicon layer, interconnects in a local interconnect layer, bitlines in a first metal layer, and

a wordline in a second metal layer. Ex. 1001, 6:17–19, 10:30–43, 11:50–51, 13:19–30. The '805 patent identifies the local interconnect layer as the first conducting layer deposited over the polysilicon layer and states that it *may* be made of polysilicon. *Id.* at 11:50–54, 12:42–45, Figs. 2–3. The '805 patent identifies the first metal layer as “the first conductive layer above the local interconnect layer,” but recognizes this “*may be a misnomer* in those cases where the local interconnect layer utilizes a metal” instead of polysilicon. *Id.* at 10:40–43, 12:40–42. Thus, the '805 patent’s “single local interconnect layer” can be a first metal layer, its “first metal layer” containing bit lines can be a misnamed second metal layer, and its “second metal layer” containing a word line can be a misnamed third metal layer.

Osada discloses an SRAM cell having a similar structure. Figure 4 of Osada is reproduced below.

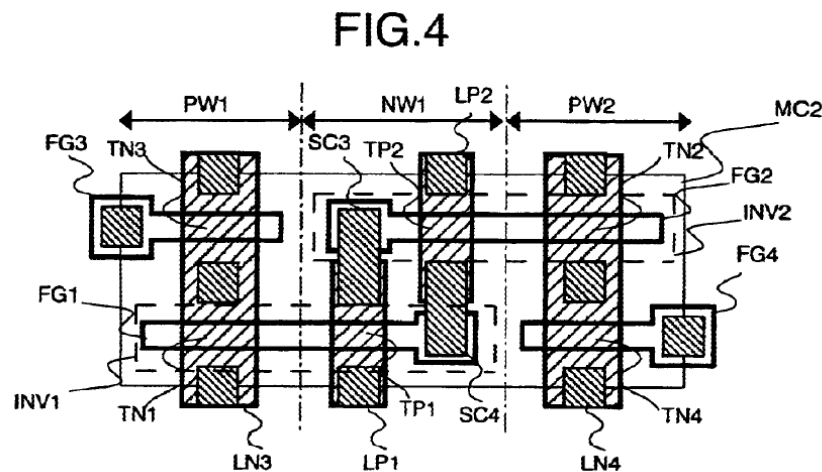


Figure 4 illustrates “an SRAM cell in accordance with Embodiment 3” of Osada. Ex. 1009, 4:10–11. The symbols in Figure 4 “are the same as those in FIG. 2.” *Id.* at 7:22–25. They include transistors TN1–TN4 and TP1–TP2 formed in a semiconductor substrate and polysilicon gates FG1–FG4

formed in a polysilicon layer. *Id.* at 5:27–45, 5:61–6:7. The remaining layers of Osada are shown in Figure 5, which is reproduced below.

FIG.5

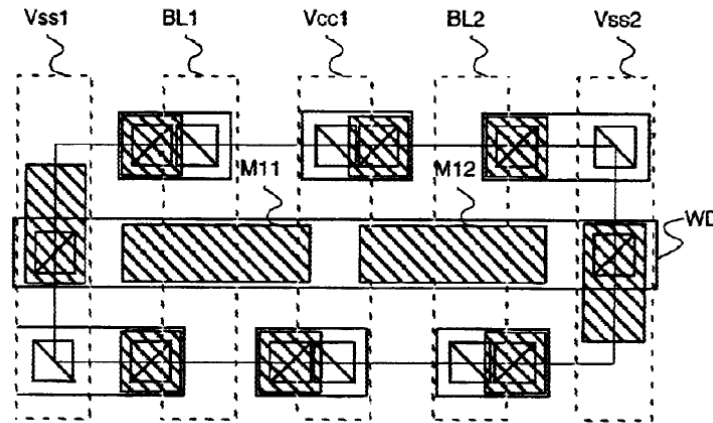


Figure 5 of Osada “is a diagram showing a layout of via holes of SRAM cells for connection between multilayered metal leads in accordance with Embodiment 3.” *Id.* at 4:15–17. As before, the symbols used in Figure 5 “are the same as those in FIG. 2.” *Id.* at 7:21–23. Figure 5 discloses (a) a first metal layer containing interconnects having a solid outline and hashed fill (M11/M12, the six interconnects above/below them, and the two interconnects to their left/right), (b) a second metal layer containing structures having a solid outline and no fill (wordline WD and the six interconnects above/below it), and (c) a third metal layer containing structures having a dashed outline and no fill (bitlines BL1/BL2, power line (V_{CC1}), and ground lines (V_{SS1}/V_{SS2})). *Id.* at 5:65–67, 6:8–20, 7:58–61.

Notably, Osada’s first metal layer contains only interconnects. It is, therefore, equivalent to the ’805 patent’s local interconnect layer because it is the first conductive layer deposited over the polysilicon layer that *exclusively* performs the interconnect function. See Ex. 1001, 11:18–23. Osada’s second metal layer is equivalent to the ’805 patent’s first metal

layer because it is “the first conductive layer above the local interconnect layer.” *Id.* at 10:40–43.¹² It is not a local interconnect layer because it contains wordline WD and, therefore, does not exclusively perform the interconnect function. Lastly, Osada’s third metal layer is equivalent to the ’805 patent’s second metal layer and is not a local interconnect layer because it contains bitlines BL1/BL2, i.e., it does not exclusively perform the interconnect function.¹³ Accordingly, for these reasons, we find the Examiner erred in finding Osada lacked a “single local interconnect layer” and that claim 8 distinguished over Osada for that reason.

E. Obviousness Over Oh

Petitioner argues claims 8–14, 16–20, 22–25, 27, 28 and 30–32 are unpatentable as obvious over Oh. Pet. 16–70. Patent Owner disagrees. PO Resp. 21–39. For the reasons discussed below, we find Qualcomm has demonstrated by a preponderance of evidence that claims 8–14, 16–20, 22–25, 27, 28, and 30–32 are unpatentable over Oh, and AMD and STM have demonstrated by a preponderance of evidence that claims 9, 11, 13, 14, 17, 19, 20, 24, 25, 27, 28, and 30–32 are unpatentable over Oh.

1. Oh

Oh discloses “a static random access memory device (SRAM) which can be manufactured by a CMOS^[14] standard logic manufacturing process and a method for manufacturing the same.” Ex. 1004, 1:7–12. “The SRAM

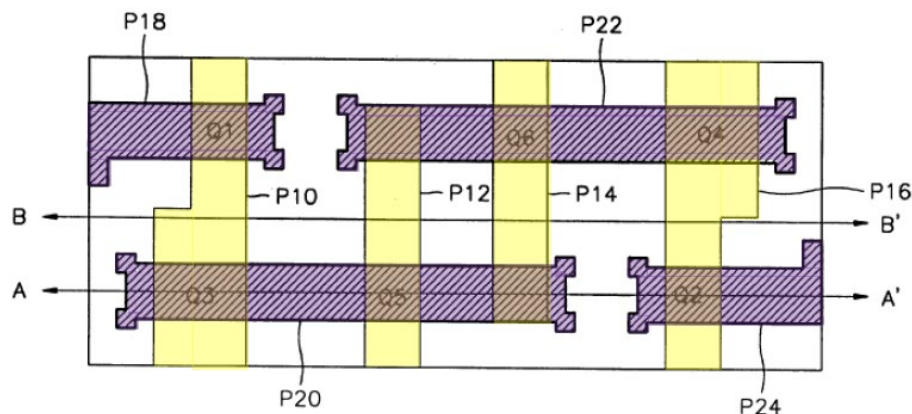
¹² Recall that the ’805 patent discloses its “first metal layer” may be a misnamed second metal layer “when the local interconnect layer utilizes a metal,” as it does in Osada. Ex. 1001, 10:40–43.

¹³ Because the ’805 patent’s “first metal layer” is a misnamed second metal layer in embodiments such as Osada’s, the ’805 patent’s “second metal layer” is a misnamed third metal layer. *See* n.9, *supra*.

¹⁴ Complementary Metal-Oxide-Semiconductor.

device comprises a semiconductor substrate in which parallel first and second active regions of a first conductive type are arranged and third and fourth active regions of a second conductive type are arranged between the first and second active regions.” *Id.* at 3:42–47.

Figures 3–9 of Oh are “layouts of the exemplary mask patterns used for manufacturing [the] SRAM device,” while Figures 10 and 11 show “the SRAM device . . . manufactured using the mask patterns of FIGS. 3 through 9.” *Id.* at 8:9–10, 12:21–24. A Petitioner-colored version of Figure 3 of Oh is reproduced below. Pet. 16.



The figure is a Petitioner-colored version of Figure 3 of Oh illustrating “the layout of mask patterns for use in forming active regions and gates” of Oh’s SRAM cell. Ex. 1004, 8:45–47. Outer masks P10/P16 (yellow) are used to form first/second active regions and inner masks P12/P14 (yellow) are used to form third/fourth active regions. *Id.* at 8:47–53. The first through fourth active regions have the same “shapes and arrangements” as masks P10–P16. *Id.* at 12:30–36, 14:49–51. The first/second active regions P10/P16 “form[] NMOS transistors . . . parallel to each other in a bar shape” and the third/fourth active regions P12/P14 “form[] PMOS transistors . . . parallel to each other between the first and second active regions P10 and

P16.” *Id.* at 8:62–67. NMOS transistors Q1 and Q3 “are formed in the first active region,” NMOS transistors Q2 and Q4 “are formed in the second active region,” and PMOS transistors Q5/Q6 are formed in the third/fourth active regions, respectively. *Id.* at 12:37–53.

Masks P18/P24 (purple) are used to form the gates of the first/second access transistors Q1/Q2, and masks P20/P22 (purple) are used to form the gates of the first/second drive transistors Q3/Q4 and the first/second load transistors Q5/Q6. *Id.* at 8:53–61. “The gate P20 . . . [is] arranged perpendicular to the first active region P10, and . . . to the third active region P12,” and the “gate P22 . . . [is] arranged perpendicular to the second active region P16, and . . . to the fourth active region P14.” *Id.* at 9:4–12.

Oh’s SRAM device includes “a first metal layer . . . , a second metal layer which forms the word line, and a third metal layer which forms bit lines.” *Id.* at 3:29–32. Figure 5 of Oh, reproduced below, illustrates the masks used to form structures in the first metal layer.

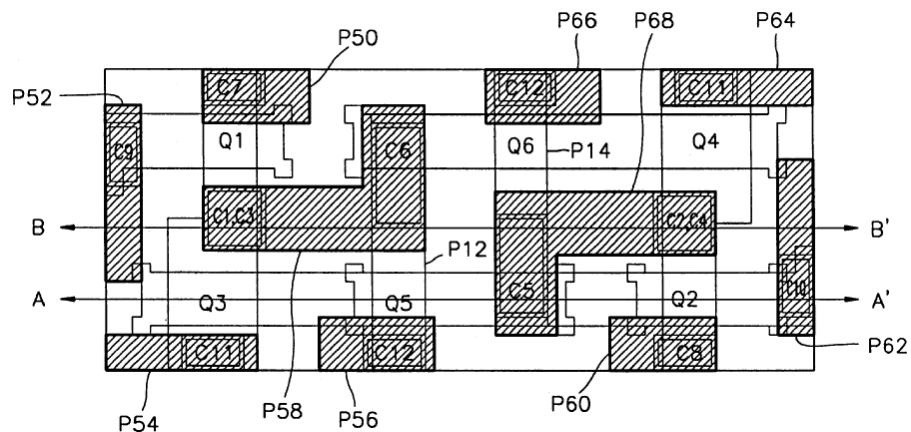


Figure 5 of Oh is a “layout of mask patterns for forming a first connection line, a second connection line and a plurality of first pad layers.” *Id.* at 10:7–9. Mask P50 “form[s] a first pad layer C7” that connects to the source of transistor Q1, mask P60 “form[s] a first pad layer C8” that

connects to the source of transistor Q2, mask P52 “form[s] a first pad layer C9” that connects to the gate of transistor Q1, and mask P62 “form[s] a first pad layer C10” that connects to the gate of transistor Q2. *Id.* at 10:9–15, 10:28–34. The sources of transistors Q1/Q2 connect through first pads C7/C8 to bitlines in the third metal layer via second pads C7/C8 formed in the second metal layer and vias C7/C8 formed in the two dielectric layers separating the three metal layers. *Id.* at 11:4–6, 11:13–15, 11:25–28, 11:35–38, 11:52–54, 11:60–62, 12:6–9, 12:14–17, Figs. 6–9. The gates of transistors Q1/Q2 connect through first pads C9/C10 to a wordline in the second metal layer through vias C9/C10 formed in the dielectric layer separating the first and second metal layers. *Id.* at 11:6–8, 11:15–17, 11:45–48, Figs. 6–7.

2. Claim 8

a) memory cell

Claim 8 recites a memory cell. Ex. 1001, Reexam. Cert. 1:25.

Petitioner argues that Oh teaches or suggests this limitation. *See* Pet. 19 (citing Ex. 1004, 1:6–13, 3:3–4:10, Figs. 3–25). Patent Owner disagrees, arguing that Oh instead is directed to “improvements to photolithography masks used to manufacture memory” cells. PO Resp. 9 (emphasis omitted).

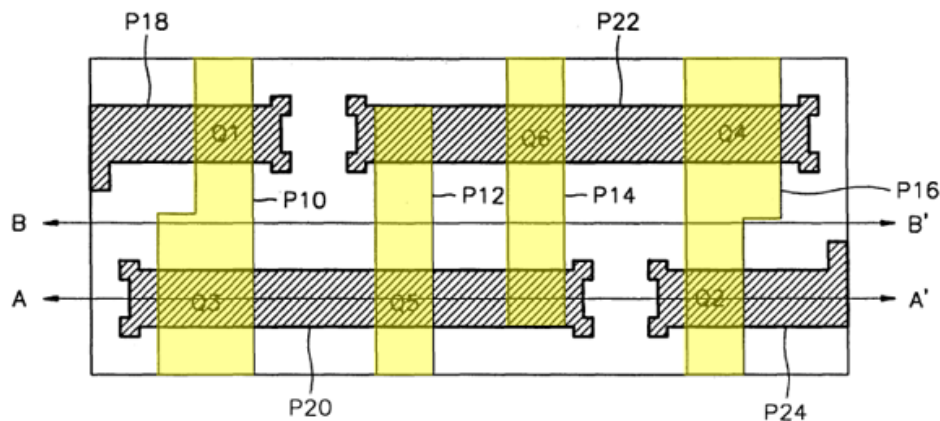
We agree with Petitioner that Oh teaches or suggests a memory cell. Oh discloses “a static random access memory (SRAM) device which can be manufactured by standard CMOS logic manufacturing processes.”

Ex. 1004, 3:3–5. Figures 3 through 9 of Oh are “exemplary mask patterns used for manufacturing [the] SRAM device.” *Id.* at 8:9–11. Figures 10 through 25 are cross-sectional views of Oh’s SRAM device made using the photolithographic masks shown in Figures 3 through 9. *Id.* at 8:15–27.

b) substantially oblong active regions

Claim 8 further requires the memory cell to include a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another. Ex. 1001, Reexam. Cert. 1:25–27.

Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. See Pet. 19–21. Petitioner illustrates Oh’s teachings with a colorized version of Figure 3 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Oh’s Figure 3 showing the mask patterns (yellow) used to make four active regions in a semiconductor substrate. Pet. 20. Petitioner demonstrates how Oh teaches the active regions formed by masks P10–P16 are substantially oblong and parallel based on Figure 3 and the express teachings of Oh. *Id.* at 20–21(citing Ex. 1004, 3:40–47, 4:11–21, 7:9–15, 8:62–67, 12:66–13:6, Fig. 3).

Oh teaches “the first and second active regions P10 and P16 . . . are arranged parallel to each other *in a bar shape*, and the third and fourth active regions P12 and P14 . . . are also arranged parallel to each other.” Ex. 1004, 8:62–67 (emphasis added). Oh also teaches “*the shapes and arrangements*

of the first through fourth active regions are the same as shown in mask patterns P10, P12, P14, and P16 in FIG. 3.” *Id.* at 14:49–51 (emphasis added). Thus, Oh’s third and fourth (i.e., inner) active regions have the same shapes as masks P12 and P14, i.e., they have “a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region,” as Petitioner contends, which is one way the ’805 patent describes “substantially oblong” inner active regions. *See* Pet. 20–21 (quoting Ex. 1001, 6:65–7:4).

Oh describes the first/second outer active regions as having the same shapes as masks P10/P16, i.e., “the first [second] active region can have a wider width at regions overlapped by the gate of the first [second] drive transistor than at regions overlapped by the gate of the first [second] access transistor.” Ex. 1004, 4:11–21, 7:9–15, 14:49–51. As Petitioner correctly contends, the ’805 patent describes outer active regions as “substantially oblong” if “the length of the region is substantially constant and the width of the region . . . varies only with the respective widths of the access and latch transistors.” *See* Pet. 21 (quoting Ex. 1001, 7:24–28)

We note that claim 8 only requires a plurality of substantially oblong active regions. *See* Reexam. Cert. 1:25–26. Thus, Petitioner demonstrates this limitation is met by demonstrating active regions P10 and P16 are substantially oblong, active regions P12 and P14 are substantially oblong, or all of these regions are substantially oblong. Petitioner demonstrates that all of active regions P10–P16 are substantially oblong.

Patent Owner makes numerous arguments that Petitioner has failed to show Oh’s active regions are substantially oblong. *See* PO Resp. 21–34; PO Sur-Reply 13–20. First, Patent Owner argues that Petitioner improperly relies on the visual appearance of Oh’s drawings because (a) Oh warns that

its drawings are not to scale, (b) Oh's specification contradicts the shapes shown in Figure 3, (c) Dr. Lee admitted that Oh did not specify the dimensions of its structures and those dimensions cannot be determined by reading Oh, and (d) patent drawings cannot be relied on to demonstrate sizes or proportions. PO Resp. 22–27 (citing/quoting Ex. 1004, 8:2–4, 8:38–40, 9:22–29; Ex. 2016, 85:10–86:10; *Nystrom v. Trex Co., Inc.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005)). Patent Owner further argues that because “the mask patterns illustrated in Oh's drawings are different—and, indeed, must be different—from the patterns of the structures formed by those masks,” Petitioner's “reliance on Oh's drawings fails to meet the ‘substantially oblong’ limitations.” PO Resp. 29, 32(emphasis omitted). We disagree with each of these arguments for the reasons that follow.

Figures 3 through 9 of Oh disclose “mask patterns used for manufacturing an SRAM” and Figures 10 and 11 disclose cross-sectional views of “the SRAM . . . manufactured using the mask patterns of FIGS. 3 through 9.” Ex. 1004, 8:9–18. Although Oh discloses that these Figures “are *not necessarily* drawn to scale,” Oh does not disclose that they are *not* drawn to scale. *Id.* at 8:2–4 (emphasis added). Moreover, Oh expressly discloses that the active regions in its SRAM device have the same shapes as the masks shown in Figure 3, and expressly describes the active regions as being bar-shaped. *Id.* at 12:30–36 (disclosing the first through fourth active regions of Oh's SRAM device correspond to masks P10–P16), 14:49–51 (disclosing “[t]he *shapes and arrangements* of the first through fourth active regions *are the same* as shown in the mask patterns P10, P12, P14, and P16 in FIG. 3”), 8:62–64 (disclosing “active regions P10 and P16 . . . are . . . in a bar shape”) (emphases added). Thus, regardless of whether Oh's figures are drawn to scale or whether the shapes of structures differ somewhat from the

shapes of the masks used to form them, Oh expressly discloses that the active regions formed in its SRAM device have the same substantially oblong shape as the shape of the masks shown in Figure 3.

Patent Owner relies on Oh's column 9 description of the shapes of masks/active regions P10/P16 to support its argument that Oh describes these shapes differently than the shapes shown in Figure 3. *See* PO Resp. 23 (citing Ex. 1004, 9:22–29). Oh's column 9 description, however, is inconsistent not only with the shapes shown in Figure 3, but with every other description of the shapes of masks/active regions P10/P16, all of which describe them as having shapes that are consistent with Figure 3. *Compare* Ex. 1004, 9:22–29, *with id.* at 4:11–21, 7:9–15, 12:66–13:6, 20:59–65, 23:30–36, Fig. 3. Consequently, we agree with Petitioner that Oh's column 9 description is simply a typographical error. *See* Pet. Reply 16–17.

Patent Owner relies on cases like *Nystrom* and *Hockerson-Halberstadt* for the proposition that Petitioner cannot rely on Oh's unscaled drawings to show the shape of masks/active regions P10–P16. But these cases stand for a different proposition—that unscaled drawings cannot be relied on to show the *precise sizes or dimensions* of objects when the specification is silent on the issue. *See Nystrom*, 424 F.3d at 1148–49 (finding drawings could not be relied on to show deck board features in a precisely claimed 1:40 ratio because “patent drawings cannot be the basis for challenging the validity of claims reciting *specific dimensions* not disclosed directly in such prior art”) (emphasis added); *see also Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 953, 956 (affirming a claim construction disavowing a wide shoe heel groove despite drawings showing a wide groove because “patent drawings do not define the *precise proportions* of the elements and may not be relied on to show *particular sizes* if the specification is

completely silent on the issue”) (emphases added); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977) (finding drawings could not be used to demonstrate a whiskey barrel chime “approximately 5/8 in length” because “[a]bsent any written description in the specification of *quantitative* values, arguments based on *measurement of a drawing* are of little value”) (emphases added).

But Petitioner does not rely on Figure 3 to demonstrate the precise dimensions of Oh’s active regions. Instead, Petitioner relies on Figure 3 to show the active regions have a “substantially oblong” shape. *See* Pet. 19–21 (citing Ex. 1004, Fig. 3). Moreover, Oh is not completely silent on the shapes of the active regions shown in Figure 3. Oh discloses “the first and second active regions P10 and P16 . . . [are] in a bar shape.” Ex. 1004, 8:62–64. Oh also discloses the first through fourth active regions have “shapes and arrangements . . . [that] are the same as shown in the mask patterns P10, P12, P14 and P16 in FIG. 3.” *Id.* at 14:49–51. Thus, if the first and second active regions P10 and P16 have a “bar shape,” the third and fourth active regions P12 and P16 also have a “bar shape.” Moreover, the actual dimensions of Oh’s active regions are immaterial to whether they are substantially oblong. Per the ’805 patent, an inner active region (e.g., Oh’s P12/P14) is substantially oblong if it has “a length that is substantially constant across the width of the region, as well as a width that is substantially constant along the length of the region” and an outer active region (e.g., Oh’s P10/P16) is substantially oblong “if the length of the region is substantially constant and the width of the region . . . varies only with the respective widths of the access and latch transistors.” Ex. 1001, 6:65–7:4, 7:24–28. Neither of these descriptions requires precise knowledge of any particular length, width, or length-to-width ratio.

Dr. Lee’s admissions regarding the inability to determine lengths, distances between, or shapes of the structures shown in Oh’s drawings do not detract from our finding that Petitioner has demonstrated that Oh’s active regions are “substantially oblong.” As discussed above, Oh expressly discloses that the active regions of its SRAM device have the shapes of the mask patterns P10–P16 shown in Figure 3. *See* Ex. 1004, 14:49–51. As also discussed above, the shapes shown in Figure 3 of Oh match express descriptions of substantially oblong active regions in the ’805 patent that do not rely on the active regions having any particular lengths, widths, or length-to-width ratios. *See* Ex. 1001, 6:65–7:4, 7:24–28.

For the reasons discussed above, we find Petitioner has demonstrated that Oh discloses a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially parallel with one another as recited in claim 8.

c) substantially oblong local interconnects

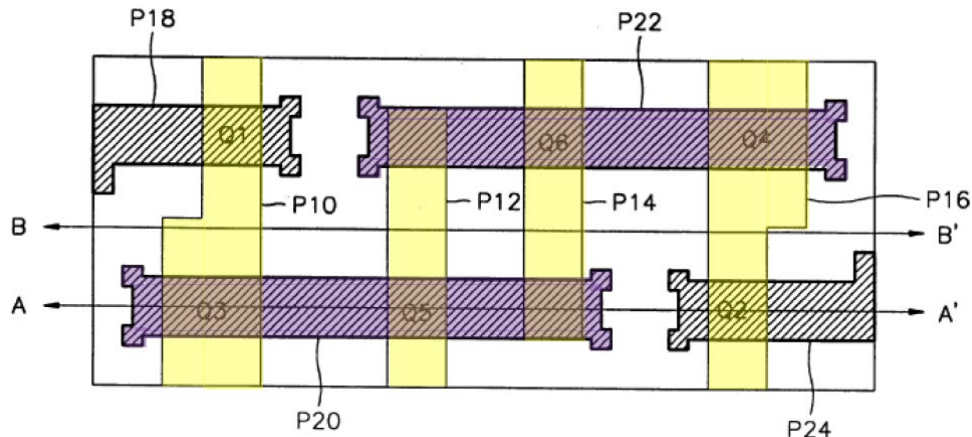
Claim 8 requires a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions (“the local interconnect” limitation). Ex. 1001, Reexam. Cert. 1:25–27.

Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. *See* Pet. 21–30. Specifically, Petitioner demonstrates how gates P20/P22 in Oh’s

polysilicon layer and interconnects P50/P60, P54/P64, P56/P66, and P58/P68 in Oh's first metal layer meet the limitation.¹⁵ *Id.*

(1) *Oh's Polysilicon Gates*

The Petitioner includes a colored version of Figure 3 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Figure 3 of Oh showing masks patterns P20/P22 (purple) used to make the gates of transistors Q3–Q6 in a semiconductor substrate. Pet. 22. Petitioner demonstrates how these gates meet the local interconnect limitation. *Id.* at 21–24 (citing Ex. 1004, 8:53–61, 9:4–21, 9:30–63, 12:54–65, Figs. 3, 10; Ex. 1019 ¶¶ 71, 72, 77, 91–93, 114–116).

Oh teaches forming gate oxide 56 over semiconductor substrate 50, and depositing a first conductive layer over gate oxide 56 to form gates for the transistors in the semiconductor substrate. Ex. 1004, 14:55–58, Fig. 10. Oh teaches mask P20 forms a common interconnected gate for transistors

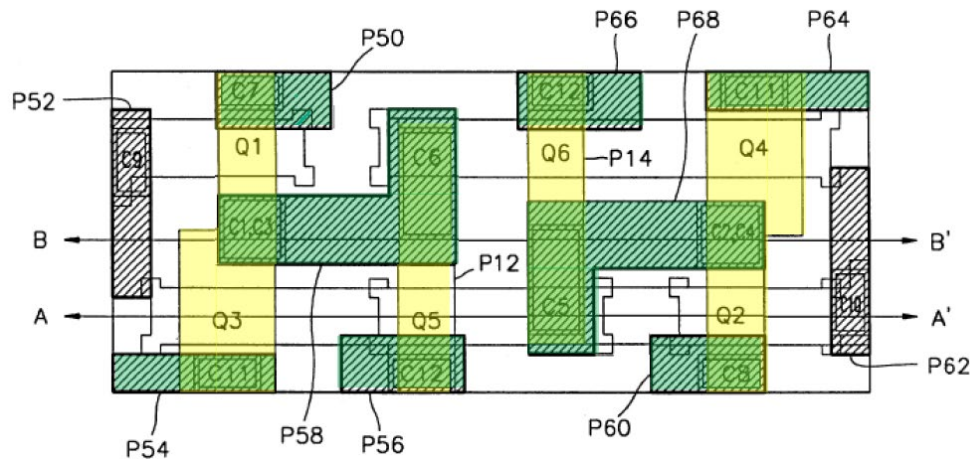
¹⁵ We note that claim 8 only requires a plurality of substantially oblong local interconnects. See Ex. 1001, Reexam. Cert. 1:27–32. Thus, Petitioner can show how this limitation is met by showing that any of gates P20/P22 or interconnects P50/P60, P54/P64, P56/P66, or P58/P68 meet this limitation.

Q3/Q5 and mask P22 forms a common interconnected gate for transistors Q4/Q6. *Id.* at 9:4–12, 14:64–15:1. Thus, gates P20/P22 are local interconnects formed above the substrate because the '805 patent identifies any structure “configured such that multiple gates are connected” as “a local interconnect.” Ex. 1001, 11:26–29. Moreover, because gates P20/P22 have a rectangular shape as shown in Figure 3, they are substantially oblong. *See* Ex. 1004, 15:3–5 (referencing Figure 3 for “understanding about the shape and arrangement of the gates”); *see* § II.D.1.b (construing substantially oblong polysilicon structures as substantially rectangular); *see also* Ex. 1001, 12:8–14 (describing “substantially rectangular” interconnects as improvements over “non-oblong” interconnects).

Oh teaches gate P20 “crosses the first, third and fourth active regions” but not the second, and gate P22 “crosses the second, fourth and third active regions” but not the first. Ex. 1004, 12:56–58, 12:60–62, 14:54–15:1, Figs. 3, 10. Thus, gates P20/P22 extend partially across the memory cell. Oh teaches gate P20 is perpendicular to “first active region P10” and “third active region P12,” and gate P22 is perpendicular to “second active region P16” and “fourth active region P14.” *Id.* at 9:4–12, Fig. 3. Thus, gates P20/P22 are substantially perpendicular to the active regions. Oh teaches that gate P20 is located on a “line parallel to . . . gate P22.” *Id.* at 9:17–20, Fig. 3. Thus, gates P20/P22 are substantially parallel to one another.

(2) *Oh’s Connection Lines and Landing Pads*

The Petition includes two colorized versions of Figure 5 of Oh, which we have combined below. *See* Pet. 25, 28.



The figure is a combination of two Petitioner-colored versions of Figure 5 of Oh showing masks patterns P50/P60, P54/P64, P56/P66, and P58/P68 (green) used to make interconnects in Oh's first metal layer. *Id.* Petitioner demonstrates how these interconnects meet the local interconnect limitation. *Id.* at 24–30 (citing Ex. 1004, 3:29–33, 4:66–5:34, 10:7–12:21, 13:7–41, 14:34–54, 16:24–67, Figs. 3–5, 10–25; Ex. 1019 ¶¶ 72, 73, 75, 77, 96, 98, 119–122).

Oh's SRAM device includes "a first metal layer which forms the first and second connection lines, a second metal layer which forms the word line, and a third metal layer which forms bit lines." Ex. 1004, 3:29–33. Figure 5 of Oh illustrates Oh's first metal layer because it has masks "for forming a first connection line, a second connection line and a plurality of first pad layers." *Id.* at 10:7–9. Figure 7 of Oh illustrates Oh's second metal layer because it has masks "for forming a word line and a plurality of second pad layers." *Id.* at 11:23–24. Figure 9 of Oh illustrates Oh's third metal layer because it has masks "for forming power supply lines and bit lines." *Id.* at 12:1–2. All of the structures in Oh's first metal layer are above the substrate because the first metal layer is deposited over a dielectric layer, which is deposited over a gate layer, which is deposited over a gate oxide

layer, which is deposited over the substrate. *Id.* at 14:55–60, 15:26–30, 16:24–29.

Masks P50/P60 form first pads C7/C8 in the first metal layer that are connected to the sources of transistors Q1/Q2 by contacts C7/C8. *Id.* at 10:9–12, 10:28–31, 16:24–31, 16:45–48, Fig. 5. First pads C7/C8 are connected by first vias C7/C8 to second pads C7/C8 formed by masks P86/P92 in Oh's second metal layer. *Id.* at 11:25–28, 11:35–38, 17:40–43, 17:50–52, Fig. 7. Second pads C7/C8 are connected by second vias C7/C8 to bit lines 102/106 formed by masks P114/P118 in Oh's third metal layer. *Id.* at 12:6–9, 12:14–17, 18:32–35, 18:40–42, Fig. 9. Thus, first pads C7/C8 are interconnects formed above the substrate "corresponding to" bit lines 102/106. Moreover, as shown in Figure 5, first pads C7/C8 extend only partially across the memory cell, are substantially perpendicular to active regions P10–P16, are parallel to other local interconnects (P54/P64, P56/P66, P58/P68), and are "substantially oblong" because they are rectangular.

Masks P54/P64 form first pads C11 in the first metal layer that are connected to the sources of transistors Q3/Q4 via first contacts C11. *Id.* at 10:15–18, 10:34–37, 16:34–37, 16:52–56, Fig. 5. First pads C11 contact power supply lines V_{SS} (ground) formed by masks P112/P120 in Oh's third metal layer through first vias C11, second pads C11 in the second metal layer, and second vias C11. *Id.* at 11:8–11, 11:17–19, 11:31–35, 11:41–45, 11:62–67, 12:2–6, 12:17–21, 13:61–64, Figs. 6–9. Thus, first pads C11 (P54/P64) are local interconnects above the substrate "corresponding to" common ground V_{SS} . Moreover, as shown in Figure 5, they extend only partially across the memory cell, are substantially perpendicular to active regions P10–P16, are parallel to other local interconnects (P50/P60,

P56/P66, P58/P68), and are “substantially oblong” because they are rectangular.

Masks P56/P66 form first pads C12 in the first metal layer that are connected to the drains of transistors Q5/Q6 via contacts C12. *Id.* at 10:18–22, 10:37–41, 16:37–40, 16:56–60, Fig. 5. First pads C12 contact power supply line V_{CC} formed by mask P116 in the third metal layer through first vias C12, second pads C12 in the second metal layer, and second vias C12. *Id.* at 11:11–13, 11:20–22, 11:28–31, 11:38–41, 11:55–60, 12:9–14, 13:59–62, Figs. 6–9. Thus, first pads C12 (P56/P66) are local interconnects formed above the substrate “corresponding to” common power. Moreover, as shown in Figure 5, they extend only partially across the memory cell, are substantially perpendicular to active regions P10–P16, are parallel to other local interconnects (P50/P60, P54/P64, P58/P68), and are “substantially oblong” because they are rectangular.

Mask P58 forms first connection line 84 that connects common drain 62 of transistors Q1/Q3 via contact C1/C3 with the common gate of transistors Q4/Q6 and source 64 of transistor Q5 via contact C6. *Id.* at 10:22–28, 12:39–45, 16:40–45, Figs. 11, 21. Likewise, mask P68 forms second connection line 86 that connects common drain 68 of transistors Q2/Q4 via contact C2/C4 with the common gate of transistors Q3/Q5 and source 66 of transistor Q6 via contact C5. *Id.* at 10:41–47, 12:45–53, 16:61–67, Figs. 11, 21. Thus, first/second connection lines (P58/P68) in Oh’s first metal layer are local interconnects formed above the substrate. Moreover, as shown in Figure 5, they extend only partially across the memory cell, are substantially perpendicular to active regions P10–P16, are substantially parallel to other local interconnects (P50/P60, P54/P64, P56/P66), and are “substantially oblong” because they are substantially rectangular and

connect to only two structures in other layers (e.g., P58 connects contacts C1/C3 and C6, and P68 connects contacts C2/C4 and C5). *See* Ex. 1001, 12:8–14 (describing interconnects contacting structures in only two areas as improvements over “non-oblong” interconnects contacting structures in three areas).

(3) *Patent Owner’s Arguments*

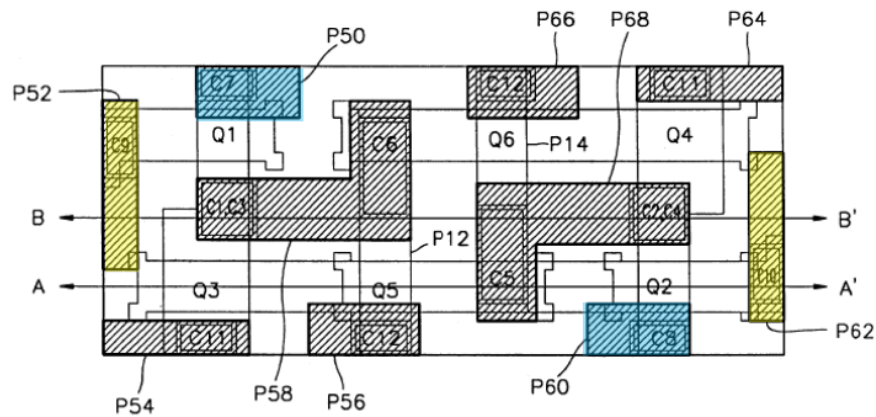
Patent Owner doesn’t dispute that the polysilicon gates in Oh’s gate layer or landing pads in Oh’s first metal layer are interconnects. *See* PO Resp. 34. Rather, Patent Owner argues that Oh’s gates P20/P22 and interconnects P58/P68 are not “substantially oblong” for the reasons discussed above with respect to Oh’s active regions. *Id.* That is, Patent Owner argues that Figures 3 and 5 of Oh depict masks rather than structures and masks have different shapes than the structures they are used to make. *Id.* at 29–32. Moreover, Patent Owner argues that even if Oh’s masks formed structures having the shapes shown in Figures 3 and 5, Petitioner cannot rely on those shapes because (1) Oh’s figures are not drawn to scale, (2) Oh does not disclose the dimensions of its structures, and (3) Petitioner cannot rely on unscaled drawings to show shapes. *Id.* at 21–29.

We disagree with Patent Owner’s contentions for the reasons discussed in § II.E.2.b, *supra*. We further note that Oh refers to P20/P22 as both the mask patterns for gates and the gates themselves. *Compare* Ex. 1004, 8:55–57 (“reference symbol P20 represents the mask pattern for forming the gate of the first drive transistor Q3”), *with id.* at 9:4–5 (“The gate P20 of the first drive transistor Q3 . . .”). In describing the SRAM cell shown in Figure 10, Oh discloses gates 58/60 correspond to masks P20/P24 of Figure 3 and the gates not shown correspond to masks P18/P22. *Id.* at 14:62–15:2. Oh further discloses these gates have the same shapes as masks

P18–P24. *See id.* at 15:3–5 (“For ease of understanding about the shape and arrangement of the gates, reference is made to FIGS. 3, 10, and 11 and the description thereof.”).

d) single local interconnect layer

Claim 8 further requires a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline. Ex. 1001, Reexam. Cert. 1:25–27. Despite Patent Owner’s arguments to the contrary, discussed *infra*, Petitioner demonstrates how Oh teaches or suggests this limitation. *See* Pet. 24–33. Petitioner illustrates Oh’s teachings with a colorized version of Figure 5 of Oh, which is reproduced below.



The figure is a Petitioner-colored version of Figure 5 of Oh showing masks for pads P50/P60 (blue) and P52/P62 (yellow) in Oh's first metal layer. *Id.* at 31. Petitioner demonstrates how these masks are for making local interconnects corresponding to bitlines and wordlines and the remaining masks in Figure 5 are for making other local interconnects. *Id.* at 24–33. Therefore, because “none of the structures shown in Figure 5 perform any other function than providing local interconnects,” Petitioner demonstrates how Figure 5 is a single local interconnect layer that

“exclusively performs interconnect functions.” *Id.* at 30 (citing Ex. 1019 ¶¶ 78, 127).

First, relying on its analysis of the “local interconnect” limitation, discussed in §§ II.E.2.c(2), *supra*, Petitioner demonstrates how P50/P60, P54/P64, P56/P66, and P58/P68 are masks that form local interconnects in Oh’s first metal layer and how interconnects C7/C8 formed by masks P50/P60 connect to bitlines 102/106 in Oh’s third metal layer. *Id.* at 30–32 (citing Ex. 1004, 10:12–15, 10:31–34, 11:3–12:21, 18:48–19:26, Figs. 5–9, 26, 27); *see also* § II.E.2.c(2), *supra*. Petitioner further demonstrates how masks P52/P62 form interconnects C9/C10 that connect to global wordline P98 in Oh’s second metal layer. *Id.* at 32–33 (citing Ex. 1004, 10:12–15, 10:31–34, 11:6–8, 11:15–17, 11:45–50, 6:31–34, 16:48–52, Figs. 5–7).

Patent Owner argues “Oh does not teach a single local interconnect layer that includes short connections that both route bitline signals and route a global wordline signal along that same layer.” PO Resp. 35. Although Patent Owner admits that “Oh discloses ‘local interconnects corresponding to . . . a global wordline’ on [Oh’s] metal 1 layer” Patent Owner denies that Oh teaches a local interconnect corresponding to bitlines because Oh “rout[es] the bitline signal vertically downward from via P70 through (rather than along) pad layer P50 to contact C7.” *Id.* at 35–36 (emphases omitted, alterations in original). Patent Owner further argues that if landing pads that route signals vertically can be considered interconnects “then the metal contacts of Osada would also have qualified as a single local interconnect layer, and the ’805 patent would not have been patentable over Osada.” *Id.* at 37.

We disagree with Patent Owner’s arguments for several reasons. First, the arguments are based on Patent Owner’s proposed construction of

“a single local interconnect layer,” which requires routing all signals laterally along the interconnect layer. We disagree with that construction for the reasons discussed in § II.D.2, *supra*. Nothing in the ’805 patent or its prosecution history requires interconnects in the single local interconnect layer to connect laterally displaced components. Indeed, the ’805 patent fails to even disclose *how* bitlines and a wordline are arranged in the first and second metal layers, respectively. *See* Ex. 1001, 13:10–32. Thus, although the embodiment shown in Figure 3 of the ’805 patent illustrates routing bitline and wordline signals along an interconnect layer to connect laterally displaced bitlines and wordlines, neither the Specification nor the claims require any particular routing arrangement because neither requires any particular bitline or wordline arrangement. *See id.* at 5:4–7 (“It should be understood, however, that the drawings . . . are not intended to limit the invention to the particular form disclosed.”).

Second, we disagree with Patent Owner’s contention that a layer of metal contacts constitutes an interconnect layer. As discussed in § II.D.2, *supra*, the Specification of the ’805 patent discloses that a local interconnect layer is a deposited layer of conducting material that is “patterned and etched” and “a distinct process layer that exclusively performs . . . short connections.” Ex. 1001, 11:22–23, 12:39–49. Thus, Osada’s dielectric layer containing metal contacts cannot be a local interconnect layer because it is not a deposited layer of conducting material. *Id.* at 8:52–55, 13:19–22 (disclosing forming “contacts” rather than “interconnects” in a deposited dielectric material layer).¹⁶

¹⁶ We note, as explained in § II.D.2, *supra*, that the first metal layer shown in Figure 5 of Osada is a single local interconnect layer because it is the only metal layer in Osada that exclusively performs the interconnect function.

e) Conclusions regarding claim 8

For the reasons discussed in §§ II.E.2.a–d, *supra*, Petitioner has demonstrated by a preponderance of evidence that Oh teaches or suggests all the limitations of claim 8. Accordingly, Qualcomm has demonstrated that claim 8 is unpatentable under 35 U.S.C. § 103(a) as obvious over Oh.

3. Claims 9 and 11

Claim 9 depends from claim 8, requires all local interconnects to be either substantially oblong or substantially square, and requires the memory cell to include substantially square local interconnects. Ex. 1001, 14:36–39. Claim 11 requires each local interconnect in the single local interconnect layer to be substantially oblong. *Id.* at Reexam. Cert. 1:36–38.

Petitioner demonstrates how all of Oh’s local interconnects—shown in Figures 3, 5, and 7—are either “substantially oblong” or “substantially square” and include “substantially square” interconnects. *See* Pet. 33–38, 40. As discussed in §§ II.E.2.c, *supra*, Petitioner demonstrates how masks P20/P22 in Figure 3 and masks P50–P66 in Figure 5 form substantially oblong local interconnects. Petitioner further demonstrates how masks P86, P88, P94, and P92 in Figure 7 are rectangular and form “substantially oblong” local interconnects and how masks P90 and P96 are square and form “substantially square” local interconnects. *Id.* at 35–38 (citing Ex. 1001, Figs. 6–8; Ex. 1019 ¶¶ 97–98, 137–139). In particular, Petitioner demonstrates how masks P90/P96 form second pads C11 in Oh’s second metal layer that connect substantially aligned first/second vias C11. *See* Ex. 1001, 11:8–10, 11:17–19, 11:31–34, 11:41–44, 11:62–67, Figs. 6–8. According to the unrebutted testimony of Dr. Lee, which we credit, a person of ordinary skill in the art would have connected substantially aligned first/second vias C11 with substantially square local interconnects because

“square interconnects exhibit less RC [resistive-capacitive propagation] delay than rectangular conductive structures.” Ex. 1019 ¶ 139.

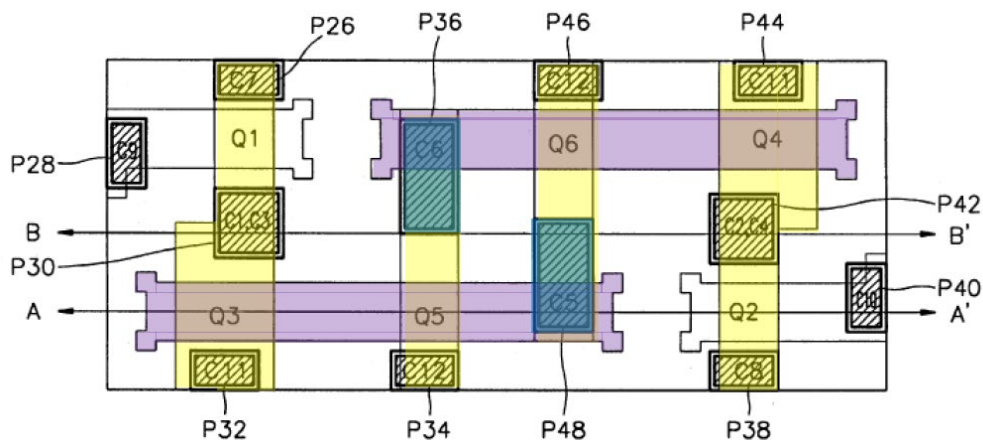
Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claims 9 and 11 for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claims 9 and 11. Accordingly, Petitioner has demonstrated that claims 9 and 11 are unpatentable over Oh.

4. Claim 10

Claim 10 depends from claim 8 and requires the memory cell to include a shared contact to one of the active regions and a polysilicon structure that is arranged substantially perpendicular to and has a portion that abuts a portion of the active region. Ex. 1001, 14:40–45.

Petitioner demonstrates how Oh teaches these limitations, illustrating its contentions with a colorized version of Figure 4 of Oh, which is reproduced below. *See* Pet. 38–40 (citing Ex. 1004, 10:1–6, Figs. 3, 4).



The figure is a Petitioner-colored version of Figure 4 of Oh showing masks P10–P16 (yellow) for making active regions for transistors Q3–Q6 in a

semiconductor substrate, masks P20/P22 (purple) for making polysilicon gates for transistors Q3–Q6, and masks P36/P48 (blue) for making contacts C5/C6. *Id.* at 39.

Oh discloses mask P36 is used to make a hole for contact C6 to the common gate of transistors Q4/Q6 and the source of transistor Q5, and mask P48 is used to make a hole for contact C5 to the common gate of transistors Q3/Q5 and the source of transistor Q6. Ex. 1004, 9:43–47, 9:60–63, 10:1–6, Fig. 4. Oh teaches filling these holes with tungsten to form plugs. *Id.* at 7:56–58, 16:4–8, Figs. 4, 21. As discussed in §§ II.E.2.b and II.E.2.c(1), *supra*, gates P20/P22 are substantially perpendicular to active regions P10–P16. Thus, contact C5 is shared by active region P14 and gate P20, and gate P20 is substantially perpendicular to and has a portion that abuts a portion of active region P14. Similarly, contact C6 is shared by active region P12 and gate P22, and gate P22 is substantially perpendicular to and has a portion that abuts a portion active region P12. Ex. 1004, Figs. 3, 4.

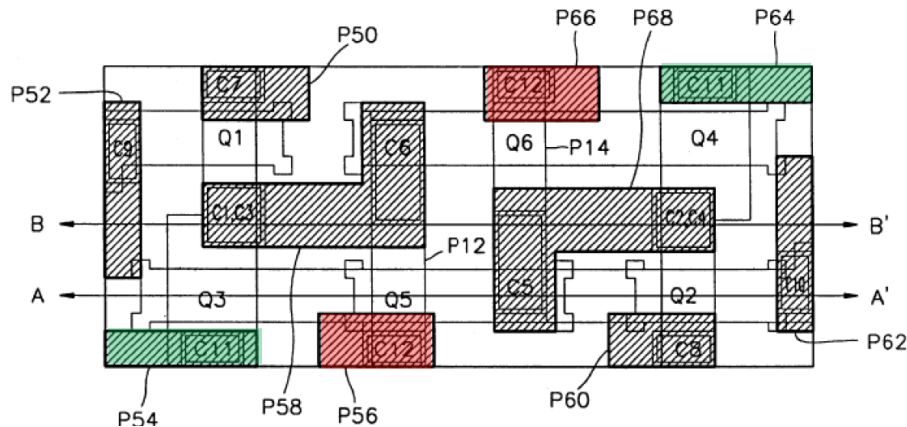
Patent Owner argues Petitioner has failed to demonstrate that claim 10 is unpatentable for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 10 and that Qualcomm has demonstrated that claim 10 is unpatentable over Oh.

5. Claim 12

Claim 12 depends from claim 8, and requires the single local interconnect layer to include local interconnects corresponding to common power and common ground. Ex. 1001, Reexam. Cert. 1:39–41.

Petitioner demonstrates how Oh teaches these limitations, illustrating its contentions with a colorized version of Figure 5 of Oh, which is reproduced below. *See* Pet. 40–45 (citing Ex. 1004, 10:7–12:21, Figs. 5–9).



The figure is a Petitioner-colored version of Figure 5 of Oh showing masks P54/P64 (green) used to make pads C11 and masks P56/ P66 (red) used to make pads C12 in Oh's first metal layer. *Id.* at 41. As discussed in §§ II.E.2.c(2) and II.E.2.d, *supra*, Petitioner demonstrates how Oh's first metal layer is a single local interconnect layer and how pads C11 and C12 in Oh's first metal layer contact and, therefore, correspond to common power V_{CC} and common ground V_{SS} in Oh's third metal layer.

Patent Owner argues that Petitioner has failed to demonstrate that claim 12 is unpatentable for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 12 and that Qualcomm has demonstrated that claim 12 is unpatentable over Oh.

6. Claim 13

Claim 13 depends from claim 12, and adds to claim 12 the same limitation that claim 11 adds to claim 8. *Compare id.* at 1:42–44, with *id.* at

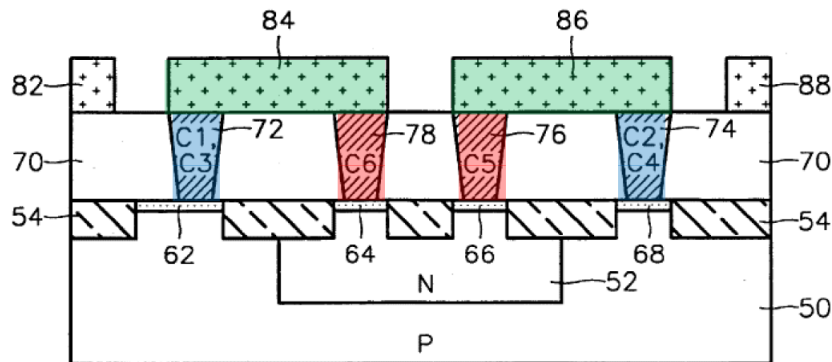
1:36–38. Petitioner, relying on its analysis of claim 11, demonstrates how the same limitation is met in claim 13. *See* Pet. 45; *see also* § II.E.3, *supra*. Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claim 13 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 13 and that claim 13 is unpatentable over Oh.

7. Claim 14

Claim 14 depends from claim 8, and requires a first contact to one active region, a shared contact to another active region and a polysilicon structure, and a substantially oblong local interconnect in the single local interconnect layer that connects the first and shared contacts. Ex. 1001, Reexam. Cert. 1:45–52.

Petitioner demonstrates how Oh teaches these limitations, illustrating its contentions with a colorized version of Figure 21 of Oh, which is reproduced below. *See* Pet. 45–51 (citing Ex. 1004, 10:1–6, 12:37–53, 13:9–23, 16:4–24, Figs. 3–5, 11, 21).



The figure is a Petitioner-colored version of Figure 21 of Oh showing first connection line 84 connecting contacts C1/C3 and C6. *Id.* at 50. Contact C1/C3 contacts common drain 62 of transistors Q1/Q3 in first (outer) active

region P10. *See* Ex. 1004, 9:36–38, 12:39–41, Figs. 3, 4, 11. Contact C6 is a shared contact that contacts source 64 of transistor Q5 in third (inner) active region P12 and common gate P22 for transistors Q4/Q6. *Id.* at 9:43–47, 12:41–45, Figs. 3, 4, 11; *see also* § II.E.4, *supra*. Thus, first connection line 84 connects (a) first contact C1/C3 to substantially oblong outer active region P10 to (b) shared contact C6 to substantially oblong inner active region P12. As discussed in § II.E.2.c(2), first connection line 84 is formed by mask P58 and is a substantially oblong local interconnect formed in Oh's first or single local interconnect layer. *See* Ex. 1004, 10:22–28, 13:10–16, Fig. 11.¹⁷

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claim 14 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 14 and that claim 14 is unpatentable over Oh.

8. Claim 16

Claims 8 and 16 are substantially similar independent claims. Both recite a memory cell having a plurality (e.g., 4) of substantially oblong and substantially parallel active regions in a semiconductor substrate and a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline. *Compare* Ex. 1001, Reexam. Cert. 1:25–35,

¹⁷ For the same reasons, Petitioner demonstrates how Oh teaches second connection line 86 made from mask P68 connects (a) first contact C2/C4 to outer active region P16 to (b) shared contact C5 to inner active region P14 and common gate P20. *See* Ex. 1004, 9:51–54, 9:60–63, 10:41–47, 13:17–23, 12:45–53, Figs. 3, 4, 11.

with id. at 1:64–2:9. Claim 16 differs from claim 8 by requiring the inner/outer active regions to have source/drain regions for p-channel/n-channel transistors and by not requiring a plurality of substantially oblong and substantially parallel local interconnects that are substantially perpendicular to the active regions. *Id.*

Given the substantial similarity between claims 8 and 16, Petitioner demonstrates how the claim 16 limitations that are common to claim 8 are met via its analysis of claim 8. *See* Pet. 51–56; *see also* §§ II.E.2.a, II.E.2.b, and II.E.2.d, *supra*. Petitioner also demonstrates how Oh teaches inner active regions P12/P14 have source/ drain regions for p-channel transistors and outer active regions P10/P16 have source/ drain regions for n-channel transistors. *See* Pet. 54–56 (citing Ex. 1004, 8:62–67, 9:30–41, 9:47–57, Figs. 3, 4). Oh’s “first and second active regions P10 and P16 [are] for forming NMOS transistors” Q1–Q4 and Oh’s “third and fourth active regions P12 and P14 [are] for forming PMOS transistors” Q5/Q6. Ex. 1004, 8:62–65, Fig. 3. Oh forms sources/drains for NMOS transistors Q1–Q4 in outer active regions P10/P12 and for PMOS transistors Q5/Q6 in inner active regions P12/P14. *Id.* at 9:30–57, 12:30–53, Figs. 3, 4, 11.

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 14 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 16 and that Qualcomm has demonstrated that claim 16 is unpatentable over Oh.

9. Claim 17

Claim 17 depends from claim 16 and adds to claim 16 the same limitation that claim 11 adds to claim 8. *Compare* Ex. 1001, Reexam. Cert. 1:36–38, *with id.* at 2:10–12. Petitioner, relying on its analysis of claim 11, demonstrates how the same limitation is met in claim 17. *See* Pet. 56; *see also* § II.E.3, *supra*. Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 17 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 17 and that claim 17 is unpatentable over Oh.

10. Claim 18

Claim 18 depends from claim 16 and adds to claim 16 the same limitation that claim 12 adds to claim 8. *Compare* Ex. 1001, Reexam. Cert. 1:39–41, *with id.* at 2:13–15. Petitioner, relying on its analysis of claim 12, demonstrates how the same limitation is met in claim 18. *See* Pet. 56; *see also* § II.E.5, *supra*. Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 18 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 18 and that Qualcomm has demonstrated that claim 18 is unpatentable over Oh.

11. Claims 19 and 20

Claim 19 depends from claim 18 and adds to claim 18 the same limitation that claim 13 adds to claim 12. *Compare* Ex. 1001, Reexam. Cert. 1:42–44, *with id.* at 2:16–18. Claim 20 depends from claim 16 and adds to claim 16 essentially the same limitations that claim 14 adds to claim 8.¹⁸ *Compare id.* at 1:45–53, *with id.* at 2:19–26. Petitioner, relying on its analyses of claims 13 and 14, demonstrates how the same limitations are met in claims 19 and 20, respectively. *See* Pet. 56–60; *see also* §§ II.E.6–7, *supra*. Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claims 19 and 20 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claims 19 and 20 and that claims 19 and 20 are unpatentable over Oh.

12. Claim 22

Claim 22 depends from claim 16 and requires a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions. Ex. 1001, Reexam. Cert. 2:37–40.

As discussed in § II.E.2.c(1), *supra*, Petitioner maps Oh’s polysilicon gates, which are formed by and have the same shapes and arrangements as masks P20/P22, to the claim 8 limitation requiring a plurality of

¹⁸ Claim 14 requires a first contact to *an* active region and a shared contact to *another* active region, whereas claim 20 requires a first contact to *an outer* active region and a shared contact to *an inner* active region. *Compare* Ex. 1001, Reexam. Cert. 1:45–53, *with id.* at 2:19–26. Petitioner’s analysis of claim 14, however, accounts for these slight differences. *See* Pet. 45–51.

substantially oblong local interconnects above said substrate and substantially perpendicular to the active regions in the substrate. Petitioner relies on these same polysilicon gates to meet the claim 22 limitation requiring a plurality of substantially oblong polysilicon structures arranged above and substantially perpendicular to the active regions. *See* Pet. 60–61. We agree for the reasons discussed in § II.E.2.c(1), *supra*.

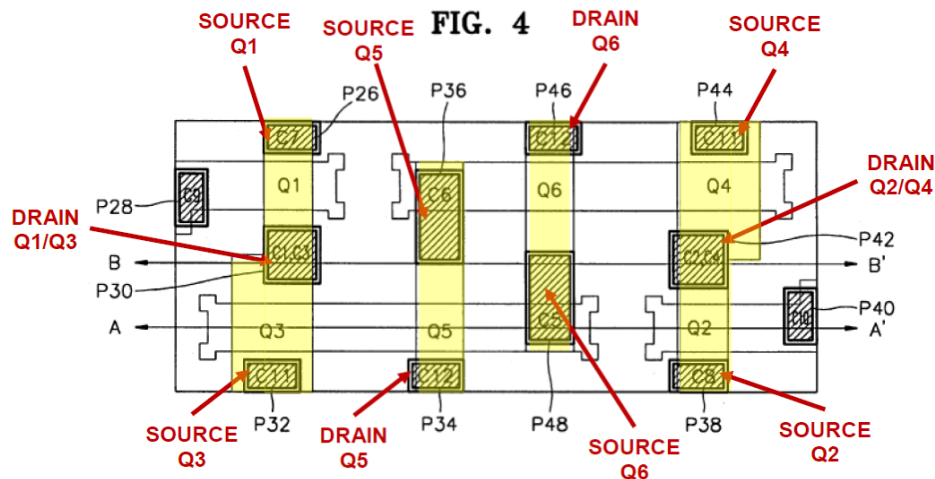
Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 22 over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 21–39. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2.a–d, *supra*.

Accordingly, for the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 22 and that Qualcomm has demonstrated that claim 22 is unpatentable over Oh.

13. Claim 23

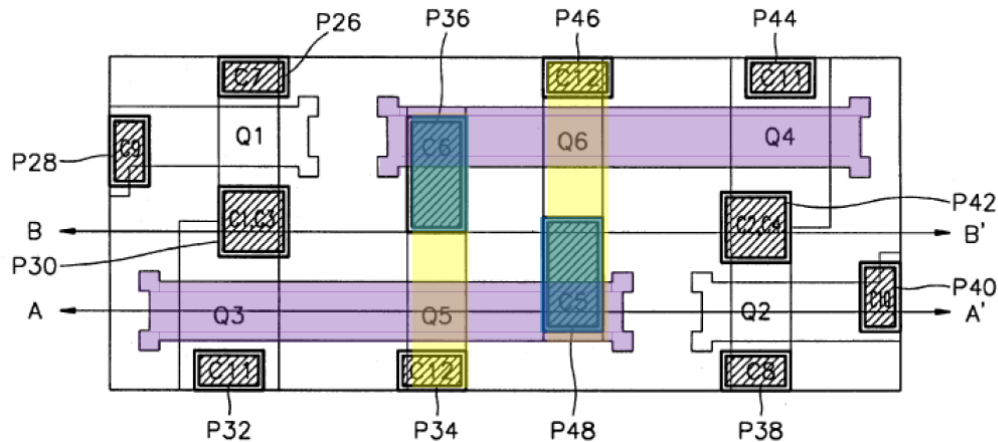
Claim 23 depends from claim 16 and requires source/drain contacts to the source/drain regions of the active region transistors, wherein at least one of the source/drain contacts comprises a shared contact to one of the inner active regions and one of the polysilicon structures. Ex. 1001, Reexam. Cert. 2:41–46.

Petitioner illustrates how Oh teaches making contacts to the source/drain regions of active region transistors in two annotated versions of Figure 4 of Oh, which we combine and reproduce below. *See* Pet. 62–63.



The figure above combines two Petitioner-annotated versions of Figure 4 of Oh showing masks C1/C3, C2/C4, C5–C8, C11, and C12 that are used to make contact holes to source/drain regions of transistors Q1–Q6. *Id.* (citing/quoting Ex. 1004, 7:56–58, 9:30–67, 16:4–23, Fig. 4). Contact hole C1/C3 reaches the common drain of Q1/Q3, contact hole C2/C4 reaches the common drain of Q2/Q4, contact hole C5 reaches both the common gate of Q3/Q5 and the source of Q6, contact hole C6 reaches both the common gate of Q4/Q6 and the source of Q5, contact hole C7 reaches the source of Q1, contact hole C8 reaches the source of Q2, contact holes C11 reach the sources of Q3/Q4, and contact holes C12 reach the drains of Q5/Q6. *Id.* at 9:30–63, Fig. 4. These contact holes are then filled with tungsten to form contacts to the sources and drains of transistors Q1–Q6. *Id.* at 7:56–58, 16:4–23.

Petitioner illustrates how Oh teaches making a shared contact to an inner active region and a polysilicon structure in a colored version of Figure 4 of Oh, which is reproduced below. *See* Pet. 64.



The figure above is a Petitioner-colored version of Figure 4 of Oh showing how masks C5/C6 (blue) are used to make contacts that are shared by inner active regions (yellow) and polysilicon gates (purple). *Id.* at 63–64 (citing Ex. 1004, 10:1–6, 10:61–11:2, Figs. 3–4). Mask C5 (lower, right) makes contact hole C5 that “exposes both the [polysilicon] gates of the first drive transistor Q3 and the first load transistor Q5 and the [active region] source of the second load transistor Q6.” Ex. 1004, 10:1–3. Likewise, mask C6 makes contact hole C6 that exposes both the polysilicon gate of transistors Q4/Q6 and the active region source of Q5. *Id.* at 10:3–6. Contact holes C5/C6 are subsequently filled with tungsten so each forms a shared contact to an inner active region and a polysilicon structure. *Id.* at 7:56–58, 16:4–9.

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claim 23 over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 21–39. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2.a–d, *supra*.

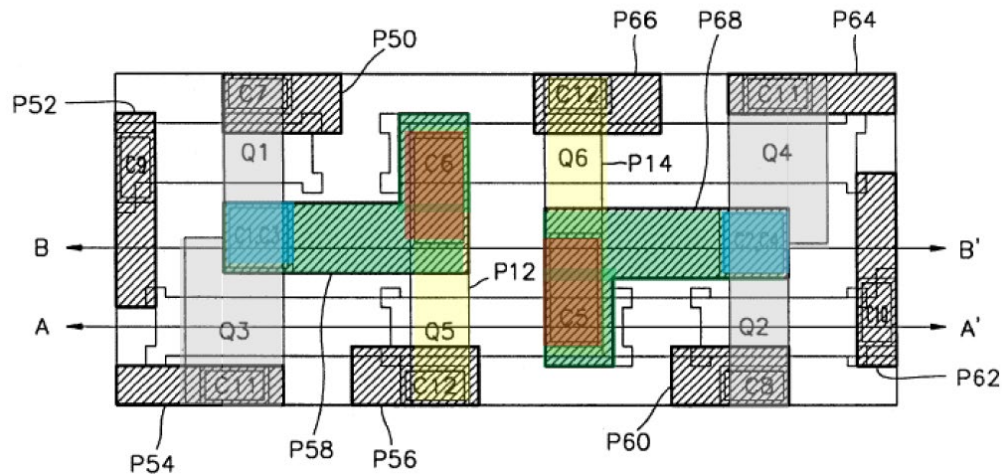
Accordingly, for the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claim 23 and that Qualcomm has demonstrated that claim 23 is unpatentable over Oh.

14. Claims 24 and 25

Claim 24 depends from claim 23 and requires a plurality of substantially oblong local interconnects substantially perpendicular to the active regions, and further requires one of the substantially oblong local interconnects to connect the shared contact required by claim 23 to another one of the source/drain contacts required by claim 23. *See* Ex. 1001, Reexam. Cert. 2:41–53.

Petitioner illustrates how Oh teaches the limitations of claim 24 in a colored version of Figure 5 of Oh, which is reproduced below. *See* Pet. 66; *see also* § II.E.2.c(2), *supra*.

FIG. 5



The figure is a Petitioner-colored version of Figure 5 of Oh illustrating how masks P58/P68 (green) form a series of substantially oblong local interconnects that are perpendicular to active regions P12/P14 (yellow). Pet. 66 (citing Ex. 1004, 13:9–23, Figs. 5, 11, 21). Mask P58 (green) forms interconnect 84, which connects contact C1/C3 (blue) to shared contact C6 (brown). *See* Ex. 1004, 10:22–28, 13:9–15, Figs. 5, 11, 21. Contact C1/C3 contacts drain 62 of transistors Q1/Q3, and shared contact C6 contacts both the gate of transistors Q4/Q6 and source 64 of transistor Q5. *Id.* Likewise,

mask P68 (green) forms interconnect 86 that connects contact C2/C4 (blue) to shared contact C5 (brown), where contact C2/C4 contacts drain 68 of transistors Q2/Q4 and shared contact C5 contacts both the gate of transistors Q3/Q5 and source 66 of transistor Q6. *Id.* at 10:41–47, 13:17–23, Figs. 5, 11, 21. Interconnects 84/86 (P58/P68) are substantially oblong and substantially perpendicular to the inner active regions P12/P14 containing transistors Q5/Q6 for the reasons discussed in § II.E.2.c(2), *supra*.

Claim 25 depends from claim 24 and requires the substantially oblong local interconnects to be dielectrically spaced above the semiconductor substrate. *See* Ex. 1001, Reexam. Cert. 2:54–56. Petitioner demonstrates how Oh teaches this limitation in a colorized version of Figure 21, which illustrates how interconnects 84/86 formed by masks P58/P68 are spaced above substrate 50 by dielectric layer 70. *See* Pet. 66–67 (citing Ex. 1004, 6:28–50, 15:26–16:67, Figs. 20–21). Oh uses masks P58/P68 to form interconnects 84/86 in a second conductive layer that is deposited over semiconductor substrate 50, gate oxide layer 56, a polysilicon gate layer, and first interlevel dielectric layer (ILD) 70. Ex. 1004, 14:55–60, 15:26–30, 16:24–29, 16:40–41, 16:61, Figs. 11, 21. Thus, interconnects 84/86 are dielectrically spaced above semiconductor substrate 50 by ILD 70.

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claims 24 and 25 over Oh for the same reasons discussed above with respect to claim 8. *See* PO Resp. 21–39. We disagree with Patent Owner’s arguments for the reasons discussed in § II.E.2.a–d, *supra*.

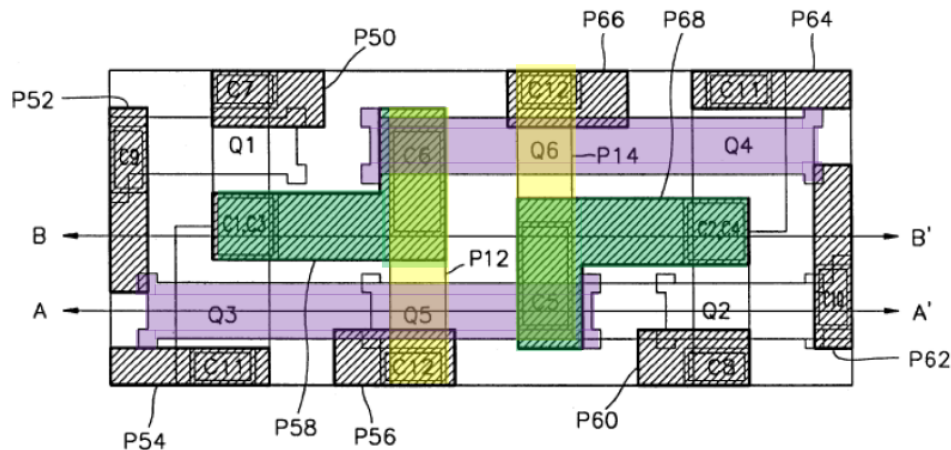
Accordingly, for the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claims 23 and 24, and that claims 23 and 24 are unpatentable over Oh.

15. Claims 27 and 28

Claim 27 is an independent claim that is substantially similar to claim 20, which depends from claim 16. *Compare* Ex. 1001, Reexam. Cert. 2:61–3:11, *with id.* at 1:64–2:9 and 2:20–27. Claim 27 differs from claim 20 by requiring the substantially oblong local interconnect that connects the first contact to an outer active region and the shared contact to an inner active region and a polysilicon structure to (a) overlap both the polysilicon structure and the inner active region, but not requiring it to (b) be part of a single local interconnect layer. *Id.*

Petitioner, relying on its analyses of claim 16 and 20,¹⁹ demonstrates how all the limitations of claim 27 are met except for the limitation requiring the substantially oblong local interconnect to overlap both the polysilicon structure and the inner active region. *See* Pet. 67–68; *see also* §§ II.E.7, II.E.8 and II.E.11, *supra*. As discussed in § II.E.7, first connection line 84 formed by mask P58 connects (a) first contact C1/C3 to substantially oblong outer active region P10 to (b) shared contact C6 to substantially oblong inner active region P12 and common gate P22. Petitioner demonstrates how Oh discloses first connection line 84 overlaps both polysilicon gate P22 and inner active region P12. *See* Pet. 68 (citing Ex. 1004, 10:48–60, Fig. 5). This is illustrated in a Petitioner-colored version of Figure 5 of Oh, which is reproduced below.

¹⁹ As discussed in § II.E.11, *supra*, Petitioner’s claim 20 analysis relies on its claim 14 analysis. Thus, Petitioner’s claim 27 analysis at times refers to its claim 20 analysis or its claim 14 analysis. *See* Pet. 67–68.



The figure is a Petitioner-colored version of Figure 5 of Oh. *Id.* at 68. First connection line 84 made by mask P58 (green, upper left) overlaps both inner active region P12 (yellow, left) and polysilicon gate P22 (purple, upper right). *See* Ex. 1004, 12:22–13:23, Figs. 5, 11.

Claim 28 adds the same limitation to claim 27 that claim 25 adds to claim 24. *Compare* Ex. 1001, Reexam. Cert. 3:12–14, *with id.* at 2:54–56. Petitioner, relying on its analyses of claim 25, demonstrates how the same limitation is met in claim 28. *See* Pet. 68; *see also* §§ II.E.14, *supra*.

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claims 27 and 28 over Oh for the same reasons as claim 8. *See* PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claims 27 and 28 and that claims 27 and 28 are unpatentable over Oh.

16. Claims 30–32

Claim 30 is an independent claim that is substantially similar to claim 14, which depends from claim 8. Claim 30 differs from claim 14 in the same way claim 27 differs from claim 16, i.e., it requires the

substantially oblong local interconnect that connects the first contact to an outer active region and the shared contact to an inner active region and polysilicon structure to overlap both the polysilicon structure and one of the active regions, but does not require it to be part of a single local interconnect layer. *Compare* Ex. 1001, Reexam. Cert. 3:40–56, *with id.* at 1:25–35 and 1:45–53. Petitioner, relying on its analyses of claims 8, 14, and 27, demonstrates how all the limitations of claim 30 are met. *See* Pet. 69; *see also* §§ II.E.2, II.E.7 and II.E.15, *supra*.

Claim 31 adds to claim 30 the same limitation that claim 9 adds to claim 8. *Compare* Ex. 1001, Reexam. Cert. 3:57–61, *with* Ex. 1001, 14:36–39. Petitioner, relying on its analyses of claim 9, demonstrates how all the limitations of claim 31 are met. *See* Pet. 69; *see also* § II.E.3, *supra*.

Claim 32 requires the polysilicon structure that shares a contact with an active region to be substantially perpendicular to that active region and to have a portion that abuts a portion of that active region. *See* Ex. 1001, Reexam. Cert. 3:62–67. Petitioner demonstrates how Oh teaches these limitations. *See* Pet. 69–70. As discussed in § II.E.7, *supra*, Oh discloses first connection line 84, made by mask P58, is a substantially oblong local interconnect that connects (a) contact C1/C3 to outer active region P10 to (b) contact C6 shared by inner active region P12 and polysilicon gate P22. *See* Ex. 1004, 9:36–47, 10:22–28, 12:39–45, 13:10–16, Figs. 3–5, 11. As discussed in § II.E.4, Petitioner demonstrates how polysilicon gate P22 is perpendicular to inner active region P12 and has a portion that abuts a portion of inner active region P12.

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claims 30–32 over Oh for the same reasons as claim 8.

See PO Resp. 21–39. We disagree for the reasons discussed in §§ II.E.2.a–d, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that Oh teaches all the limitations of claims 30–32 and that claims 30–32 are unpatentable over Oh.

F. Obviousness over Oh and Lee

Petitioner argues that claims 7, 15, 21, 26, and 29 are unpatentable as obvious over the combination of Oh and Lee. Pet. 77–91. Patent Owner disagrees. PO Resp. 83–85. For the reasons discussed below, we find Petitioner has demonstrated by a preponderance of evidence that claims 7, 15, 21, 26, and 29 are unpatentable over Oh and Lee.

1. Lee

Lee discloses the damascene technique “for forming planar metal/insulator structures” on the surface of a semiconductor substrate. Ex. 1020, 2:16–17. The damascene technique is illustrated in Figure 6 of Lee, which is reproduced below.

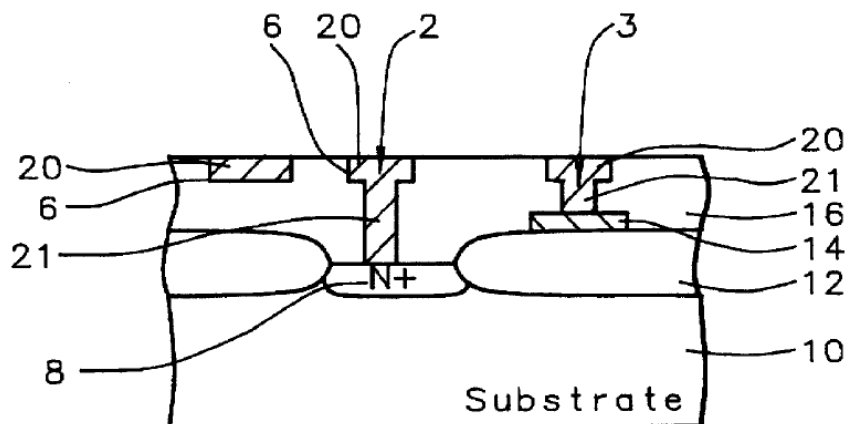


Figure 6 of Lee is a cross-sectional view showing the “process steps for forming a single level of planar electrical interconnections and buried metal plugs on a [semiconductor] substrate.” *Id.* at 3:55–58. Semiconductor substrate 10 has active region 8, separated from other active regions by field

oxides 12, and polysilicon layer 14 that can be, e.g., an FET (field-effect transistor) gate or bit lines for an SRAM. *Id.* at 4:44–47, 4:59–63. Lee’s process begins by depositing insulating layer 16 on semiconductor substrate 10, active region 8, field oxides 12, and polysilicon gate 14. *Id.* at 5:1–4. Contact openings 2 and 3, respectively, are etched into insulating layer 16 down to active region 8 and polysilicon gate 14. *Id.* at 5:21–25. Trenches 6 are then etched into insulating layer 16, including into upper portions of contact openings 2 and 3. *Id.* at 6:1–9. Contact plugs 21 and interconnects 20 are then concurrently formed by depositing a metal layer in contact openings 2/3 and trenches 6. *Id.* at 6:23–55. Chemical, mechanical polishing (CMP) removes the portion of the metal layer lying above insulating layer 16, thereby making interconnects 20 coplanar with insulating layer 16. *Id.* at 7:3–9, 7:22–24. This allows a second metal/insulating layer to be formed on top of the first. *Id.* at 7:18–20. The second layer is made by depositing insulating layer 30 on top of the first layer, etching trenches and contact holes 32 (vias) in insulating layer 30, filling the trenches and contact holes 32 with metal, and planarizing the deposited metal to make the trenches and vias coplanar with insulating layer 30. *Id.* at 7:20–41. The process can be repeated, as needed, “to fabricate the necessary number of levels to complete the wiring for the integrated circuit.” *Id.* at 7:41–43.

2. Reasons to Combine Oh and Lee

Petitioner argues that Oh discloses making SRAM cells using a process “in which contacts (Oh Figure 4) and interconnects (Oh Figure 5) are formed through two deposition steps.” Pet. 81 (citing Ex. 1004, 14:27–17:7, Figs. 12–14, 19–21). Petitioner argues that a person skilled in the art would have found it obvious to replace this two-step process with the single

step damascene process described in Lee. *Id.* (citing Ex. 1019 ¶¶ 218–219). Doing so would have resulted in the benefits disclosed in Lee, including reducing the number of process steps and avoiding shortcomings in the two-step process (e.g., intra-level shorts, low yield and reliability, and increasingly irregular and non-planar metal layers). *Id.* at 82–83 (citing/quoting Ex. 1020, 1:27–54; 4:3–11). Petitioner argues this modification would amount to no more than applying “a known technique (e.g., Lee’s manufacturing process) to a known device (e.g., Oh’s SRAM circuit) ready for improvement to yield predictable results.” *Id.* at 83 (citing Ex. 1019 ¶¶ 51–53, 222).

Patent Owner argues a person skilled in the art “would not have been motivated to combine Oh with Lee” because the proposed modification “would increase the number of masks used to form [Oh’s] SRAM cell” despite Oh’s stated purpose of making SRAM cells using “standard CMOS logic manufacturing processes without the need for additional masks or processes.” PO Resp. 83–84 (quoting Ex. 1004, 3:2–7 (emphasis omitted); citing Ex. 2015 ¶¶ 223–225). Patent Owner argues Lee’s damascene process would increase the number of masks/process steps needed to make the contacts and metal interconnects shown in Figures 4 and 5 of Oh. *Id.* at 85.

Petitioner replies that Patent Owner cites no evidence that Lee’s process would increase the number of masks/steps needed by Oh and that Lee states the exact opposite, i.e., “that because ‘metal lines’ and ‘contact openings or via holes’ . . . ‘both are simultaneously filled with metal and etched back at the same time,’ this ‘further reduce[s] the number of processing steps.’” Pet. Reply 21 (quoting Ex. 1020, 2:16–35) (emphasis omitted, second alteration in original). Petitioner further argues that Patent Owner also ignores Lee’s teachings regarding the benefits of the damascene

metallization process, including avoiding non-planar metal layers, intra-level shorts, low yields, and reliability problems. *Id.* (citing Ex. 1020, 1:33–54; Ex. 1019 ¶ 219). Finally, Petitioner argues that Lee’s “[d]amascene processing was a standard semiconductor manufacturing process” when the ’805 patent was filed in 2001 and Oh teaches making SRAMs using “standard CMOS logic manufacturing processes.” *Id.* at 22 (citing Ex. 1020, 2:16–35) (emphasis omitted).

We find Petitioner has articulated sufficient reasoning with rational underpinning to combine the teachings of Oh and Lee. Oh teaches a conventional process for making SRAM cells, and Lee teaches the disadvantages of the then-conventional metallization process and how those disadvantages can be overcome using the damascene metallization process. *See* Ex. 1020, 1:27–54, 2:16–28, 4:3–11. Thus, Petitioner’s proposed combination substitutes “one element for another known in the field” to yield a predictable and beneficial result. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

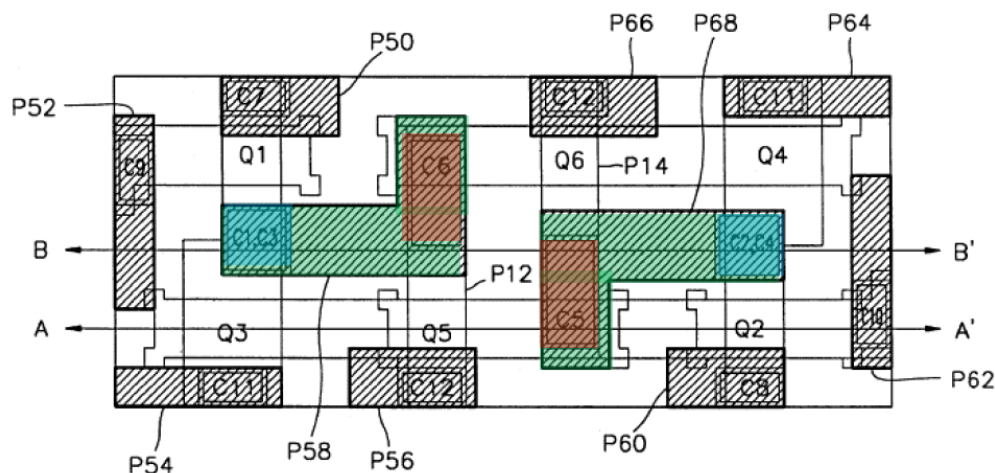
Patent Owner’s arguments to the contrary don’t dissuade us from this finding. Indeed, we agree with Petitioner that Lee’s process for forming contacts and metal layers *reduces* the number of steps in Oh’s process as taught by Lee. *See* Pet. Reply 21 (quoting Ex. 1020, 2:16–35). Both Oh and Lee start their metallization process by depositing an insulating layer, masking it, and etching contact openings. *Compare* Ex. 1004, 15:26–16:3 *with* Ex. 1020, 5:1–3, 5:20–25. Oh forms contacts in this insulating layer by (1) depositing metal and (2) planarizing the metal using CMP, and forms interconnects over the contacts by (3) depositing a second metal layer, (4) masking the second metal layer, and (5) etching to form interconnects. *See* Ex. 1004, 16:4–17:7. Lee, by contrast, simultaneously forms contacts

and interconnects in the insulating layer by (1) masking the insulating layer having contact openings (2) etching to form trenches, (3) depositing metal to simultaneously form contacts in the contact openings and interconnects in the trenches, and (4) planarizing using CMP. *See* Ex. 1020, 2:16–24. Thus, as stated by Lee, the damascene process “reduce[s] the number of processing steps” by simultaneously filling contact holes and interconnect trenches. *Id.* at 2:24–28.

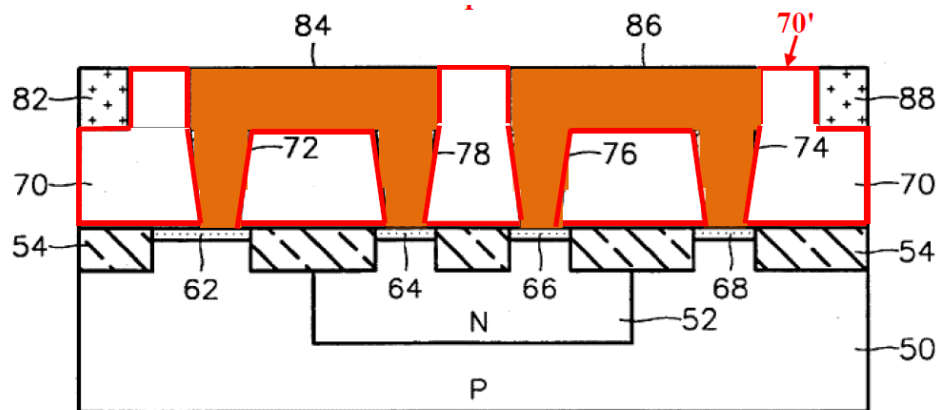
3. Modification of Oh in view of Lee

Petitioner proposes modifying Oh’s method of manufacturing SRAM cells by using the damascene process to make interconnects and vias/contacts in its metal layers. Petitioner argues “[s]uch a modification would leave the structures of Oh unchanged from a plan view with all structures—contacts, vias, metal lines—remaining present and at the same location and with the same interconnections as disclosed by Oh,” but would integrate these structures into a single metal structure that can be seen in the cross-sectional view. Pet. 83–85.

Petitioner illustrates its contentions with Petitioner-colored versions of Figures 5 and 21 of Oh. Petitioner’s colored version of Figure 5 is reproduced below.



The figure is a Petitioner-colored version of Figure 5 of Oh showing how the locations of contacts C1/C3 (blue), C2/C4 (blue), C5/C6 (brown), and interconnects P58/P68 (green) in Oh's first metal layer do not change when they are made using Lee's damascene process. *See* Pet. 83–84 (citing Ex. 1019 ¶ 223). Petitioner argues interconnect P58 (P68) would be integrated with contacts C1/C3 and C6 (C2/C4 and C5) when Oh's first metal layer is made using the damascene process because they would be made by filling the contact holes and trenches in the same metal deposition step. *Id.* at 84–85 (citing Ex. 1019 ¶ 224). This is shown in Petitioner's colored version of Figure 21 of Oh, which is reproduced below. *See* Pet. 85.



The figure is a Petitioner-colored version of Figure 21 of Oh, which is a cross-sectional view of Oh's SRAM device. Using Lee's damascene process, Oh would first create contact holes 72 (C1/C3), 74 (C2/C4), 76 (C5), and 78 (C6) in dielectric layer 70, then create interconnect trenches 84 (P58) and 86 (P68), then fill the contact holes and trenches with metal (orange) in a single metal deposition step. *Id.* at 15:38–39, 15:46–47, 15:56–57, 15:66–67, 16:40–41, 16:61–62.

4. Claims 7, 26, and 29

Claim 7, which depends from and incorporates all the limitations of cancelled claims 1, 2, 4, and 5, was not reexamined. *See* Ex. 1001, Reexam. Cert. 1:17, 1:24; Ex. 1001, 13:44–14:27; 35 U.S.C. § 112 ¶ 4. Claim 7 has limitations that are substantially similar to limitations recited in claims 16 and 22–24. Claim 7 differs from the limitations recited in claims 16 and 22–24 in that claim 7 requires the upper surfaces of the local interconnects and source/drain contacts to be substantially coplanar, but does not require the local interconnects to be part of a single local interconnect layer having interconnects corresponding to bitlines and a global wordline. *Compare* Ex. 1001, 13:44–14:8, 14:12–21, 14:25–27 *with* Ex. 1001, Reexam. Cert. 1:64–2:9, 2:37–53.

Claim 26 depends from claim 24, and adds to claim 24 the same limitation that claim 7 adds to cancelled claim 5. *Compare* Ex. 1001, Reexam. Cert. 2:57–60, *with* Ex. 1001, 14:25–27. Claim 29 is an independent claim that is substantially similar to independent claim 27. *Compare* Ex. 1001, Reexam. Cert. 3:16–39, *with id.* at 2:61–3:11. Claim 29 adds to claim 27 (a) the same limitation claim 7 adds to cancelled claim 5 and (b) the same limitation claim 23 adds to claim 16. *Compare id.* at 3:27–30 and 3:36–38, *with id.* at 2:41–46 and Ex. 1001, 14:25–27. As discussed in § II.E.15, *supra*, claim 27 is substantially similar to claim 20.

Petitioner, relying on its analyses of claims 16, 20, 22–24, and 27, demonstrates how all the limitations of claims 7, 26, and 29 are met by Oh except for the limitation requiring the upper surfaces of local interconnects and source/drain contacts to be substantially coplanar. *See* Pet. 86–87, 90–91; *see also* §§ II.E.8 and II.E.11–15, *supra*.

As discussed in § II.E.14, *supra*, interconnect 84 formed by mask P58 connects contact C1/C3 to shared contact C6 and interconnect 86 formed by mask P68 connects contact C2/C4 to shared contact C5. *See* Ex. 1004, 10:22–28, 10:41–47, 13:9–23, Figs. 5, 11, 21. C1/C3 contacts drain 62 of transistors Q1/Q3, C2/C4 contacts drain 68 of transistors Q2/Q4, C6 contacts source 64 of transistor Q5 and C5 contacts source 66 of transistor Q6. *Id.* Petitioner demonstrates how interconnects 84/86 (P58/P68) are coplanar with source/drain contacts C1/C3, C2/C4, C5, and C6 when Oh is modified to use Lee’s damascene process because Lee’s process would “‘form[] the electrically isolated metal lines [] in the trenches [], and concurrently form[] the metal plug contacts [] in the contact openings,’ thereby making interconnects and contacts ‘coplanar.’” Pet. 87 (citing Ex. 1019 ¶¶ 224, 255; citing/quoting Ex. 1020, 3:28–30, 7:3–7) (second, third, and fifth alterations in original).

In addition to arguing that a person skilled in the art would not have modified Oh to use Lee’s damascene process, Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claims 7, 26, and 29 by failing to demonstrate how the combination teaches a plurality of substantially oblong local interconnects and polysilicon structures. *See* PO Resp. 83–85. We disagree for the reasons discussed in §§ II.E.2.c and II.F.2, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that the combination of Oh and Lee teaches all the limitations of claims 7, 26, and 29, and that claims 7, 26, and 29 are unpatentable over the combination of Oh and Lee.

5. *Claims 15 and 21*

Claim 15 is substantially similar to claim 14. *Compare* Ex. 1001, Reexam. Cert. 1:54–63, *with id.* at 1:45–53. It differs from claim 14 in that it (a) requires the local interconnect that connects the first contact to the shared contact to be “formed from a trench opening as a contact to one of the substantially oblong active regions,” but (b) does not require that local interconnect to be part of the single local interconnect layer. *Id.* Claim 21 is substantially similar to claim 20 in the same way claim 15 is substantially similar to claim 14. *Compare id.* at 2:28–36, *with id.* at 2:20–27.

Petitioner, relying on its analyses of claims 14 and 20, demonstrates how all the limitations of claims 15 and 21 are met by Oh, except for the limitation requiring the local interconnect that connects the first contact to the shared contact to be formed from a trench opening as a contact to one of the substantially oblong active regions. *See* Pet. 88–90; *see also* §§ II.E.7 and II.E.11, *supra*.

As discussed in §§ II.E.7 and II.E.11, *supra*, interconnect 84 formed by mask P58 connects contact C1/C3 to shared contact C6 and interconnect 86 formed by mask P68 connects contact C2/C4 to shared contact C5. *See* Ex. 1004, 10:22–28, 10:41–47, 13:9–23, Figs. 5, 11, 21. C1/C3 contacts drain 62 of transistors Q1/Q3, C2/C4 contacts drain 68 of transistors Q2/Q4, C6 contacts source 64 of transistor Q5 and C5 contacts source 66 of transistor Q6. *Id.* Petitioner further demonstrates how modifying Oh to use Lee’s damascene process results in interconnect 84 (P58) being formed from a trench opening as (a) contact C1/C3 to transistors Q1/Q3 in active region P10 and (b) contact C6 to transistor Q5 in active region P12. *See* Pet. 89–90 (citing Ex. 1019 ¶¶ 217, 224, 229, 230; citing/quoting Ex. 1004, 8:39–9:67, 10:61–11:2, 14:55–15:5, Fig. 3). Petitioner similarly demonstrates how the

same modification results in interconnect 86 (P68) being formed from a trench opening as (a) contact C2/C4 to transistors Q2/Q4 in active region P16 and (b) contact C5 to transistor Q6 in active region P14. *Id.*

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claims 15 and 21 over Oh for the same reasons as claim 7. *See* PO Resp. 83–85. We disagree for the reasons discussed in § II.F.4, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that the combination of Oh and Lee teaches all the limitations of claims 15 and 21, and that claims 15 and 21 are unpatentable over the combination of Oh and Lee.

G. Obviousness over Oh and Nii

Petitioner argues claims 53–57 and 59–61 are unpatentable as obvious over the combination of Oh and Nii. Pet. 92–114. Patent Owner disagrees. PO Resp. 85–87. For the reasons discussed below, we find Petitioner has demonstrated by a preponderance of evidence that claims 53–57 and 59–61 are unpatentable over the combination of Oh and Nii.

1. Nii

Nii discloses “a layout of a multi-port SRAM . . . cell having CMOS construction.” Ex. 1021, 1:5–7. The memory cell includes “bit lines BL and /BL . . . formed as second metal-wiring layers” and “[a] word line WL . . . formed as a third metal-wiring layer.” *Id.* at 1:66–67, 2:8–9.

2. Reasons to Combine Oh and Nii

Petitioner argues that Oh discloses two embodiments, one having three metal layers and the other four. *See* Pet. 92–94. In both embodiments, the second metal layer contains a wordline and the third metal layer contains bitlines. *Id.* However, in the first embodiment the third metal layer also

contains power lines, whereas in the second embodiment the third metal layer only contains bitlines—the power lines are moved to the fourth metal layer. *Id.* (citing Ex. 1004, 19:38–51). Nonetheless, the underlying cell structure in Figures 3–5 can be used for both embodiments because it allows “vertical connections . . . up to the [bit, word, and power] lines without conflicting with each other.” *Id.* at 98 (citing Ex. 1019 ¶¶ 88, 96–106).

As discussed in § II.G.1, *supra*, Nii teaches locating bitlines in the second metal layer and a wordline in the third metal layer. Pet. 98 (citing Ex. 1021, 1:5–2:9, 2:31–34). Petitioner argues that a person skilled in the art would have found it obvious to modify Oh’s second embodiment in view of Nii’s teaching—i.e., by moving Oh’s bitlines to the second metal layer and Oh’s wordline to the third metal layer. *Id.* at 101–103. Petitioner argues that this rearrangement of Oh’s bitlines and wordline would have been obvious because it “was one of a finite set of known design choices.” *Id.* at 103 (citing Ex. 1019 ¶ 274). Petitioner further argues that this rearrangement would have been obvious because Nii’s “configuration minimizes issues with RC delay and power consumption.” *Id.* at 101. Petitioner argues that both Oh and Nii arrange the SRAM wordline in the longer, longitudinal cell dimension, and Nii teaches this is done to reduce power consumption. *Id.* (citing Ex. 1021, 2:22–31). However, because this arrangement increases RC signal delay along the wordline, Nii places the wordline in a higher metal layer whose thicker and wider metal traces lower the resistance, capacitance, and RC signal delay. *Id.* at 101–102 (citing Ex. 1021, 2:58–62; Ex. 1019 ¶ 270). Thus, Petitioner argues, a person skilled in the art would have been motivated to modify Oh based on the teachings of Nii because “Nii’s arrangement would improve the similar device of Oh in the same way.” *Id.* at 102–103 (citing Ex. 1019 ¶¶ 268,

270). Patent Owner does not dispute Petitioner’s reasoning to combine the teachings of Oh and Nii. See PO Resp. 85–87.

We find Petitioner has articulated sufficient reasoning with rational underpinning to combine the teachings of Oh and Nii. First, placing Oh’s wordline above or below Oh’s bitlines appears to be a design choice for which there are only two possibilities. See *KSR*, 550 U.S. at 421. Second, Petitioner’s proposed modification “‘simply arranges old elements with each performing the same function it had been known to perform’ and yields not more than one would expect from such an arrangement.” *Id.* at 417 (internal citation omitted). Finally, it is obvious to use “a technique that has been used to improve [Nii’s] device. . . [to] improve [Oh’s] similar device[] in the same way.” *Id.*

3. Modification of Oh in view of Nii

Petitioner provides detailed illustrations of the modifications needed to move the wordline in Oh’s second embodiment to the third metal layer and to move the bitlines to the second metal layer. See Pet. 103–109. Petitioner, after summarizing these modifications, states they “are fully compatible with the existing underlying (Figures 5-6) and overlying (Figures 28-29) layers.” *Id.* at 103–104 (citing Ex. 1019 ¶¶ 268, 275).

The modifications involve removing wordline P98 and bitline pads P86/P92 from the second metal layer (Figure 7). *Id.* at 104. Next, bitlines P114/P118 are removed from the third metal layer (Figure 27) and arranged to contact vias P70/P78 (Figure 6) in the second metal layer. *Id.* at 105–106. Wordline pads WL1/WL2 that contact wordline vias P72/P80 (Figure 6) are added to the modified second metal layer. *Id.* Bitline vias P100/P106, which are no longer needed, are removed from the dielectric layer (Figure 26) that separates the modified second and third metal layers. *Id.* at 106.

New vias WL1/WL2 are added to this modified dielectric layer to connect wordline pads WL1/WL2 in the modified second metal layer to wordline P98, which is added to the modified third metal layer. *Id.* No further modifications are needed. Ground/power vias P102–P110 (Figure 28) extend power to power bus P116 and ground buses P112/P120 in the fourth metal layer (Figure 29).

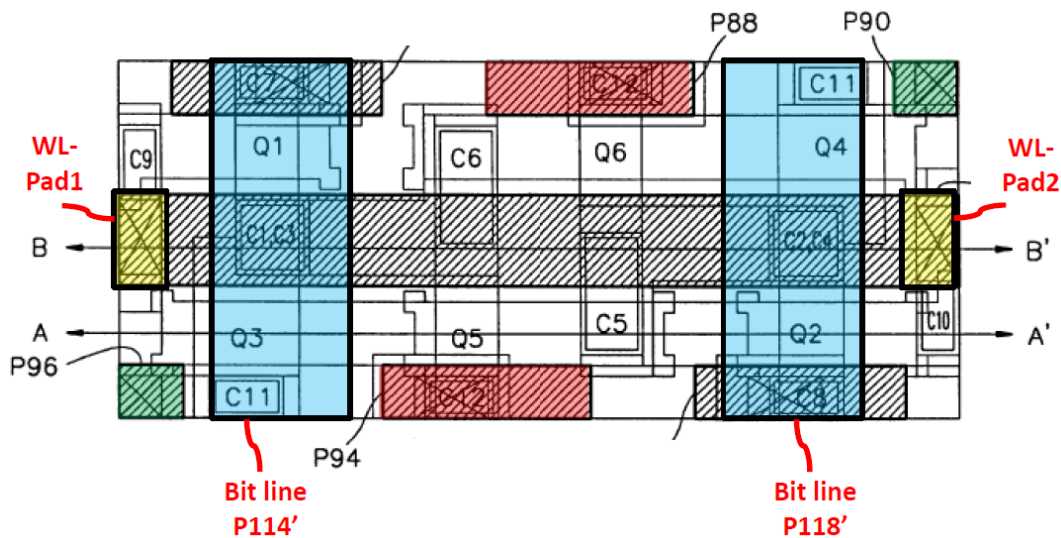
4. Claim 53

Claim 53 is substantially similar to claim 16. *Compare* Ex. 1001, Reexam. Cert. 5:60–6:10, *with id.* at 1:64–2:9. It differs from claim 16 in that it requires (a) a first metal layer above the substrate that contacts bitlines, common power, and common ground across memory cells and (b) a second metal layer above the first and configured as a global wordline, but does not require (c) a single local interconnect layer that includes interconnects corresponding to bitlines and a global wordline. *Id.* Given the substantial similarity between claims 16 and 53, Petitioner demonstrates how the claim 53 limitations that are common to claim 16 are met via its analysis of claim 16. *See* Pet. 109; *see also* §§ II.E.8, *supra*.

Petitioner demonstrates how Oh’s second metal layer, when modified to replace wordline P98 with bitlines P114 and P118, teaches a first metal layer above the substrate that contacts bitlines, common power, and common ground across a plurality of memory cells.²⁰ *See* Pet. 109–111. Petitioner

²⁰ Oh’s first metal layer, shown in Figure 5, maps to the claimed local interconnect layer. *See* § II.E.2.c(2), *infra*. Oh’s second metal layer, shown in Figure 7, maps to the claimed first metal layer, which the Specification describes as “the first conductive layer above the local interconnect layer,” and which may be a misnomer when “the local interconnect layer utilizes a metal,” as Oh does. Ex. 1001, 10:40–43.

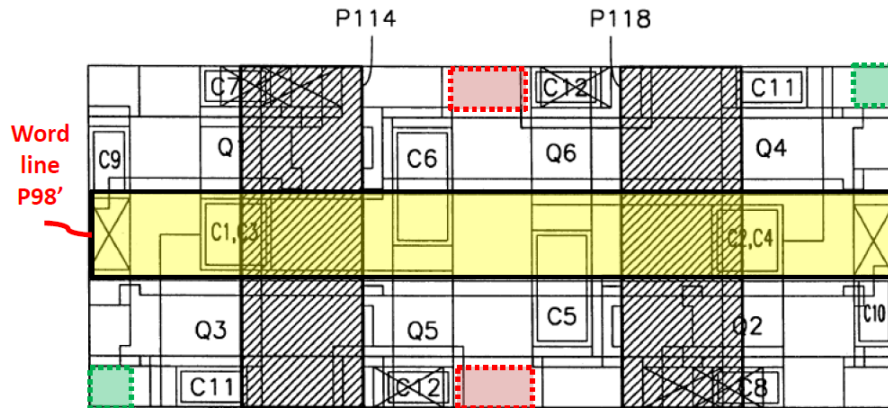
illustrates its contentions with a modified and colorized version of Oh's Figure 7, which is reproduced below.



The figure is a Petitioner-modified and colorized version of Figure 7 of Oh, showing modifications to Oh's second metal layer, including deleting wordline P98 (grey/hashed), deleting landing pads P86/P92 (grey/hashed), adding bitlines P114'/P118' (blue), and adding landing pads WL-Pad1/2 (yellow). *Id.* at 110; *see also id.* at 104–106. Petitioner demonstrates how Oh's modified second metal layer directly contacts bitlines P114'/P118' and indirectly contacts power P116 (V_{CC}) and ground P112/P120 (V_{SS}) in Oh's fourth metal layer, e.g., pads P88/P94 (red) contact P116 through vias P102/P104 and pads P90/P96 (green) contact P112/P120 through vias P108/P110. *Id.* at 110–111 (citing Ex. 1004, 10:7–12:21, 18:48–19:26, Figs. 5–9, 26–29).

Petitioner also demonstrates how Oh's third metal layer, when modified to replace bitlines P114 and P118 with wordline P98, teaches a

second metal layer above the first that is configured as a global wordline.²¹
See Pet. 112. Petitioner illustrates its contentions with a modified and colored version of Oh's Figure 27, which is reproduced below.



The figure is a Petitioner-modified and colored version of Figure 27 of Oh, showing modifications to Oh's third metal layer, including deleting bitlines P114/P118 (grey/hashed) and adding wordline P98' (yellow). *Id.* at 112 (citing Ex. 1004, 19:42–50, Figs. 21, 25).

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claim 53 by failing to demonstrate how the combination of Oh and Nii teaches a plurality of substantially oblong local interconnects and polysilicon structures. See PO Resp. 85. We disagree for the reasons discussed in § II.E.2.c, *supra*. Patent Owner further argues that Petitioner has failed to demonstrate the unpatentability of claim 53 because claim 53 requires the first metal layer to contact bitlines, common power, and common ground, but Petitioner's modification "separates the global bitline and bitline-bar signals from the common power and common ground signals." PO Resp. 85–86.

²¹ See n.26, *supra*. Oh's third metal layer maps to the claimed second metal layer because Oh's second metal layer maps to the claimed first metal layer.

Petitioner replies that claim 53 does not require the bitlines, common power, and common ground to “exist in the ‘first metal layer.’” Pet. Reply 22–23 (citing Ex. 1001, Reexam. Cert. 6:4–5) (claim 53). Instead, it requires the first metal layer to *contact* bitlines, common power, and common ground. *Id.* Petitioner argues pads P94/P98 in Oh’s second metal layer *contact* common power P116 (V_{CC}) in Oh’s fourth metal layer and pads P90/P96 in Oh’s second metal layer *contact* common ground P112/P120 (V_{SS}) in Oh’s fourth metal layer. *Id.* at 23 (citing Pet. 110–111).

We are persuaded by Petitioner’s arguments. Claim 53 requires “a first metal layer above the semiconductor substrate, wherein the first metal layer contacts bitlines, common power, and common ground.” Ex. 1001, Reexam. Cert. 6:4–5. The claim does not require the first metal layer to *include* bitlines, common power, and common ground lines. Rather, it requires the first metal layer to *contact* them. Petitioner demonstrates how bitlines P114’/P118’ in Oh’s second metal layer *contact* global bitlines because they are segments of global bitlines, how pads P90/P96 in Oh’s second metal layer *contact* a global ground bus via ground bus segments P112/P120 (V_{SS}) in Oh’s fourth metal layer through vias P108/P110, and how pads P88/P94 in Oh’s second metal layer *contact* global power bus via power bus segments P116 (V_{CC}) in Oh’s fourth metal layer through vias P102/P104. *See* Ex. 1004, 11:28–45, 11:55–67, 18:65–19:26, Figs. 5–8, 26–29).

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that the combination of Oh and Nii teaches all the limitations of claim 53, and that claim 53 is unpatentable over the combination of Oh and Nii.

5. *Claims 54–57 and 59–61*

Claim 54 depends from claim 53, and adds the same limitation to claim 53 that claim 22 adds to claim 16. *Compare* Ex. 1001, Reexam. Cert. 6:11–14, *with id.* at 2:37–40. Claim 55 depends from claim 54, and adds the same limitation to claim 54 that claim 23 adds to claim 22. *Compare id.* at 6:15–20, *with id.* at 2:41–46. Claim 56 depends from claim 55, and adds the same limitation to claim 55 that claim 24 adds to claim 23. *Compare id.* at 6:21–27, *with id.* at 2:47–53. Claim 57 depends from claim 56, and adds the same limitation to claim 56 that claim 25 adds to claim 24. *Compare id.* at 6:28–30, *with id.* at 2:54–56. Given the substantial similarity between claims 54–57 and claims 22–25, respectively, Petitioner demonstrates how the limitations of claims 54–57 are met by relying on its analysis of claims 22–25, respectively. *See* Pet. 113; *see also* §§ II.E.12–II.E.14, *supra*.

Claim 59 is an independent claim that is substantially similar to independent claim 8. *Compare* Ex. 1001, Reexam. Cert. 6:36–52, *with id.* at 1:25–35. Claim 59 differs from claim 8 in the same way that independent claim 53 differs from independent claim 16, i.e., it requires (a) a first metal layer above the substrate that contacts bitlines, common power, and common ground across memory cells and (b) a second metal layer above the first and configured as a global wordline, but does not require (c) a single local interconnect layer that includes interconnects corresponding to bitlines and a global wordline. *Id.* Claim 60 depends from claim 59, and adds the same limitation to claim 59 that claim 9 adds to claim 8. *Compare id.* at 6:53–57, *with* Ex. 1001, 14:36–39. Claim 61 depends from claim 59, and adds the same limitation to claim 59 that claim 10 adds to claim 8. *Compare* Ex. 1001, Reexam. Cert. 6:58–64, *with* Ex. 1001, 14:40–45.

Given the substantial similarity between claims 8 and 59, and the fact that the limitations in claim 59 that are not recited in claim 8 are recited in claim 53, Petitioner demonstrates how all the limitations of claim 59 are met by relying on its analysis of claims 8 and 53. *See* Pet. 113–114; *see also* §§ II.E.2 and II.G.4, *supra*. Moreover, given the substantial similarity between claims 60/61 and claims 9/10, Petitioner demonstrates how the limitations of claims 60/61 are met by relying on its analysis of claims 9/10. *See* Pet. 114; *see also* §§ II.E.3 and II.E.4, *supra*.

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claims 54–57 and 59–61 over Oh and Nii for the same reason Petitioner has failed to demonstrate the unpatentability of claim 53 over that combination. *See* PO Resp. 85–87. We disagree for the reasons discussed in § II.G.4, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that the combination of Oh and Nii teaches all the limitations of claims 54–57 and 59–61, and that claims 54–57 and 59–61 are unpatentable over the combination of Oh and Nii.

H. Obviousness over Oh, Nii, and Lee

Petitioner argues claim 58 is unpatentable as obvious over the combination of Oh, Nii, and Lee. Pet. 114–115. Patent Owner disagrees. PO Resp. 87. For the reasons discussed below, we find Petitioner has demonstrated by a preponderance of evidence that claim 58 is unpatentable over the combination of Oh, Nii, and Lee.

1. Reasons to Combine Oh, Nii, and Lee

Petitioner argues it would have been obvious to combine the teachings of Oh and Lee for the reasons discussed in § II.F.2, *supra*, and to combine the teachings of Oh and Nii for the reasons discussed in § II.G.2, *supra*. *See*

Pet. 114. Petitioner argues the Nii and Lee modifications of Oh can be “implemented simultaneously because they are non-overlapping, with modifications in view of Lee related to the fabrication process used and the modifications in view of Nii related to the placement of signal and power lines.” *Id.* at 115 (citing Ex. 1019 ¶ 308). Patent Owner does not dispute this.

We agree with Petitioner that the teachings of Lee and Nii are separately combinable with Oh, and that the modifications based on Lee (metallization process) would not interfere with the modifications based on Nii (bitlines and wordline rearrangement). *See* Ex. 1019 ¶ 308. Moreover, for the reasons discussed in §§ II.F.2, and II.G.2, *supra*, we find Petitioner has articulated sufficient reasoning for combining the teachings of Oh with the teachings of Lee, and Nii.

2. Claim 58

Claim 58 depends from claim 56, and adds the same limitation to claim 56 that claim 26 adds to claim 24. *Compare* Ex. 1001, Reexam. Cert. 6:32–35, *with id.* at 2:57–60. Moreover, as discussed in § II.F.4, *supra*, this limitation is the same limitation that claim 7 adds to cancelled claim 5. *Compare id.* at 2:57–60, *with* Ex. 1001, 14:25–27. Given the substantial similarity between claim 58 and claims 7/26, Petitioner demonstrates how the combination of Oh, Lee, and Nii teaches the limitations of claims 58 by relying on its analysis of claim 7. *See* Pet. 115; *see also* § II.F.4, *supra*.

Patent Owner argues that Petitioner has failed to demonstrate the unpatentability of claim 58 by failing to demonstrate how the combination of Oh, Lee, and Nii teaches a plurality of substantially oblong active regions, local interconnects, and polysilicon structures. *See* PO Resp. 87. We disagree for the reasons discussed in §§ II.E.2.b–c, *supra*.

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of evidence that the combination of Oh, Lee, and Nii teaches all the limitations of claim 58, and that claim 58 is unpatentable over the combination of Oh, Lee, and Nii.

I. Obviousness over Oh and Hara or Oh, Hara, and Lee

Petitioner argues claims 53–57 and 59–61 are unpatentable as obvious over the combination of Oh and Hara and that claim 58 is unpatentable as obvious over the combination of Oh, Hara, and Lee. *See* Pet. 116–117. For the reasons discussed in §§ II.G and II.H, *supra*, Petitioner has shown by a preponderance of evidence that these claims are unpatentable over Oh and Nii or Oh, Lee, and Nii. This finding is dispositive of Petitioner’s challenge to the patentability of claims 53–57 and 59–61. Accordingly, we need not address whether Petitioner has further shown, by a preponderance of evidence, that these claims are also unpatentable as obvious over the combination of Oh and Hara or Oh, Hara, and Lee. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but also can “greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

J. Obviousness Grounds that Include Baker

For the reasons discussed in §§ II.E–II.H, *supra*, Qualcomm has shown by a preponderance of evidence that claims 7–32 and 53–61 of the ’805 patent are unpatentable over Oh alone or in combination with one or more of Nii and Lee. This finding is dispositive of Qualcomm’s

challenge to the patentability of all challenged claims. Accordingly, we need not address whether Qualcomm has further shown by a preponderance of evidence that these claims are also unpatentable as obvious over the combination of Oh and Baker, either alone or in further combination with one or more of Nii and Lee. *See Beloit*, 742 F.2d at 1423. For the same reasons, we need not address whether AMD and STM have shown that claims 7, 9, 11, 13–15, 17, 19–21, 24–32 and 53–61 are also unpatentable as obvious over the combination of Oh and Baker, either alone or in further combination with one or more of Nii and Lee.

III. CONCLUSION

We have reviewed the Petition, Patent Owner Response, Petitioner Reply, and Patent Owner Sur-Reply. We have considered all of the evidence and arguments presented by Petitioner and Patent Owner. We find, on this record, Qualcomm has demonstrated by a preponderance of evidence that claims 7–32 and 53–61 of the '805 patent are unpatentable, and AMD and STM have demonstrated by a preponderance of evidence that claims 7, 9, 11, 13–15, 17, 19–21, 24–32 and 53–61 of the '805 patent are unpatentable.²²

²² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. §§ 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
8-14, 16-20, 22-25, 27, 28, 30-32	103(a)	Oh	8-14, 16-20, 22-25, 27, 28, 30-32	
8-14, 16-20, 22-25, 27, 28, 30-32	103(a)	Oh, Baker		
7, 15, 21, 26, 29	103(a)	Oh, Lee	7, 15, 21, 26, 29	
7, 15, 21, 26, 29	103(a)	Oh, Baker, Lee		
53-57, 59-61	103(a)	Oh, Nii	53-57, 59-61	
53-57, 59-61	103(a)	Oh, Baker, Nii		
58	103(a)	Oh, Nii, Lee	58	
58	103(a)	Oh, Baker, Nii, Lee		
53-57, 59-61	103(a)	Oh, Hara		
53-57, 59-61	103(a)	Oh, Baker, Hara		
58	103(a)	Oh, Hara, Lee		
58	103(a)	Oh, Baker, Hara, Lee		
Overall Outcome			7-32, 53-61	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Qualcomm has shown on this record that claims 7-32 and 53-61 of the '805 patent are unpatentable;

FURTHER ORDERED that AMD, and STM have shown on this record that claims 7, 9, 11, 13-15, 17, 19-21, 24-32 and 53-61 of the '805 patent are unpatentable; and

FURTHER ORDERED that this Decision is final, and a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-01491
Patent 6,534,805 C1

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