

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES, LLC,
Patent Owner.

IPR2020-01568¹
Patent 7,282,951 B2

Before KARL D. EASTHOM, BARBARA A. BENOIT, and
SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Taiwan Semiconductor Manufacturing Co. Ltd. “TSMC” filed a petition in IPR2021-00736, and the Board joined it as a party to this proceeding. *See also* Paper 38 (order dismissing-in-part TSMC as a party with respect to claims 1, 4, 5, 8, 10, and 13–15).

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1, 2, 4–6, and 8–29 (the “challenged claims”) of U.S. Patent No. 7,282,951 B2 (Ex. 1001, “the ’951 patent”). Petitioner filed a Declaration of Dr. Paul Franzon (Ex. 1002) with its Petition. Arbor Global Strategies, LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

After the Institution Decision (Paper 12, “Inst. Dec.”), Patent Owner filed a Patent Owner Response (Paper 18, “PO Resp.”) and a Declaration of Dr. Shoukri J. Sourì (Ex. 2011); Petitioner filed a Reply (Paper 22) and a Reply Declaration of Dr. Paul Franzon (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 26, “Sur-reply”). Thereafter, the parties presented oral arguments via a video hearing (Dec. 3, 2021), and the Board entered a transcript into the record. Paper 32 (“Tr.”).

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

Petitioner identifies Xilinx, Inc. as the real party-in-interest. Pet. 68. Patent Owner identifies Arbor Global Strategies LLC. Paper 4, 1. Joined party Taiwan Semiconductor Manufacturing Co. Ltd. is also a real party-in-interest. *See supra* note 1.

B. *Related Proceedings*

The parties identify *Arbor Global Strategies LLC, v. Xilinx, Inc.*, No. 19-CV-1986-MN (D. Del.) (filed Oct. 18, 2019) as a related infringement action involving the ’951 and three related patents, U.S.

Patent No. RE42,035 E (the “’035 patent,”), U.S. Patent No. 6,781,226 B2 (the “’226 patent”) and U.S. Patent No. 7,126,214 B2 (the “’214 patent”). *See* Pet. 68–69; Paper 4. Petitioner “contemporaneously fil[ed] *inter partes* review (IPR)] petitions challenging claims in each of these patents,” namely IPR2020-01567 (challenging the ’214 patent), IPR2020-01570 (challenging the ’035 patent), and IPR2020-01571 (challenging the ’226 patent). *See* Pet. 68. Final written decisions for these three cases issue concurrently with the instant Final Written Decision.

The parties also identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) (filed October 11, 2019) as a related infringement action involving the ’035, ’951, and ’226 patents. *See* Pet. 69; Paper 4. Subsequent to the complaint in this district court case, Samsung Electronics Co., Ltd. (“Samsung”) filed petitions challenging the three patents, and the Board instituted on all challenged claims, in IPR2020-01020, IPR2020-01021, and IPR2020-01022. *See* IPR2020-01020, Paper 11 (decision instituting on claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, and 29 of the ’035 patent); IPR2020-01021, Paper 11 (decision instituting on claims 1, 4, 5, 8, 10, and 13–15 the ’951 patent); IPR2020-01022, Paper 12 (decision instituting on claims 13, 14, 16–23, and 25–30 of the ’226 patent).

The Board recently issued final written decisions in the three Samsung cases, determining all challenged claims unpatentable. *See* IPR2020-01020, Paper 30 (holding unpatentable claims 1, 3, 5–9, 11, 13–17, 19–22, 25, 26, 28, 29 of the ’035 patent); IPR2020-01021, Paper 30 (holding unpatentable claims 1, 4, 5, 8, 10, and 13–15 of the ’951 patent); IPR2020-01022, Paper 34 (holding unpatentable claims 13, 14, 16–23, and 25–30 of the ’226

patent). The Board joined Taiwan Semiconductor Manufacturing Co. Ltd. as a party in each of the prior proceedings as it did here.

C. The '951 patent

The '951 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array ("FPGA") on a die, a memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '951 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.*

Figure 4 follows:

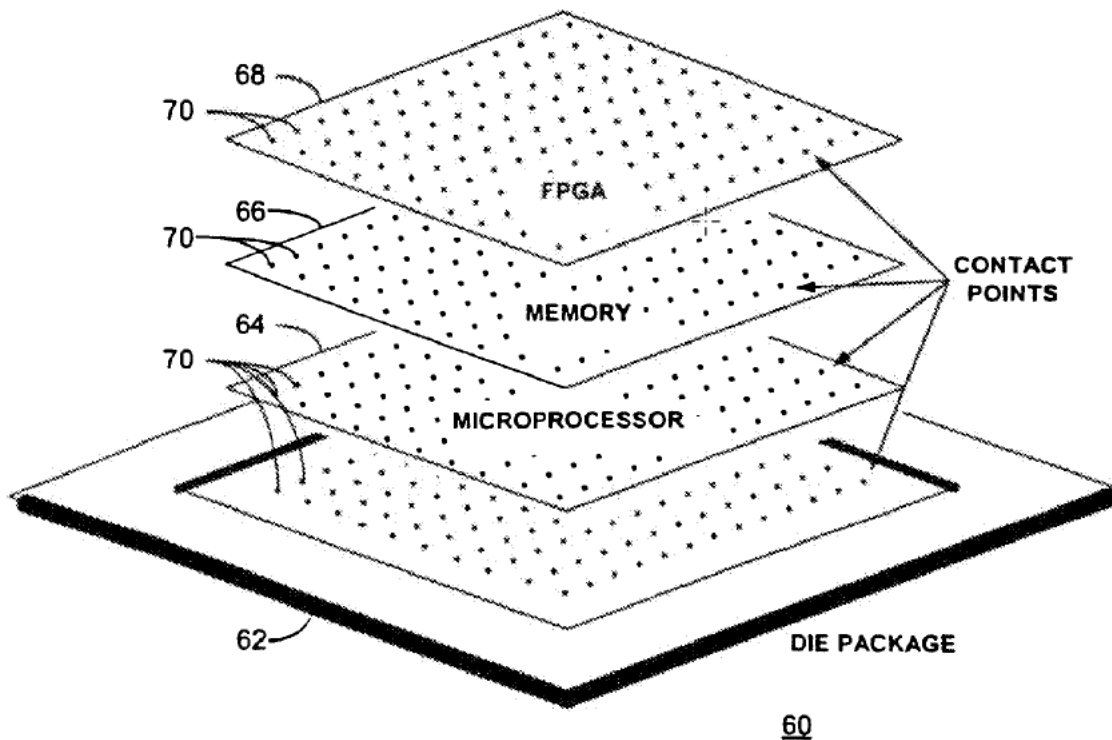


Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using metal and contact holes 70. Ex. 1001, 4:61–5:8.

The '951 patent explains that an FPGA provides known advantages as part of a “reconfigurable processor.” *See* Ex. 1001, 1:26–41. Reconfiguring the FPGA gates alters the “hardware” of the combined “reconfigurable processor” (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., “the conventional ‘load/store’ paradigm”) to run applications. *See id.* Such a “reconfigurable processor” also provides a known benefit of flexibly providing of different logical units required by an application after manufacture or initial use. *See id.*

D. Illustrative Claim 1

Independent claim 1 illustrates the challenged claims at issue:

1. A processor module comprising:

[1.1] at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and

[1.2] at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element [1.3] wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and [1.4] wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.

Ex. 1001, 7:58–8:4; *see* Pet. 23–30 (addressing claim 1).

E. The Asserted Grounds

Petitioner challenges claims 1, 2, 4–6, and 8–29 of the '951 patent on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. §	References
1, 2, 4–6, 8–24, 27, 29	103 ²	Zavracky, ³ Chiricescu, ⁴ Akasaka ⁵
25	103	Zavracky, Chiricescu, Akasaka, Trimberger ⁶
26	103	Zavracky, Chiricescu, Akasaka, Satoh ⁷
28	103	Zavracky, Chiricescu, Akasaka, Alexander ⁸

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. For purposes of trial, the '951 patent contains a claim with an effective filing date before March 16, 2013 (the effective date of the relevant amendment), so the pre-AIA version of § 103 applies.

³ Zavracky et al., US 5,656,548, issued Aug. 12, 1997. Ex. 1003.

⁴ Silviu M. S. A. Chiricescu and M. Michael Vai, *A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data*, Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 1998, ISBN 0-7803-4455-3/98. Ex. 1004.

⁵ Yoichi Akasaka, *Three-Dimensional IC Trends*, Proceedings of the IEEE, Vol. 74, Iss. 12, pp. 1703-1714, Dec. 1986, ISSN 0018-9219. Ex. 1005.

⁶ Steve Trimberger, Dean Carberry, Anders Johnson, and Jennifer Wong, *A Time-Multiplexed FPGA*, Proceedings of the 1997 IEEE International Symposium on Field-Programmable Custom Computing Machines, April 1997, ISBN 0-8186-8159-4. Ex. 1006.

⁷ Satoh, PCT App. Pub. No. WO00/62339, published Oct. 19, 2000. Ex. 1008 (English translation).

⁸ Michael J. Alexander, James P. Cohoon, Jared L. Colflesh, John Karro,

II. ANALYSIS

Petitioner challenges claims 1, 2, 4–6, and 8–29 as obvious based on the grounds listed above. Patent Owner disagrees.

A. *Legal Standards*

35 U.S.C. § 103(a) renders a claim unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

Tribunals resolve obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Relying on the testimony of Dr. Franzon, Petitioner contends that

[t]he person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’951 patent would have been a person with a Bachelor’s Degree in Electrical Engineering or Computer Engineering, with at least two years of industry experience in integrated circuit design, packaging, or fabrication.

Pet. 7 (citing Ex. 1002 ¶¶ 58–60).

and Gabriel Robins, *Three-Dimensional Field-Programmable Gate Arrays*, Proceedings of Eighth International Application Specific Integrated Circuits Conference, Sept. 1995. Ex. 1009.

Relying on the testimony of Dr. Souri, Patent Owner contends that

[a] person of ordinary skill in the art (“POSITA”) around December 5, 2001 (the earliest effective filing date of the ’951 Patent) would have had a Bachelor’s degree in Electrical Engineering or a related field, and either (1) two or more years of industry experience; and/or (2) an advanced degree in Electrical Engineering or related field.

PO Resp. 8–9 (citing Ex. 2011 ¶ 37).

We adopt Petitioner’s proposed level of ordinary skill in the art as we did in the Institution Decision, because it comports with the teachings of the ’951 patent and the asserted prior art. *See* Inst. Dec. 20–21. Patent Owner’s proposed level largely overlaps with Petitioner’s proposed level. Even if we adopted Patent Owner’s proposed level, the outcome would not change.

C. *Claim Construction*

In an *inter partes* review, the Board construes each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2020). Under this standard, which is the same standard applied by district courts, claim terms take their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

The parties' arguments raise a claim construction issue regarding "a memory array functional to accelerate external memory," "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 1, 5, and 10. Independent claims 16, 18, and 23 similarly recite "wherein said memory is functional to accelerate external memory references to [the/said] processing element." Neither party provides an explicit construction.

In the Institution Decision, we determined that

[t]he parties' arguments raise a claim construction issue regarding "a memory array functional to accelerate external memory," "said memory array is functional to accelerate external memory references to the processing element," and "wherein said memory is functional to accelerate external memory references to said programmable array" as recited respectively in claims 1, 5, and 10. Independent claims 16, 18, and 23 similarly recite "wherein said memory is functional to accelerate external memory references to [the/said] processing element." Neither party provides an explicit construction.

Inst. Dec. 21–22. Tracking the institution decision in related IPR2020-01021 (also challenging the '951 patent), in the Institution Decision here, we preliminarily construed the "'functional to accelerate' limitations [as] requir[ing] a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and processor."

Inst. Dec. 25–26. Likewise, in the final written decision in IPR2020-01021 and in co-pending IPR2020-01570, the Board construed these "functional to accelerate" limitations in materially the same manner. *See* IPR2020-

01021, Paper 30, 26, Paper 33 (Errata); IPR2020-01570, Paper 40 (final written decision) § II.C.

In particular, the “functional to accelerate” clauses require “a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array.” *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata). We herein adopt and incorporate the construction and the rationale supporting it from the final written decision of IPR2020-01021.

Petitioner states that “[e]ven beyond the Board’s construction, the Petition shows that the Zavracky-Chiricescu-Akasaka Combination provides the ‘memory array . . . accelerate’ limitations under *any* reasonable construction,” “even under [Patent Owner’s] flawed construction.” Reply 7, 9. Patent Owner states that it “construes all terms in ‘accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.’” PO Resp. 9 (quoting 37 C.F.R. § 42.100(b)).

Patent Owner argues that “the claims require . . . structure provided *within the memory array* (i.e. the wide configuration data port disclosed in the ’951 Patent) that is responsible for accelerating the programmable array’s accelerated external memory references.” PO Resp. 20 (citing Ex. 2011 ¶ 55). However, Patent Owner fails to describe the particular structure of a wide configuration data port (WCDP) within a memory array the challenged claims require under “the ordinary and customary meaning” or otherwise. *See* PO Resp. 19–20. The ’951 patent does not describe a

WCDP “within the memory array.” Figure 5, for example, depicts “VERY WIDE CONFIGURATION DATA PORT” 82, but Figure 5’s WCDP is a separate black box from any structure involving memory or memory array. Compare Ex. 1001, Fig. 4 (memory die 66 and vias 70), with *id.* at Fig. 5 (WCDP 82). See Ex. 1001, 5:29–49 (describing Figure 5).

Figure 5 follows:

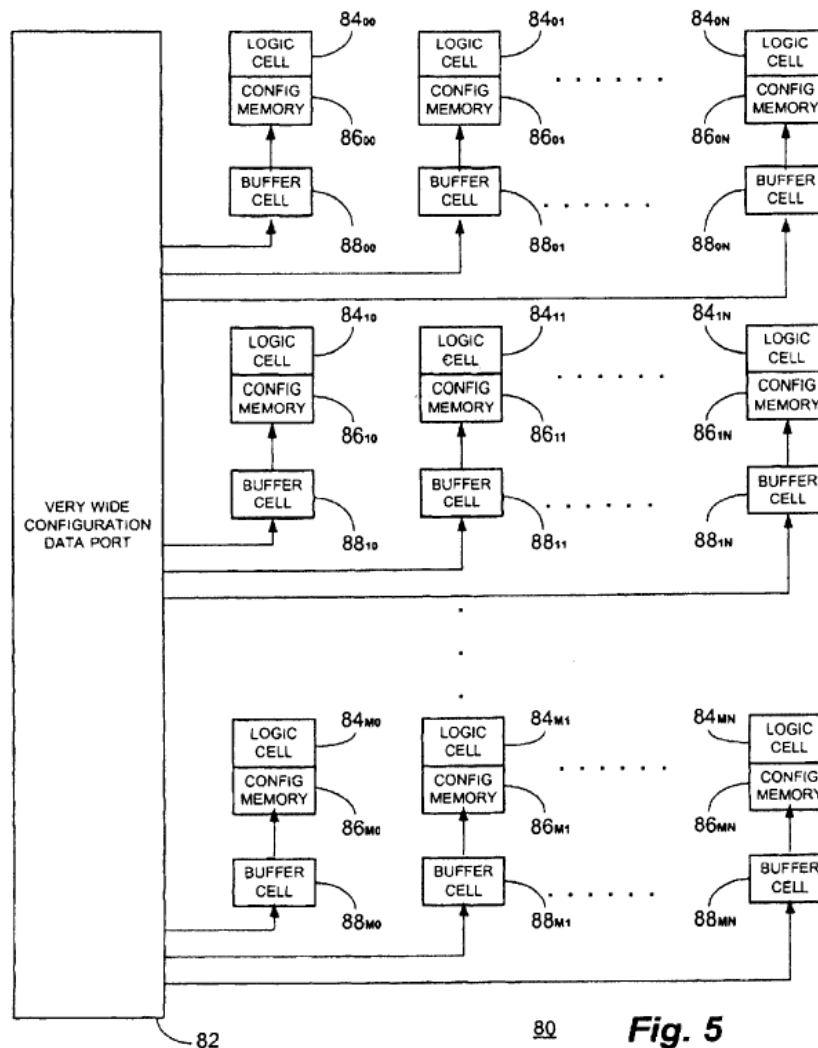


Figure 5 above illustrates a “VERY” WCDP 82 on the left connected to buffer cells 88, and configuration memory cells 88 and logic cells 84, toward the middle and right. See Ex. 1001, Fig. 5; 5:30–49. Buffer cells 88

(“preferably on a portion of the memory die 66” (*see* Fig. 4)), “can be loaded while the FPGA 68 *comprising the logic cells 84 are* [sic] *in operation.*” *Id.* at 5:38–42 (emphasis added).⁹

Therefore, the central purpose of the buffer cells is “*they can be loaded while the FPGA 68 comprising the logic cells are in operation,*” which “then enables the FPGA 68 to be totally reconfigured in one clock cycle with all of it[s] configuration cells 84 updated in parallel.” *Id.* at 5:39–43 (emphasis added). But none of the challenged claims require loading the FPGA while it is in operation. Also, configuration cells and the FPGA can be updated in parallel (e.g., in one clock cycle) without the buffer cells. *See id.*; *see also infra* note 10 (disclosure regarding cache memory providing

⁹ Although the ’951 patent states that “[t]he buffer cells 88 are preferably on a portion of the memory die 66 (FIG. 4)” (*id.*) in reference to Figure 5, buffer cells 88 in Figure 5 appear to be near or connected to FPGA logic cells 84 and configuration memory cells 86—perhaps depicting something other than the preferred embodiment describing buffer cells on the memory die. For example, Dr. Chakrabarty testified that the FPGA is to the right of Figure 5’s WCDP 82, while memory die 66 (*see* Fig. 4), although undepicted in Figure 5, is to the left of Figure 5’s WCDP 82. Ex. 1075, 157:5–158:7; *see also* Reply 9 (quoting 1075, 157:23–158:3). In any event, Figure 5 depicts WCDP 82 as a separate circuit or structure (in black box form) from buffer cells 88 and any memory die or array, and it is not clear how Figure 5’s WCDP relates structurally to a memory die or memory array. *See id.* at Fig. 5.

During the Oral Hearing, Patent Owner’s arguments further blurred what Figure 5 illustrates. That is, Patent Owner argued that “when the buffer cells are on the FPGA, it then raises the question, okay, well, what’s on the memory array, right. And my answer would be *probably* more buffer cells.” Tr. 54:21–24 (emphasis added). But there is no disclosure for buffer cells in or on both a memory array and an FPGA die. *See id.* at 55:3–6 (Patent Owner arguing that “I don’t think there’s anything *that prevents*” buffer cells from being on both dies (emphasis added)).

reconfiguration). Therefore, the challenged claims do not require buffer cells even by implication.

Regardless of the location of the disclosed but unclaimed buffer cells, Figures 4 and 5 and the disclosure indicate that the numerous connections between memory die 66 (with or without buffer cells 88 thereon) and FPGA die 68 (with or without configuration memory cells 86 thereon) facilitate the claimed “functional to accelerate” limitations, in line with our claim construction.¹⁰ In other words, to the extent the claims implicate a WCDP, it is the numerous via connections associated with that port connected to a memory or memory array that support the “functional to accelerate” limitations as discussed further below.

Patent Owner correctly notes that “the ’951 Patent discloses that loading configuration data through a typical, relatively narrow [i.e., 8 ‘bit’ or single ‘byte’] configuration data port [with respect to prior art Figure 3] led to unacceptably long reconfiguration times.” *See* PO Resp. 20 (citing Ex. 1001, 4:47–60); Ex. 1001, 4:54–60 (“Configuration data is loaded through a configuration data port in a *byte serial* fashion and must configure the cells sequentially progressing through the entire array of logic cells 54 and associated configuration memory. It is the loading of this data through a relatively narrow, for example, *8 bit port* that results in the long

¹⁰ The ’951 patent implies that configuration memory cells 66 are on FPGA die 68 in one embodiment, but a cache memory provides reconfiguration without them in other embodiments. *See* Ex. 1001, 5:43–50 (stating that “[o]ther methods for taking advantage of the significantly increased number of connections to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68 as well as to provide larger block random access memory (‘RAM’) than can be offered within the FPGA die itself”).

reconfiguration times.” (emphasis added)).¹¹ Patent Owner contends that “[t]he inventors solved this problem not only by stacking a memory die with a programmable array die, but also by *interconnecting those two elements* with a ‘wide configuration data port’ that employs through-silicon contacts, with the potential for even further acceleration where the memory die is ‘triported.’” *Id.* (citing Ex. 1001, 5:18–25) (emphasis added). This argument itself (which mimics the testimony of Dr. Souri (Ex. 2011 ¶ 56)) shows that any structure associated with the WCDP implicated here simply “interconnect[s] those two [die] elements”—i.e., implicating the numerous vias/contacts 70 as depicted in Figure 4 that connect die elements 66, 66, and 68 together. Therefore, Patent Owner’s argument and Dr. Souri’s testimony support our analysis and claim construction.

In addressing Petitioner’s allegation of obviousness, Patent Owner argues that Petitioner “does not account for all aspects of the claimed invention,” and states “[f]or example, . . . the ’951 patent . . . discloses utilizing a portion of the memory array as a wide configuration data port including buffer cells.” PO Resp. 22 (citing Ex. 1001, 5:34–39). This argument for “buffer cells” differs from Patent Owner’s argument on page 20 of its Response, which does not mention “buffer cells” and only mentions

¹¹ This description indicates that 8 bits of the single byte load in parallel to the first 8 bit locations of configuration memory 56, and then in succession (serial) to the other 8 bit configuration memory cells. In other words, the quoted description about “byte serial” loading and Figure 3 together show that each byte (i.e., 8 bits) loads over a parallel bus into 8 bit blocks (i.e., a byte) of configuration memory cells in succession (i.e., series). *See* Ex. 1001, Fig. 3 (showing 8 bit configuration data port 52 connected by a bus to a block configuration memory cells 56_{M0} and then in serial to successive blocks of configuration memory cells 56_{M1}–56₀₀).

a “wide configuration data port” as “responsible for accelerating the programmable array’s accelerated external memory references.” Again, the argument does not explain how the ’951 patent shows “utilizing a portion of the memory array as a wide configuration data port.”

Based on the specification and claim language as discussed above and further below, apart from numerous vias 70 as depicted in Figure 4, none of the “functional to accelerate” clauses at issue here require any structure associated with a WCDP beyond that included in our construction. In support of our claim construction, Figure 4 of the ’951 patent, depicted next, illustrates vias 70 throughout each die, 64, 66, and 68:

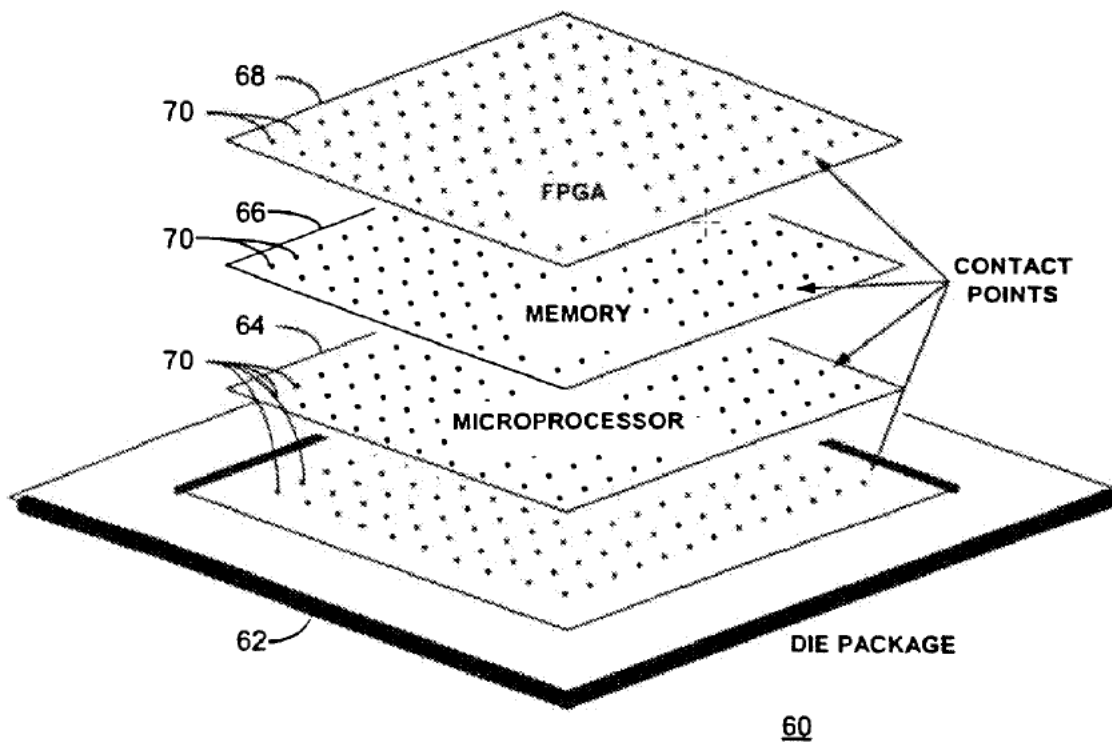


Fig. 4

As depicted above, Figure 4 shows a number of vias 70 throughout the periphery of each die (i.e., microprocessor die 64, memory die 66, and

FPGA 68 die). According to the abstract as quoted above, these “contacts [i.e., vias] . . . traverse the thickness of the die. The processor module disclosed allows for a *significant acceleration* in the sharing of data between the microprocessor and the FPGA element” Ex. 1001, code (57) (emphasis added). This description of “*significant acceleration*” does not mention a WCDP or buffer cells.

Moreover, the '951 patent specification consistently ties data acceleration to stacking techniques that include vias throughout the stacked dies without requiring other structure. In addition to the abstract, the '951 patent describes “taking advantage of the significantly increased number of connections to the cache memory die.” Ex. 1001, 5:44–46. It describes “an FPGA module that uses *stacking techniques* to combine it with a memory die for the purpose of *accelerating FPGA reconfiguration*.” *Id.* at 2:64–65 (emphasis added). Similarly, it states that “the FPGA module may employ *stacking techniques* to combine it with a memory die *for the purpose of accelerating external memory references*.” *Id.* at 2:65–3:2 (emphasis added). The stacking techniques include and refer to the short multiple through-via interconnections *70 distributed throughout the dies* as depicted in Figure 4. *Id.* at 2:41–46 (“[S]ince these differing die do not require wire bonding to interconnect, it is now also possible to place interconnect pads throughout the total area of the various die rather than just around their periphery. This then allows for many more connections between the die than could be achieved with any other known technique.”).

The '951 patent also explains that “[b]ecause the various die 64, 66 and 68 (FIG. 4) have *very short electrical paths* between them, the signal levels can be reduced while at the same time *the interconnect clock speeds*

can be increased.” Ex. 1001, 5:53–56 (emphasis added). Similarly, “there is an added benefit of . . . *increased operational bandwidth.*” *Id.* at 5:50–53 (emphasis added). As summarized here, these descriptions of shorter electrical paths, increased speed and bandwidth (leading to data acceleration), and acceleration in general, all because of the disclosed stacking techniques (which include multiple short through-vias), apply generally to such speed increases (i.e., acceleration) in the context of Figure 4 without mention of Figure 5’s WCDP and buffer cell embodiment, or any tri-port structure. As noted above, even reconfiguration may occur without the specific black box WCDP embodiment of Figure 5, for example, “[o]ther methods for *taking advantage of the significantly increased number of connections* to the cache memory die 66 (FIG. 4) may include its use to totally replace the configuration bit storage on the FPGA die 68.” *Id.* at 5:43–47 (emphasis added); *see also supra* note 10.

Based on the arguments and evidence of record, no reason exists to depart from the claim construction set forth in the final written decision in IPR2020-01021. As Petitioner also argues, Patent Owner did not assert a clear requirement for a WCDP and/or buffer cells for the “functional to accelerate” clauses in related district court litigation. *See* Reply 2–3 (arguing that Patent Owner does not justify incorporating limitations from the specification and “has taken five inconsistent positions on the ‘accelerate’ terms across co-pending IPRs and litigations”) (citing Ex. 1071 (district court claim chart)); Ex. 1071 (listing various claim construction statements by Patent Owner); Ex. 1072, 27). For example, in the district court litigation, Patent Owner argued as follows:

The specification teaches *in several sections that the short interconnects to the memory die allows for accelerated external*

memory references, providing additional context for a POSITA to interpret the claims. Darveaux Decl., ¶ 35. For example, the ‘951 Patent states that in reference to Figures 4 and 5 that *acceleration to external memory is performed because “the FPGA module may employ stacking techniques to combine it with a memory die for accelerating external memory references as well as to expand its on chip block memory.”* Ex. 2, ‘951 Patent at Figs. 4 and 5, 2:56-3:2 (emphasis added).

Ex. 1072, 29 (emphasis added).

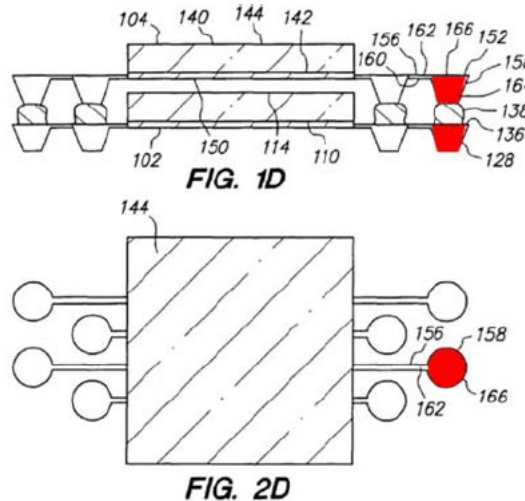
In other words, this passage shows that Patent Owner argued in the district court that “short interconnects” of the disclosed “stacking techniques” improve the speed relative to the prior art—without relying specifically on a WCDP, buffer cells, or parallel processing. *See id.* Therefore, contrary to arguments in the Sur-reply, even though Patent Owner advanced other arguments during the district court litigation, none are clear enough to overcome Patent Owner’s broad statements in the district court litigation as quoted above, and Patent Owner has not “taken consistent positions across all IPRs and litigations.” *See* Sur-reply 2.

As the Board also preliminarily determined in the Institution Decision, prosecution history of the ‘951 patent application also plays an important role in understanding the claims and supports the preliminary claim construction. *See* Inst. Dec. 24–25; *accord* Ex. 2006 (institution decision in IPR2020-01021), 24–25. The prosecution history of the ‘951 patent application further supports our construction.

Specifically, the Examiner indicated allowance of dependent claim 35 of the ‘951 patent (if written in independent form) over Lin (U.S. Patent No. 6,451,626 B1 (Ex. 1054; Ex. 1107, 67)), finding Lin does not teach or suggest “wherein said memory array is functional to accelerate

external memory references to said processing element.” Ex. 1107, 72–73; Inst. Dec. 24–25.

Noting this in our Institution Decision, we pointed to petitioner Samsung’s annotation in the IPR1020-01021 proceeding of the following figures from Lin to illustrate the issue:



Ex. 2006, 25; Inst. Dec. 25. Lin’s annotated Figures 1D and 2D above show that Lin discloses contacts (red) on the sides of dies, instead of a number contact vias extending throughout the area of each die within the periphery thereof, in line with the Examiner’s reasons for allowance. *See id.*; Ex. 1054 (Lin), Figs. 1D, 2D; Ex. 1107, 72–73.

Accordingly, as we noted in the Institution Decision,

in light of Lin’s teachings and absent explicit explanation during prosecution by the Examiner, the rejection and reasons for allowance provide further support the understanding that the “functional to accelerate” limitations require a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory and process[ing element].

Inst. Dec. 25–26; *compare*, Ex. 1001, Fig. 4 (showing numerous contact points), *with* Ex. 1054, Figs. 1D, 2D (showing peripheral contact points).

During the Oral Hearing, Patent Owner argued that with respect to a WCDP that “[*t*]*he spec is very clear that what we’re talking about is it has enough connections to allow the parallel updating of data.*” Tr. 48:20–22 (emphasis added). When asked to compare the ’951 patent’s Figure 3 (which depicts a prior art eight bit configuration data port) and Figure 5 (which depicts a WCDP), Patent Owner stated that the WCDP “could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-bit with 32 bits?” Tr. 49:1–9 (answering “yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what’s critical is not the number of bits and . . . [i]t’s not necessarily the number of bits that’s in the configuration data port, but how they’re arranged”). Patent Owner continued by answering that “parallel connections between cells on the die. . . get to the heart of what the wide configuration data port is, how it works, and how the interconnections between the die work even absent . . . the data being used to configure the FPGA.” *Id.* at 49:11–16. Then, Patent Owner argued that “*we all agree that the wide configuration data port . . . at least includes these interconnections between the die. So, what we’re talking about is moving data from one die to another. That’s the use of the wide configuration data port.*” *Id.* at 49:22–50:2 (emphasis added).

These arguments support our construction because our construction “at least includes these interconnections between the die” and allows data movement between dies. In addition, contrary to Patent Owner’s arguments in the Sur-reply, our construction implicitly distinguishes over

the small number of connections in the narrow configuration data port of the '951 patent's prior art Figure 3. *See* Sur-reply 8 (arguing that "Petitioner's . . . interpretation of the wide configuration data port as simply meaning 'a data port used for configuration . . . [with] a lot of connections though these TSVs' [through silicon vias] . . . directly contradict[s] the specification [and] . . . also encompasses the conventional 'data port,' which the '951 Patent distinguishes the wide configuration data port from" (quoting Reply 8).

In other words, the "functional to accelerate" clauses require "a number of contacts extending throughout the thickness of the wafers in a vertical direction (vias) within the periphery of the die to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array." *See* IPR2020-01021, Paper 30, 26, Paper 33 (Errata). This construction implicitly represents more vias than prior art Figure 3 of the '951 patent describes (i.e., eight), as supported in view of the specification and prosecution history of the '951 patent. *See* Ex. 1001, Fig. 3 ("8 BIT CONFIGURATION DATA PORT 52"). In addition, as discussed further below and as Petitioner shows, to the extent any of the "functional to accelerate" claims implicate parallel data transfer, our claim construction *allows for* such parallel data transfers—in line with Patent Owner's arguments. *See* Tr. 49:13–16 (Patent Owner arguing that "parallel connections between cells on the die . . . get to the heart of what the wide configuration data port is, how it works, and how the interconnections between the die work"); Sur-reply 2 (arguing that "the novel die-area interconnection arrangement with buffer cells (i.e., wide configuration data port) *allows the parallel*

loading of data from the memory die to the programmable array that is responsible for the claimed acceleration” (emphasis added)).

Moreover, Patent Owner concedes that “[t]he ’951 Patent makes clear that stacking die and short interconnections are simply ‘added benefits’ that allow for *increased operational bandwidth and speed*.” Sur-reply 6 (citing Ex. 1001, 5:51–66) (emphasis added). But increased speed is acceleration—not merely “an added benefit.” So is increased bandwidth in context to the ’951 patent, because both benefits of *increase in speed* and bandwidth fall within the “functional to accelerate” limitations at issue here for the reasons discussed above. *See* Ex. 1001, 5:30–50; Tr. 56:11–14 (Patent Owner arguing that “[i]f you have a data port that connects in parallel the cells in the memory array with the FPGA cells, that does massively increase bandwidth. . . . but just increasing bandwidth doesn’t get you parallel connections”). As noted, our claim construction allows for parallel data transfers (i.e., “a number of vertical contacts distributed throughout . . . to allow multiple short paths for data transfer”) so that an increase in bandwidth due to such multiple paths (vias and connections) both satisfies and supports the “functional to accelerate” clauses.

Therefore, as indicated above, we construe the “functional to accelerate” limitations as “a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array.”

Based on the current record, no other terms require explicit construction. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean*

Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness, Claims 1, 2, 4–6, 8–24, 27, 29

Petitioner contends the subject matter of claims 1, 2, 4–6, 8–24, 27, and 29 would have been obvious over the combination of Zavracky, Chiricescu, and Akasaka. Pet. 18–52. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 27–44.

1. Zavracky

Zavracky, titled “Method for Forming Three Dimensional Processor Using Transferred Thin Film Circuits,” describes “[a] multi-layered structure” including a “microprocessor . . . configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure.” Ex. 1003, codes (53), (57). Zavracky’s “invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing.” *Id.* at 2:5–10. Zavracky includes numerous types of stacked elements, including “programmable logic device[s]” stacked with “memory” and “microprocessor[s].” *See id.* at 5:19–23.

Zavracky's Figure 12 follows:

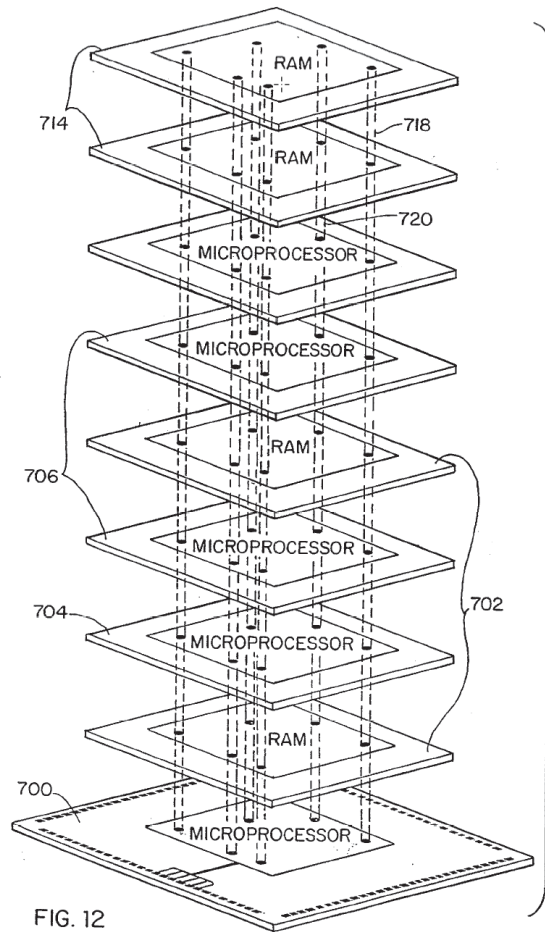


Figure 12 above illustrates a stack of functional circuit elements, including microprocessor and RAM (random access memory) elements wherein “buses run vertically through the stack by the use of inter-layer connectors.” Ex. 1003, 12:24–26.

2. *Chiricescu*

Chiricescu, titled “A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data,” describes a three-dimensional chip, comprising an FPGA layer, memory layer, and routing layer. Ex. 1004, II-232. Chiricescu’s FPGA includes a “layer of on-chip random access memory . . . to store configuration information.” *Id.*

Chiricescu describes and cites the published patent application that corresponds to Zavracky (Ex. 1003) as follows:

At Northeastern University, the 3-D Microelectronics group has developed a unique technology which allows us to design individual CMOS circuits and stack them to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.

See id. at II-232, II-235 (citing “P. Zavracky, M. Zavracky, D-P Vu and B. Dingle, ‘*Three Dimensional Processor using Transferred Thin Film Circuits*,’ US Patent Application # 08-531-177, allowed January 8, 1997”).¹²

Chiricescu describes “[a]nother feature of architecture [as] a layer of on-chip random access memory . . . to store configuration information.” Ex. 1004, II-232. Chiricescu also describes using memory on-chip to “significantly improve[] the reconfiguration time,” explaining as follows:

The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application. Furthermore, a management scheme similar to one used to manage cache memory can be used to administer the configuration data.

Id. at II-234.

¹² Zavracky lists the same four inventors and “Appl. No. 531,177,” which corresponds to the application number cited by Chiricescu (“08-531-177”). Ex. 1003, codes (75), (21).

Figure 2 of Chiricescu follows:

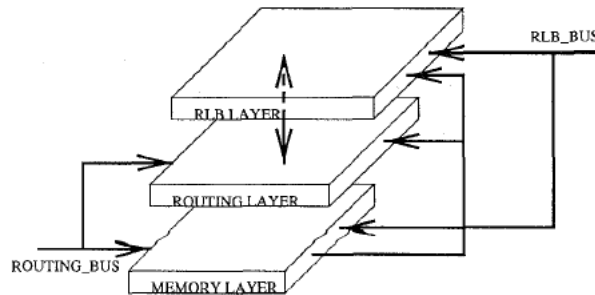


Figure 2. The layers of our 3-D FPGA architecture.

Chiricescu's Figure 2 above illustrates three layers in the 3-D-FPGA architecture, with a "routing and logic blocks" (RLB) layer arranged in a "sea-of-gates FPGA structure," a routing layer, and the aforementioned memory layer (to program/reconfigure the FPGA). *See* Ex. 1004, II-232–233. "[E]ach RLB is connected with the switch-boxes . . . in the routing layer (RL) by means of inter-layer vias. Each RLB can be configured to implement a D-type register and an arbitrary logic function of up to three variables." *Id.* at II-232. Figure 2 also depicts an external ROUTING_BUS to access the 3-D structure with external circuitry to provide configuration data. *Id.* at II-232 ("A routing bus provides the configuration information of the routing layer . . .").

3. Akasaka

Akasaka, titled "Three-Dimensional IC Trends" (1986), generally describes trends (several years before the 2001 effective filing date of the invention) in three-dimensional integrated stacked active layers. Ex. 1005, 1703. Akasaka states that "tens of thousands of via holes" allow for parallel processing in stacked 3-D chips, and the "via holes in 3-D ICs" decrease the interconnection length between IC die elements so that "the signal processing speed of the system will be greatly improved." *Id.* at 1705.

Akasaka further explains that “[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing” so that “twice the operating speed is possible in the best case of 3-D ICs.” *Id.*

Also, “input and output circuits . . . consume high electrical power.” Ex. 1005, 1705. However, “a 10-layer 3-D IC needs only one set of I/O circuits,” so “power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs.” *Id.*

Figure 4 of Akasaka follows:

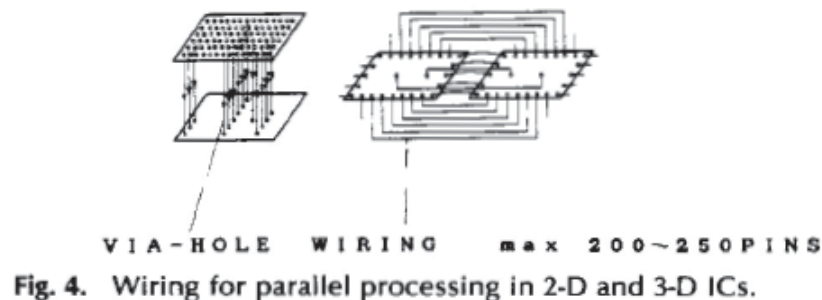


Figure 4 compares short via-hole connections in 3-D stacked chips with longer connections in 2-D side-by-side chips.

According to Akasaka, “[p]arallel processing is expected to be realized more easily in 3-D structures. Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or *vice versa*) through them.” Ex. 1005, 1705. As one example, Akasaka describes one 3-D chip as including “a video sensor on the top layer, then an A/D converter, ALU [(arithmetic logic unit)], memory, and CPU in the lower layers to realize and intelligent image processor in a multilayered 3-D structure.” *Id.*

4. *Petitioner’s Showing, Claims 1, 2, 4–6, 8–16, 23, 27, and 29*

Claim 1’s preamble recites “[a] processor module comprising.”

Petitioner relies on the combined teachings of Zavracky, Chiricescu, and

Akasaka, as discussed below, and provides evidence that Zavracky discloses a processor module, including a programmable array, memory (RAM), and microprocessor as part of a layered stack forming a 3-D device. *See* Pet. 23 (reproducing Ex. 1003, 5:19–20, 5:21–23, 12:12–38, Figs. 12–13; citing Ex. 1002 ¶¶ 282–288). Zavracky states that “[e]ach circuit layer can be fabricated in a separate wafer . . . and then transferred onto the layered structure and interconnected.” Ex. 1003, code (57).

Claim 1 recites limitation [1.1], “at least a first integrated circuit element including a programmable array that is programmable as a processing element.” *See* Pet. 24. Petitioner contends that the combined teachings of Zavracky and Chiricescu render the limitation obvious. *Id.* Petitioner relies on Zavracky’s “programmable logic array 802,” and notes that Zavracky states “[t]he array can be formed in any of the layers of a multilayer structure as described elsewhere herein.” *Id.* at 25 (quoting Ex. 1003, 12:28–38).¹³ Even if Zavracky does not disclose “a programmable array . . . programmable as a processing element,” Petitioner contends that “Chiricescu teaches reconfiguring the FPGA as such a processing element wherein the ‘FPGA is reconfigured from performing AxB to AxC or vice versa.’” *Id.* at 26–27 (quoting Ex. 1002 ¶ 303 (citing Ex. 1004, 234 (the “example shown is the multiplication of a 4-bit

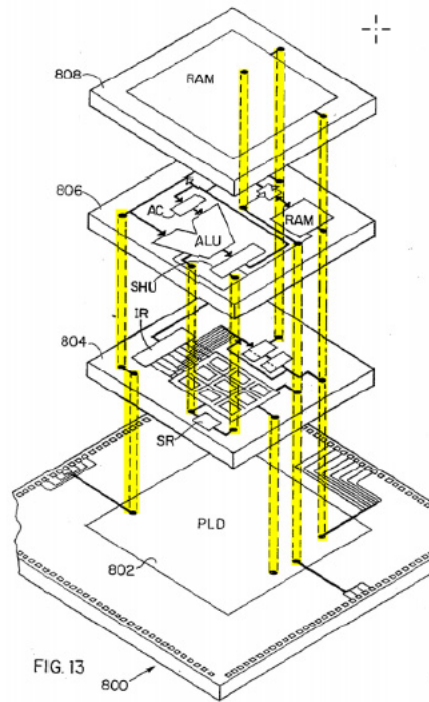
¹³ Referring to its analysis of claim 2, Petitioner contends that “the POSITA would have understood Zavracky to be describing a programmable array called a field **programmable** gate **array** (FPGA), which provides the programmable array element.” *See* Pet. 25 n.2 (citing Ex. 1002 ¶¶ 293–299), 34 (contending, *inter alia*, that “Chiricescu literally describes Zavracky as teaching technology ‘to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip.’” (quoting Ex. 1004, II-232)).

variable”)). Petitioner contends that adding such logic to an FPGA would have been obvious because it can be “quickly reconfigured” according to one of Chiricescu’s key features. *See id.* at 26 (citing Ex. 1004, II-233–34).

Petitioner also contends that in view of Akasaka, it would have been obvious to modify Zavracky’s programmable array to perform different types of processing, including math calculations, signal processing, or image processing. *Id.* at 27 (citing Ex. 1005, 1704–05, 1707, 1709; Ex. 1002 ¶¶ 229, 235 (citing Ex. 1048; Ex. 1021)). Petitioner adds that an artisan or ordinary skill would have been motivated to employ Akasaka’s teachings with Zavracky’s stacks for various reasons, including predictably providing multiple distributed contact points and parallel processing to implement a common data memory and cache memory system, and generally to increase bandwidth and processing speed. *See id.* at 20–22 (citing Ex. 1002 ¶¶ 233, 235, 237–239; Ex. 1005, 1705, 1713, Fig. 25).

Claim 1 recites elements [1.2] “at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element” and [1.3]: “wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements.”

Petitioner’s annotated version of Zavracky’s Figure 13 depicts stacked functional elements and the coupled contact points relied upon by Petitioner (Pet. 28):



Zavracky's Figure 13 above as annotated by Petitioner portrays (highlighted) inter-layer via connections (buses), one or more second integrated circuit (IC) functional elements (memory 808 (RAM) die, and microprocessor dies 804 and 806), stacked with "programmable logic array 802." *See* Pet. 27–29.

Petitioner provides evidence that "Zavracky teaches that 'openings or via holes'. . . 'can be placed anywhere on the die' of various functional elements, such that the connections 'are not limited to placement on the outer periphery'." *See* Pet. 30–31 (quoting or citing Ex. 1003, 6:43–47, 13:43–46, 14:56–63).

Petitioner quotes Zavracky as teaching vertically stacked and interconnected circuit element layers:

One significant aspect in the formation of three-dimensional circuits involves interconnecting the layered devices. . . . Via holes are formed through the upper contact areas to gain access to the lower contact areas. . . . **Electrical contact** between the

upper and lower devices is made by filling the via holes 1022 with an electrically conductive material . . . [.]

Pet. 28 (quoting Ex. 1003, 14:51–63). Petitioner points to Zavracky’s teaching that “[i]nstead of running buses along the surface of the wafer, many of these run in a vertical direction (the third dimension) between functional blocks freeing up significant real estate for active circuitry.” *See id.* (quoting Ex. 1003, 2:48–53).

Petitioner relies on similar teachings in Akasaka: “Akasaka further teaches the contact points are distributed throughout the surfaces of said functional elements, including through the ‘tens of thousands of via holes.’” Pet. 31 (quoting Ex. 1004, 1705). Petitioner quotes Akasaka: “Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or vice versa) through them.” *Id.* at 30 (quoting Ex. 1004, 1705). Petitioner further notes that in Akasaka, “[t]he contact points on the surface of the IC functional elements are created by ‘etching [the] via holes.’” *Id.* (citing Ex. 1004, 1707; citing Ex. 1002 ¶¶ 327–332).

Petitioner provides several reasons to combine the reference teachings to suggest providing numerous via holes between stacked dies or chips. *See* Pet. 18–22. As an example, Petitioner points out that Akasaka teaches that “‘tens of thousands of via holes’ *permit parallel processing*, and that use of the ‘via holes in 3-D ICs’ *shortens the interconnection length* between IC die elements so that ‘the *signal processing speed of the system will be greatly improved.*’” *Id.* at 18 (emphasis added) (quoting Ex. 1004, 1705).

Petitioner also points out that “Chiricescu . . . explicitly references and uses the interconnections of Zavracky.” Pet. 18–19 (*see supra* § II.D.2 (noting the explicit citation to and description of Zavracky in Chiricescu)).

Petitioner contends that an artisan of ordinary skill would have understood that combining Zavracky's electrically coupled stacked dies with Chiricescu's teachings of stacked memory for reconfiguring the FPGA (*see* limitation [1.4] below) would significantly improve the reconfiguration time of the FPGA. *See id.* at 18 (citing Ex. 1002 ¶¶ 221–228; Ex. 1004, II-234; Ex. 1003, 5:65–66; Ex. 1020, 2; Ex. 1055 ¶ 14; Ex. 1040, 317). Petitioner adds that an artisan of ordinary skill would have enhanced and expanded Zavracky's programmable logic device within its co-stacked microprocessors and memories to include image and signal processing tasks as Chiricescu's suggests by teaching the use of FPGAs to implement arbitrary logic functions. *See id.* at 19 (citing Ex. 1002 ¶¶ 229–30; Ex. 1005, 1705; Ex. 1003, 12:25–30; Ex. 1004, II-232; Ex. 1058, 41; Ex. 1048).

Petitioner also contends that it was “a predictable advantage and also suggested by Akasaka itself that applying Akasaka's distributed contact points, e.g., in the 3-D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity.” Pet. 20 (citing Ex. 1002 ¶¶ 233; Ex. 1005, 1705). Petitioner adds that “Zavracky and Chiricescu . . . invited such a combination.” *Id.* (citing Ex. 1003, 6:43–47 (“connections . . . can be placed anywhere on the die”); Ex. 1004, 232 (similar)).

Petitioner further reasons as follows:

the POSITA knew of the need for replicated “common data memory” in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence. Ex. 1002 ¶236 (citing Ex. 1034, 466–469; Ex. 1005, 1713 & Fig. 25). *That structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky.* Ex. 1002 ¶237. A POSITA thus would have been motivated to seek out Akasaka's

distributed contact points in order to build a “common data memory.” The POSITA’s background knowledge, including prior art successes, would have suggested success in this combination. *Id.* (citing Ex. 1005, Ex. 1021).

Pet. 21 (emphasis added). At the cited passage of Dr. Franzon’s declaration, Dr. Franzon further explains that the common data memory “still obtain[s] the speed and cost advantages of having an FPGA-based stack (e.g., the FPGA being faster than the software running on a microprocessor, and cheaper than an ASIC).” Ex. 1002 ¶ 237.¹⁴ Dr. Franzon also explains that “the POSITA would have known that the more densely connected communication structure of Akasaka would enable desirable uses of the Zavracky-Chiricescu 3D chip stack.” *Id.* ¶ 236.

Claim 1 also recites limitation [1.4]: “wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.” Petitioner relies partly on its showings above with respect to the second integrated circuit in limitations [1.2] and [1.3], which include Zavracky’s memory array in the stack connected via multiple via connection points. *See* Pet. 32 (citing Ex. 1003, 11:63–65 (“memory may be stacked on top of the multi-layer microprocessor.”), 12:15–28 (“random access memory array [with] buses run vertical through the stack”), 12:33–35, Figs. 10, 12, 13 (showing RAM memory 808)).

¹⁴ In addition to speed, Dr. Franzon explains that the common data memory employs multi-processor cache coherence in a stacked memory processor design as Akasaka discloses to ensure each shared memory obtains the same updated data that the system broadcasts over the parallel bus. *See* Ex. 1002 ¶ 236 (discussing Ex. 1005, 1713, Fig. 25; citing Ex. 1034, 466–469).

Petitioner adds the RAM “cache memory” array teachings from Chiricescu further to address the acceleration limitation in limitation [1.4]:

Chiricescu observes that “[t]he main bottleneck in the implementation of a high performance configurable computing machine is the high configuration time of an FPGA.” Ex. 1004 at II-232. This bottlenecking problem is caused in part by having to load configuration data from off-chip memory. Chiricescu’s proposed solution used a “memory layer” where the “random access memory is provided to store configuration information.” Ex. 1004 at II-232. Rather than having to go “off-chip” each time to load the FPGA reconfiguration data (i.e., load such external memory references each time the data is referenced), Chiricescu’s random access memory (i.e., a memory array) acts as a “cache memory” for that reconfiguration data, accelerating access to those external memory references. Ex. 1004, II-234. Therefore, when the FPGA (i.e., the processing element) needs to be reconfigured with new data, access to that data is accelerated by already having been loaded into the memory array. Ex. 1004, II-234. Therefore, the Zavracky-Chiricescu-Akasaka Combination, which includes Chiricescu’s FPGA and memory, provides this claim element. Ex. 1002 ¶¶304–307.

Pet. 32–33. As summarized above, Petitioner relies on multiple reasons for combining the references, including to increase processing speed by stacking chips with multiple parallel via connections to allow for parallel processing. *See* Pet. 8–9 (citing Bertin (Ex. 1025) as teaching “a stack of chips . . . to minimize latency between the device and chips and to maximize bandwidth” (citing Ex. 1025, 7:18–22, Fig. 22; Ex. 1001 ¶¶ 41–43), 12 (“It was well known that ‘interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,’ and that ‘wide buses are very desirable’ and were made possible by 3-D stacking.” (citing Ex. 1020, 2–3; Ex. 1002 ¶¶ 53–57)), 18 (“Akasaka further explains that ‘shorter interconnection delay time and parallel processing’

means that the processing of data between layers is accelerated such that “twice the operating speed is possible in the best case of 3-D ICs.” (quoting Ex. 1005, 1705)), 20 (“[I]t was a predictable advantage and also suggested by Akasaka itself that applying Akasaka’s distributed contact points, e.g., in the 3D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity.” (citing Ex. 1002 ¶ 233 as quoting Ex. 1005, 1705)), 18–22 (listing other reasons to combine), 60 (“The POSITA would have known (as Zavracky notes) that multiprocessor systems were needed for ‘parallel processing applications,’ for example, ‘signal processing applications.’” (citing Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶ 258)).

Claim 2 depends from claim 1 and recites “[t]he processor module of claim 1 wherein said programmable array of said first integrated circuit die element comprises an FPGA.” Petitioner generally refers to the “[t]he Zavracky-Chiricescu-Akasaka Combination” as it does for claim 1. *See* Pet. 34–35. Citing the testimony of Dr. Franzon and other evidence, Petitioner relies on Zavracky’s PLD (programmable logic device) 802 at the bottom of the stack in Figure 13 as an FPGA. *Id.* at 29–31 (citing Ex. 1002 ¶¶ 292–297; Ex. 1035, 1:29–30; Ex. 1036, 4:1–9; Ex. 1037, 1:13–22; Ex. 1038, code (57) (describing “transistors of a programmable logic device (PLD), such as a field programmable gate array (FPGA)”).

Petitioner relies on other teachings, including Chiricescu’s teachings, including its “sea-of-gates” FPGA layer, and the knowledge of an artisan of ordinary skill, to show that Zavracky’s PLD is or at least suggests an FPGA based on Chiricescu’s teachings. *See* Pet. 30–31 (citing 1002 ¶¶ 294–297; Ex. 1004, II-232; Ex. 1040; Ex. 1051). Petitioner also generally relies on

reasons for combining the references as outlined above with respect to claim 1 to suggest modifying Zavracky's 3-D stack (memory, processor, FPGA) based on Chiricescu's layer/stack teachings (FPGA, memory). *See id.* at 34–35 (citing Pet. §§ VII.A.2, A.4). Petitioner also notes that Chiricescu specifically describes Zavracky's teachings (*see supra* § II.D.2) as useful for providing 3-D FPGA stacks. *See id.* at 34 (“Chiricescu literally describes Zavracky as teaching technology ‘to build 3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip’” (quoting Ex. 1004, II-232)).

Claim 4 depends from claim 1 and recites “[t]he processor module of claim 1 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.” Petitioner relies on its analysis of claims 1 and 2, and explains that “the Zavracky-Chiricescu-Akasaka Combination teaches the stacking of microprocessor and FPGA functional elements, but it also teaches that the memory and FPGA functional elements, are ‘stacked with and electrically coupled to’ each other, readily providing this element.” Pet. 35. Petitioner alternatively relies on “other ways” that Zavracky teaches this element, pointing out that the “‘third integrated circuit functional element’ is not limited to a particular function in this claim.” *Id.* As such, Petitioner relies on Zavracky's disclosure of multilayer electrically coupled stacks, including those illustrated in Figures 10, 12, and 13. *Id.* (citing Ex. 1003, Fig. 10, 11:63–65 (“memory may be stacked on top of the multi-layer microprocessor”), Fig. 12, 12:15–28 (“stacked microprocessor and random access memory array [with] buses run vertical through the stack”), Fig. 13, 12:33–35

(“microprocessor [stacked and electrically coupled] with random access memory”); Ex. 1002 ¶¶ 313–326).

Independent claim 5 is a system claim. As Petitioner contends, “[c]aim 5 takes limitations from claim 1 and combines them with a generic processor and memory.” Pet. 36. Specifically, claim 5 recites “[a] reconfigurable computer system comprising: a processor; a memory;” and “at least one processor module” that materially recites the same limitations as the “processor module” of claim 1. The processor module of claim 1 reads on the “Zavracky-Chiricescu-Akasaka Combination” as determined above. Other than at most implying some type of electrical connection through the recitation of “a reconfigurable computer system comprising” in the preamble, claim 5 does not specify any electrical communication between the processor, memory, and “processor module.”

Petitioner contends that “Zavracky-Chiricescu-Akasaka Combination in further combination with [general knowledge of the POSITA] renders obvious claim 5.” Pet. 36. Petitioner explains that the “the Zavracky-Chiricescu-Akasaka Combination teaches the use of numerous microprocessors and numerous memories – any of which can satisfy the additional requirement for one more processor and one more memory in claim 5, and indeed, the teachings of Figure 13 already shows such a reconfigurable computer system.” *Id.* “Beyond this,” Patent Owner contends that a person of ordinary skill would have known to connect an FPGA of the Zavracky-Chiricescu-Akasaka Combination in a system with memory and a processor as evidenced by admissions in the ’951 patent, including prior art Figure 1, which shows a “prior art ‘MAPTM’ element . . . taught to ‘comprise a field programmable gate array ‘FPGA’ [and] read

only memory.”” *Id.* at 36–37 (quoting Ex. 1001, 3:22–24; citing *id.* at Fig. 1). Petitioner points out that admitted prior art Figure 1 is one example that evidences the general knowledge of an artisan of ordinary skill, and “[t]he general knowledge of the POSITA would have other examples of reconfigurable computer systems with a processor, memory, and processor module.” *Id.* at 37 (citing Ex. 1002 ¶¶ 267–73, 289; Ex. 1026).¹⁵

Petitioner points out that admitted prior art Figure 1 shows microprocessor 12 and system memory 16 coupled electrically with the MAPTM (which includes an FPGA). Pet. 37 (annotating Ex. 1001, Fig. 1). Petitioner asserts that it would have been obvious to employ the Zavracky-Chiricescu-Akasaka 3-D stack in a system with processor and memory in order to configure the FPGA using off-chip resources during start-up with a reasonable expectation of success where such systems were well-known. *See id.* at 37–39 (citing Ex. 1003, 12:37; Ex. 1002 ¶¶ 272–73; Ex. 1004, II-234 (describing “during the initiation phase of the application . . . loading configuration data . . . from memory off-chip”).

Claim 6 depends from claim 5 and recites “the computer system processor module of claim 5 wherein said third integrated circuit die element comprises a memory.” Petitioner points to its analysis of claim 2 to address claim 6. Pet. 39. Petitioner’s analysis of claim 2 includes an annotated version of Zavracky’s Figure 13, which depicts at least three integrated

¹⁵ In other words, the admitted prior art evidences the knowledge of the ordinary artisan and does not form the “basis” of the rejection. *Cf. Apple Inc. v. Qualcomm Inc.*, 2022 WL 288013, slip op. at *5 (Fed. Cir. Feb. 1, 2022) (holding that that applicant admitted prior art (AAPA) may not form the “basis of a ground in an *inter partes* review because it is not contained in a document that is a prior art patent or prior art printed publication.”).

circuit layers, including memory, a processor, and RAM (random access memory 806). *Id.* at 33.

Claim 8 depends from claim 5 and recites “[t]he computer system of claim 5 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.” Petitioner relies on its analysis of claim 4 to address claim 8. Pet. 39.

Claim 9 depends from claim 8 and recites “[t]he computer system of claim 8 wherein said third integrated circuit functional element comprises a memory.” Petitioner refers to its analysis of claims 1 and 4 to address claim 9. Pet. 40. Petitioner also explains that “Zavracky . . . teaches the POSITA an embodiment where multiple IC functional elements, such as the claimed second and third elements, comprise memory.” *Id.* (citing Ex. 1002 ¶¶ 318, 322). Petitioner quotes Zavracky as teaching that “[t]his configuration lends itself well to use in signal processing applications.” *Id.* (quoting Ex. 1003, 12:27–28).

Independent claim 10 is materially similar to claim 1 but includes at least a third “integrated circuit functional element” in addition to the at least first and second integrated circuit functional elements, with the three functional elements stacked and electrically coupled (without requiring a number of contact points distributed throughout the surfaces of the functional elements and extending through a thickness thereof as recited in claim 1). The three functional elements include a programmable array, processor, and memory. Petitioner primarily relies on its showing for claims 1, 4, and 9 to address claim 10. Pet. 40–42. Referring to, and similar to, its analysis of claim 1, Petitioner explains generally that “Zavracky’s 3D stack

includes multiple IC ‘functional elements’,” including microprocessor in relation to Figures 12 and 13. *See id.* at 41. Similarly, in its analysis of claim 4, Petitioner states that “Zavracky, for example, describes stacks with at least three layers wherein memory and microprocessor functional elements are stacked and electrically coupled.” *Id.* at 35–36 (citing Ex. 1003, Fig. 10, 11:63–65 (“memory may be stacked on top of the multi-layer microprocessor”), Fig. 13 (showing stacked RAM, microprocessor, and PLD/FPGA layers)).

Dependent claims 11–15 recite materially the same added limitations addressed above in connection with claims 1, 2, 4, and 10. Petitioner refers to its showing for the latter claims to address claims 11–15. Pet. 43–44.

Independent claim 16 is materially similar to claim 1 but broader, because while, similar to claim 1, it recites “a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element wherein said memory array is functional to accelerate external memory references to the processing element,” it does not specifically recite “electrically coupl[ing] by a number of contact points distributed throughout the surfaces of said functional elements,” as claim 1 does. Petitioner primarily relies on its showing for claim 1 to address claim 16. Pet. 44–45.

Independent claim 23 is materially the same as claim 1, with claim 1 reciting a “processor module” in its preamble and a programmable array in its body, and claim 23 reciting a “programmable array” in its preamble and reciting an FPGA in its body, with other differences with respect to coupling that Petitioner’s showing for claim 1 addresses. Petitioner primarily relies on its showing for claims 1 and 16 to address claim 23. Pet. 49–50.

Dependent claim 27 depends from independent claim 23 and recites “at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.” Dependent claim 29 depends from claim 27 and recites “wherein said third integrated circuit functional element includes an I/O controller.”

To address claim 27, Petitioner relies on its analysis of claim 4. Pet. 50. To address claim 29, Petitioner relies on Zavracky’s “‘controller’ as controlling connections ‘to and from the common data bus’ and containing ‘arbitration logic, hosted in the controller [run] in accordance with [a] bus arbitration protocol.’” *Id.* at 51 (quoting Ex. 1003, 5:54–60). According further to Petitioner, Zavracky’s Figure 1 and Figure 13 illustrate the same or a similar controller, and Zavracky discloses a bus controller that arbitrates logic under a bus arbitration protocol to communicate with off-chip resources as “a third IC functional element.” *See id.* at 51–52 (citing Ex. 1002 ¶¶ 324–325; Ex. 1003, 6:58–60). Petitioner alternatively relies on another controller in Zavracky that provides communication protocols between microprocessor and peripheral devices, and contends that “Zavracky teaches that such a programmable I/O controller ‘can be formed in any of the layers of a multilayer structure as described elsewhere herein.’” *Id.* at 52 (quoting Ex. 1003, 12:28–38; citing Ex. 1002 ¶¶ 325–326).

We adopt and incorporate Petitioner’s showing for claims 1, 2, 4–6, 8–16, 23, 27, and 29, as presented in the Petition and summarized above, as our own. *See* Pet. 7–12, 14–52.

5. *Arguments with Respect to Alleged Obviousness Based on Zavracky, Chiricescu, and Akasaka*

Patent Owner does not argue any of claims 1, 2, 4–6, 8–16, 23, 27, and 29 individually, but groups various claims together in separate arguments, as discussed below. Sections below address claims 17–22, 25, 26, and 27, although Patent Owner groups some of these claims together with claims 1, 2, 4–6, 8–16, 23, 27, and 29 in generic arguments or more specific arguments. We address some of the more generic arguments in this section and other more specific arguments below. *See infra* §§ II.D.6–7; II.E–G.

Patent Owner argues that “[t]he *Zavracky-Chiricescu-Akasaka* combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, including a “memory array [that] is functional to accelerate external memory references to said processing element.” PO Resp. 19 (listing claims 1, 5, 10, 16, and 23). *See infra* §§ II.4 (analyzing claims 5, 10, 16, and 23, which materially track the limitations of claim 1 based on the issues raised herein). Claims 1, 5, 10, 16, and 23 do not recite die elements, so Patent Owner’s argument in that respect is not clear.

In any event, on one hand, Patent Owner admits that “[t]he ’951 Patent provides accelerated external memory references due to its technique of stacking a programmable array with a memory die using through-silicon vias (TSVs).” *Id.* On the other hand, Patent Owner contends that “it is not simply stacking of a memory die with a programmable array that accelerates the programmable array’s access to memory. . . . [r]ather, as the claims themselves require, it is the structure provided ***within the memory array*** (i.e. the [WCDP] disclosed in the ’951 Patent) that is responsible for accelerating

the programmable array's accelerated external memory references.” PO Resp. 20. The latter argument is a claim construction argument, which we discuss above, and it is unavailing for the reasons noted. *Supra* § II.C (Claim Construction)).

Similarly, as also discussed above (§ II.C), Patent Owner argues that the inventors solved the problem of “loading configuration data through a typical, relatively narrow configuration data port [which] led to unacceptably long reconfiguration times,” by “stacking a memory die with a programmable array die” and “interconnecting” them “with a ‘wide configuration data port’ that employs through-silicon contacts, with the potential for even further acceleration where the memory die is ‘tri-ported.’” PO Resp. 20 (citing Ex. 1001, 5:18–25). It is not clear how this argument addresses Petitioner’s showing or a claim limitation. As summarized above and further below, Petitioner shows how the combined teachings of Zavracky, Chiricescu, and Akasaka satisfy the adopted claim construction, namely “a number of vertical contacts distributed throughout the surface of and traversing the memory die in a vertical direction (vias) to allow multiple short paths for data transfer between the memory array/memory and processing element/programmable array.” *See supra* § II.C.

Patent Owner also argues that “Petitioner’s expert admits” in his deposition testimony that “Chiricescu’s ‘RLB BUS’ that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the ’951 Patent.” *Id.* at 21 (citing Ex. 2012, 80:12–17 (“That memory would be narrower because that’s the structure of memory, is you access in DRAM; for example, you wouldn’t have thousands of bits wide access to the DRAM in a normal memory structure in this time frame.”))). According to

Patent Owner, “even though Chiricescu discloses stacking a memory layer with an RLB, its narrow configuration data port still loads configuration data ‘in a byte serial fashion and must configure the cells sequentially.’” *Id.* (citing Ex. 1001, 4:55–60; Ex. 2011 ¶ 57).

As discussed further below, Dr. Zavracky does not admit that Chiricescu describes a narrow port between a memory layer and the FPGA/RLB layer. *See* Reply 11 (explaining that Dr. Zavracky’s testimony relates to narrow ports for loading data from an *external* (off-chip) memory source to the FPGA module) (citing Ex. 2012, 80:10–22)). There is no credible evidence to support the argument that Chiricescu transfers data from its on-chip memory layer to its RLB (“sea-of-gates”) FPGA layer over a narrow data port or in byte-serial fashion. *See* Ex. 1004, II-232, Fig. 2. Dr. Sourì does not cite to any evidence in Chiricescu to support the testimony that “as Dr. Franzon acknowledges, *Chiricescu* discloses only a narrow configuration data port between the RLB and memory layers.” Ex. 2011 ¶ 57 (citing Ex. 2012, 80:10–22). Dr. Zavracky credibly testifies that he “did not ‘admit’ that ‘Chiricescu’s RLB BUS that interconnects the memory and RLB layers is the same type of narrow data port distinguished in the [challenged patents].’” *See* Ex. 1070 ¶ 68 (testifying “[t]hat is factually an incorrect statement about Chiricescu - Dr. Sourì’s claim about Chiricescu is not true, and his claim about my testimony is not true”). And in any event, as discussed above and further below, Petitioner relies on the combined teachings of the references as suggesting a large number of vias extending throughout the die areas in contrast to any narrow data port.

Patent Owner also argues that “Petitioner has not demonstrated that its combination of references ‘accelerates external memory references to said

processing element’ over the baseline of the relatively narrow configuration port distinguished in the ’951 Patent (and taught in *Chiricescu*).” PO Resp. 22. Patent Owner also argues that “[b]ecause Petitioner fails even to allege that any aspect of *Chiricescu*’s ‘memory layer’ itself is functional to accelerate external memory references, it has not even raised a *prima facie* case of obviousness.” *Id.* at 23 (citing Ex. 2011 ¶ 59).

These arguments do not address Petitioner’s reliance on multiple vertical vias in the stacked memory chip structure of Zavracky, as modified by the combined teachings of *Chiricescu* and Akasaka, to accommodate the memory array operating as a cache or other memory to accelerate the loading of the reconfiguration data. *See* Pet. 17–22, 27–33. Petitioner notes, for example, that “Akasaka teaches that these ‘tens of thousands of via holes’ permit parallel processing, and that use of the ‘via holes in 3-D ICs’ shortens the interconnection length between IC die elements so that ‘the signal processing speed of the system will be greatly improved.’” *Id.* at 18 (quoting Ex. 1705, 5). Petitioner also states that “Akasaka further explains that ‘shorter interconnection delay time and parallel processing’ means that the processing of data between layers is accelerated such that ‘*twice the operating speed is possible* in the best case of 3-D ICs.’” *Id.* (emphasis added) (quoting Ex. 1705, 5). Petitioner also relies on an article by Dr. Franzon and states that “the POSITA in 2001 was also aware of the many advantages of stacking IC die elements, including accelerated processing of data as compared to 2-D devices.” *Id.* at 12 (citing Ex. 1020, 2–3; Ex. 1002 ¶¶ 53–57). Petitioner also relies on vias in a “vertical bus” connecting each of Zavracky’s layers, including random access memory array layers, to

microprocessor layers. *Id.* at 32 (citing Ex. 1003, 11:63–65, 12:15–28, 12:33–35, Figs. 12, 13).

Contrary to Patent Owner’s claim construction arguments, apart from numerous vias that the parties agree are part of a WCDP, none of the challenged claims require other aspects of a WCDP and/or buffer cells under our claim construction, and the specification does not describe Figure 5’s WCDP (depicted as black box) as part of a memory array. *See supra* § II.C; Ex. 1001, Fig. 5. As Petitioner persuasively argues and as summarized above, the Petition relies on the combined teachings of Zavracky, Chiricescu, and Akasaka to teach the “functional to accelerate clause.” *See* Reply 4–12. As Petitioner also persuasively argues, even if the claims require other structure of a WCDP, according to Patent Owner’s expert in IPR2020-01020, IPR2020-01021, and IPR2020-01022, a “**configuration data port . . . is . . . just a data port used for configuration . . . And data port is just an interface to send data** from one place to another.” Reply 9 (emphasis by Petitioner) (quoting Ex. 1075, 163:8–21). “And ‘the reason it’s a very wide configuration data port is because it has **a lot of connections** through these TSVs between the memory die and the FPGA die.’” *Id.* (quoting Ex. 1075, 157:23–158:3).

In other words, under Petitioner’s persuasive showing, even if the challenged claims require some aspects of a WCDP, the combined teachings meet the claims for the reasons noted. Petitioner persuasively shows that the Zavracky-Chiricescu-Akasaka 3-D module uses numerous vias throughout the dies to transfer data *between* the dies—i.e., functional to accelerate all manner of data and signals in parallel (like a WCDP). *See, e.g.*, Pet. 18 (showing that Akasaka teaches that “‘tens of thousands of via holes’ permit

parallel processing” by utilizing the many interconnections; as a result of this parallel processing, “the signal processing speed of the system will be greatly improved”; and due to “shorter interconnection delay time and parallel processing” made possible from the area-wide interconnects, the processing of data between layers is accelerated such that “twice the operating speed is possible in the best case of 3-D ICs” (quoting Ex. 1005, 1705)), 20 (arguing that “it was a predictable advantage and also suggested by Akasaka itself that applying Akasaka’s distributed contact points, e.g., in the 3-D stacks of Zavracky or Chiricescu, would increase bandwidth and processing speed through better parallelism and increased connectivity” (citing Ex. 1002 ¶ 233; Ex. 1005, 1705)). Petitioner also shows that “[i]t was well known that ‘interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems,’ and that ‘*wide buses are very desirable*’ and were made possible by 3-D stacking.” *Id.* at 12 (emphasis added) (quoting Ex. 1020, 12).

Patent Owner argues that “in *Akasaka*, the 3-D chip design that uses vertical interconnections is only mentioned for a flip-chip design and a monolithic design, which means it is fabricated as a single piece of silicon with multiple layers.” PO Resp. 16. Patent Owner argues that “Akasaka explains that among the expected improvements are the use of ‘[s]everal thousands or tens of thousands of via holes’ in monolithic chips to take advantage of parallel processing.” *Id.* at 17 (quoting Ex. 1005, 1705). According to Patent Owner, Akasaka’s “flip-chip design is limited . . . in that ‘the number of connections are restricted by reliability and bump size constraints.’” *Id.* at 16 (quoting Ex. 1005, 1704).

Contrary to these arguments, Akasaka states that with respect to flip chips, “the number of connections will be greatly increased by this technology.” Ex. 1005, 1704. Moreover, Akasaka refers to the flip chip structures in a section titled “3-D IC Structure.” *Id.* And contrary to Patent Owner’s arguments, Akasaka generally indicates that for all known “3-D structures” at the time, “[s]everal thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers or vice versa through them.” *Id.* at 1705; *see also* Reply 20 n. 6 (showing that 3-D die stacking with numerous chips was well-known known (citing Ex. 1002 ¶¶ 328, 332); *id.* at 21 n. 8 (persuasively showing that Patent Owner “describes Akasaka’s teachings inaccurately” (citing 1002 ¶¶ 233–239; Ex. 1070 ¶¶ 59–66); Ex. 1070 ¶¶ 60–61 (disputing Dr. Souris’s testimony and stating that Akasaka shows “vertical interconnections between multiple chips and other chip attachment mechanisms,” and testifying that “Akasaka does not limit its via fabrication teachings to two layers or a monolithic chip”); Ex. 1002 ¶ 238 (testifying that chip stacking was known and “[t]here were many references teaching stacked dies with thousands of distributed connections, including those discussed in my technology backgrounder above, Section V, and the papers in Section IX”). Akasaka also indicates that even in 1986, about five years before the 2001 date of the invention, artisans of ordinary skill would have mixed flip chip technology and monolithic technology to provide stacked layers: “Mixing of assembly technology with monolithic chip technology can also provide 4 layers or 6 layers from 2-layer or 3-layer stacked monolithic ICs, respectively.” Ex. 1005, 1713.

Therefore, Petitioner shows that the numerous via connections between the memory die and FPGA in the modified stack of Zavracky connect to the memory array to render the “memory array functional to accelerate memory references to the processing element,” as the challenged claims require. *See, e.g.*, Pet. 20–21 (showing that Akasaka’s numerous connections would have motivated a POSITA to replicate common data memory, and “increase bandwidth and processing speed through better parallelism and increased connectivity”); 32 (relying on Zavracky’s “random access memory array [with] buses run vertical through the stack” implemented as a cache memory according to Chiricescu’s teachings in order to accelerate access to memory references and reconfigure the FPGA (quoting Ex. 1004, 12:15–28; citing *id.* at 11:63–65, Figs. 12, 13; Ex. 1004, II-232)).

As indicated above, Petitioner also persuasively shows that Patent Owner “misrepresents Dr. Franzon’s testimony” regarding an alleged narrow port in Chiricescu. *See* Reply 11. As Petitioner persuasively argues, “Dr. Franzon’s cited testimony: (1) has nothing to do with Chiricescu; (2) was given in response to a question about Trimberger; and (3) was discussing the connection to “an **off-chip** memory.” *Id.* (citing Ex. 2012, 80:10–22).

Dr. Franzon’s cited deposition testimony supports Petitioner. Dr. Franzon’s cited deposition testimony refers to Trimberger in the context of “off-chip memory that loads in through the data port,” and Dr. Franzon testifies “a POSITA would interpret figure 5 [of the ’951 patent] as [including an undepicted] similar narrow structure on the left of the very wide configuration data port” to load data from an external source. *See* Ex. 2012, 80:3–22. In other words, Dr. Franzon’s testimony does not describe

Chiricescu's stacked memory layer as using a *narrow* port to transfer reconfiguration data to the RLB (with FPGA gates) layer from this "on-chip" memory within the 3-D stack. *See* Ex. 1004, Fig. 2; *supra* § II.D.2; Ex. 1070 ¶ 68 (refuting Dr. Souris's testimony and characterization with respect to Chiricescu and Dr. Franzon's testimony about Chiricescu).

As Petitioner also argues, Patent Owner's "'narrow data port' arguments are contrary to Chiricescu's teachings" and do not address the combined teachings of Chiricescu, Zavracky, and Akasaka. Reply 11 (citing PO Resp. 20–21). Petitioner notes that Zavracky describes "interconnects as being '*placed anywhere on the chip*' without restriction." *Id.* (emphasis added) (quoting Ex. 1004, 232). In addition, Petitioner notes that Chiricescu "discloses 'three separate layers with metal interconnects [including a "memory layer"] between them.'" *Id.* (quoting Ex. 1004, 232) (addition by Petitioner) (emphasis omitted). Vias running everywhere throughout the different stacked layers or dies, as Zavracky, Chiricescu, and Akasaka individually and collectively teach, distinguish over any alleged narrow port, and Petitioner provides well-known reasons for employing numerous vias of wide data ports, such as allowing for increased bandwidth and parallelism. *See* Pet. 12, 18, 20 (discussed and quoted above); Ex. 1001, 5:16–21 (describing "through-die array contacts 70 . . . routed up and down the stack in three dimensions" as "not known to be possible with any other currently available stacking techniques *since they all require the stacking contacts to be located on the periphery of the die*," so that by placing contacts throughout, "*cells that may be accessed within a specified time period is increased*") (emphasis added).

With respect to all challenged claims, Patent Owner also argues that “Petitioner and Dr. Franzon fail to explain how a POSITA would have integrated Akasaka’s thousands of distributed contact points with Zavracky-Chiricescu’s design to achieve the claimed 3-D processor modules and would have had a reasonable expectation of success in doing so.” PO Resp. 38 (citing Ex. 2011 ¶ 78). According to Patent Owner, “Petitioner and Dr. Franzon concede that *Zavracky* and *Chiricescu* both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical communications between functional blocks (such as memory elements, logic unit, etc.) of the multi-layer microprocessor.” *Id.* (citing Ex. 1003, 11:62–12:39; Ex. 1004, 1–2). According further to Patent Owner, “Dr. Franzon’s analysis, like Petitioner’s analysis, seems to say no more than that a POSITA would have understood that the references ***could be*** combined.” *Id.* at 40 (citing Ex. 1002 ¶ 239). Patent Owner also asserts that “[a]t the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language (“HDL”) algorithms, which must be considered.” *Id.* at 41 (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89).

Patent Owner’s arguments are unavailing. As discussed above, Petitioner persuasively relies on the knowledge of the artisan of ordinary skill and the combined teachings of Zavracky, Chiricescu, and Akasaka supported by specific reasons and rational underpinning to show how the combination teaches or suggests increasing the number of contact points or via holes for electrically coupling FPGA, memory, and processors together. Petitioner also shows the “why”—to allow for parallel data transfers, speed

increases, larger bandwidth, etc., all with a reasonable expectation of success.

As indicated above, Zavracky already specifically describes connecting several bus lines (depicting 4 in Fig. 13) from the FPGA/PLD to other circuits, including memory and a processor. *See* Pet. 23–24. Patent Owner contends that “Zavracky proposes using these vertical connections ‘for the same reasons any lines otherwise restricted to a single layer are used.’” PO Resp. 10 (quoting Ex.1003, 6:48–49). This argument supports Petitioner, because it shows that an artisan of ordinary skill easily would and could have re-routed connections of known circuitry using vias. Petitioner shows a number of other stacked dies or layers with multiple via connections, including Akasaka (Ex. 1005, Fig. 4), Franzon (Ex. 1020, Fig. 4), Koyanagi (Ex. 1021, Fig. 1(a)), and Alexander (Ex. 1028, Fig. 2(g)). *See* Pet. 31. As discussed further below, Trimberger (Ex. 1006) shows parallel loading by “*flash reconfiguring* all [100,000] bits in logic and interconnect array [i.e., an FPGA] . . . simultaneously from one memory plane.” *See infra* § II.E.1 (quoting Ex. 1006, 22).¹⁶

Patent Owner concedes Zavracky and Chiricescu each show how to connect “memory, logic, etc.” using “address and data buses,” albeit on what Patent Owner describes as “only a small number of interconnect paths.” PO Resp. 38 (“Zavracky and Chiricescu both disclose only a small number of interconnect paths (e.g., the address and data buses) that provide for vertical

¹⁶ Petitioner employs Trimberger to address challenged claim 25 as discussed further below (§ II.E), but it is further evidence of a reasonable expectation of success as it relates to connecting several thousands of bit lines in parallel.

communications between functional blocks (such as memory elements, logic unit, etc.) of the multi-layer microprocessor.”). But Patent Owner also agrees that the number of interconnects is not critical to the claimed invention. *See supra* § II.C (discussing Oral Hearing arguments); Tr. 49:1–9 (answering “yes, . . . if you have a very, . . . small FPGA, the number of bits can be . . . relatively smaller, but what’s critical is not the number of bits and . . . [i]t’s not necessarily the number of bits that’s in the configuration data port, but how they’re arranged”). In any event, Petitioner shows that a large number of vias would have been obvious in view of the combined teachings, to enhance speed, allow parallel processing and data transfer, minimize latency, and maximize bandwidth, as noted throughout this Final Written Decision.

Alleging a lack of a reasonable expectation of success, Patent Owner acknowledges that “[a]t the time of the invention, *a POSITA was aware* of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language (‘HDL’) algorithms.” PO Resp. 41 (emphasis added) (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89). Here, the challenged claims are broad and do not specify a minimal number of interconnections, FPGA size, or chip size that would even raise TSV congestion or other issues. The ’951 patent says nothing about interconnection issues or congestion. Even if such issues were a consideration and relevant to a reasonable expectation of success given the breadth of the challenged claims, as Petitioner persuasively argues, “[t]he supposed ‘TSV interconnection issues’ that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a

combination.” Reply 20 (citing Ex. 1070 ¶¶ 13–28 (Dr. Franzon addressing Dr. Souris’s testimony as to the purported TSV issues)).

For example, as Dr. Franzon credibly testifies,

even if routing congestion or TSV placement were an issue, Kim gives several solutions that would have been known to POSITA, such as to change the TSV “coarseness” or to “increase the chip area to address the placement and routing congestion caused by TSV insertion.” [Ex. 2014 (Kim), 85]. But again, the [’951] patent[] and claims are silent on any of these issues; Kim is at worst irrelevant, and at best would have actually encouraged the combination.

Ex. 1070 ¶ 26. With respect to alleged HDL (hardware description language) issues, Dr. Franzon also credibly testifies that

Alexander (Ex. 1009) has a whole section titled “Placement and Routing in 3D” (Ex. 1009, p. 256). Alexander names then-existing CAD tools that performed these functions, including DAGmap and Mondrian. Designing distributed 3D interconnects was a routine engineering problem by the time of the Huppenthal Patents, and not an impediment to reasonable expectation of success in making the Zavracky, Chiricescu, Akasaka combination.

Ex. 1070 ¶ 27.

Petitioner provides other evidence that at the time of the invention, an artisan of ordinary skill would have had a reasonable expectation of success in combining the references to arrive at multiple vias connecting circuits (including memory arrays) on stacked chips and to allow for parallel processing or data transfers. *See, e.g.*, Pet. 8–13 (discussing known wafer processing technology by artisans of ordinary skill supported by evidence (citing Ex. 1002 ¶¶ 47–51, 262–266; Ex. 1001, 2:29–35; 5:13–18; Ex. 1009, Fig. 2; Ex. 1020, 5, 9–12, Fig. 4; Ex. 1021, 17, Fig. 1(a); Ex. 1022; Ex. 1023, Fig. 4(b); Ex. 1025, code (57), 1:59–65, 2:11–13, Fig. 1; Ex. 1027,

code (57); Ex. 1030, 94; Ex. 1031, 70)), 28–29 (pointing to Zavracky’s memory as an example vertical integrated circuit on stacked dies connected by via connections including vertical buses “placed anywhere on the die” and providing evidence that “each of the programmable array, microprocessor, and memory are pairwise stacked with and electrically coupled with each other” (citing Ex. 1003, 2:7–8, 2:18–22, 2:27–35, 6:43–7:9, 10:8–21, 11:63–12:2, 12:13–39, 14:51–63, Fig. 13), 25–26 (further relying on Akasaka as teaching thousands of vias to connect upper and lower circuit layers (citing Ex. 1005, 1705, 1707; Ex. 1002 ¶¶ 327–332)).

Furthermore, the ’951 patent describes “recently available wafer processing techniques” including those developed by “Tru-Si Technologies,” indicating, for purposes of institution, that artisans of ordinary skill would have been aware of any such wafer processing techniques for forming vias at the time of the invention. *See* Ex. 1001, 2:19–40. Therefore, Petitioner persuasively shows ample evidence of a reasonable expectation of success.

In addition, as noted above, Patent Owner argued during the Oral Hearing that the number of contacts is not important, depending on the size of the FPGA, provided that the contacts allow for parallel processing. *See supra* § II.C (discussing Tr. 49:1–9 (Patent Owner arguing that the number of vias “could be as small as 32 bits . . . if you have a small FPGA, ... [and] [i]f you want to update something in parallel, you could update 32-bit with 32 bits,” further stating that “if you have a very . . . small FPGA, the number of bits can be . . . relatively smaller, but what’s critical is not the number of bits”). The challenged claims at issue here do not specify an FPGA size.

In any event, as summarized above, Petitioner provides persuasive motivation with a reasonable expectation of success to explain why a person of ordinary skill would have increased the number of vias using known techniques, relying on teachings that providing multiple vias in stacked chips using conventional via and metallization processing allowed for faster processing speeds and reconfiguration times, shorter latency, higher bandwidth, and parallel processing, with a known desire for wide buses. *See* Pet. 7–12, 18–22; Ex. 1002 ¶¶ 53–57; 212–239. Dr. Franzon also shows that the combined teachings of Zavracky and Chiricescu suggest “processing tasks . . . [in] co-stacked microprocessors and memories . . . as good applications for 3-D stacked chips that required parallel computation.” Ex. 1002 ¶ 229.

As Petitioner also persuasively notes, Zavracky does not limit the number of connections, contrary to Patent Owner’s arguments. For example, Petitioner quotes Zavracky as describing “**inter-layer connections** [that] provide for vertical communication. . . . [and] [s]uch connections can be placed **anywhere on the die** and therefore are not limited to placement on the outer periphery.” Reply 4–5 (emphasis by Petitioner) (quoting Ex. 1003, 6:43–47) (emphasis by Petitioner). Petitioner quotes Zavracky as teaching “buses run vertically through the stack by the use of inter-layer connectors” in describing Figures 12 and 13. *Id.* (quoting Ex. 1003, 12:24–26). Petitioner persuasively explains that “Zavracky visually shows a number of vertical contacts that traverse the memory die in the internal periphery of the die and provide contacts on the surface of the memory die, just as the Board’s construction requires.” *Id.* at 5–6 (annotating Ex. 1003, Figs. 12, 13).

Petitioner also persuasively relies on Zavracky's teaching that "this approach **accelerates** communication between the dies in the chip by way of "**smaller delays and higher speed** circuit performance." Reply 6 (emphasis by Petitioner) (quoting Ex. 1003, 3:4–14). Petitioner persuasively notes that Chiricescu describes Zavracky's teachings as "allow[ing] us" to build stacked circuit layers on a chip with "vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip." *See id.* (quoting Ex. 1004, 232). Petitioner also persuasively argues that Chiricescu teaches the recited "functional to accelerate" clauses, with "significantly **improved[d FPGA] reconfiguration time**" through its "interconnected layers, including a memory layer configured as a cache for fast access to 'configuration data . . . from memory off-chip.'" *Id.* at 6 (quoting Ex. 1004, 232) (emphasis by Petitioner). Other than disclosing an 8-bit configuration port as prior art with respect to Figure 3, the '951 patent does not specify how many via interconnections the claimed "accelerate" functionality requires. *See id.* at 2:56–3:2 (describing stacking an FPGA with a "memory die" "for the purpose of accelerating FPGA reconfiguration" and "for the purpose of accelerating external memory references" and stacking "a microprocessor, memory and FPGA . . . for the purpose of accelerating the sharing of data"), 5:20–21 (describing cache memory purpose of serving "its traditional role of fast access memory").

Patent Owner restricts Chiricescu teachings as suggesting only "the use of 'on-chip' memory to mitigate the time it takes to transfer configuration data from 'off-chip,' rather than making any use of Zavracky's die-area vertical interconnections to transfer configuration data from the 'on-chip' memory into the FPGA." *See* PO Resp. 29 (citing Ex. 1004, 1, 3).

Patent Owner also argues that “[n]either *Zavracky* nor *Chiricescu* even contemplate using die-area inter-layer vertical interconnections to move data between a programmable array and a memory, such as is recited in Claims 1, 5, 10, 16, 18, and 23.” *Id.* at 29 (citing Ex. 2011 ¶ 66). The record does not support this line of argument. As discussed above, *Zavracky*’s Figure 13 shows that *Zavracky* contemplates moving data on vertical buses between RAM memory 808 (and RAM memory on processor layer 806) and programmable array 802 (Ex. 1003, 12:29–39), and *Chiricescu*’s Figure 2 shows that *Chiricescu* contemplates moving data on “vertical metal interconnections (i.e., interlayer vias) placed anywhere on the chip” (based on *Chiricescu*’s characterization of *Zavracky*) between memory layer and the “sea of gates FPGA” RLB layer (Ex. 1004, II-232); *see also* Ex. 1004, II-232 § 1 (“Another feature of our architecture is that a layer of on-chip random access memory is provided to store configuration information.”).

Also, Petitioner shows persuasively that an artisan of ordinary skill would have recognized that speed improvement emanates largely from shorter interconnection distances and/or parallel processing using a large number of vias (as compared to long metal connections running on the same plane). *See* Reply 6 (arguing *Zavracky*’s “approach **accelerates** communication between the dies in the chip by way of ‘**smaller delays** and **higher speed** circuit performance’” (emphasis by Petitioner (quoting Ex. 1003, 3:4–14)), and arguing that “*Zavracky*’s short interior ‘inter-layer connectors’ to stacked ‘random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system.’ (emphasis by Petitioner (quoting 11:63–12:2)).

Patent Owner's observations support Petitioner. For example, asserting that "[t]he '951 Patent provides accelerated external memory references due to its technique of stacking a programmable array with a memory die using through silicon vias (TSVs)," Patent Owner quotes the '951 patent as providing "increased" "bandwidth" and providing the "traditional role of fast access memory." *See* PO Resp. 19–20 (quoting Ex. 1001, 5:18–28).

Patent Owner also argues that "[b]ecause Petitioner does not allege that any 'external memory references' occur in *Chiricescu* (let alone that such references are accelerated), Petitioner cannot have met its burden to establish that Claims 1, 5, 10, 16, and 23 and their dependents are obvious." PO Resp. 23. According to Patent Owner, "Petitioner misinterprets the term 'external memory references,' suggesting that this term too can be satisfied simply by storing a certain type of data in *Chiricescu*'s memory." *Id.* (citing Pet. 32–33; Ex. 1002 ¶ 307). Patent Owner also argues that "memory references are not data, but are instructions directed to a particular place memory address [sic] in memory." *Id.* (citing Ex. 2011 ¶ 60; Ex. 2015, 181; Ex. 2012, 49:11–50:1).

These arguments are unavailing. Dr. Souri's cited declaration testimony does not tie his opinion that "[a] skilled artisan understands that memory references are not data" to the limitations recited in claim 1, 5, 10, 16, and 23 as viewed in light of the '951 patent specification. *See* Ex. 2011 ¶ 60. In addition to citing the Dr. Franzon's deposition testimony, which does not support Dr. Souri as indicated above, Dr. Souri cites "Ex. 2015 at 181." This particular extrinsic evidence, which includes a single page out of what appears to be a text book, is not helpful because it does not have

anything to do with accelerating memory references, and it describes types of “operands,” which are not at issue in the ’951 patent. *See* Ex. 2015, 181 (“The third type of operand is a memory reference.”). In other words, Dr. Souri’s testimony is conclusory as it does not address how this extrinsic evidence relates to the recited “functional to accelerate external memory references” clause as recited in the challenged claims and in the context of the cache memory or reconfiguration scheme as set forth in the ’951 patent specification. *See* Ex. 2011 ¶ 60 (citing Ex. 2015, 181). Patent Owner and Dr. Souri also do not explain clearly how the cited deposition testimony of Dr. Franzon supports Patent Owner. *See* PO Resp. 23 (citing Ex. 2012, 49:11–50:1; Ex. 2011 ¶ 60); Ex. 2012, 49:11–50:1 (generally testifying that “Chiricescu’s FPGA processing element” is “agnostic” as “to what actually is stored in it”).

Petitioner persuasively shows that caching external memory references in a stacked cache memory satisfies the “functional to accelerate” limitations relative to loading them from off-chip (outside of the stack), because of “caching” *and* “the use of short electrical paths, or significantly increased number of connections,” including “Akasaka’s area-wide distributed interconnects.” *See* Reply 8 (citing Pet. 13–31, 44–47); *see also id.* at 12 (discussing hitting the cache with external memory references (citing Ex. 1002 ¶¶ 215–216; Ex. 2012, 42:9:14, 48:6–50:1)).

Petitioner also persuasively explains that even under Patent Owner’s narrow interpretation of “external memory references” as related to memory addresses, Chiricescu teaches that interpretation because the memory address references will “hit” the cache. *See* Reply 11–12 (citing Ex. 1002

¶¶ 215–216). Supporting Petitioner, Dr. Franzon persuasively testifies at the cited paragraphs of his declaration as follows:

215. . . . The POSITA would recognize that what Chiricescu is teaching is to use that memory as a “cache” By doing so, the FPGA’s external memory references . . . will be accelerated because [they] will “hit” in the “cache” and be returned from the on-chip memory without having to go off-chip.

216. Chiricescu is thus teaching to the POSITA to accelerate memory lookups that are directed to the external chip by sending them instead to the on-chip memory, perhaps keeping a relevant set of data to the application. This is what Chiricescu means when it says that “a management scheme similar to one used to manage cache memory can be used to administer the configuration data.”

Ex. 1002 ¶¶ 215–216; Reply 12 (quoting part of the same two paragraphs).

As Petitioner also persuasively argues, the ’951 patent does not limit “external memory references” in particular, but it does refer to cache memory and enhancing reconfiguration speed with such memory. *See* Reply 12 (citing Ex. 1001, 2:11, 2:25, 4:31, 4:57–58); Ex. 1001, 4:31–36 (referring to “cache memory 66” as serving its “traditional role of fast access memory,” and also including accessing by “both the microprocessor 64 and FPGA 68 with equal speed,” in the context of “reconfigurable computing systems”).

Patent Owner also argues that “[b]ecause the claims require a ‘*memory array* is functional to accelerate external memory references to said processing element,’ Petitioner’s focus on the type of data stored in the array misses the mark.” PO Resp. 23 (citing Ex. 2012, 43:13–44:3, 49:20–50:1). Contrary to this argument, as discussed above, Petitioner relies on a cache memory array as combined in a 3-D stack with short via connections, not the type of data. As discussed throughout this Final

Written Decision, the Petition persuasively relies on such short and numerous distributed vias as structure for the “functional to accelerate” clauses, because such structure provides shorter path delays and allows for increased bandwidth and parallel data transfer from a memory in the stack, including cache memory. *See supra* § II.D.3 (Akasaka’s parallel processing and multiple via teachings); Pet. 7–12, 18–22; Ex. 1002 ¶¶ 53–57, 212–239. Essentially, the cache memory relied upon by Petitioner carries all of these advantages because it is within Zavracky’s modified 3-D stack with the FPGA and microprocessor.¹⁷

¹⁷ Throughout its briefing, Patent Owner limits all “on-chip” advantages to a *single die* and confuses issues by arguing that even chips in the same stack are “off-chip” relative to each other, such that all “off-chip” vias are part of a “narrow” data port—even with thousands of vias connecting chips in the same stack as proposed by Petitioner. On the other hand, Petitioner, like Zavracky, generally refers to “off-chip resources” to refer to a resource *outside* of a *chip stack*. *See, e.g.*, Pet. 51 (“The data bus is used to ‘provide communication between logic units or between a logic unit and off-chip resources.’” (quoting Ex. 1003, 5:49–52)); Ex. 1003, 5:53–54 (“Paths which connect off-chip are routed to bonding pads 226 [Fig. 1], which are bonded to the chip carrier pins.”); Ex. 1070 ¶ 44 (Dr. Franzon noting that “Dr. Sourì apparently means ‘chip’ here as limited to a single die.”). Patent Owner exploits this difference of terminology usage to confound issues, characterizing, for example, Dr. Franzon’s testimony as follows: “Dr. Franzon’s testi[fies] that ‘*off-chip* access [*e.g., off-chip* memory separate from the FPGA die] can’t be, for example, 100,000 bits wide.” Sur-reply 9 (emphasis added) (second bracketed information by Patent Owner). As another example, Patent Owner argues that Petitioner “rel[ies] on Dr. Franzon’s discussion that thousands of interconnections for *off-chip* access of a 3D stacked structure is not feasible.” *Id.* (emphasis added (citing Reply 18)). This conflation is the opposite of Dr. Franzon’s testimony and Petitioner’s showing. The thrust of Dr. Franzon’s testimony and Petitioner’s showing is that numerous stacked via connections in a stack of chips (dies) or layers of a single chip are better (faster, shorter, less congested, etc.) than connections running on the same plane. *See, e.g.*,

In the Sur-reply, Patent Owner argues that “[t]he entire point of *Chiricescu* is that it achieves accelerated FPGA configuration by storing configuration data ‘on-chip’ so that it does not need to load configuration data from off-chip.” Sur-reply 5. Patent Owner also argues that “all off-chip connections are carried out through a typical narrow configuration data port, that suffers the same problems as the prior art distinguished in the ’951 Patent.” *Id.* Patent Owner then argues that “moving *Chiricescu*’s cache memory off-chip (i.e., into *Zavracky*’s 3-D stacked memory die) eliminates the benefit gained from moving the memory on-chip, [so] a POSITA would not have contradicted *Chiricescu*’s fundamental teachings to arrive at Petitioner’s proposed combination.” *Id.* at 5–6.

These arguments mischaracterize Petitioner’s showing and confuse the issues. *See supra* note 17. Patent Owner essentially conflates narrow ports having large signal delays over long electrical planar paths with “all off-chip connections” as applying to *Zavracky*’s 3-D stack by referring to each separate chip in *Zavracky*’s modified 3-D stack as “off-chip” and ignoring the central fact that each chip in *Zavracky* directly connects to the other chips in the 3-D stack by numerous short vias. There is no support for this line of argument. Moreover, “Dr Franzon not[ed] the routine use of on-

Reply 17–18 (characterizing Dr. Franzon’s testimony as “noting the routine use of on-chip area-wide connections in 3D stacks, including his prior work.” (citing Ex. 1020; Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)); Ex. 1070 ¶ 44 (“But a POSITA would have recognized that [a] 3D chip that consists of multiple dies would do a better job than the 2D chip and provid[e] fast large connectivity. . . . The point here is that a shorter vertical interconnect allows for a shorter ‘longest path’ and a faster chip. This was commonly understood in the other art as well. . . . [such as] Akasaka’s . . . 3-D ‘high speed performance’” (citing Ex. 1005, 1705)).

chip area-wide connections in 3D stacks, including his prior work.” Reply 17–18 (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65; Ex. 1020; *see also* Ex. 1004, Fig. 2, II-232 § 1 (describing “on chip random access memory . . . provided to store configuration memory”—i.e., the memory layer of Figure 2). Patent Owner agrees that Chiricescu discloses “on-chip cache memory” as a separate layer of an FPGA chip, further suggesting providing a separate layer in Zavracky’s modified stack of layers. *See* Sur-reply 5.

Nevertheless, Patent Owner contends that “the movement of *Chiricescu*’s on-chip cache memory to *Zavracky*’s off-chip memory would throttle” speed gains. Sur-reply 5. For the reasons explained above, this line of argument confuses issues and mischaracterizes Petitioner’s showing. *See supra* note 17. Chiricescu’s teachings bolster Zavracky’s FPGA teachings, and Petitioner shows that in this context, Zavracky describes a memory layer, microprocessor layer, and FPGA layer in a 3-D stack with each layer connected by numerous short vias to increase speed and provide other advantages. *See, e.g.*, Pet. 14–15, 23–33. Patent Owner’s attempt to conflate all “off-chip” narrow port disadvantages to Zavracky’s modified stack of chips by calling chips in that stack “off-chip” is unsupported. As Petitioner persuasively shows throughout its briefing, Zavracky’s stack of chips, connected by numerous vias, and bolstered by Akasaka’s numerous via and Chiricescu’s FPGA teachings, operates just like Chiricescu’s “on-chip” circuit layers in a single chip connected by numerous vias in terms of speed and acceleration. *See* Reply 6 (“Zavracky’s short interior ‘inter-layer connectors’ to stacked ‘random access memory . . . results in **reduced** memory access **time**, **increasing the speed** of the entire system,” and “Chiricescu also teaches the **acceleration** advantages and ‘significantly

improve[d FPGA] reconfiguration time’ achieved by its interconnected layers, including a memory layer configured as a cache for fast access to ‘configuration data . . . from memory off-chip.’” (quoting Ex. 1003, 11:63–12:2; Ex. 1004, 23[4])), 7 (noting Akasaka’s “**acceleration** advantages” based on “teaching, e.g., that ‘[h]igh-speed performance is associated with shorter interconnection delay time and parallel processing’ and that ‘shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems.”” (quoting Ex. 1005, 1705)). In other words, as Petitioner shows, in addition to “stacking techniques,” “[t]he Zavracky-Chiricescu-Akasaka Combination also discloses the other ways that the ’951 patent even arguably implies increases speed—i.e., through caching, the use of short electrical paths, or significantly increased number of connections.” *Id.* at 8 (citing Pet. 14–22).

Patent Owner similarly contends that “Dr. Franzon admitted that a wide configuration data port that accelerates a programmable array’s external memory references to a stacked memory die as compared with the slow narrow bus disclosed in Chiricescu was not obvious at the time of the invention.” PO Resp. 33 (citing Ex. 1012, 71:19–72:1). Based on this contention, Patent Owner also argues that “the wide configuration data port of the ’951 Patent provides precisely the answer to what Dr. Franzon admits was practically impossible at the time of the invention.” *Id.* at 33–34 (citing Ex. 1012, 71:19–72:1, 80:3–22; Ex. 1011 ¶ 72). Patent Owner adds that this “skepticism of Petitioner’s own expert demonstrates that the challenged claims are patentable.” *Id.* at 34 (citing Ex. 1011 ¶ 73). Contrary to this line of argument, similar to the discussion above, Dr. Franzon does not admit

that a wide configuration data port was not obvious, and does not admit that Chiricescu discloses a narrow data bus for transferring data between its stacked layers. *See* Ex. 1012, 71:19–72:1, 80:3–22; *supra* note 17. Rather, at the cited deposition testimony, Dr. Franzon testifies that “*off-chip* [i.e., external] access can’t be, for example, 100,000 bits wide.” Ex. 1012, 71:21–23. Here, in context, Dr. Franzon states that “you can’t have that number of IO. . . . in [the] *case of Trimberger and the ’226 patent* [which is related to the ’951 patent, *see* IPR2020-01571] *memory going from the external to the module.*” *Id.* at 71:23–72:1 (emphasis added). Here again, Patent Owner conflates a narrow data port from a data source “external to the module” (i.e., external to the claimed 3-D stack) with a wide data port from a memory *within the stack* to other chips *in that stack*.

Patent Owner argues that “*Chiricescu* says . . . [that] ‘[t]he elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.’” Sur-reply 4–5 (quoting Ex. 1004, 234). Based on this “off-chip” characterization, Patent Owner argues that “Petitioner concocts its hypothetical structure based on its demonstrably false claim that *Chiricescu’s* improved FPGA reconfiguration time ‘is achieved by its interconnected layers, including a memory layer configured as a cache for fast access to “configuration data . . . from memory off-chip.”’” *Id.* at 4 (quoting Reply 6; last internal quote quoting Ex. 1004, II-234). Patent Owner contends that “*Chiricescu* says just the opposite.” *Id.* at 5 (citing Ex. 1004, 234).

Again, contrary to this line of argument, Petitioner’s showing is opposite to how Patent Owner characterizes it. In other words, Petitioner

argues that Chiricescu improves FPGA reconfiguration time because Chiricescu's cache pre-stores and holds configuration data on-chip that it obtains from an external source (i.e., off-chip memory)—so that the FPGA need not access that external (off-chip memory) source to load the FPGA through a “typical narrow configuration data port” (Sur-reply 5) during FPGA reconfiguration. *See* Reply 6; Ex. 1004, II-234 (“The elimination of loading configuration data on an as needed basis from memory off-chip significantly improves the reconfiguration time for an on-going application.”); *see also supra* n.17. In other words, it is because of the numerous short vias within Chiricescu's layered chip that it reconfigures the FPGA/RLB layer from the stacked memory layer more quickly as compared to reconfiguring it through long data lines from an external source. *See* Ex. 1004, II-232, II-234, Fig. 2.

Petitioner also persuasively addresses Patent Owner's argument that the claims require acceleration over a “baseline” and other related arguments. *See* PO Resp. 20–22; Reply 11–12 (persuasively arguing that the combined teachings contribute to acceleration, the combination does not include a “narrow port,” and “Dr. Franzon testified in both his declaration and deposition that the Zavracky-Chiricescu-Akasaka combination provides acceleration compared to the baseline of other prior art with different structural characteristics.” (citing Ex. Ex. 1002 ¶¶ 212, 215–17, 304–05; Ex. 2012, 28:9–21, 29:15–33:15)); *see also supra* §§ II.C (claim construction in relation to prior art Figure 3's 8-bit narrow port—i.e., one type of baseline). Zavracky by itself, for example, indicates that 32 bit microprocessors were routine in 1993, years before the effective date of the invention, indicating that Zavracky's microprocessor buses at least handled

32 bits in parallel. *See* Ex. 1003, 1:6–8 (continuity date of 1993), 31–40 (discussing prior art microprocessors). As noted above, Patent Owner indicated during the Oral Hearing that the challenged claims embrace devices transfer data over a port that “could be as small as 32 bits . . . if you have a small FPGA, right? If you want to update something in parallel, you could update 32-bit with 32 bits?” Tr. 49:1–9; *supra* § II.C (claim construction)

Patent Owner also argues that “major modifications would need to be made to the combination of *Zavracky* and *Chiricescu* in order to configure a stacked module to meet the acceleration limitations of Independent Claims 1, 5, 10, 16, and 23.” PO Resp. 32. Patent Owner explains that this major modification requires a “wide configuration data port (or other similar structure) between the memory and the FPGA.” *Id.* Patent Owner also argues that such a modification would “alter *Chiricescu*’s principle operation, which relies on an entirely different strategy for routing data throughout the FPGA, namely its narrow RLB Bus and its ‘routing layer,’ which *Chiricescu* declares ‘*is of critical importance*’ since it is used for the implementation of the interconnection of the non-neighboring RLBs.” *Id.* (quoting Ex. 1004, 2) (emphasis by Patent Owner).

Here, Patent Owner concedes that “the ’951 Patent discloses a memory array that achieves the claimed acceleration (*i.e.*, utilizing a *portion of the wide configuration data port*), which significantly reduces the amount of time it takes to move data from a memory die into a programmable array.” PO Resp. 33 (emphasis added). Patent Owner does not describe what “portion” of the wide configuration data (which Figure 5 of the ’951

patent depicts as a black box) the claimed “functional to accelerate” limitations require.

With respect to Chiricescu’s principle of operation, as Petitioner also persuasively argues, no “‘modifications’ are required to Chiricescu at all because the Petition’s combination involves ‘fold[ing] in Chiricescu’s teachings (including using stacked memory to reconfigure[] the FPGA) with Zavracky’s 3D stacks.” Reply 17 (quoting Pet. 19). Even if employing Chiricescu’s FPGA structure also suggests implementing its routing layer on a separate layer, contrary to Patent Owner’s arguments, Chiricescu does not describe its routing layer as a narrow port. *See id.* (noting that Dr. Franzon did not admit Chiricescu includes a narrow port and citing Dr. Franzon’s testimony that on-chip area-wide connections in 3-D stacks were well-known (citing Ex. 1002 ¶¶ 47–51; Ex. 1070 ¶¶ 65, 68)). Also, Chiricescu’s Figure 2 depicts connections between the memory layer, routing layer, and RLB layer (a “sea-of-gates FGPA structure”) with connections that are distinct from the RLB bus. Ex. 1004, II-232 § 2.1, Fig. 2. Chiricescu notes that “routing congestion will also be improved by the separation of layers,” further suggesting that the routing layer is not part of a narrow port and suggesting stacking of separate layers in Zavracky’s stack. *Id.* at II-232.

As Petitioner persuasively argues, “Chiricescu describes ‘vertical metal interconnections (i.e., interlayer vias),’ and ‘**three separate layers with metal interconnects between them.**’” Reply 15 (citing Ex. 1004, II-232). Chiricescu’s “express ‘architecture is based on’ technology developed by Zavracky at Northeastern University.” *Id.* (quoting Ex. 1004, 232). And Chiricescu states that Zavracky’s architecture provides “3-D layered FPGAs which can have vertical metal interconnections (i.e., interlayer vias) *placed*

anywhere on the chip.” *Id.* at II-232 (emphasis added). Therefore, contrary to Patent Owner’s arguments, Chiricescu’s principle of operation does not require a narrow port. *See also* Reply 15 (“The combination involves ‘fold[ing] in Chiricescu’s teachings (including using stacked memory to reconfigure the FPGA) with Zavracky’s 3D stacks.’” (citing Pet. 19)).

Increasing via connections based further on Akasaka’s teachings would have been obvious by facilitating more connections between well-known available circuits such as memory, FPGA, and processors. *See, e.g.*, Reply 19 (“Zavracky and Chiricescu envision connections ‘anywhere on the die.’” (citing Pet. 20–22; Ex. 1002 ¶¶ 41–51, 237–238)); Pet. 22 (“Akasaka’s distributed contact points would have been the logical extension to Zavracky and Chiricescu’s teaching of connections anywhere, especially in view of the POSITA’s background knowledge.” (citing Ex. 1002 ¶ 239)).

Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 1, 2, 4–6, 8–16, 23, 27, and 29 would have been obvious.

6. *Claims 17 and 24*

As determined above (§ II.D.5), independent claims 16 and 23 are materially the same as claim 1, and Petitioner largely relies on its showing for claim 1 to address those independent claims. Pet. 44–45, 49–50. Claims 17 and 24 respectively depend from independent claims 16 and 23 and recite “wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as said processing element.” Petitioner

relies on its showing in claim 1, including Chiricescu's disclosure about accelerating FPGA reconfiguration using a memory array. *See* Pet. 45, 49–50.

Further regarding claims 16 and 23, as discussed above in connection with claim 1, Zavracky discloses a random access memory layer, or memory array, with buses running through the vertical stack that contains a microprocessor, FPGA, and memory. *See* Pet. 32 (citing Ex. 1003, Figs. 10, 13, 11:63–65, 12:33–35). Chiricescu describes using a random access memory layer as a cache memory to reconfigure the FPGA as a processing element. *Id.* (citing Ex. 1004, II-232, II-234). As also indicated above in connection with claim 1, Petitioner provides multiple reasons to combine Zavracky, Chiricescu, and Akasaka, including to allow for speed and bandwidth gains and parallelism, and minimize reconfiguration and propagation delays, with a well-known desire to increase bus sizes. *See* Pet. 12, 18, 20; Reply 5–8. Petitioner also contends it would have been obvious to employ Chiricescu's cache memory teachings in the combined 3-D stack to reconfigure data in order to accelerate access to the external memory references of claim 1. *See* Pet. 32 (“Therefore, when the FPGA (i.e., the processing element) needs to be reconfigured, with new data, access to that data is accelerated by already having been loaded into the memory array.” (citing Ex. 1004, II-234) (emphasis omitted)).

Addressing claims 17 and 24, Patent Owner argues that “[t]he *Zavracky-Chiricescu-Akasaka* combination fails to teach or suggest a 3-D processor module that includes a second integrated die element, separate from a first integrated die element having a programmable array, wherein the ‘memory array is functional to accelerate reconfiguration of said field

programmable gate array as a processing element.” PO Resp. 24. Patent Owner states the “cited references” do not teach or suggest the “functional to accelerate external memory references” and “functional to accelerate reconfiguration” clauses, points to Petitioner’s rationale with respect to claim 1 as discussed in the previous section (§ II.D.4), and concludes that claims 17 and 24 “are patentable.” *Id.* at 24 (noting that “Petitioner relies on the same rationale for this claim element as it did for the element discussed directly above, i.e. ‘memory array is functional to accelerate external memory references to said processing element’”).

In other words, Patent Owner does not argue claims 1, 16, 17, 23, and 24 separately in a clear fashion. As noted above, claims 16 and 23 are materially the same as claim 1, and we address arguments with respect to claims 1, 16, and 23 (which Patent Owner groups together) above. *See supra* §§ II.D.4–5.

Patent Owner’s argument with respect to claims 17 and 24, which essentially lists the limitations thereof and concludes that Petitioner fails to show obviousness, does not undermine Petitioner’s persuasive showing for these claims as summarized herein and also for the reasons discussed in this section and above in connection with claim 1 and other argued claims. As summarized above, Petitioner’s showing that external memory references in the combined teachings of include data or other references for reconfiguring the FPGA is persuasive. *See* Pet. 31–33, 44–45, 49–50; *supra* §§ II.D.4–5.

We adopt and incorporate Petitioner’s showing for claims 17 and 24, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 45, 49–50. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above

and below that tend to overlap to a certain extent with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 17 and 24 would have been obvious.

7. *Claims 18–22*

Independent claim 18 is similar to claim 1 and recites a “reconfigurable processor module comprising” at least three integrated circuit elements including “a programmable array including a processing element,” a processor electrically coupled thereto, and “a memory stacked with and electrically coupled” to both integrated circuit elements, “whereby said processor and said programmable array are operational to share data therebetween.”

Addressing the three integrated circuit elements, Petitioner relies on its similar showing with respect to claims 1, 4 (third integrated circuit), 9 (third integrated circuit is a memory), and 10 (programmable array, processor, and memory electrically coupled with memory functional to accelerate external memory references). *See* Pet. 23–33, 35–36, 40–42, 45–46. Petitioner relies on Zavracky’s disclosure of programmable logic array 802 (FPGA) in a stacked 3-D processor module with microprocessor layers 804 and 806 (Ex. 1003, Fig. 13), and Chiricescu’s teaching of a 3-D chip comprising FPGA, memory, and routing layers (Ex. 1004, Fig. 2). *See id.* Further relying on Zavracky’s Figure 13, Petitioner asserts that “each of the programmable array, microprocessor, and memory IC functional elements are pair-wise stacked with and electrically coupled with each other” through vertical vias and buses. *Id.* at 28–29 (also noting that Zavracky teaches that “[i]nter-layer connections . . . can be placed anywhere on the die” of the functional element(s), meaning the connections “are not limited to

placement on the outer periphery” (quoting Ex. 1003, 6:43–7:9)). Petitioner also relies on Akasaka’s teaching and suggestion that in a 3-D stack, “[e]ach active layer is connected electrically through via holes” (*id.* at 30 (quoting Ex. 1005, 1707)), and on similar motivation as for claim 1 (*see id.* at 18–22, 31–33, 48 (citing Pet. § VII.A.4; Ex. 1002 ¶¶ 233–239, 347–348)).

Addressing the claim 18 limitation “whereby said processor and said programmable array are operational to share data therebetween,” Petitioner refers to Akasaka’s disclosure of 3-D chips wherein “memory data are kept common by the interlayer (vertical) signal [so that] **each processor can use the common memory data.**” Pet. 49 (emphasis by Petitioner) (quoting Ex. 1005, 1713). In addition, Petitioner argues that “the POSITA knew of the need for replicated ‘common data memory’ in stacked designs, including as taught in Akasaka, to enable, e.g., multi-processor cache coherence.” *Id.* at 21 (citing Ex. 1002 ¶ 236; Ex. 1034, 466–469; Ex. 1005, 1713, Fig. 25). Petitioner further explains that “[t]hat structure would be more difficult to accomplish with a limited number of interconnections as in Zavracky,” further motivating “[a] POSITA . . . to seek out Akasaka’s distributed contact points in order to build a “common data memory.” *Id.* at 20 (citing Ex. 1002 ¶ 237).

Petitioner also relies on Akasaka’s teaching that that “information signals can be transferred” through “several thousands or tens of thousands of via holes . . . present in these devices” to further suggest employing Akasaka’s “thousands of via holes in the context of Zavracky” as further suggesting the claimed data sharing feature. Pet. 47–48 (first two quotes quoting Ex. 1005, 1705; citing Ex. 1002 ¶¶ 233–239, 347–348). As noted throughout this Final Written Decision, Petitioner also relies on known

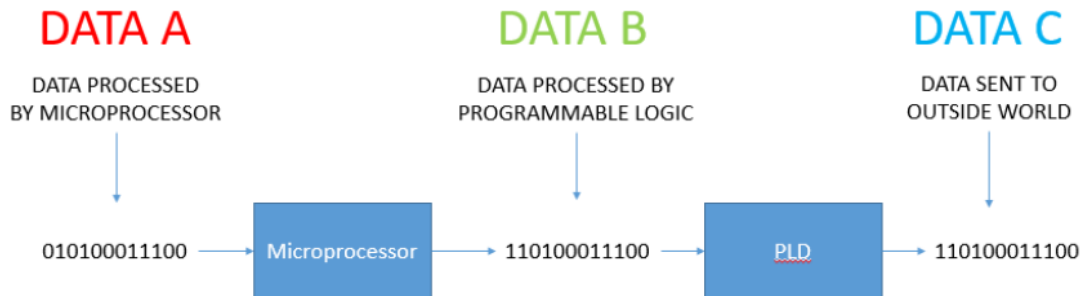
benefits of increased speed, bandwidth, and capability for parallel processing based on well-known teachings, to suggest stacking layers, including memory layers, using numerous vias, to combine the teachings of Zavracky, Chiricescu, and Akasaka. *See id.* at 8–9, 12, 17–22. For example, Petitioner states that “[t]he POSITA would have sought out Akasaka’s connectivity to improve Zavracky’s stacks in applications requiring parallel processing. Such applications included image processing algorithms [that] run simultaneously over an entire image in memory.” *Id.* at 20–21 (Ex. 1002 ¶ 235; Ex. 1048; Ex. 1005; Ex. 1021).

Petitioner explains that Zavracky also teaches that its programmable logic 802 is an FPGA and serves as “an intermediary between ‘the microprocessor and any off-chip resources.’” Pet. 47 (citing Ex. 1003, 12:28–36). Petitioner also relies on Zavracky’s “[i]nterconnect lines” operating as a “data bus.” *Id.* (quoting Ex. 1003, 6:39–42). According to Petitioner, a “POSITA would have recognized that communication between ‘the microprocessor and any off-chip resources’ via the FPGA (under the Zavracky-Chiricescu-Akasaka Combination as explained in [1.1], [1.2] and [2]) means that data is shared between the microprocessor and the FPGA.” *Id.* (citing Ex. 1002 ¶ 342).

Claims 19–22 depend from independent claim 18. Claim 19 recites “wherein said memory is operational to at least temporarily store said data.” *See* Pet. 48–49. Petitioner argues that “[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data.” *Id.* at 48 (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory))). Petitioner also relies on Akasaka’s shared memory as discussed above and further below in connection with

claim 18. *See id.* (citing Ex. 1005, 1713). Petitioner asserts that the added claim limitations of claims 20–22, which depend from claim 18 and recite an “FPGA,” a “microprocessor,” and a “memory array,” respectively, read on Zavracky’s stack as depicted in Figure 13. *See id.* at 49 (relying on the analysis for claims 1, 2, and 10); *supra* § II.D.4 (analyzing claims 1, 2, and 10). In other words, Petitioner relies on its showing with respect to materially the same limitations in claims 1, 2, and 10 to address claims 20–22. Pet. 49. Patent Owner does not challenge claims 19–22 separately.

Addressing claim 18, Patent Owner argues that “[t]he Zavracky microprocessor and programmable logic are not operational to *share* data, such as might be stored in a stacked memory die, for example.” PO Resp. 25 (citing Ex. 2011 ¶ 63). Patent Owner reproduces the following diagram from Dr. Souris’s declaration to illustrate its point:



Ex. 1012 ¶ 63. According to Patent Owner, Zavracky’s microprocessor on the left does not share data with the FPGA (PLD) on the right, because “it is the output of Zavracky’s microprocessor that is sent to the FPGA.” PO Resp. 25 (citing Ex. 1012 ¶ 63).

Patent Owner attempts to distinguish “sharing” data and “transferring” data by arguing that “[t]he claims require more than a processor transferring data to a field programmable gate array.” *See* PO Resp. 25–26. Neither the ’951 patent specification nor claim 18 requires this distinction.

Nevertheless, Patent Owner argues that shared data “might be stored in a stacked memory die, for example.” PO Resp. 25. Grouping claims 18–22 together, Patent Owner similarly argues in its Sur-reply that “[a] POSITA would recognize that this data on the stacked memory die is literally ‘data shared between a microprocessor and an FPGA.’” Sur-reply 11–12 (citing Ex. 2011 ¶ 64; Ex. 1001, 2:1–9, 2:56–60, 5:18–29).

Contrary to this line of argument, claims 18–22 do not require a “stacked memory die” to hold data to support the recited shared data functionality. Although claim 19 recites “wherein said memory is operational to at least temporarily store said data,” claim 19 is broad enough to read on Zavracky’s modified memory (which is operational to store the shared data) *after* the microprocessor and FPGA (are operational to) share it per claim 18. *See* Pet. 48 (arguing that “[t]he POSITA would have understood that memory is—by definition—operational to at least temporarily store data” (citing Ex. 1002 ¶ 308 (citing Ex. 1039 (trade dictionary defining memory))).¹⁸

Moreover, even under Dr. Souri’s diagram of Zavracky’s process, Zavracky’s microprocessor processes the input data to create the shared output data, and then transfers that shared output data onto the data bus and then to the FPGA. *See* Reply 13–14 (citing Ex. 1070 ¶¶ 73–74; Ex. 1083); Ex. 1070 ¶ 73 (quoting Ex. 1083, 1:26–34 (describing computers “shar[ing] data” by “transfer[ing] data”)); Pet. 47–48 (citing Ex. 1002 ¶¶ 343–349). As

¹⁸ As indicated herein, Patent Owner does not address Petitioner’s persuasive showing for claim 19 separately from claim 18. Petitioner also persuasively relies on Akasaka’s shared memory for claims 18–22 as discussed further below. *See* Pet. 47–50 (citing Ex. 1005, 1713).

discussed further below, Petitioner also persuasively explains how Zavracky's microprocessor and FPGA share and process the same data from off-chip resources to implement a user-defined protocol. *See* Pet. 47.

Patent Owner also argues that Petitioner's theory based on Akasaka's teaching and suggestion to share "'common memory data' does not cure this fundamental deficiency in *Zavracky* because it also does not involve any processing of data shared between a microprocessor and an FPGA (or any other type of chip)." PO Resp. 26. Claims 18–22 do not require "processing of [shared] data," but even if the claims imply that interpretation, the combined teachings suggest it, as Petitioner persuasively shows as discussed next.

To support its point, Patent Owner reproduces *Akasaka's* Figure 25 as follows:

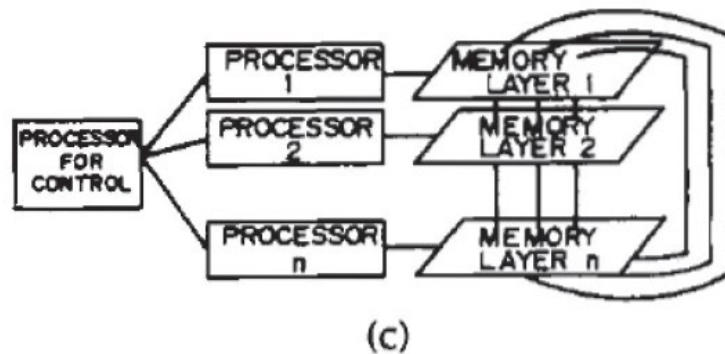


Fig. 25. New concept of 3-D IC. (a) 3-D PLA model (by Prof. T. Nanya of the Tokyo Institute of Technology). (b) Integration of CAM RAM in the same chip (by T. Ogura of NTT). (c) Common memory data system for 3-D memory chip (by Prof. M. Hirose of Hiroshima University).

PO Resp. 27. Figure 25(c) above depicts a "[c]ommon memory data system for a "3-D memory chip" wherein processors 1, 2, n (on the left) share data

on memory layers 1, 2, n (on the right). Ex. 1005, 11. Akasaka states that “memory in each chip belongs to corresponding independent microprocessors in the same layer, *and the memory data are kept common by the interlayer (vertical signal) transfer.*” *Id.* (emphasis added).

Patent Owner argues that “although *Akasaka* proposes that memory data is ‘kept common by the interlayer (vertical) signal transfer,’ the individual microprocessors do not process any shared data because each only processes the data in its corresponding memory.” PO Resp. 27. This argument misses the mark, because Akasaka’s system transfers the same data between the memories so that each processor is operational to process the same data. Stated differently, Akasaka contradicts Patent Owner’s argument that transferring the same data at one memory location (the “common” data in Akasaka) to another memory location shows a lack of data sharing—i.e., Akasaka describes the data as “common.” *See* Ex. 1005, 11.

As to sharing data between a processor and an FPGA, Petitioner relies on Akasaka’s teaching as suggesting the sharing of common data through vertical data transfers in the combined 3-D structure of Zavracky, Chiricescu, and Akasaka, instead of relying on a bodily incorporation of the processor memory layer scheme of Akasaka. *See* Pet. 47–48; Reply 14 (arguing that Patent “attacks the physical die-stacking technique in Akasaka—but Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also teaches memories can be at any layer” (citing Ex. 1003, 11:63–12:2, Figs. 10, 12)). Claims 18–22 are agnostic as to how the FPGA and microprocessor share data—i.e., with or without a separate memory in each layer—i.e., claim 18 recites “whereby

said processor and said programmable array are operational to share data therebetween” without reference to the “memory” recited earlier in the claim.

As proposed by Petitioner, it would have been obvious for the FPGA and microprocessor of Zavracky-Chiricescu, based on Akasaka’s teachings, to share data using numerous (e.g., thousands) of vertical vias to implement the data transfer and thereby increase processing speeds and bandwidth. *See* Pet. 47–48 (citing Pet. § VII.A.4 (reasons to combine the references); Ex. 1002 ¶¶ 233–239; 347–348). For example, as Petitioner shows, using Akasaka’s teachings, including its memory teachings to share data using thousands of vertical vias would have “increase[d] bandwidth and processing speed through better parallelism and increased connectivity.” *See* Pet. 20 (citing Ex. 1002 ¶ 233; Ex. 1005, 1705); Reply 6–7 (citing known advantages of numerous vertical vias). Petitioner also persuasively shows that skilled artisans would have recognized that using Akasaka’s memory teachings and dense via structure allows for increases in processing speed and improved parallelism and ensures cache coherency in the modified stack of Zavracky. *See id.* at 20–21 (citing Ex. 1002 ¶¶ 236–237; Ex. 1005, 1705, 1713).

Patent Owner’s arguments do not address Petitioner’s more general showing that a “POSITA would have recognized that communication between ‘the microprocessor and any off-chip resources’ via the FPGA (under the Zavracky-Chiricescu-Akasaka Combination as explained in [1.1], [1.2] and [2]) means that data is shared between [and processed by] the microprocessor and the FPGA.” *See* Pet. 47 (citing Ex. 1002 ¶¶ 342–346). In other words, Dr. Souri’s diagram above only refers to data *from* the PLD

(FPGA) as “DATA SENT TO THE OUTSIDE WORLD,” but this analysis does not address Petitioner’s persuasive showing that data from the outside world (off-chip) passes through the FPGA as an intermediary to the microprocessor. *See* Pet. 48–49 (quoting citing Ex. 1003, 12:28–36). At the cited passage, prior to describing Figure 13, Zavracky states that “[p]rogrammable logic arrays can be used to provide communication between a multi-layered microprocessor and the outside world.” Ex. 1003, 12:29–31. Zavracky also states that “programmable logic array 802 [an FPGA in Figure 13] can be programmed to provide for user-defined communications protocol between the microprocessor and any off-chip resources.” *Id.* at 12:36–37. Figure 13 shows bus connections on the PLD 802 (FPGA) to the outside world, with bus connections from PLD 802 to microprocessor 804/806 and memory 808. *See* Ex. 1003, Fig. 13, 12:29–39. Therefore, as Petitioner argues, Zavracky shows that communication occurs between the microprocessor and the FPGA, thereby teaching the sharing of data between the two (in at least one of the two directions). *See* Pet. 48–49.

In addition, in advancing another argument, Patent Owner admits that the combination teaches data sharing: “[T]he approach of Zavracky-Chiricescu would result in a structure in which *data is removed from the microprocessor cache and placed in the FPGA’s on-chip memory*,” and “*data . . . might be shared between Chiricescu’s FPGA and Zavracky’s microprocessor.*” PO Resp. 29 (emphasis added).

Patent Owner also argues that “to modify the *Zavracky-Chiricescu* system with *Akasaka*, . . . the ***stacked*** memory layer of *Chiricescu* would need to be moved into its RLB layer because *Akasaka* requires each memory layer to be located on the same layer as its associated processor,” thereby

requiring a “major modification” of Chiricescu. PO Resp. 37. Patent Owner similarly argues that implementing the combination requires “adding *more* structure to *Chiricescu*’s RLB layer, in the form of *Akasaka*’s memory, destroys *Chiricescu*’s principle of operation, which relies on moving as much structure *out of* the RLB layer as possible.” *Id.*

This line of argument incorrectly assumes that Petitioner must show how to bodily incorporate the common memory teachings of Akasaka into Chiricescu’s structure as part of its obviousness showing. This argument is unavailing, because Petitioner relies on Zavracky’s 3-D stack structure, including its memory as a separate layer and on Akasaka’s thousands of via holes, informed by the common memory teachings of Akasaka, without any modification to Chiricescu’s FPGA teachings required. The common memory teachings of Akasaka are agnostic as to the memory location.

That is, Akasaka does not “require[] each memory layer to be located on the same layer as its associated processor.” *See* PO Resp. 37. Even though Figure 25 of Akasaka shows a stack of processors and memory, with a processor and memory on the same layer, nothing in Akasaka states that the memory cannot be elsewhere in the stack on a separate layer. Rather, Figure 25 shows all memories connected together electrically with each memory connected electrically to its respective processor. *See* Ex. 1005, Fig. 25. These electrical connections suggest to an artisan of ordinary skill that the memory layer’s location is less important than the electrical connections. *See id.* Moreover, Petitioner relies on Zavracky’s separate layer for each memory in a stack with via connections to enhance speed, as the combination suggests. *See* Reply 14 (“Zavracky already teaches stacked memories that are interconnected to other dies in the stack, and also teaches

memories can be at any layer” (citing Ex. 1003, Figs. 10, 12, 11:63–12:2 (“[A]n additional layer or several layers of random access memory may be stacked This configuration results in reduced memory access time, increasing the speed of the whole system”)).

We adopt and incorporate Petitioner’s showing for claims 18–22, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 46–49. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner persuasively shows that claims 18–22 would have been obvious.

8. *Summary*

After a full review of the record, including Patent Owner’s Response and Sur-reply and evidence, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, and Akasaka would have rendered obvious claims 1, 2, 4–6, 8–24, 27, 29.

E. *Obviousness, Claim 25*

1. *Trimberger*

Trimberger, titled “A Time-Multiplexed FPGA” (1997), describes an FPGA with on-chip memory distributed around the chip. Ex. 1006, 22. Trimberger teaches that the memory “can also be read and written by on-chip [FPGA] logic, giving applications access to a single large block of RAM.” *Id.* Trimberger teaches this “storage [can] be used as a block memory efficiently.” *Id.* at 28.

Trimberger’s Figure 1 follows:

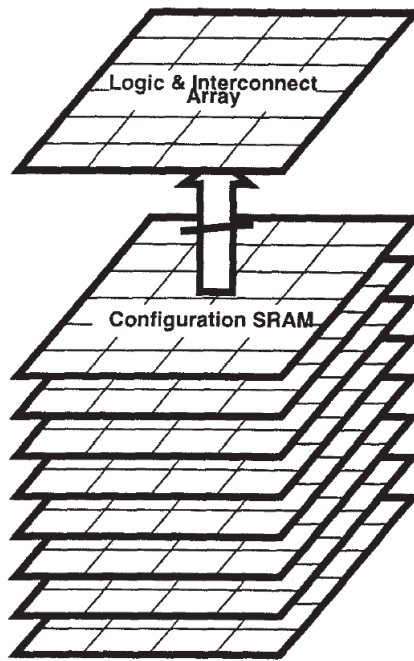


Figure 1. Time-Multiplexed FPGA Configuration Model

Figure 1 of Trimberger above depicts eight planes of SRAM (static random access memory) for an FPGA. *See* Ex. 1006, 22–23. “The configuration memory is distributed throughout the die This distributed memory can be viewed as eight *configuration memory planes* (figure 1). Each plane is a very large word of memory (100,000 bits in a 20x20 device).” *Id.* at 22.

Trimberger also teaches accessing each plane of memory as one simultaneous parallel transfer of 100,000 memory data bits to reconfigure the FPGA quickly: “When the device is *flash reconfigured* all bits in logic and interconnect array are updated simultaneously from one memory plane. This process takes about 5ns. After flash reconfiguration, about 24ns is required for signals in the design to settle.” Ex. 1006, 22.

2. *Claim 25*

Dependent claim 25 recites “[t]he programmable array module of claim 23 wherein said memory array is functional as block memory for said processing element.” Petitioner contends that claim 25 would have been

obvious over the combination of Zavracky, Chiricescu, Akasaka, and Trimberger. Pet. 52–55.

Petitioner relies on Trimberger’s block memory teachings to address claim 25. *See* Pet. 58–60. According to Petitioner,

Trimberger teaches that its co-located “memory is **accessible as block RAM** for applications,” that are running in the FPGA, i.e., that the memory “can also be read and written by on-chip [FPGA] logic, giving applications access to a single large block of RAM.” Ex. 1006, 22. Trimberger teaches that “the configuration storage to be used **as a block memory efficiently.**” [*Id.* at 28].

Pet. 55 (emphasis by Petitioner) (quoting Ex. 1006, 22, 28). Petitioner contends that it would have been obvious to employ Trimberger’s block memory to support fast local memory in FPGA applications like that in the combined teachings of Zavracky, Chiricescu, and Akasaka, with “the memory stacked and electrically coupled nearby.” *See id.* at 53–55 (citing Ex. 1002 ¶¶ 247–256; Ex. 1020; Ex. 1048). Petitioner also contends that “[t]he POSITA would have known that FPGAs have limited programmable logic space, and that for certain tasks it would be more cost efficient and silicon-efficient to use the FPGA for reconfigurable processing and to use a separate task-dedicated memory element for block memory.” *Id.* at 54 (citing Ex. 1002 ¶ 247). Petitioner advances other reasons for the combination. *See id.* at 54–55 (characterizing Trimberger’s on-chip block memory as faster relative to off-chip memory).

Patent Owner argues that “[d]ependent [c]laim 25 requires the “the ‘block memory’ and ‘field programmable gate array’ to be on ***different*** chips.” PO Resp. 44. According to Patent Owner “*Trimberger . . . teaches away from having its block memory and FPGA on different chips as*

it attributes its quick FPGA reconfiguration to the massive connectivity *within* the chip.” *Id.* (citing Ex. 1006, 22; Ex. 2011 ¶ 88); *see also id.* at 50–51 (same argument (citing Ex. 2011 ¶ 97)). Patent Owner primarily relies on this “within the chip” or “on-chip memory” argument as the basis for its allegations of lack of motivation, lack of reasonable expectation of success, teaching away, requirement for major modifications, and other related arguments. *See id.* at 43–51.

For example, Patent Owner argues that “implementing Trimberger’s FPGA structure in Xilinx’s combination would result in a complete redesign of the hypothetical 3-D stacked structure of the *Zavracky-Chiricescu-Akasaka* Combination,” because “the block memory is no longer stacked with the FPGA, but instead located on *Trimberger’s* FPGA die as on-chip memory.” PO Resp. 49 (citing Ex. 2011 ¶ 95). Patent Owner explains that “*Trimberger’s* FPGA structure requires that its configuration memory planes are located on the same die as the FPGA’s logic cells, so that the FPGA can quickly switch between different configurations.” *Id.* at 50 (citing Ex. 2011 ¶ 97). Patent Owner asserts that “Petitioner admits this.” *Id.* (citing Pet. 53 (characterizing the Petition as stating that Trimberger teaches a time multiplexed FPGA with on-chip memory distributed around the chip)). Based on these assertions, Patent Owner contends that evidence lacks as to “how or why a POSITA would have had a reasonable expectation of success in making the combination.” *Id.* at 45; *see also id.* at 49–51 (similar arguments).

Petitioner persuasively shows that Trimberger does not teach away or support Patent Owner’s related arguments based on the single-chip theory, including hypothetical re-designs, and lack of a reasonable expectation of

success and motivation. Petitioner does not admit that Trimberger “*requires* that its configuration memory planes are located on the same die as the FPGA’s logic cells.” *See* PO Resp. 50 (citing Pet. 53); Pet. 53 (describing Trimberger’s on-chip memory without characterizing it as a requirement).

Petitioner persuasively points out that Trimberger does not “criticize, discredit, or otherwise discourage investigation into the invention claimed,” merely because it discloses embodiments having block memory and an FPGA within the same chip. Reply 22 (quoting *Depuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009)). Petitioner persuasively argues that Patent Owner’s “‘massive connectivity’ observations about Trimberger confirm that the POSITA would have been further encouraged to make the combination.” *Id.* at 23 (citing Ex. 1070 ¶¶ 44–45); *see* PO Resp. 50 (arguing Trimberger’s block memory includes “massive connectivity” with the FPGA).

Petitioner’s response, supported by Dr. Franzon’s testimony, is persuasive. Trimberger’s Figure 1 shows eight different memory planes on a single chip. Ex. 1006, 22. Trimberger states that “[t]he entire configuration of the FPGA can be loaded from this on-chip memory in 30ns.” *Id.* Trimberger does not teach, and Dr. Souris does not testify, that Trimberger’s “on-chip memory” *requires* each memory plane to be on *the same layer* as the FPGA of a chip, such as a multi-layered chip or stack of chips. *See id.*; Ex. 2011 ¶ 97 (describing Trimberger as employing “massive connectivity *within* the chip”).

Dr. Franzon explains credibly that “Trimberger’s one-cycle teachings would be **improved** by applying its teaching to a 3D chip.” Ex. 1070 ¶ 44. Dr. Franzon explains that Trimberger’s reconfiguration clock cycle “(i.e., the

delay in Trimberger) is set [by] determin[ing] the length of the longest path after routing.” *Id.* (quoting Ex. 1006, 27). Then, Dr. Franzon testifies that “[t]he point here is that a shorter vertical interconnect allows for a shorter ‘longest path’ and a faster chip” and “[t]his was commonly understood in the other art.” *Id.* (noting that “Akasaka taught that 3-D ‘high speed performance’ was enhanced because ‘[i]n 2-D ICs, the longest signal interconnection length becomes several to ten millimeters, but in 3-D ICs the length between upper and lower layers is on the order of 1–2 μm .” (quoting Ex. 1005, 1705); also noting that Zavracky teaches that “[i]n the proposed approach, shorter busses will result in smaller delays and higher speed circuit performance” (quoting Ex. 1003, 3:4–14) (emphasis by Dr. Franzon)).

This testimony goes hand-in-hand with Petitioner’s showing as summarized above in connection with the challenged claims discussed above. That is, Petitioner shows persuasively that the combined teachings of Zavracky, Chiricescu, and Akasaka suggest short conductor runs using numerous distributed vias of a 3-D multi-layer chip to increase speed and bandwidth, decrease path delays, and facilitate parallel processing. *See supra* § II.D.4–7; Pet. 7–9, 17–22 (background knowledge of an artisan of ordinary skill includes stacking chips with multiple distributed vias to minimize latency, interconnection delay, and reconfiguration times, allow for parallel processing, and increase operating speed, etc.). The Petition also persuasively points to a “concern[] with the speed of access between the FPGA and the block of memory” as a reason to use Trimberger’s “block memory . . . combined with Zavracky-Chiricescu-Akasaka’s teaching of having the memory stacked and electrically coupled nearby.” Pet. 54.

Supported by Dr. Franzon's testimony, Petitioner also persuasively responds that arranging a block memory on a separate layer from an (FPGA) processing element is not a major modification and the evidence shows how to do it would have been well within the level of ordinary skill. *See* Reply 23–24; Ex. 1070 ¶ 46 (“Dr. Souri does not understand the combination being made. The Zavracky, Chiricescu, Akasaka combination already has a memory and an FPGA. It is already connected via a wide-area distributed set of interconnections as taught in Akasaka.”).

Petitioner persuasively points to the Petition as stating that “[t]he POSITA would have sought Trimberger's teaching of using memory as a block memory and combined that with Zavracky-Chiricescu-Akasaka's teaching of **having the memory stacked and electrically coupled nearby.**” Reply 23 (citing Pet. 54). In other words, Petitioner does not propose “*“moving” Trimberger's on chip memory*” to the same layer as the FPGA in Zavracky-Chiricescu-Akasaka's 3-D stack, contrary to Patent Owner's argument. *See* PO Resp. 50; Sur-reply 20. Rather, Petitioner proposes modifying the existing memory of Zavracky's modified 3-D stack to function as a block memory according to Trimberger's teachings. *See* Pet. 54; Reply 24. Moreover, Trimberger's eight plane memory design suggests different layers at least for each plane of memory, and challenged claim 25 does not require more than one of Trimberger's block memory planes. *See* Pet. 54 (describing “us[ing] a separate task-dedicated memory element for block memory”); Ex. 1006, Fig. 1 (showing eight different time multiplexed memory planes); Ex. 1070 ¶ 45 (testifying that in Trimberger's Figure 1 (*see supra* § II.E.1), “the fat arrow with a line in the traditional representation of ‘many signals’ – i.e., this is suggesting an architecture where different

‘planes of memory’ (i.e., layers of a die in a stack) are transferred from the configuration SRAMs to the FPGA”).¹⁹

In any event, claim 25 does not preclude eight separate memory layers in a stack, or all eight memory planes on the same layer in the stack, or a multiplexor to select the different memory planes. Patent Owner essentially argues that an artisan of ordinary skill can connect eight memory planes to an FPGA on a single layer, but cannot do the same with vias on separate layers with a reasonable expectation of success. The record shows otherwise, for the reasons outlined above.

Petitioner persuasively points to testimony by Dr. Franzon cited in the Petition, who in turn relies credibly on evidence of record, to show a reasonable expectation of success, showing that implementing block memory with an FPGA was well-known in the prior art. *See* Reply 24 (citing Pet. 57; Ex. 1002 ¶ 145, 248; Ex. 1003, Figs. 12, 13; Ex. 1003, 11:63–12:2; Ex. 1002 ¶ 145); Ex. 1002 ¶ 145 (testifying that “Cooke also discloses that the ‘memory planes not being used for configuration may be used as memory,’ i.e., an extra memory block for use by the FPGA” (citing Ex. 1032), ¶ 144 (testifying that Casselman shows connecting “memory . . . directly to FPGA . . . through address and data busses.” (citing Ex. 1026)).

¹⁹ As summarized above, each memory plane in Trimberger contains 100,000 bits of memory. *Supra* § II.E.1. Also, “[w]hen the device is *flash reconfigured* all bits in logic and interconnect array are updated simultaneously *from one memory plane*. *Id.*; Ex. 1006, 22 (emphasis added). Contrary to Patent Owner’s arguments in connection with claims 1 and 23–25 discussed above, Trimberger provides another example of the prior art showing the connection of a large plane of memory (block memory) directly to an FPGA for reconfiguration in one cycle.

As discussed above in connection with challenged claims 1, 2, 4–6, 8–24, 27, and 29, Petitioner persuasively outlines several good reasons to combine related teachings from the references to arrive at a 3-D stack that includes memory, FPGA, and a processor, reasons that apply to Trimberger’s block memory. *See supra* § II.D.4–7; Pet. 7–9, 17–22, 55–57. For example, Petitioner notes that Trimberger teaches a block memory to provide access to a “single large block of RAM” such that memory “can . . . be read and written by on-chip [FPGA] logic.” Pet. 56 (quoting Ex. 1006, 22). Petitioner also states that implementing Trimberger’s block memory teachings with the 3-D chip combination as suggested by Zavracky’s “stack [of] memories together with processors or the programmable array” addresses “concern[s] *with the speed of access* between the FPGA and the block memory.” *See id.* at 57 (emphasis added). Petitioner notes that “FPGAs have limited programmable logic space” suggesting “a separate task-dedicated memory element for block memory.” *Id.* Petitioner also persuasively argues that applying Trimberger as a separate layer (or layers) of memory in the 3-D stack of Zavracky, Chiricescu, and Akasaka “would have merely been a combination of prior art elements according to known methods to yield a predictable result” and “would have been a well-known use of a memory,” showing a reasonable expectation of success in “improv[ing] on the memory options of the FPGA.” *Id.* As outlined above, the record supports Petitioner.

Patent Owner repeats or repackages its arguments addressed above, by arguing that “Trimberger does not cure any of the aforementioned deficiencies,” “*Chiricescu* does not employ *Zavracky*’s interconnections to connect a memory die to an FPGA die,” and Petitioner does not show why

or how “the modification would have been achieved with any reasonable expectation of success.” *See* PO Resp. 46. Contrary to these arguments, as outlined above, Petitioner relies on the combined teachings of the references and the knowledge of an artisan of ordinary skill, and Trimberger provides more and persuasive evidence as to how and why an artisan of ordinary skill would have employed block memory as a single plane or several planes as separate layers in a 3-D stack, including to enhance reconfiguration speeds between a large block of memory and FPGA by facilitating a large parallel data transfer of 100,000 bits in one clock cycle.

We adopt and incorporate Petitioner’s showing for claim 25, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 52–55. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Trimberger would have rendered obvious claim 25.

F. Obviousness, Claim 26

1. Satoh

Satoh, titled “Semiconductor Integrated Circuit, Method for Testing the Same, and Method for Manufacturing the Same,” describes using an FPGA to generate test stimuli to test memory elements on the same chip.

Ex. 1008, code (54). In one embodiment, Satoh describes

a method for testing this semiconductor integrated circuit is such that, in a semiconductor integrated circuit incorporating a variable logic circuit (FPGA) for outputting a signal indicating whether or not a circuit is normal [wherein] . . . a memory test circuit is built for testing the memory circuits in accordance with

a specified algorithm . . . without using an external high-performance tester.

Ex. 1008, 46.²⁰

Satoh also describes a “memory array” and testing DRAMs (dynamic random access memory arrays) such that “a test circuit . . . for testing the DRAMs 150 to 180 is formed in the portion of the FPGA 120 . . . , and the DRAMs 150 to 180 are tested in succession.” *See* Ex. 1008, 15, Fig. 7.

2. *Claim 26*

Dependent claim 26 recites “[t]he programmable array module of claim 23 wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element.” Petitioner contends claim 26 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Satoh. *See* Pet. 60–63.

Petitioner contends that “[i]t was well-known to test stacked modules in order to avoid the expense and waste of silicon by creating ‘dead’ chips, and improve yield.” Pet. 57 (citing Ex. 1002 ¶ 241; Ex. 1009; Ex. 1043). Petitioner states that “Satoh specifically praised the use of an FPGA to test ‘memory circuits’ for ‘improving yield and productivity of the semiconductor integrated circuit.’” *Id.* (quoting Ex. 1008, 47:23–27).

Petitioner explains that Satoh describes an FPGA that “generates a specified test signal [and] supplies the test signal to the memory circuit.” Pet. 58 (citing Ex. 1002 ¶¶ 350–359; Ex. 1008, 5:1–28, 49:32–37). Petitioner maintains that Satoh’s test signal suggests a “test stimulus” to a second integrated circuit memory array to evoke a response therefrom. *See*

²⁰ Page citations refer to original page numbers.

id. (citing Ex. 1008, 49:32–37; Ex. 1002 ¶ 358). Based on Satoh’s teaching, Petitioner explains that “[i]n the Zavracky-Chiricescu-Akasaka-Satoh Combination,” it would have been obvious to implement “the test signal . . . through the contact points between the FPGA of the first IC functional element and the memory of the second IC functional element,” because that “is how those elements are stacked and electrically coupled.” *See id.* (citing Ex. 1002 ¶ 359).

In addition to avoiding “dead chips,” Petitioner cites other reasons to combine Satoh’s testing functionality with the 3-D chip of Zavracky-Chiricescu-Akasaka:

Recognizing the need to test the 3D stack of the Zavracky-Chiricescu-Akasaka Combination, the POSITA would have sought out Satoh’s teaching of using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip’s (1) additional expense, (2) chip real estate, and (3) design complexity. Ex. 1002 ¶242. Moreover, (4) a FPGA is reusable: after being configured for testing in manufacture, the FPGA would then be reconfigured for its normal “in the field” purpose. *Id.* (citing Ex. 1045 (“Another advantage . . . is that after testing is complete, the reconfigurable logic (FPGA 28) can be reconfigured for post-testing adapter card functions.”); Ex. 1046).

Pet. 57.

Petitioner also relies on the following evidence and rationale to support a reasonable expectation of success:

It was well known to use a FPGA to test circuitry with 2-D chips as taught by Satoh. Ex. 1002 ¶241 (citing Ex. 1043). The POSITA would have recognized Satoh’s teaching would readily apply to the 3-D chip elements in the Zavracky-Chiricescu-Akasaka Combination. This includes because such a combination would have been a routine use of an FPGA, whose

testing ability was not dependent on structure. Ex. 1002 ¶¶242–43. The result of this combination would have been predictable, by known FPGA testing to the 3D stack according to known methods to yield a predictable result. Ex. 1002 ¶244.

Pet. 57–58.

Patent Owner relies on the same unavailing arguments it advances with respect to the challenged claims addressed above. *See* PO Resp. 51–52 (“Because Petitioner does not contend that *Satoh* cures any of the deficiencies of the combination of *Zavracky*, *Chiricescu*, and *Akasaka*, as discussed above with respect to Ground 1, its reliance on the same rationales for Ground 3 also fail.”).

Patent Owner also argues that “Petitioner’s contention that a POSITA would be motivated to make the combination because it was well-known to test stacked die and *Satoh* tested memory elements on the same semiconductor chip (*see* Petition at 57) is divorced from the claimed invention.” PO Resp. 52. Patent Owner contends that “Petitioner’s generic rationale for using FPGAs for testing is wanting in particularity as to why a POSITA would combine the references as recited in the Challenged Claim.” *Id.* Patent Owner contends that “[w]hether the use of *Satoh*’s FPGA is beneficial for testing does not sufficiently explain why a POSITA would have combined the references to yield the claimed invention.” *Id.* at 53. Patent Owner contends that Petitioner’s rationale fails “as it lacks sufficient explanation of how or why a POSITA would have been motivated to use *Satoh*’s FPGA for testing with the hypothetical 3-D structure of *Zavracky-Chiricescu-Akasaka* ‘in the way the claimed invention does.’” *Id.* (quoting *ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)).

Patent Owner's arguments appear to accept Petitioner's showing that applying Satoh's testing structure and technique in "the hypothetical 3-D structure of *Zavracky-Chiricescu-Akasaka*" would have been "beneficial" and "predictable." *See* PO Resp. 52–53. That is, Patent Owner characterizes the rationale as "generic" without disputing it. *See id.*

In any event, Petitioner provides specific reasons related to specific recitations in the claims as outlined above, including tying Satoh's testing of a memory array using FPGA testing circuitry to the similar claim elements in claim 26. For example, using Satoh's FPGA test circuitry and memory testing teachings to avoid "dead chips" is a specific "beneficial" reason, and tying these teachings to FPGA contact points in the *Zavracky-Chiricescu-Akasaka* stack to test memory in that stack also is specific. *See* Reply 24–25 (re-listing reasons supplied in the Petition, including, for example, "the known problem of the need to test stacked modules to avoid the expense and waste of silicon by creating 'dead' chips" (citing Ex. 1002 ¶ 241; Ex. 1009; Ex. 1020; Ex. 1043); Pet. 63 (explaining that "[i]n the *Zavracky-Chiricescu-Akasaka-Satoh* Combination, the test signal is sent through the contact points between the FPGA of the first IC functional element and the memory of the second IC functional element, which is how those elements are stacked and electrically coupled" (citing Ex. 1002 ¶ 359)). As Dr. Franzon also credibly explains, Satoh's use of generating a test signal "*within* an FPGA" to test a memory array is agnostic "to the particular way in which the FPGA is stacked." *See* Ex. 1002 ¶ 245 ("The POSITA would thus have realized that Satoh could be used to solve the existing need (which was also recognized by Ex. 1043, for example) to achieve the benefits discussed above.").

In other words, Petitioner persuasively shows a reasonable expectation of success with specific reasons to combine, all supported by the record, including beneficial testing to avoid dead chips and maintain reliable memory to reconfigure the 3-D stack's FPGA post-manufacture, thereby showing how to apply the teachings to the claimed 3-D stack as suggested by Zavracky, Chiricescu, and Akasaka. Specifically, claim 26 recites "wherein said contact points are further functional to provide test stimulus from said [FPGA] to said at least second integrated circuit die element," and Petitioner persuasively applies Satoh's teachings to these contact points in order to avoid dead chips. Another set of specific and persuasive reasons to combine is "using a FPGA for testing the co-stacked memory to achieve known predictable benefits: rigorous testing while avoiding a separate testing chip's (1) additional expense, (2) chip real estate, and (3) design complexity." Pet. 57.

As Petitioner also persuasively argues, Petitioner's "evidence-backed assertions are uncontroverted, specific to relevant teachings of the references, and explain why a POSITA would have sought the Zavracky-Chiricescu-Akasaka-Satoh Combination to reach the '951 patent's claims." Reply 25 (citing Ex. 1070 ¶¶ 76–77).

Patent Owner advances a new (unresponsive) argument in its Sur-reply that "[t]he references Petitioner and Dr. Franzon cite do not disclose testing of 3D stacked processor but instead disclose that individual die are tested independently and prior to any 3D packaging." Sur-reply 22. This argument is not relevant to a claim limitation at issue here. Claim 26, a device claim, does not recite packaging, and it does not preclude

“provid[ing] test stimulus from said field programmable gate array to said at least second integrated circuit die element” prior to any packaging.

We adopt and incorporate Petitioner’s showing for claim 26, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 55–58. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Satoh would have rendered obvious claim 26.

G. Obviousness, Claim 28

1. Alexander

Alexander, titled “Three-Dimensional Field-Programmable Gate Arrays” (1995), describes “stacking together a number of 2D FPGA bare dies” to form a 3-D FPGA. Ex. 1009, 253. Alexander explains that “each individual die in our 3D paradigm has vias passing through the die itself, enabling electrical interconnections between the two sides of the die.” *Id.*

Alexander’s Figure 2 follows:

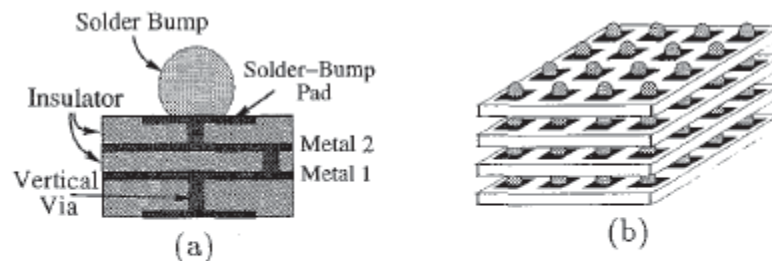


Figure 2: (a) The solder bump, pad, and vertical via geometry; and (b) stacked 2D FPGA dies.

Figure 2(a) shows vertical vias traversing a chip with a solder pad and solder bump on top, and Figure 2(b) shows a stack of chips prior to connection by solder bumps. Ex. 1009, 253.

Alexander explains that stacking dies to form a 3-D FPGA results in a chip with a “significantly smaller physical space,” lower “power consumption,” and greater “resource utilization” and “versatility” as compared to conventional layouts. Ex. 1009, 253.

2. *Claim 28*

Dependent claim 28 depends from dependent claim 27, which depends from independent claim 23, and recites “[t]he programmable array module of claim 27 wherein said third integrated circuit functional element includes another field programmable gate array.” As noted above, independent claim 23 is materially the same as independent claims 1 and 16. *Supra* § II.D.4; Pet. 49–50 (relying on its analysis for claims 1 and 16 to address claim 23). Dependent claim 27 involves materially the same analysis as claim 4 (also analyzed above), and recites “[t]he programmable array module of claim 23 further comprising: at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.” *See* § II.D.5; Pet. 50 (relying on the showing for claim 4 to address claim 27).

Accordingly, claim 28 essentially adds another FPGA to claims 23 and 27 as addressed above, requiring at least three stacked integrated circuit die elements: a memory array stacked with “another” FPGA (i.e., a total of two FPGAs), with the “integrated circuit functional elements,” which “include[]” the memory array and two FPGAs, electrically coupled together by “a number of contact points distributed through the surfaces of said

functional elements,” “wherein said memory array is functional to accelerate external memory references to said processing element [one of the FPGAs]” (as recited in independent claim 23).

Petitioner contends that claim 28 would have been obvious over the combination of Zavracky, Chiricescu, Akasaka, and Alexander. *See* Pet. 59–61. Addressing the two stacked FPGAs, Petitioner relies on Alexander’s teaching of stacked FPGAs in a 3-D package, and contends as follows:

The POSITA would have known (as Zavracky notes) that multiprocessor systems were needed for “parallel processing applications,” for example, “signal processing applications.” Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶258. But in this context, the POSTIA would have appreciated Alexander’s teaching of stacked FPGAs as preferable over alternatives, such as (1) general purpose microprocessors running software (too slow), or (2) customized parallel hardware (too expensive and inflexible). The POSITA would have sought out Alexander’s multiple stacked FPGAs to enhance the Zavracky-Chiricescu-Akasaka Combination by upgrading it for this type of application. Ex. 1002 ¶259.

Pet. 60.

Petitioner contends that Alexander’s similar structure of multiple stacked FPGAs, as similar to multiple processors stacked with multiple memories of the Zavracky-Chiricescu-Akasaka Combination, evidences a reasonable expectation of success of stacking FPGAs with memories, “with multiple functional elements stacked and vertically interconnected including using thousands of contact point vias (holes).” *See* Pet. 60. Petitioner also asserts that “[t]he result of this combination would have been predictable, simply combining the extra FPGA of Alexander with the existing 3-D stack according to known methods to yield a predictable result.” *Id.* at 61 (citing Ex. 1002 ¶¶ 260–261).

Patent Owner responds that “[w]hether 3D FPGA dies are preferable over general purpose microprocessors or customized parallel hardware have no bearing on whether a POSITA would have been motivated to combine *Alexander* with *Zavracky-Chiricescu-Akasaka* to reach a 3-D processor module having ‘a third integrated circuit functional element [that] includes another field programmable gate array.’” PO Resp. 54–55 (citing Ex. 2011 ¶ 100). This argument appears to accept Petitioner’s showing that FPGAs are preferable to processors in a 3-D stack. Petitioner’s unchallenged showing of faster FPGAs relative to general purpose processors in the 3-D stack of *Zavracky-Chiricescu-Akasaka*, where *Zavracky* contemplates multiple layers of processors, memory layers, and an FPGA, is a persuasive reason for the combination. *See* Ex. 1003, Fig. 12 (stacked multiple processor and memory layers/chips), Fig. 13 (stacked processor, memory, and PLA/FPGA layers/chips).

Patent Owner also argues that Petitioner’s “conclusory rationale is further discredited by Petitioner’s suggestions elsewhere in the Petition that *Chiricescu* discloses a FPGA application that enhances *Zavracky*.” PO Resp. 55 (citing Pet. 19). In particular, Patent Owner argues that the Petition elsewhere suggest that a “POSITA would have taken *Chiricescu*’s suggestion of a FPGA to perform ‘arbitrary logic functions,’ . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in *Zavracky*, e.g., to perform image and signal processing tasks that would have taken advantage of co-stacked microprocessors and memories as taught in *Zavracky*.” *Id.* (quoting Pet. 18). Patent Owner argues that “there is no reason . . . to combine *Alexander* with *Zavracky-Chiricescu-Akasaka*,” because “Petitioner acknowledges that,

Chiricescu, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky*'s microprocessor.” *Id.* (citing Ex. 2011 ¶ 101).

Patent Owner's arguments are unavailing. For example, Patent Owner concedes that “*Chiricescu*, like *Alexander*, offers FPGAs to enhance parallel processing image and signal tasks of *Zavracky*'s microprocessor.” PO Resp. 55. Claim 28 does not preclude employing a microprocessor, because it is open-ended and recites “comprising” and “at least” a “first,” “second,” and “third” “integrated circuit functional element.” Petitioner specifically and persuasively argues that “[t]he POSITA would have known (as *Zavracky* notes) that *multiprocessor* systems were needed for ‘parallel processing applications,’ for example, ‘signal processing applications.’” Pet. 60 (citing Ex. 1003, 12:13–28, Fig. 12; Ex. 1002 ¶ 258). And Petitioner repeatedly points to *Zavracky*'s microprocessor in Figure 13 to address claim 1, and refers to this showing in addressing claim 23. *See* Pet. 23–24 (reproducing and annotating *Zavracky*'s Figs. 12 and 13), 27 (addressing limitation [1.2], stating that “Figure 13 shows memory 808 and microprocessor 804 and 806 stacked above the programmable array”); Pet. 50 (addressing claim 23 and referring to “analysis in [1.2]”). Therefore, Patent Owner's characterization that *Chiricescu* and *Alexander* “offer[] FPGAs to enhance parallel processing image and signal tasks of *Zavracky*'s microprocessor” and Petitioner's argument that *Chiricescu* suggests FPGAs for performing arbitrary logic functions and expanding packet processing tasks with microprocessors, are specific and persuasive reasons to employ FPGAs in the stack of *Zavracky-Chiricescu-Akasaka-Alexander*. PO Resp.

55; Pet. 19. So too is simply replacing one or more of Zavracky's microprocessors with one or more preferable FPGAs for speed reasons.

In other words, as Petitioner persuasively argues, “[a]s to the ‘why,’ the Petition shows that (i) the POSITA would have been prompted to pursue a ‘multiprocessor system’ to facilitate ‘parallel processing applications’; and (ii) the POSITA would have viewed Alexander’s ‘stacked FPGAs as preferable over alternatives’ for achieving such a system.” Reply 26 (quoting Pet. 60–61; Ex. 1002 ¶¶ 257–61). “And as to the ‘how,’ the Petition explains that ‘the POSITA would have realized that using multiple FPGA dies in the stack as taught by Alexander would work in a straightforward manner similar manner to stacking multiple memories, or multiple microprocessors, as already taught in the Zavracky-Chiricescu-Akasaka Combination.’” *Id.* (quoting Pet. 60–61).

Patent Owner also alleges that the Petition fails to explain how to combine the references with a reasonable expectation of success. PO Resp. 55–57. Patent Owner alleges that “other sections of *Alexander* . . . [that] Petitioner wholly ignores . . . do not suggest . . . that using multiple FPGA dies would work in a straightforward manner, let alone in Petitioner’s proposed combination, so as to have a reasonable expectation of success.” *Id.* at 56. Patent Owner provides little support for this argument. *See id.* Contradicting Patent Owner, Alexander itself states that using multiple FPGAs in a stack results in a chip with “significantly smaller physical space,” lower “power consumption,” “shorter signal propagation delay,” and “greater resource utilization and versatility” due to the “increased number of logic block neighbors” as “compared with a circuit-board-based 2D FPGA implementation.” Ex. 1009, 253. In other words, Alexander suggests that

stacked FPGAs implement the same circuitry of well-known single layer FPGAs, with numerous advantages.

Patent Owner also refers to sections in Alexander that describe thermal issues. PO Resp. 56. Patent Owner also argues that “Petitioner’s threadbare argument that the combination is based on known methods to yield a predictable result (*see* Petition at 60–61) is . . . untethered to the features of the claimed invention.” *Id.* at 57.

Contrary to these arguments, the Petition tethers the claimed stacking of two FPGAs to several reasons to combine the references. Patent Owner itself cites these reasons offered by Petitioner, including “offer[ing] FPGAs to enhance parallel processing image and signal tasks of *Zavracky’s* microprocessor,” and similarly “perform[ing] ‘arbitrary logic functions,’ . . . as a cue to enhance and expand upon the packet processing task performed by the programmable logic device in *Zavracky*,” as noted above. *See* PO Resp. 55 (citing Pet. 19).

As Petitioner also argues, Patent Owner does not dispute that “*Zavracky* already taught combining an FPGA with a memory and microprocessor.” Reply 27 (citing Ex. 1003, 12:29–39, Figure 13). Adding another FPGA layer in place of one of *Zavracky’s* microprocessors (Ex. 1003, Figs. 12, 13) therefore would have reduced thermal problems, “because FPGAs were more energy-efficient than microprocessors for the same size die, reducing heat.” *Id.* (citing Ex. 1070 ¶¶ 37–41; Ex. 1058; Ex. 1082). Dr. Franzon’s testimony includes an excerpt from DeHon (Ex. 1058) and Scrofano (Ex. 1082), which support Dr. Franzon’s testimony that “FPGAs needed less power to get the same level of computing capability” as a processor. *See* Ex. 1070 ¶¶ 37–38 (citing Ex. 1058, 43).

Similar to Alexander's teaching that "3D FPGAs have good implications with respect to power consumption" (Ex. 1009, 263), the '951 patent also evidences that 3D stacks "overall reduced power requirements" (Ex. 1001, 4:63). Reduced power translates to less heat, as was well-known and as Petitioner shows. *See infra* note 21.

Describing dual layer FPGA stacks, the '951 patent states as follows:

It should be noted that although a single FPGA die 68 has been illustrated, *two or more FPGA die 68 may be included in the reconfigurable module 60. Through the use of the through-die area array contacts 70*, inter-cell connections *currently limited to two dimensions of a single die*, may be routed up and down the stack in three dimensions. *This is not known to be possible with any other currently available stacking techniques since they all require the stacking contacts to be located on the periphery of the die.* In this fashion, the number of FPGA die 68 cells that may be accessed within a specified time period is increased by up to $4VT/3$, where "V" is the propagation velocity of the wafer and "T" is the specified time of propagation.

Ex. 1001, 6:1–13 (emphasis added). Here, the '951 patent offers no description of any specific connection scheme between the two FPGA dies. It simply describes vias throughout the periphery of each die (instead of just at the periphery thereof) as a new technique (which is not correct), without any mention of heat problems associated with stacking two FPGAs. The '951 patent's lack of description and focus on vias throughout the whole die as a solution (providing speed gains) further evidences a reasonable expectation of success and supports Petitioner's showing.

As Petitioner also argues, thermal issues were a routine consideration, with known viable options to address the issues. Reply 27–28 (citing Ex. 1020, 11; Ex. 1070 ¶¶ 29–41; Ex. 1020; Ex. 1012; Ex. 1009; Ex. 1058;

Ex. 1082). Dr. Franzon credibly lists known ways to dissipate heat, including use of low thermal resistance substrates, forced fluid coolants, thermal vias, and thermally conductive adhesives. Ex. 1070 ¶ 32.

The record also supports Dr. Franzon’s testimony that “Alexander itself noted that thermal concerns were standard in any multi-chip design.” *Id.* ¶ 36 (citing Ex. 1009, 256 (teaching that reducing power by eliminating I/O buffers, which Dr. Franzon states mitigates thermal issues (*see* Ex. 1070 ¶ 37 n.2)).²¹ In addition to mitigating heat concerns by eliminating I/O buffers (or “restrict[ing] I/O to one layer and plac[ing] it close to the heat sink,” Ex. 1009, 256 § 5), in the same section, Alexander further supports Dr. Franzon’s testimony, stating that “[a] number of . . . thermal-reduction techniques (i.e., thermal bumps and pillars . . . , thermal gels . . . , etc.) may also be applicable for 3D FPGAs.” Ex. 1009, 255 § 5 (“Thermal Issues”). Alexander also states that “[a]s the power-to-area/volume ratio increases, so does the operating temperature unless heat can be effectively dissipated.” *Id.*

As Petitioner also persuasively reasons, Patent Owner’s arguments about heat dissipation concerns here do not undermine Petitioner’s showing of a reasonable expectation of success, because a reasonable expectation of success “does not require a certainty of success.” Reply 28 (quoting *Medichem v. Rolabo S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006)). As found above, Alexander promotes using multiple FPGAs in a module stack, and

²¹ Testimony from footnote 2 of Dr. Franzon’s declaration follows: “It would have been well known to the POSITA that in a chip, an increase in power usage generally translated to an increase in heat. For example, a processor using more power to perform computations will put off more heat than when the processor is using less power.”

myriad additional evidence further supports a reasonable expectation of success. *See id.* (citing Ex. 1002 ¶¶ 44–45 (listing prior art showing FPGA stacks or FPGA stacks with microprocessors and memory), ¶¶ 260–261; Ex. 1009, 1).

Finally, none of the challenged claims, including claim 28, specifies the size of the claimed 3-D modules or FPGAs or a corresponding amount of computing power. Therefore, the breadth of claim 28 encompasses a 3-D stack operable on a minimal power basis (and without any limit on the area of each element, further dissipating heat as the chip area increases), rendering heat concerns nonexistent or at least well within the bounds of a reasonable expectation of success. *See supra* note 21; Ex. 1009, 255–256 § 5 (discussed above, e.g., as power per unit area decreases, so does temperature).

We adopt and incorporate Petitioner’s showing for claim 28, as presented in the Petition and summarized above, as our own. Pet. 7–12, 14–22, 58–61. Based on the foregoing discussion and a review of the full record, including evidence and arguments addressed in sections above and below that may overlap with issues in the instant section due to the format of the Response, Petitioner shows by a preponderance of evidence that the combined teachings of Zavracky, Chiricescu, Akasaka, and Alexander would have rendered obvious claim 28.

H. Exhibit 1070

Patent Owner argues that “[p]aragraphs 5–9, 13–28, 29–41, 44, 45, 59–66, 68, 73, 74, 76, 77, and 94–103 from Dr. Franzon’s [Reply D]eclaration (Ex. 1070) addressing Petitioner’s alleged obviousness grounds are not sufficiently discussed in the Reply” at pages 10, 13, 20, 21, 22, 25,

and 27 of the Reply. Sur-reply 25. Patent Owner contends that the noted paragraphs are “not discussed in the Reply, but instead incorporated by citation or a cursorily parenthetical.” *Id.* Patent Owner further contends that “the Board should not and cannot play archeologist with the record to search for the arguments” and “should not . . . consider[] Dr. Franzon’s arguments.” *Id.* (citing 37 C.F.R. § 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”)).

Patent Owner also cites *General Access Solutions, Ltd. v. Sprint Spectrum L.P.*, 811 F. App’x 654, 658 (Fed. Cir. 2020), as showing that the Board “cannot ‘play[] archaeologist with the record.’” Sur-Reply 25. The situation here is different than in *Sprint Spectrum*, because there, the court noted a problem with identifying a party’s substantive arguments *prior to turning to the declaration at issue*: “*To identify GAS’s substantive arguments, the Board was forced to turn to a declaration by Struhsaker, and further to delve into a twenty-nine-page claim chart attached as an exhibit.*” *Id.* (emphasis added).

Here, Patent Owner does not describe or allege any problem with identifying Petitioner’s substantive arguments. In context, except as discussed below, the cited paragraphs of Dr. Franzon’s Reply Declaration (Ex. 1070) properly support Petitioner’s substantive arguments at the pages of the Reply identified by Patent Owner.

Regarding the first citation, page 10 of the Reply cites paragraphs 94–103 of Dr. Franzon’s Reply Declaration, and discusses how, even if the “functional to accelerate” clauses require “a wide configuration data port,” the combination of Zavracky, Chiricescu, and Akasaka teaches it. *See* Reply 9–10 (citing Ex. 1070 ¶¶ 94–103). This citation is a misprint or oversight by

Petitioner, because Dr. Franzon's Reply Declaration does not include paragraphs 96–102. Therefore, any issue with respect to those paragraphs is moot. The remaining cited paragraphs of Dr. Franzon's Reply Declaration on page 10 of the Reply directly relate to what a "wide configuration data port" constitutes. Also, paragraph 95 reproduces some of the same testimony by Dr. Chakrabarty (Patent Owner's expert in IPR2020-01021) that the Reply discusses and reproduces on page 10 of the Reply.

Regarding the second citation, page 13 of the Reply cites two paragraphs with a parenthetical as follows: "Ex. 1070 ¶¶ 73–74 (citing Ex. 1083, an example of common usage of 'share data' as 'transfer data')." Prior to the citation, the Reply addresses the plain meaning of "share," tracking the parenthetical. *See* Reply 13. Notwithstanding that Patent Owner generally implies that citation is one of several examples of "a cursorily parenthetical" (Sur-reply 25), the parenthetical is clear as to how Dr. Franzon's cited testimony supports Petitioner's Reply argument.

Regarding the third citation, page 19 of the Reply (citing Ex. 1070 ¶¶ 13–28), Petitioner's argument merely responds to a summary argument by Patent Owner about four different "TSV interconnection issues." *See* PO Resp. 41 ("At the time of the invention, a POSITA was aware of numerous []TSV interconnection issues, such as routing congestion, TSV placement, granularity, hardware description language ('HDL') algorithms, which must be considered." (citing Ex. 2011 ¶ 82; Ex. 2014, 85, 87, 89); Reply 19 ("The supposed 'TSV interconnection issues' that [Patent Owner] cursorily identifies were at most normal engineering issues, not problems preventing a combination. Ex. 1070 ¶¶ 13–28 (Dr. Franzon rebutting Dr. Souris's testimony as to every purported issue with citations to evidence)." Here,

Petitioner's parenthetical generally informs the reader that Dr. Franzon's testimony responds to Dr. Souri's "cursor[y]" summary alleging "TSV interconnection issues." *See* Reply 20; PO Resp. 41.

Paragraphs 13–20 of Dr. Franzon's Reply Declaration provide background context leading to thrust of paragraphs 21–28, which directly support Petitioner's Reply argument that TSV issues were normal engineering issues in the context of combining the references. Therefore, we consider cited paragraphs 13–20 only as background information and context.

In comparison, providing his testimony about the TSV issues, Dr. Souri's support for TSV issues is a citation to "Ex. 2014 at 85, 97, 90." Ex. 2011 ¶ 82. Patent Owner provides the same citation without any explanation of the citation. PO Resp. 41. This amounts to the same type of incorporation-by-reference of pages of evidence that Patent Owner attributes to Petitioner. Also, the cited three pages of Exhibit 2014 are in the middle of an industry article, and the pages are densely packed two-column pages that facially appear to have at least the same number of words in some of the complained-about citations to multiple paragraphs that Petitioner provides to Dr. Souri's Reply Declaration. Here, Patent Owner leaves it to the Board to dig into the cited pages of Exhibit 2014 to find the alleged TSV interconnection issues and place it in context to the background information in the whole article. In reaching our decision, we exercised judgment as to all the evidence cited by the parties for its relevance, context, and substance, and weighed it accordingly.

Finally, an examination of the other citations identified by Patent Owner in full context, reveals (like the citations addressed above) that

Petitioner's use of and citation to Dr. Souris's testimony is not improper. In summary, the remaining pages of the Reply identified by Patent Owner include citations with a clear sentence preceding the citation and/or clear parenthetical informing the reader clearly how the cited testimony supports the sentence. *See* Reply 21 n.8 (clear parenthetical and preceding sentence) (citing Ex. 1070 ¶¶ 59–66), 22 (clear preceding sentence (citing Ex. 1070 ¶¶ 44–45)), 25 (clear preceding sentence (citing Ex. 1070 ¶¶ 76–77)), 27 (clear parentheticals and preceding sentences (citing Ex. 1070 ¶¶ 37–41 and Ex. 1070 ¶¶ 29–41)).

III. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows.²² In summary:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent -able
1, 2, 4–6, 8–24, 27, 29	103(a)	Zavracky, Chiricescu, Akasaka	1, 2, 4–6, 8– 24, 27, 29	

²² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatent- able	Claims Not shown Unpatent -able
25	103(a)	Zavracky, Chiricescu, Akasaka, Trimberger	25	
26		Zavracky, Chiricescu, Akasaka, Satoh	26	
28		Zavracky, Chiricescu, Akasaka, Alexander	28	
Overall Outcome			1, 2, 4–6, 8– 29	

IV. ORDER

Accordingly, it is

In consideration of the foregoing, it is hereby

ORDERED that claims 1, 2, 4–6, and 8–29 of the '951 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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PETITIONER:

David M. Hoffman
Kenneth W. Darby Jr.
Jeffrey Shneidman
FISH & RICHARDSON P.C.
hoffman@fr.com;
k.darby@fr.com;
shneidman@fr.com
IRP42653-00301IP1@fr.com;
ptabinbound@fr.com

James M. Glass
Zyong Li
QUINN EMANUEL URQUHART & SULLIVAN LLP
jimglass@quinnemanuel.com
seanli@quinnemanuel.com

PATENT OWNER:

Jonathan S. Caplan
James Hannah
Jeffrey H. Price
KRAMER LEVIN NAFTALIS & FRANKEL LLP
jcaplan@kramerlevin.com
jhannah@kramerlevin.com
jprice@kramerevin.com