

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-00752
Patent 6,774,033 B1

Before FRANCES L. IPPOLITO, ROBERT L. KINDER, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Microchip Technology Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–17 of U.S. Patent No. 6,774,033 B1 (Ex. 1001, “the ’033 patent”). Petitioner filed a Declaration of Jack Lee, Ph.D. (Ex. 1002) with its Petition. HD Silicon Solutions LLC (“Patent Owner”) filed a Preliminary Response to the Petition (Paper 6, “Prelim. Resp.”). With the Preliminary Response, Patent Owner filed the Declaration of Bruce Gnade, Ph.D. (Ex. 2001).

After the Institution Decision (Paper 9, “Dec. on Inst.”), Patent Owner filed a Patent Owner Response (Paper 16, “PO Resp.”), a second Declaration of Bruce Gnade (Ex. 2009); Petitioner filed a Reply (Paper 18) and a Reply Declaration of Jack Lee, Ph.D. (Ex. 1020); and Patent Owner filed a Sur-reply (Paper 21, “Sur-reply”). Thereafter, the parties presented oral arguments on August 17, 2022, and the Board entered a transcript into the record. Paper 26 (“Tr.”).

For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrated by a preponderance of evidence that claims 1–7 and 9–17 of the ’033 patent are unpatentable. Petitioner has not demonstrated by a preponderance of evidence that claim 8 of the ’033 patent is unpatentable.

A. *Real Parties in Interest*

The parties identify themselves as the real parties-in-interest. Pet. 1; Paper 3, 2.

B. *Related Proceedings*

The parties indicate that the ’033 patent has been asserted in *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092 (W.D. Tex), filed November 30, 2020 (“District Court Litigation”). Pet. 1;

Paper 3, 2. On October 25, 2021, the District Court Litigation was transferred to the Northern District of California from the Western District of Texas. Ex. 3001 (Judge Albright’s Order Granting Microchip Technology Inc.’s Motion to Transfer Venue).

C. The '033 Patent

The '033 patent, titled “Metal Stack for Local Interconnect Layer,” is directed to an improved technique for forming a local interconnect layer in an integrated circuit. Ex. 1001, code (54), 1:48–50. Figure 5 of the '033 patent, reproduced below, illustrates a side cross-sectional view of an embodiment of an integrated circuit. *See* Ex. 1001, 1:65–67.

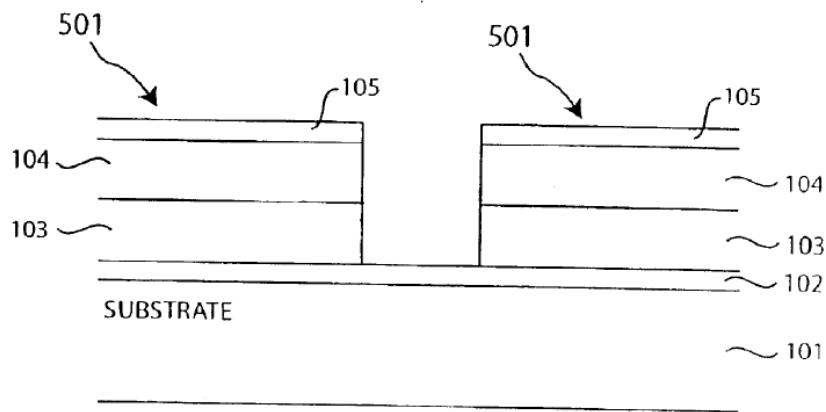


FIG. 5

As shown in Figure 5, the integrated circuit comprises substrate 101, which may be a semiconductor substrate. Ex. 1001, 2:53–54. Oxide layer 102 is deposited on substrate 101. *Id.* at 2:52–53. Film 103 is deposited over oxide layer 102. *Id.* at 2:63–64. According to the '033 patent, film 103 may comprise titanium nitride that is deposited using a sputtering process such as reactive sputtering. *Id.* at 2:64–3:1. Film 104 is deposited over film 103. *Id.* at 3:11. Film 104 may comprise tungsten and may also be deposited using a sputtering process. *Id.* at 11–13. Further, masks 105 may be formed over film 104 using conventional lithography techniques. *Id.* at 3:60–63.

Masks 105 may be a resist material, such as a negative or positive photoresist. *Id.* at 3:61–62.

In one embodiment, the '033 patent teaches that tungsten film 104 is deposited in-situ after the deposition of titanium nitride film 103. *Id.* at 3:21–22. More specifically, tungsten film 104 may be deposited using the same multi-chamber physical vapor deposition system used to deposit titanium nitride film 103. *Id.* at 3:23–25. The '033 patent explains that one advantage of this process is that depositing both tungsten and titanium nitride in-situ using the same physical vapor deposition system allows for an efficient process flow. *Id.* at 3:36–40. The '033 patent adds that another advantage is that because tungsten has a relatively low resistivity compared to titanium nitride, the metal stack may be relatively thin, while keeping resistivity relatively low. *Id.* at 3:41–44. The '033 patent teaches that a thin metal stack reduces the aspect ratio of the resulting interconnect line, thereby allowing for better sidewall and bottom coverage during deposition. *Id.* at 3:44–46.

D. Illustrative Claim

Petitioner challenges claims 1–17 (“challenged claims”), which are all of the claims of the '033 patent. Pet. 1. Claims 1 and 15 are independent. Claim 1 is reproduced below.

1. A method of forming a local interconnect layer in an integrated circuit, the method comprising:

depositing a first film over an oxide layer, the first film comprising titanium nitride; and

depositing a second film over the first film, the second film comprising tungsten, the first film and the second film forming a metal stack of the local interconnect layer.

Ex. 1001, 5:55–6:4.

E. The Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–17 would have been unpatentable on the following grounds:

Basis	35 U.S.C. §¹	Claims Challenged
Trivedi ²	103(a)	1, 9, 10, 14
Trivedi, Joo ³	103(a)	2–6, 15, 16
Trivedi, Yang ⁴	103(a)	8
Trivedi, Joo, Yang	103(a)	7
Trivedi, Lien ⁵	103(a)	2, 11, 12
Trivedi, Johnson ⁶	103(a)	13
Trivedi, Joo, Johnson	103(a)	17

See Pet. 4.

II. LEGAL STANDARDS

In *Graham v. John Deere Co.*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long-felt but unsolved needs,

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the challenged patent was filed before March 16, 2013, we refer to the pre-AIA version of § 103.

² Trivedi et al. (US 5,847,463, issued Dec. 8, 1998) (Ex. 1004).

³ Joo et al. (US 6,534,401 B2, issued Mar. 18, 2003) (Ex. 1005).

⁴ Yang et al., *A Comparison of TiN Processes for CVD W/TiN Gate Electrode on 3nm Gate Oxide*, International Electron Devices Meeting 459–462, IEEE (1997) (Ex. 1006).

⁵ Lien et al. (US 6,103,623, issued Aug. 15, 2000) (Ex. 1007).

⁶ Johnson et al. (US 6,815,959 B2, issued Nov. 9, 2004) (Ex. 1008).

failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the Federal Circuit has “repeatedly emphasized that an obviousness inquiry requires examination of all four *Graham* factors and that an obviousness determination can be made only after consideration of each factor.” *WPIP v. Kohler*, 829 F.3d 1317, 1328 (Fed. Cir. 2016) (“A determination of whether a patent claim is invalid as obvious under § 103 requires consideration of all four *Graham* factors, and it is error to reach a conclusion of obviousness until all those factors are considered.”).

We note that, with respect to the fourth *Graham* factor, the final record in this proceeding does not include any argument or evidence directed to secondary considerations of nonobviousness.

III. LEVEL OF ORDINARY SKILL IN THE ART

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus. Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends that a person of ordinary skill in the art at the time of the invention of the ’033 patent would have had the following education and experience:

at least (1) a master’s degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor’s degree in electrical engineering,

materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies.

Pet. 5. Patent Owner does not dispute this level of skill. *See generally* PO Resp.

Petitioner's proposal is reasonable and consistent with the prior art presented. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art may reflect an appropriate level of skill in the art). We accordingly adopt Petitioner's proposal, which is supported by Dr. Lee's testimony. *See* Ex. 1002 ¶ 32.

IV. CLAIM CONSTRUCTION

The Board uses “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2019); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

“[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which [it] appears, but in the context of the entire patent, including the specification.” *Id.* at 1313.

The specification may reveal a special definition given to a claim term by the patentee. *Phillips*, 415 F.3d at 1316. If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). Nonetheless, a “claim construction that excludes [a] preferred embodiment [described in the

specification] is rarely, if ever, correct and would require highly persuasive evidentiary support.” *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed. Cir. 2010) (citation omitted). But “a claim construction must not import limitations from the specification into the claims.” *Douglas Dynamics, LLC v. Buyers Prods. Co.*, 717 F.3d 1336, 1342 (Fed. Cir. 2013).

Finally, only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A. “*comprising tungsten*”

Independent claims 1 and 15 both recite “the second film comprising tungsten.”

In the Decision on Institution, we determined that “comprising tungsten” does not require a specific form of tungsten, particularly elemental tungsten. Dec. on Inst. 20–23 (citing Ex. 1001, 6:1–2, 6:47–48).

After institution, Patent Owner maintains that “comprising tungsten” requires “at least elemental tungsten.” PO Resp. 23–25. Patent Owner contends that “there is no reference to a tungsten compound” in the ’033 patent and that “the inventors of the ’033 patent describe the reasons that they chose the element tungsten.” *Id.* at 24 (citing Ex. 2009 ¶ 48). Patent Owner further contends that the ’033 patent teaches that “tungsten has low resistivity and is a stable material” and that these properties are unique to elemental tungsten. *Id.* (citing Ex. 1001, 3:41–42, 3:47–48; Ex. 2009 ¶ 48). Patent Owner adds that Petitioner’s expert, Dr. Lee, testified that the ’033 patent referenced elemental tungsten when describing chemically stable tungsten. PO Resp. 24 (citing Ex. 2010, 80:21–81:11, 82:18–83:8).

Patent Owner further asserts that a person of ordinary skill in the art (“POSITA”) would understand the language “comprising tungsten” to mean that it must have at least the element tungsten, because the ’033 patent uses the term “tungsten” when referring to that specific layer while referring to “titanium nitride” when referring to the other layer. PO Resp. 24–25 (citing Ex. 2009 ¶ 48). According to Patent Owner, “[t]he reference to an element alone in one instance (tungsten) and a compound in the other instance (titanium nitride) would inform a POSITA as to the intention for each layer.” *Id.* at 25 (citing Ex. 2009 ¶ 48). Patent Owner contends that the ’033 patent refers to “a compound when the same is intended and refers to an element when the same is intended.” *Id.* Patent Owner adds Dr. Lee acknowledged that when read in isolation, the references to tungsten in the specification could be referring to elemental tungsten. Sur-Reply 7 (citing Ex. 2010, 82:18–83:20).

In its Reply, Petitioner argues that the express language “comprising tungsten” in claim 1, “does not inform a POSITA that the claim implies a distinction between metal elements and compounds.” Pet. Reply 5 (citing Ex. 1020 ¶¶ 11–12). According to Petitioner, “the term ‘comprising’ indicates an open-ended construction . . . [that] allow[s] but does not require elemental tungsten.” Pet. Reply 2 (citing *Vehicular Techs. Corp. v. Titan Wheel Int’l, Inc.*, 212 F.3d 1377, 1382–83 (Fed. Cir. 2000)). Petitioner argues that any material, including a compound, that contains tungsten satisfies the claim language. *Id.*

Petitioner further argues that there is no reference to elemental tungsten anywhere in the ’033 patent and its file history to support PO’s construction. Pet. Reply 2 (citing Ex. 1003). Petitioner contends that “[w]hile tungsten may have low resistivity and may be stable, independent

claims 1 and 15 do not recite any such requirements.” *Id.* Petitioner adds that the ’033 patent does not suggest that tungsten compounds were undesirable. Pet. Reply 2.

We begin with the claim language. *See Allergan Sales, LLC v. Sandoz, Inc.*, 935 F.3d 1370, 1373 (Fed. Cir. 2019) (“[C]laim construction must begin with the words of the claims themselves.”) (quoting *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 457 F.3d 1293, 1301 (Fed. Cir. 2006)). Independent claims 1 and 15 both recite the open-ended transitional phrase, “comprising.” Ex. 1001, 5:55–6:5, 6:42–49. “In the patent claim context, the term ‘comprising’ is well understood to mean ‘including but not limited to.’” *CIAS, Inc. v. All. Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007). As such, we understand the phrase “comprising tungsten” to mean including but not limited to “tungsten.”

Further, consistent with Petitioner’s arguments, we do not limit the term “tungsten” to any particular form of tungsten, e.g., elemental tungsten. Independent claims 1 and 15 do not expressly recite “elemental” tungsten or indicate otherwise that elemental tungsten is required. Patent Owner directs us to passages in the ’033 patent that refer to the chemical stability, low resistivity, and hardening properties that Patent Owner contends are unique to elemental tungsten. PO Resp. 24; Ex. 2009 ¶ 48. Yet, neither independent claim recites “elemental tungsten” or these specific properties that are purportedly indicative of tungsten in elemental form. *See* Ex. 1001, 5:55–6:56.

We further observe that claim 8, which depends from independent claim 1, recites a sheet resistance that is “equal to or less than about 10 Ohm/sq.” Ex. 1001, 6:23–25. Unlike claim 8, independent claims 1 and 15 do not recite sheet resistance or other properties of the interconnect layer

that may imply “elemental” tungsten. To the extent that Patent Owner argues that other claims implicitly require a specific resistivity for a specific form of tungsten, we note that “[t]he concept of claim differentiation . . . states that claims should be presumed to cover different inventions. This means that an interpretation of a claim should be avoided if it would make the claim read like another one.” *Laitram Corp. v. Rexnord, Inc.*, 939 F.2d 1533, 1538 (Fed. Cir. 1991) (quoting *Autogiro Co. of Am. v. United States*, 384 F.2d 391, 404 (Ct. Cl. 1967)); see *Phillips*, 415 F.3d at 1314–15 (“[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.”) (citation omitted).

Patent Owner also contends that the Specification is particular in how it refers to compounds and elements. Patent Owner contends that

the claims and specification refer to “an oxide layer” rather than a layer “comprising oxygen.” (*See, e.g.*, Ex. 1001, claim 1). The claims and specification also refer to a “fluorine-based etchant” and “chlorine-based etchant” (*see* Ex. 1001 at claims 11 and 12). This choice of language becomes clear from the specification, which explains that a “chlorine-based etchant” may be a compound such as “boron trichloride” or “chlorine” only. (Ex. 1001 at 4:12-16). Thus, *the specification and claims of the ’033 patent demonstrate that particular language is used to distinguish among, a compound, an element, and either option.*

PO Resp. 25 (emphasis added).

We do recognize that “understanding the claim language may be aided by the explanations contained in the written description,” but “it is important not to import claim limitations that are not a part of the claim.” *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004). “[A] particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.” *Id.*

Our reviewing court has “cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification.”

Williamson v. Citrix Online, LLC, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015) (quoting *Teleflex, Inc. v. Ficos N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002)).

Referring to Figure 2, the '033 patent recounts the advantages of using a tungsten film 104 over titanium nitride film 103. *See id.* at 3:36–59. Similarly, in Tables 1 and 2, the '033 patent provides sheet resistance data for metal stacks of varying W/TiN⁷ thicknesses. *Id.* at 5:1–47. Still, the '033 patent also teaches that “[t]he first film may comprise titanium nitride, while the second film may comprise tungsten, *for example*.” *Id.* at 1:53–54 (emphasis added). In this way, we consider the Specification to describe the titanium nitride and elemental tungsten stack as one exemplary embodiment consistent with the broad “comprising tungsten” language recited in independent claims 1 and 15. Consistent with this understanding, the prosecution history for the '033 patent also does not discuss “elemental tungsten.” Ex. 1003; *see* Ex. 1027, 14:11–21. Thus, absent some definition or disclaimer in the intrinsic record (whether explicit or implicit), none of the claims require the overly narrow limitation argued by Patent Owner that “tungsten” must contain at least “elemental tungsten.” *See Trustees of Columbia University v. Symantec Corp.*, 811 F.3d 1359, 1363–64 (Fed. Cir. 2016).

Outside of the intrinsic evidence, “extrinsic evidence is generally [viewed] as less reliable than the patent [itself] and its prosecution history in determining how to define claim terms.” *Phillips*, 415 F.3d at 1318. Here,

⁷ Symbol “W” for tungsten and “TiN” refers to titanium nitride.

Petitioner relies on certain extrinsic evidence and contends that a POSITA would have understood that “comprising tungsten” means “containing tungsten.” Pet. Reply 5 (citing Ex. 1020 ¶¶ 14–15; Exs. 1022–1024). Patent Owner responds that “none of the references cited in Petitioner’s Reply include the phrase “comprising” much less the term “comprising tungsten.” Sur-reply 1–2. Patent Owner also argues that Petitioner relies on references that do not relate to the field of semiconductors. Sur-reply 5.

Patent Owner’s position is contradicted by the record, which includes Exhibit 1034 that clearly relates to a local interconnect. Exhibit 1034 is European Patent Application Publication No. 0463373 A2 titled “Local Interconnect Using a Material *Comprising Tungsten*.” Ex. 1034 (“Gunturi”) (emphasis added). Gunturi teaches that the phrase “comprising tungsten” includes tungsten silicide. *Id.* at 3:39–42. Relying in part on Gunturi, Petitioner’s expert, Dr. Lee, testifies that

tungsten silicide is not so different from tungsten that a POSITA would not know that tungsten silicide can be used to form a local interconnect. Trivedi, and other prior art references, e.g., Malwah (Ex.1033) and Gunturi (Ex.1034) disclose such use explicitly. *See, e.g.*, Ex.1004, 1:6-12 (stating that “the local interconnect has tungsten silicide” layer); Ex.1033, Abstract (stating that a “metal silicide layer (82) provides an additional layer of local interconnect), at 6, ll. 6-11, Figure 5 (disclosing that the “metal silicide layer 82” can be formed as a film of “tungsten silicide”); *Ex.1034, at 1, col. 1 (stating a “tungsten silicide interconnect (28) is formed on device (10) as a local interconnect between devices”)*.

Ex. 1020 ¶ 30 (emphasis added).

As such, given both the intrinsic and extrinsic record, we agree with Petitioner’s arguments and therefore do not construe “comprising tungsten”

to require elemental tungsten. No further construction of “comprising tungsten” is needed to resolve a dispute before us.

B. Other Claim Terms

Based on the final record, we determine that no other claim term requires an express construction for the purpose of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. OBVIOUSNESS OVER TRIVEDI – CLAIMS 1, 9, 10, AND 14

Petitioner asserts claims 1 and dependent claims 9, 10, and 14 would have been obvious over Trivedi. Pet. 19–33. We begin with an overview of Trivedi and then turn to the parties’ contentions.

A. Overview of Trivedi

Trivedi is titled “Local Interconnect Comprising Titanium Nitride Barrier Layer,” and generally relates to “[a] method of forming a local interconnect structure.” Ex. 1004, codes (54), (57). Trivedi discloses a local interconnect in an integrated circuit, the local interconnect having tungsten silicide and titanium nitride layers, or a tungsten layer covered on opposite sides thereof with titanium nitride. *Id.* at 1:6–12. Trivedi explains that refractory material nitrides, such as titanium nitride and tungsten nitride, are typically used as a barrier layer during an etch process. *Id.* at 1:66–2:5. Trivedi further teaches a process that “forms an interconnect structure from titanium nitride (TiN) with tungsten silicide, or from a tungsten layer covered on opposite sides thereof by titanium nitride.” *Id.* at 4:39–42. Trivedi explains that one application of its “process is used with a gate stack

and a contact to an adjacent active area in a semiconductor substrate.” *Id.* at 4:42–44.

Figure 3, reproduced below, depicts a partial cross-sectional elevation view of an interconnect structure. *See id.* at 3:56–59.

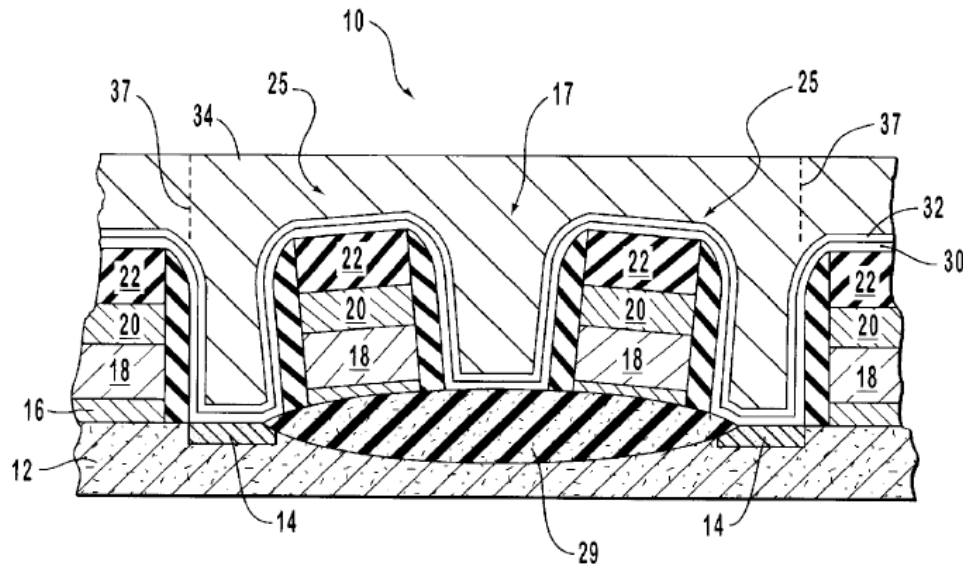


FIG. 3

Figure 3 illustrates first barrier layer 30 formed over gate contacts 25. *Id.* at 5:11–13. According to Trivedi, first barrier layer 30 is substantially composed of titanium nitride (TiN) and is formed using a conventional process such as sputtering a TiN target or sputtering a titanium target and then heating the semiconductor substrate in a gaseous nitrogen environment to form titanium nitride. *Id.* at 5:13–18. A hard mask layer 32 is then formed over first barrier layer 30. *Id.* at 5:31–32. “Hard mask layer 32 is used to assist in selectively removing material when an etching process cannot be performed with sufficient control.” *Id.* at 5:32–34. “Hard mask layer 32 is preferably formed using chemical vapor deposition (CVD) and substantially comprises material selected from the group comprising

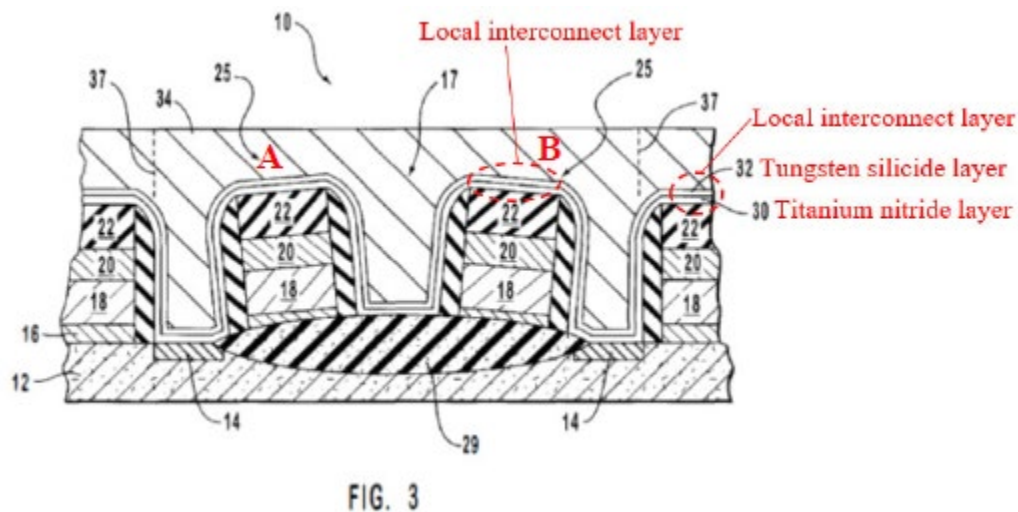
tungsten silicide, titanium-tungsten, titanium-tungsten nitride or boron nitride.” *Id.* at 5:34–38.

B. Analysis of Independent Claim 1

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 1 is unpatentable under 35 U.S.C. § 103(a) as obvious over Trivedi.

*1. “A method of forming a local interconnect layer in an integrated circuit, the method comprising”*⁸

To the extent the preamble is limiting, Petitioner asserts that Trivedi discloses a method of forming the local interconnect structure shown in Figure 3. Pet. 19–20. Specifically, Petitioner provides an annotated version of Trivedi’s Figure 3 provided below:



Pet. 20. In the annotated version of Trivedi’s Figure 3, Petitioner argues that the local interconnect can electrically connect a first gate stack A to a second gate stack B. *Id.*

⁸ Neither party addresses whether the preamble of claim 1 is limiting, but Petitioner addresses each clause of the preamble. Although we find the evidence supports that the prior art teaches the preamble, we need not make a determination that the preamble of claim 1 is limiting.

Patent Owner does not present any arguments specific to the preamble. *See generally* PO Resp. 27–33.

Based on our review and consideration of the complete record, we determine Petitioner has persuasively established that Trivedi teaches the preamble.

2. *“depositing a first film over an oxide layer, the first film comprising titanium nitride”*

Claim 1 further recites the step: “depositing a first film over an oxide layer, the first film comprising titanium nitride.” Ex. 1001, 5:57–58.

Petitioner asserts that Trivedi’s first barrier layer 30 (first film) includes a titanium nitride layer deposited over gate stacks 25, “where the gate stacks 25 include an oxide layer 16, an oxide region 29, and the TEOS [(tetraethyl orthosilicate)] layer 22.” Pet. 21.

Patent Owner does not provide arguments specific to these limitations. *See generally* PO Resp. 27–33.

Based on our review and consideration of the entire record, we agree with Petitioner’s arguments and credit the testimony of Dr. Lee because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. For example, Trivedi teaches that “First barrier layer 30 is preferably substantially composed of titanium nitride (TiN) and is formed using a conventional process such as sputtering a TiN target or sputtering a titanium target and then heating the semiconductor substrate in a gaseous nitrogen environment to form titanium nitride.” Ex. 1004, 5:13–18, Fig. 3; *see also* Ex. 1002 ¶¶ 88–89. After consideration of the contentions and the evidence of the final record, we find that Petitioner has shown that Trivedi teaches “depositing a first film over an

oxide layer, the first film comprising titanium nitride.” *See* Ex. 1001, 5:57–58.

3. “*depositing a second film over the first film, the second film comprising tungsten*”

Claim 1 further recites “depositing a second film over the first film, the second film comprising tungsten.” Ex. 1001, 6:1–2.

For these limitations, Petitioner asserts “[Trivedi’s] [l]ayer 32 (the second film) comprises tungsten (W) in the form of tungsten silicide (WSi_x), and the first barrier layer 30 comprises TiN.” Pet. 23–24 (citing Ex. 1004, Fig. 3; Ex. 1002 ¶¶ 94–95).

Patent Owner contends that Trivedi does not teach “comprising tungsten” because this limitation requires at least elemental tungsten, not a tungsten compound. PO Resp. 27–28. Patent Owner adds that Trivedi does not teach the specific mixture or stoichiometric compound for tungsten silicide (WSi_x). *Id.* at 29 (citing Ex. 2010, 59:1–8; Ex. 2009 ¶ 82). Patent Owner contends that

[a] POSITA would not have understood the claimed tungsten layer to have been met by the tungsten silicide layer of Trivedi. Of particular note, Trivedi itself establishes how different tungsten silicide is. A POSITA would understand that the purpose, composition, deposition technique, and the resistivity of the structure in Trivedi are clearly different than the structure proposed in the ’033 patent . . . For example, the purpose of the tungsten silicide (WSi_x) layer in the Trivedi patent is to be a hard mask layer to use for subsequent etching . . .

Id. (citing Ex. 2009 ¶¶ 80–81; Ex. 1004, 5:44–49). Patent Owner argues that tungsten silicide has higher resistance than pure tungsten and would thus be undesirable for a local interconnect. *Id.* at 31 (citing Ex. 2009 ¶ 83; Ex. 2010 at 71:16–72:13). Patent Owner further argues that Dr. Lee agreed a

POSITA would understand that “tungsten has lower resistivity than tungsten silicide” and “if your goal is to use lower resistivity material, a POSITA would use tungsten.” *Id.* at 30–31 (citing Ex. 2010, 71:16–72:13). Patent Owner asserts that “[a] stated benefit of the tungsten layer is that it does not significantly harden . . . [and] [t]he ’033 patent describes that the tungsten layer is used because it will keep the local interconnect thin and also provide low resistivity. *Id.* (citing Ex. 2009 ¶ 81; Ex. 1001, 3:41–44, 3:47–59). In its Sur-reply, Patent Owner relies primarily on its proposed claim construction that “comprising tungsten” requires “at least elemental tungsten.” *See* Sur-reply 4.

In its Reply, Petitioner asserts that claim 1 recites a film “comprising tungsten” not elemental tungsten. “Because tungsten-silicide comprises tungsten, a POSITA would understand that Trivedi’s tungsten-silicide layer meets the claim limitation “comprising tungsten.” Pet. Reply 7 (citing Ex. 1020 ¶ 18). Petitioner further argues that the resistivity and other alleged properties of tungsten are not dispositive because claim 1 does not recite these properties. *Id.* Petitioner also relies on the testimony of Dr. Lee that tungsten-silicide based local-interconnects also demonstrate the resistivity and other properties well-suited for forming local-interconnects. *Id.* (citing Ex. 1020 ¶¶ 30, 34).

We note first that Patent Owner’s contentions are premised on Patent Owner’s proposed construction, which we decline to adopt for the reasons set forth above. *See* § IV.A. For the reasons discussed above (*id.*), we agree with Petitioner that the claim language “comprising tungsten” does not require “at least elemental tungsten.” *Id.*

With this construction in mind, we agree with Petitioner that Trivedi’s tungsten silicide layer teaches a “second film comprising tungsten” recited

in claim 1. Consistent with Petitioner's contentions and Dr. Lee's testimony, we observe that Trivedi describes a local interconnect in an integrated circuit where the local interconnect has a tungsten silicide layer and a titanium nitride layer. Ex. 1004, 1:6–12; Ex. 1002 ¶ 62. Trivedi explains that “layer 32 is preferably formed using chemical vapor deposition (CVD) and substantially comprises material selected from the group comprising tungsten silicide, titanium-tungsten, titanium-tungsten nitride or boron nitride.” Ex. 1004, 5:34–37; *see* Ex. 1002 ¶¶ 93–95.

Moreover, we observe that Trivedi itself teaches that either tungsten silicide or elemental tungsten may be used to form the local interconnect layers. Dr. Lee notes:

Trivedi discloses “a local interconnect in an integrated circuit, and particularly to a method of making a local interconnect structure situated on an active area within a semiconductor substrate, where the local interconnect has tungsten silicide and titanium nitride layers, *or has a tungsten layer covered on opposite sides thereof with titanium nitride.*”

Ex. 1002 ¶ 59 (citing Ex. 1004, 1:6–12) (emphasis added). Thus, contrary to Patent Owner's position, Trivedi teaches that a tungsten layer in the disclosed local interconnect can use either tungsten or tungsten silicide.

Further, we do not agree with Patent Owner's arguments that tungsten silicide would not meet the requirements of claim 1 of the '033 patent because (1) Trivedi does not teach the mixture/stoichiometric make-up of tungsten silicide, and (2) tungsten silicide provides higher resistance than pure tungsten and would thus be undesirable for a local interconnect. PO Resp. 29, 31 (citing Ex. 2009 ¶ 83; Ex. 2010, 71:16–72:13); *see* Ex. 2009 ¶ 40; Ex. 1001, 3:41–59. This is because stoichiometric compounds/mixtures, low resistivity, hardness properties, chemical stability,

thermal stability, and high conductivity are not recited or required by independent claim 1.

Even assuming that tungsten silicide and tungsten have different properties, such as sheet resistance (*see* PO Resp. 27–33), there is no dispute that Trivedi expressly discloses an “inventive process forms an interconnect structure from titanium nitride (TiN) with tungsten silicide.” Ex. 1004, 4:39–40. Patent Owner’s main complaint is that Trivedi’s interconnect structure is “*undesirable*.” *See* PO. Resp. 27–28. Nonetheless, “[i]t is well settled that a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art, including non-preferred embodiments. *Merck & Co., Inc. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807 (Fed. Cir. 1989) (“all disclosures of the prior art, including unpreferred embodiments, must be considered”) (quoting *In re Lamberti*, 545 F.2d 747, 750 (CCPA 1976)).

In summary, we agree with Petitioner’s arguments and credit the testimony of Dr. Lee because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. Petitioner’s contentions are not undermined by Patent Owner’s arguments. After consideration of the contentions and the evidence of record, we find that Petitioner has shown that Trivedi teaches these limitations of claim 1 and a person of ordinary skill in the art would not have been deterred from using Trivedi’s tungsten silicide layer for the reasons set forth above.

4. “*the first film and the second film forming a metal stack of the local interconnect layer*”

Claim 1 further recites “the first film and the second film forming a metal stack of the local interconnect layer.” Ex. 1001, 6:2–4.

For these limitations, Petitioner argues “Trivedi discloses a titanium nitride layer 30 (first film) and a tungsten silicide layer 32 (second film) that are both metallic, and form a multilayer structure (metal stack) of a local interconnect structure (local interconnect layer).” Pet. 25.

Patent Owner contends that Petitioner has failed to address whether a POSITA would consider tungsten silicide to be a metal that forms a metal stack. PO Resp. 31–33. In particular, Patent Owner relies on the testimony of its expert, Dr. Gnade, to argue that tungsten silicide is usually referred to as a conductive ceramic material, not a metal. *Id.* at 32 (citing Ex. 2009 ¶ 87; Ex. 2015, Abstract). Patent Owner contends that Dr. Lee agrees that tungsten silicide could be a conductive ceramic material depending on the “x” in WSi_x . *Id.* (citing Ex. 2010, 87:14–21). “While pure tungsten has a resistivity of about 6 micro Ohm – cm, WSi_x is typically 60-80 micro Ohm-cm Most metals that are to be used as conductors are <10 micro Ohm - cm. *Id.* (citing Ex. 2009 ¶ 87). Patent Owner argues that claim 8 of the ’033 patent requires a sheet resistance of the metal stack equal to or less than 10 Ohm/sq,” but “claim 1 of Trivedi requires a sheet resistance for the WSi_x layer of 100-150 Ohm/sq.” *Id.* (citing Ex. 2009 ¶ 87).

To Patent Owner’s point, the experts agree that a POSITA would understand tungsten silicide (WSi_x) to include both a conductive ceramic material and metal silicide compound. *See* Ex. 2009 ¶ 87; Ex. 2010, 87:14–21; *see* Ex. 1020 ¶ 26. Dr. Lee testifies that “[w]hile tungsten silicide may be referred to as ‘ceramic’ . . . it is conductive . . . and it is also ‘metallic’” and contains a metal. Ex. 1020 ¶ 26 (citing Ex. 2009 ¶ 87; Ex. 2010, 87:22–25).

Additionally, Dr. Lee relies on Exhibits 1031 and 1032, to demonstrate that a POSITA would have understood tungsten silicide to form

a metal stack. Exhibit 1031 is U.S. Patent No. 6,262,450 B1 issued on July 17, 2001. Ex. 1031 (“Kotacki”). Exhibit 1032 is an article titled “Properties of Tungsten Silicide Film on Polycrystalline Silicon” published on April 30, 1981, in the Journal of Applied Physics. Ex. 1032 (“Tsai”). According to Dr. Lee, Kotacki discloses

a metal stack having a tungsten silicide layer. Ex. 1031, 4:1–6 (stating “[i]n FIGS. 6a and 6b, a metal stack 52, consisting of a first layer which is typically titanium or titanium nitride and a second metal layer which can be tungsten or tungsten silicide, is deposited on the surface by a combination of chemical vapor deposition (CVD), physical vapor deposition (PVD) or evaporation”), FIGS. 6a and 6b.

Ex. 1020 ¶ 25 (quoting Ex. 1031, 4:1–6) (emphasis added). Dr. Lee further testifies that Tsai teaches a “metallic silicide layer on poly-Si could reduce the sheet resistance” and “[e]vaporated WSi₂ is an attractive candidate for silicide device fabrication.” *Id.* ¶ 26 (citing Ex. 1032 at 5350, col. 1).

While Exhibits 1031 and 1032 are not bases for Petitioner’s unpatentability challenge, these references provide insight as to a POSITA’s background knowledge. *See Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415–22 (2007)); *see also Arendi S.A.R.L. v. Apple, Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016) (“[W]e do consider common sense, common wisdom, and common knowledge in analyzing obviousness.”). These references support Dr. Lee’s rebuttal testimony that a POSITA would understand that “WSi_x,” includes a metal silicide like WSi₂.

Dr. Lee’s testimony is also supported by Trivedi. Trivedi teaches that a [r]efractory *metal* silicide layer 20 may comprise any refractory *metal* including but not limited to titanium, *tungsten*, tantalum, and molybdenum. Preferably, refractory *metal* silicide layer 20 is substantially composed of tungsten silicide (WSi_x).

Ex. 1004, 4:52–56 (emphases added); *see* Ex. 1020 ¶ 62. Although this disclosure discusses layer 20, we note that Trivedi expressly teaches tungsten silicide (WSi_x) may be a *metal* silicide. With respect to Trivedi’s layer 32, Trivedi also refers to tungsten silicide as WSi_x , which is the same formula notation given to the *metal* silicide described for layer 20.

Ex. 1001, 4:52–56. As such, given Dr. Lee’s testimony and the background knowledge evidenced by Exhibits 1031 and 132, we agree that a POSITA would have understood Trivedi to contemplate at least the use of a metallic form of tungsten silicide when referring to WSi_x for layers 20 and 32.

Accordingly, we agree with Petitioner’s arguments and credit the testimony of Dr. Lee because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. Petitioner’s contentions are not undermined by Patent Owner’s arguments. After consideration of the contentions and the evidence of record, we find that Petitioner has shown that Trivedi teaches these limitations of claim 1.

5. Conclusion

After consideration of the contentions and the evidence of record, we find that Petitioner has shown Trivedi teaches each recitation of claim 1. Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 1 is unpatentable under 35 U.S.C. § 103(a) as obvious over Trivedi.

C. Analysis of Claims 9, 10, and 14

Petitioner contends that dependent claims 9, 10, and 14, which depend directly or indirectly from independent claim 1, would have been obvious over Trivedi, and provides explanation as to how the prior art teaches each claim. Pet. 26–33.

Claim 9 depends directly from claim 1 and further recites “etching the second film to stop on the first film; and etching the first film to stop on the oxide layer.” Ex. 1001, 6:26–29. Relying on the testimony of Dr. Lee, Petitioner argues that Trivedi discloses etching tungsten silicide layer 32 to stop at the TiN layer 30 (e.g., “etching the second film to stop on the first film.”). Pet. 28 (citing Ex. 1002 ¶¶ 105, 107; Ex. 1004, 5:55–56, 5:59–61). Petitioner quotes Trivedi’s disclosure that

[a] preferred chemical etch process for hard mask layer 32 is a dry etch. The dry etch is selective to first barrier layer 30 and only removes the exposed tungsten silicide of hard mask layer 32 over gate stack 23. First barrier layer 30 is substantially not etched by the dry etch.

Id. (citing Ex. 1004, 5:61–65; Figs. 3–4; Ex. 1002 ¶ 106).

Petitioner additionally asserts that “Trivedi discloses removing (etching) a TiN layer 30 (first film) to stop on the TEOS layer 22 (oxide layer.” Pet. 28 (citing Ex. 1002 ¶¶ 108–109). Petitioner contends that Trivedi’s Figure 5 depicts etching a TiN layer 30 (first film) such that the TEOS layer 22 (oxide layer) is exposed and not etched. *Id.* (citing Ex. 1002 ¶ 109; Ex. 1004, Fig. 5). Petitioner further contends that Trivedi discloses

a “process flow [that] selectively removes the titanium nitride of first barrier layer 30 over adjacent gate stacks 23. In this case, the preferred chemical etch is a wet etch that is selective to hard mask layer 32 comprising tungsten silicide and substantially removes only first barrier layer 30 comprising titanium nitride.”

Pet. 29 (quoting Ex. 1004, 6:6–11; Fig. 5; Ex. 1002 ¶ 110).

For claim 9, Patent Owner does not dispute Petitioner’s arguments or evidence separately from claim 1. Pet. 27–33.

We agree with and adopt Petitioner’s arguments because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. Based on the complete record now before us, we find

that Petitioner has shown that the further recitation in claim 9 is taught by Trivedi.

Claim 10 depends from claims 1 and 9, and further recites “wherein the oxide layer is over a semiconductor substrate.” Ex. 1001, 6:30–31.

Petitioner contends that “Trivedi’s oxide region 29, oxide layer 16, and TEOS layer 22 (each an oxide layer) are deposited over a ‘silicon base layer 12’ (a semiconductor substrate).” Pet. 30 (citing Ex. 1004, 4:45–60, Figs. 1–3; Ex. 1002 ¶ 113). Additionally, Petitioner asserts that “Trivedi discloses ‘a semiconductor substrate 10 having a silicon base layer 12’ and that overlying the ‘silicon base layer 12 is oxide layer 16.’” *Id.* at 31 (citing Ex. 1004, 4:45–48, Figs. 1–3; Ex. 1002 ¶ 114).

Patent Owner does not dispute separately Petitioner’s arguments or evidence regarding the further recitation in claim 10. Pet. 27–33.

We agree with and adopt Petitioner’s arguments because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. Based on the complete record now before us, we find that Petitioner has shown that the further recitation in claim 10 is taught by Trivedi.

Claim 14 depends from claim 1 and further recites “depositing a resist material over the second film.” Ex. 1001, 6:40–41.

Petitioner contends that “Trivedi discloses depositing a photoresist layer 34 (resist material) over a tungsten silicide layer 32 (second film).” Pet. 32 (citing Ex. 1004, 5:53–54, Fig. 3; Ex. 1002 ¶¶ 84–100, 117–119).

Patent Owner does not dispute separately Petitioner’s arguments or evidence regarding the further recitation in claim 14. Pet. 27–33.

We agree with and adopt Petitioner’s arguments because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the

evidence of record. Based on the complete record now before us, we find that Petitioner has shown that the further recitation in claim 14 is taught by Trivedi.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claims 9, 10, and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Trivedi.

D. Obviousness over Trivedi and Joo – Claims 2–6, 15 and 16

Petitioner contends claims 2–6, 15 and 16 would have been obvious over the combination of Trivedi and Joo. Pet. 33–49.

1. Overview of Joo

Joo is titled “Method for Selectively Oxidizing a Silicon/Metal Composite Film Stack,” and generally relates to the field of semiconductor manufacturing and discloses a method and apparatus for the selective oxidation of a composite silicon/metal film. Ex. 1005, code (54), Abstract, 1:7–10. Figure 4A of Joo, reproduced below, is a cross sectional view of a semiconductor wafer substrate prior to a selective oxidation process. *Id.* at 1:55–57.

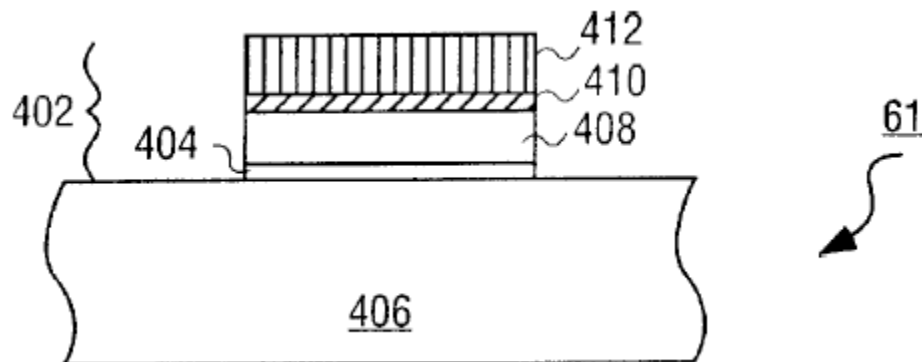


Figure 4A illustrates composite gate electrode 402 formed on gate insulating layer 404 such as silicon oxide or silicon oxynitride which in turn is formed

on doped silicon substrate 406. *Id.* at 4:53–55. “As shown in Figure 4A, composite gate stack 402 includes lower polycrystalline silicon film 408 formed on gate insulating layer 404, tungsten nitride (WN_x) barrier layer 410 disposed on lower polysilicon layer 408 and tungsten metal layer 412 disposed on tungsten nitride barrier layer 410.” *Id.* at 4:57–62. “The purpose of tungsten metal layer 412 is to provide a low resistance film in order to reduce the overall resistance of composite gate electrode 402.” *Id.* at 4:62–64. According to Joo, “[t]he purpose of the tungsten nitride (WN_x) barrier layer 410 is to prevent the interaction between silicon film 404 and tungsten film 410 during high temperature processing so that the tungsten film does not react with the silicon film and form an undesired higher resistance (WSi_x) film.” *Id.* at 4:64–5:2.

2. *Analysis of Claim 2*

Claim 2 depends from claim 1 and further recites “the first film and the second film are deposited in-situ.” Ex. 1001, 6:5–6.

a) *Petitioner’s Contentions*

For these limitations, Petitioner relies on the combination of Trivedi and Joo. Specifically, Petitioner contends that Joo teaches TiN layer 410 and tungsten film 412 “can both be deposited by PVD or both be deposited by CVD.” Pet. 33 (citing Ex. 1002 ¶¶ 84–100, 122–127, 131–133; Ex. 1005, 5:12–15, 5:22–25). Petitioner adds that a POSITA would have understood: (1) “two layers, when deposited by the same process, can be deposited using the same cluster tool, or even in the same chamber, e.g., in situ”; and (2) “manufacturing efficiency can be improved in terms of time and/or effort by avoiding movement of the partially formed semiconductor material from one chamber or tool to another.” Pet. 33–34 (citing Ex. 1002 ¶ 133).

b) Patent Owner's Contentions

Patent Owner relies on its arguments presented for ground 1 and further contends that ground 2 lacks “motivation to combine Trivedi and Joo because Joo does not relate to a local interconnect.” PO Resp. 33. Patent Owner contends a POSITA would not have been motivated to combine Trivedi and Joo because Joo relates to gate electrodes and not a local interconnect. *Id.* (citing Ex. 2009 ¶ 89). Patent Owner argues that a POSITA would consider gate electrodes and local interconnects to be distinct and would not look to one to solve a problem in the other because semiconductor industry roadmaps had separate chapters for Front End Processes (Ex. 2012) and Interconnect (Ex. 2013) in 2001, around the time of the invention. *Id.* (citing Ex. 2009 ¶ 89). According to Patent Owner, “[a]round the time frame of the ’033 patent, gate stack development was a very specific problem, and there would be no reason for a POSITA working on interconnect to consider gate stack as a possible solution for local interconnect.” *Id.* at 34 (citing Ex. 2009 ¶ 33).

Patent Owner further contends that the prosecution history supports the notion that gate electrode prior art is distinct from local interconnect prior art. PO. Resp. 34. Patent Owner asserts that, during prosecution, the Applicant explained, and the Examiner agreed, that “Fujiwara relates to a gate electrode, not a local interconnect.” *Id.* at 34–35 (citing Ex 1003, 37). Patent Owner concludes that Joo’s disclosure regarding gate electrodes is like that of Fujiwara’s addressed during examination and, therefore, should not be applied to the local interconnect methods taught in Trivedi or claimed in the ’033 patent. *Id.*

Additionally, Patent Owner contends that using the same PVD or CVD process for two different films does not suggest depositing two

different films “in-situ.” PO Resp. 37. Patent Owner contends that the Petition does not point to any disclosure in Joo or Trivedi that discloses using the same chamber. *Id.* at 38. Patent Owner argues that “the same PVD or CVD process could be used in two separate/isolated PVD chambers or two separate/isolated CVD chambers. Such a process would not constitute ‘in-situ.’” *Id.*

c) Non-analogous Art

Initially, we note that Patent Owner contends Joo’s gate electrode disclosure is inapplicable to local interconnect fabrication. PO Resp. 34–36. Patent Owner has not argued that Joo is non-analogous art, nor has Patent Owner addressed either test for non-analogous art. *See generally PO Resp.* Specifically, Patent Owner has not addressed whether Joo is within the same field of endeavor as the claimed invention or whether Joo is otherwise reasonably pertinent to the problem faced by the inventor. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Rather, Patent Owner contends that gate electrodes are different from local interconnects. *See PO Resp.* 7–11, 33–36.

In any event, we agree with Petitioner that Joo is in the same field of endeavor as the ’033 patent. In the Background, the ’033 patent states that present invention relates to “integrated circuits, and more particularly to integrated circuit fabrication processes and structures.” Ex. 1001, 1:5–8. Similarly, Joo is directed to “the field of semiconductor manufacturing and more specifically to a method and apparatus for the selective oxidation of a composite silicon/metal film.” Ex. 1005, 1:5–10. Moreover, Joo states that its described processes and “composite film need not necessarily be used to form a gate-electrode but can be used to form other device features such as but not limited to capacitor electrodes and interconnects.” Ex. 1005, 5:41–

45; Ex. 1002 ¶ 123 (emphasis added). Dr. Lee further explains that “a POSITA would have understood and appreciated that ‘other device features’ that are not ‘capacitor electrodes and interconnects’” include local interconnects.” Ex. 1002 ¶ 37. Dr. Gnade’s cross-examination testimony is consistent in this regard. Dr. Gnade acknowledged that Joo’s composite film is “just a metal film” and what “you use it for would depend on what properties you need.” Ex. 1027, 27:12 – 28:7.

We are not persuaded otherwise by the prosecution history. Patent Owner contends that the “applicant advised the Examiner that ‘gate electrodes and local interconnects have very different process requirements’” and that in its December 16, 2003 response, the applicant distinguished the prior art on the sole basis that ‘Fujiwara does not disclose or suggest the formation of a local interconnect layer.’” PO Resp. 34 (citing Ex 1003, 37).

Joo is *not* Fujiwara. Joo explicitly teaches that its disclosure applies to interconnects and other device features. *See* Ex. 1005, 5:41–45. Patent Owner has not explained why we must ignore the express teachings of Joo because, a completely separate reference, Fujiwara, was discussed during prosecution. *See* PO Resp. 33–35.

We thus, conclude that Joo is analogous art to the field of endeavor of the ’033 patent.

d) *“the first film and the second film are deposited in-situ.”*

First, we observe the meaning of “in-situ” is not dispositive. Patent Owner contends the term means deposited in the same chamber, or in chambers that are connected through a central chamber. PO Resp. 36 (citing Ex. 2009 ¶ 50). Dr. Lee agrees. Ex. 2010, 89:13–23; *see also* Tr. 20:8–12

(Petitioner’s counsel, Mr. Dutta, confirming that “as far as in-situ is concerned, I don’t think the parties are that far apart in our understanding in that as long as, you know, the reference is disclosing the ability for a wafer to be processed in the same chamber, that would satisfy in-situ.”).

Second, as we noted in the Decision on Institution, Joo expressly teaches in-situ deposition where

[c]omposite gate electrode 402 can be formed by first blanket depositing onto a gate insulating layer 404 an amorphous or polycrystalline silicon film by well-known techniques such as by chemical vapor deposition (CVD) or by physical vapor deposition (PVD) to a thickness between 200-800 Å. The silicon film can be undoped but is preferably doped to concentration level greater than 1×10^{19} atoms/cm³. The silicon film can be doped *in situ* (*i.e., during the deposition of the silicon film*) or can be subsequently doped after deposition by for example ion implantation. Next, a tungsten nitride barrier layer can be blanket deposited onto the silicon film 408 by well-known techniques such as by PVD or CVD.

Ex. 1005, 5:3–15 (emphasis added); *see* Dec. on Inst. 35–36. We further noted Dr. Lee’s testimony that “[a] POSITA would have been motivated to use a single chamber because as Trivedi teaches, there are no intervening layers between the tungsten nitride layer 30 and the tungsten silicide layer 32 (*see* Ex.1004, FIG. 3) and, as such, using a single chamber can improve manufacturing efficiency.” Ex. 1002 ¶ 135.

Patent Owner does not address Joo’s disclosure in column 5, lines 3 through 15 other than to point out that Joo does not explicitly teach the same chamber. *See* PO Resp. 37–38. However, Patent Owner does not disagree that the term “in-situ” used in Joo also suggests deposition in the same chamber. *Id.* In fact, Dr. Gnade acknowledges that in the mid-1990s, “in-situ deposition could be done in a single chamber.” Ex. 2009 ¶ 96. Rather,

Patent Owner finds fault in the fact that Joo may also teach PVD/CVD processes in two separate/isolated chambers. *Id.* at 38.

But the disclosure of one does not detract from other. Based on the complete record, we maintain that this cited passage (Ex. 1005, 5:3–15) supports Dr. Lee’s testimony that a POSITA would have understood that Joo teaches in-situ processes and that when combined with Trivedi, the two layers could be deposited by the same process described in Joo, which may occur in the same chamber or connected chambers, such as the doping of the silicon film during deposition. *See* Ex. 1002 ¶ 133; *see* Ex. 2009 ¶ 96. Moreover, we note that Patent Owner does not disagree with Dr. Lee’s testimony that “using a single chamber can improve manufacturing efficiency.” Ex. 1002 ¶ 135; *see* PO Resp. 33–35.

Third, we are not persuaded by Patent Owner’s arguments that Petitioner has not offered articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined the teachings of Trivedi and Joo in the manner recited in claim 2. Patent Owner contends that “Petitioner provides only conclusory arguments in support of a motivation to combine the Joo patent, describing a gate electrode, with Trivedi, directed to a local interconnect.” PO Resp. 33.

We disagree. Joo expressly states that “[t]he present invention relates to the field of semiconductor manufacturing and more specifically to a method and apparatus for the selective oxidation of a composite silicon/metal film.” *See* Ex. 1005, 1:7–10. Moreover, Joo explicitly applies its teachings to interconnects and other device features. Ex. 1005, 5:41–45; Ex. 1002 ¶ 123. Consistent with this explicit disclosure, Dr. Lee testifies that “[a] POSITA would have understood and appreciated that ‘other device

features’ that are not ‘capacitor electrodes and interconnects’ include local interconnects.” Ex. 1020 ¶ 37.

Dr. Gnade testifies that the “2001 version of the International Technology Roadmap for Semiconductors (ITRS) has separate chapters for Front End Processes (Ex. 2012) and Interconnect (Ex. 2013).” Ex. 2009 ¶ 32; *see also* Sur-reply 10 (“Petitioner does not address that the semiconductor industry placed gate stacks and local interconnects in separate roadmap chapters.”). Based on this, Dr. Gnade testifies that “there would be no reason for a POSITA working on interconnect[s] to consider gate stack as a possible solution for local interconnect.” *Id.* ¶ 33. Dr. Gnade does not explain sufficiently, however, why the arrangement or content of the chapters in the Roadmap detract from Joo’s explicit disclosure that contradicts his testimony. *See* Ex. 2009 ¶¶ 32–38. Indeed, under cross-examination, Dr. Gnade conceded that Joo’s disclosure of a composite film “could be used as, I guess, both a gate electrode and a capacitor electrode or an interconnect . . . it’s just a metal film . . . so what you use it for would depend on what properties you need.” Ex. 1027, 27:24 – 28:7. Thus, in this regard, we determine Dr. Lee’s testimony to be more credible, supported by the record, and entitled to greater weight.

Additionally, Dr. Gnade asserts that Joo cautions against using WSi_x . Specifically, Dr. Gnade contends that Joo teaches that

[i]t is to be appreciated that if not cured, when exposed to a hydrogen rich ambient the barrier layer would break down causing the undesired reaction between silicon film 408 and tungsten film 412 which would lead to undesired formation of tungsten silicide and resulting increase in resistance and degradation in performance.

Ex. 2009 ¶ 90 (citing Ex. 1005, 8:3–9). Dr. Gnade adds that “Dr. Lee and the Petition do not address why a person of ordinary skill in the art would be motivated to combine Joo and Trivedi when Joo cautions against the formation of a tungsten silicide layer as used by Trivedi.” *Id.* ¶ 91; *see also* Sur-reply 7–8 (“[T]he Petition fails to address why a POSITA would be motivated to combine Joo and Trivedi and that Joo cautions against the formation of a tungsten silicide layer as used by Trivedi.”).

For claim 2, Petitioner relies upon Trivedi for the formation of the tungsten-silicide layer (second film) recited in independent claim 1. Pet. 21–26. Petitioner relies upon Joo solely for the teaching that “the TiN layer 410 (first film) and the tungsten film 412 (second film) can both be deposited by PVD or both be deposited by CVD.” *Id.* at 33 (citing Ex. 1002 ¶¶ 84–100, 122–127, 131–133; *see* Ex. 1005, 5:12–15, 5:22–25). With this in mind, we understand that Petitioner relies on Trivedi’s intentional formation of a tungsten-silicide layer in combination with Joo’s film deposition techniques.

Joo does caution against the *unintentional* formation of tungsten-silicide in its disclosed structures. Ex. 1005, 8:3–9. This happens when the titanium nitride barrier is not cured and exposed to a hydrogen rich ambient. *Id.* at 8:3–4. Joo teaches that the “barrier layer would break down causing the *undesired reaction between silicon film 408 and tungsten film 412* which would lead to *undesired formation of tungsten silicide* and a resulting increase in resistance and degradation in performance.” *Id.* at 8:4–9 (emphases added).

The key here is that Joo teaches the formation of tungsten silicide is undesirable in this specific situation because the tungsten silicide results from a reaction between silicon film 408 and tungsten film 412 caused by a breakdown of the barrier layer. *Id.* Joo does not discourage Trivedi’s

process of intentionally depositing tungsten silicide to form a local interconnect layer. Instead, Joo cautions against the *undesired breakdown* of the tungsten nitride barrier layer that can lead to undesirable interactions between silicon film 408 and tungsten film 412. Read in context, we do not find that Joo's disclosure undercuts the proposed motivation to combine because a POSITA would understand Trivedi intentionally forms tungsten silicide through deposition, which is a different process from an undesired breakdown of a barrier layer.

Patent Owner further argues a POSITA would not combine Trivedi and Joo because Trivedi's films are deposited on an oxide layer and the films in Joo's gate electrodes are deposited on polysilicon. PO Resp. 35–36. Petitioner counters that around and before 2000, polysilicon was also used to form gate-electrodes and local interconnects. Pet. Reply 12.

We agree with Petitioner. Dr. Lee's and Dr. Gnade's testimonies are aligned in this instance. Both experts confirm that polysilicon was used for gate electrode fabrication. Ex. 1020 ¶¶ 45–46; Ex. 1027, 15:9–25 (acknowledging polysilicon-gate fabrication); Ex. 2009 ¶ 31; Ex. 1028, 11–12, 45–46 (disclosing polysilicon-gate fabrication). Both agree that polysilicon was used to form local interconnects. Ex. 1020 ¶ 47 (citing Ex. 1038, Abstract; Ex. 1039, 3:26–43, 4:54–58, Figs. 1, 2, and 8; Ex. 1040, 1:53–56); Ex. 1027, 16:10–13 (“Q: So before 2002, is it your understanding that polysilicon was used to form a local interconnect as well? A: In some instances, yes.”). Thus, on this point, the record better supports Petitioner's position that a POSITA would not distinguish between oxide and polysilicon layers for gate electrode or local interconnect fabrication.

Further, as discussed above, we are not persuaded that prosecution history statements regarding a separate reference, Fujiwara, necessarily limit

the disclosure in Joo. Even assuming that “Fujiwara relates to a gate electrode, not a local interconnect,” this does not in turn require us to find that Joo’s disclosure is the same, especially where Joo’s teachings explicitly apply to interconnects and other device features. *See* PO Resp. 34–35 (citing Ex 1003, 37).

After consideration of the contentions and the evidence of record, we find that Petitioner has shown that the combination of Trivedi and Joo teaches each recitation of claim 2. We are also persuaded that Petitioner has offered articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined the teachings of Trivedi and Joo in the manner recited in claim 2.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 2 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Trivedi and Joo.

3. *Analysis of Claim 3*

Claim 3 depends from claim 1, and further recites “the first film and the second film are deposited using a sputtering process.” Ex. 1001, 6:7–8.

For these limitations, Petitioner contends that “Joo discloses that the TiN layer 410 (first film) and the tungsten film 412 (second film) can both be deposited by PVD, which has been a well-known sputtering process since before 2002.” Pet. 35 (citing Ex. 1002 ¶¶ 84–100, 122–127, 138–140). Petitioner adds that “[i]n the context of forming local interconnect structures, Trivedi relates PVD to sputtering.” *Id.* at 36 (citing Ex. 1002 ¶ 143; Ex. 1004, 1:32–36).

In its Sur-reply, Patent Owner contends that Petitioner does not adequately explain why a POSITA would apply the PVD process disclosed

in Joo to Trivedi's tungsten silicide layer when Trivedi discloses that the tungsten silicide hard mask layer is "preferably formed" using chemical vapor deposition (CVD) to provide "good step coverage." Sur-reply 8 (citing Ex. 1004, 5:33–37).

Patent Owner concedes that "Trivedi was aware of the PVD process because it does use the PVD technique for its titanium nitride layer and states that the TiN layer 'is formed using a conventional process such as sputtering.'" Sur-Reply 8 (citing Ex. 1004, 5:14–16). However, Patent Owner argues that Trivedi indicated a preference for a CVD tungsten silicide layer.

While Trivedi may have expressed a preference for CVD with the tungsten silicide layer, we find that Trivedi also teaches the PVD process to form layers in the local interconnect. A prior art reference is analyzed from the vantage point of all that it teaches one of ordinary skill in the art. *See In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968) ("The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain.").

We are mindful that Petitioner's proposed combination of Trivedi with Joo's processes may very well result in a tradeoff between Trivedi's preferred CVD process and the increased manufacturing efficiencies via the in-situ technique. *See* Ex. 1002 ¶ 135. "[O]bviousness must be determined in light of all the facts . . . [and] a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006). Here, there is evidence in the record that the tradeoff is minimal. Dr. Lee testifies that

PVD is a well established process, and it can be designed to achieve excellent step coverage. So the – now of course, you know, whether Trivedi – Trivedi had choose CVD for the purpose -- for the advantage of step coverage and but the person of ordinary skill in the art would understand that PVD would be able to achieve a very good, excellent step coverage as well.

Ex. 2017, 45:9–17. Patent Owner does not dispute Dr. Lee’s testimony and instead contends that Trivedi’s CVD process is preferred. Nonetheless, a reference is not limited to its preferred embodiment, but must be evaluated for all of its teachings, including its teachings of non-preferred embodiments. *See In re Burckel*, 592 F.2d 1175, 1179 (CCPA 1979).

After consideration of the contentions and the evidence of record, we find that Petitioner has shown that the combination of Trivedi and Joo teaches each recitation of claim 3. Also, we are persuaded that Petitioner has offered articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined the teachings of Trivedi and Joo in the manner recited in claim 3.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Trivedi and Joo.

4. *Analysis of Claim 15*

Independent claim 15 is directed to a method of forming a local interconnect layer in an integrated circuit, the method including the steps:

sputtering a first film over an oxide, the first film comprising titanium nitride; sputtering a second film over the first film in a same tool employed to sputter the first film, the second film comprising tungsten, the first film and the second film forming a metal stack of the local interconnect layer.

Ex. 1001, 6:44–50.

For these limitations, Petitioner relies on the arguments presented with respect to claims 1–3. *See* Pet. 43 (“Joo teaches ‘sputtering’ the titanium nitride film (first film) as set forth for Claim 3 under this Ground”), 44 (“Also, Claim 2 recites that the first and second films are deposited ‘in-situ’ and Element 15[b] recites ‘in a same tool.’ A POSITA would have understood these respective requirements of Claim 1[b]/Claim 2 and Element 15[b] to be substantially the same. (Ex.1002, ¶173.)”).

Patent Owner relies on the arguments presented for claims 1 and 2. *See* PO. Resp. 38–39 (“[T]he Petition argues that a POSITA would have understood the limitation ‘in the same tool’ of Claim 15 to be the substantially the same as the *in-situ* limitation of Claim 2. (Paper No. 1 at 44). As explained above, the same technique PVD or CVD could be used, but in different chambers. Joo does not disclose in-situ deposition nor the same tool. Petitioner’s arguments that a POSITA would be motivated to use the same tool are, at best, conclusory and Ground 2 fails for at least that reason.”).

Similar to our consideration of Patent Owner’s arguments with respect to claim 2, we determine that Petitioner relies on Joo’s general teaching regarding semiconductor manufacturing, which describes in-situ doping of the silicon film during deposition. *See* Ex. 1005, 5:3–15. Additionally, for the reasons discussed above with respect to similar limitations recited in claims 1–3, we determine that Petitioner has shown that the combination of Trivedi and Joo teaches each recitation of claim 15. Also, we are persuaded that Petitioner has offered articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined the teachings of Trivedi and Joo in the manner recited in claim 15. As such we adopt the Petitioner’s reasoning and supporting evidence. *See* Pet. 41–45.

Additionally, Patent Owner's arguments presented for claims 1–3 are addressed above. For the same reason discussed above, Petitioner's contentions are not undermined by Patent Owner's arguments.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Trivedi and Joo.

5. *Analysis of Claims 4, 5, 6 and 16*

Claim 4 depends from claim 1 and further requires that the first film and the second film form “a metal stack having a thickness equal to or less than about 600 Angstroms.” Ex. 1001, 6:10–12.⁹

Claim 5 depends from claim 1 and further recites “the first film is deposited to a thickness equal to or less than about 300 Angstroms.” Ex. 1001, 6:13–15.

Claim 6 depends from claim 1 and further recites “the second film is deposited to a thickness equal to or less than about 300 Angstroms.” Ex. 1001, 6:16–18.

Claim 16 depends from claim 15 and further recites, “the first film and the second film form a metal stack having a thickness equal to or less than about 600 Angstroms.” Ex. 1001, 6:50–52.

Petitioner makes similar arguments for each of these dimensional limitations recited in dependent claims 4–6 and 15. *See* Pet. 37–41, 45–46. For example, with respect to claim 4, Petitioner asserts Joo teaches that titanium nitride may be used as a barrier metal instead of tungsten nitride. Pet. 40 (citing Ex. 1005, 5:36–39; Ex. 1002 ¶ 156). According to Petitioner,

⁹ Certificate of Correction.

Joo teaches that the “tungsten nitride barrier layer is preferably formed as thin as possible, less than 100 Å” and that the “tungsten nitride barrier” can have a “thickness between 25-75 Å.” *Id.* at 56 (citing Ex. 1005, 5:15–22, Fig. 4A; Ex. 1002 ¶ 156). Petitioner adds that Joo discloses the “tungsten film is blanket deposited over tungsten nitride barrier 410 . . . to a thickness between 200-700 Å.” *Id.* at 55 (citing Ex. 1005, 5:22–25; Fig. 4A; Ex. 1002 ¶ 156). Petitioner relies on the same or similar arguments for claims 5, 6, and 16. Pet. 39–41, 45–46.

Patent Owner responds that Petitioner has not sufficiently explained why a POSITA would modify the thickness of a local interconnect to the thickness of layers in Joo’s gate electrode. PO Resp. 40–41; *see* Sur-reply 9–10. Patent Owner contends that a POSITA would not apply the thicknesses of Joo’s gate electrode to Trivedi’s local interconnect layers because these thicknesses would not lead to predictable results in a local interconnect. *Id.* at 40 (citing Ex. 2009 ¶ 99). Patent Owner further asserts that “the thicknesses of gate stacks and local interconnects were known to be different around the time of the invention. In 2001, a typical gate electrode thicknesses would be 65-130 nm (which is 650-1300Å).” *Id.* (citing Ex. 2009 ¶ 35; Ex. 2012, 20, Table 51a). Dr. Gnade further testifies that “a person of ordinary skill in the art would not be motivated to use the thickness disclosed in Joo for its tungsten layer and apply it to the tungsten silicide layer disclosed in Trivedi because Joo cautions away from the formation of a tungsten silicide layer.” Ex. 2009 ¶ 99.

Based on the complete record, we agree with Petitioner. We observe first that Joo’s disclosed film/layer thicknesses overlap with the ranges claimed in claims 4, 5, 6, and 16.

Regarding claim 4, the first film and the second film form “a metal stack having a *thickness equal to or less than about 600 Angstroms*.” Ex. 1001, 6:10–12 (emphasis added). As Petitioner observes, Joo teaches that “the composite gate stack 402 includes . . . a tungsten nitride (WN_x) barrier layer 410” and “a tungsten metal layer 412 disposed on the tungsten nitride barrier layer 410.” Ex. 1005, 4:57–62, Fig. 4A; Ex. 1002 ¶ 150. Joo further discloses that titanium nitride (TiN) may be used instead of tungsten nitride for barrier layer 410. Ex. 1005, 5:36–39; Ex. 1002 ¶ 150. Joo also teaches that the barrier layer is preferably formed as thin as possible, less than 100 Å and that the “tungsten film is blanket deposited over tungsten nitride barrier 410 . . . to a thickness between 200-700 Å.” Ex. 1005, 5:22–25, Fig. 4A; Ex. 1002 ¶ 150. Together these disclosed thicknesses overlap with the claimed range of equal to or less than 600 Angstroms – a TiN layer less than 100 Å with a tungsten film between 200-700 Å.

Similarly, claim 16 depends from claim 15 and recites the same thickness range: “the first film and the second film form a metal stack having a thickness equal to or less than about 600 Angstroms.” Ex. 1001, 6:50–52. As with claim 4, we agree with Petitioner that Joo discloses an overlapping thickness range based on Joo’s teaching of a TiN layer less than 100 Å thickness with a tungsten film between 200-700 Å thickness.

The same applies to claim 5, which depends from claim 1 and further recites “the first film is deposited to a thickness equal to or less than about 300 Angstroms.” Ex. 1001, 6:13–15. Joo teaches that the TiN layer is less than 100 Å, which overlaps with the range claimed in claim 5.

Likewise, Joo’s teaching of a tungsten film with a thickness range between 200-700 Å overlaps with claim 6’s second film thickness of “equal to or less than about 300 Angstroms.” Ex. 1001, 6:16–18.

Next, we find that Joo explicitly states that its disclosure applies broadly to the field of semiconductor manufacturing and that its films can be used to form interconnects or other device features. More specifically, Joo states:

It is to be appreciated that although the selective oxidation process of the present invention is ideally suited for selectively oxidizing a composite polysilicon/tungsten nitride/tungsten gate electrode stack 402 shown in FIG. 4A, *the present invention is equally useful for selectively oxidizing other composite silicon/barrier metal/metal film stacks.* For example, *although barrier metal 410 is preferably tungsten nitride (WN_x) other suitable barrier metals such as but not limited to titanium nitride (TiN) may be used.* Similarly, although metal layer 410 is preferably tungsten (W) other metal layers such as but not limited to cobalt (Co) and titanium (Ti) maybe used. Still further *it is to be appreciated that the composite film need not necessarily be used to form a gate electrode but can be used to form other device features such as but not limited to capacitor electrodes and interconnects.*

Ex. 1005, 5:30–45 (emphases added). As such, we determine that Joo’s express disclosure contradicts Patent Owner’s arguments and Dr. Gnade’s testimony that a POSITA would read Joo so narrowly as to limit Joo’s teachings to only gate electrode fabrication. PO Resp. 40–41; *see* Ex. 2009 ¶ 99. Joo’s express disclosure supports Dr. Lee’s testimony that “[a] POSITA would have understood and appreciated that ‘other device features’ that are not ‘capacitor electrodes and interconnects’ include local interconnects.” Ex. 1020 ¶ 37. Moreover, we note again that Dr. Gnade’s cross-examination testimony acknowledges Joo’s composite film can be used for other devices depending on the properties needed. *See* Ex. 1027, 27:12–28:7.

We also are not persuaded by Patent Owner's arguments that gate electrodes and local interconnects must have different film/metal stack thicknesses. Patent Owner cites to Dr. Gnade's testimony that typical gate electrode thicknesses would be 65–130 nm (which is 650–1300Å). PO Resp. 40 (citing Ex. 2009 ¶ 35; Ex. 2012, 20, Table 51a). Be that as it may, the "typical gate electrode thickness" shown on page 20 (Table 51a) of Exhibit 2012 may inform a POSITA of "typical" gate electrode thicknesses, but that disclosure does not at the same time contradict, detract, or otherwise persuade us to ignore Joo's separate, independent teachings of film thicknesses that also apply to other device features. *See* Ex. 1005, 5:15–25.

Patent Owner contends that Joo's thicknesses would not lead to predictable results for local interconnects because gate electrode are different structures. PO Resp. 40. Dr. Gnade testifies that

a person of ordinary skill in the art would not be motivated to use the thicknesses disclosed in Joo, a gate electrode, and apply them to the local interconnect layers of Trivedi, a local interconnect. *I do not believe that using thicknesses of layers disclosed in a gate electrode would lead to predictable results in a local interconnect.* Further, as discussed above, I do not believe a person of ordinary skill in the art would be motivated to use the thickness disclosed in Joo for its tungsten layer and apply it to the tungsten silicide layer disclosed in Trivedi because Joo cautions away from the formation of a tungsten silicide layer. Petitioner does not address why a POSITA would be motivated to use the thicknesses disclosed in Joo and apply them to Trivedi's layers.

Ex. 2009 ¶ 99 (emphasis added). Again, Patent Owner's position and Dr. Gnade's testimony against the proposed combination stem from the perceived differences between gate electrodes and local interconnects, which we have dispelled based on, among other things, the express disclosure in Joo. For example, as discussed in detail with respect to claim 2, Joo

cautions against the formation of unwanted tungsten silicide created from the breakdown of the barrier layer. We do not read this teaching to discourage or malign Trivedi's intentional deposition (i.e., not resulting from the undesired breakdown of a barrier layer) and use of tungsten silicide as a layer in a local interconnect structure.

Moreover, Dr. Lee explains a POSITA would be aware that Trivedi provides no explicit thicknesses and that Joo provides functional ranges. Ex. 1020 ¶ 69; Ex.1002 ¶ 126. Dr. Lee further reasons that a POSITA would have understood the electrical properties, e.g., sheet resistance, of Trivedi's local interconnect, modified according to Joo, would not be the same as that of Joo's corresponding layers. Ex. 1020 ¶ 69. According to Dr. Lee, a POSITA would have understood how to determine resistivity of Trivedi's layers with Joo possible thicknesses; "using those in combination with the known resistivities, a POSITA would have been able to compute, readily and predictably, the sheet resistance of Trivedi's local interconnect structure." *Id.* ¶ 70. In short, Dr. Lee has explained why it would have been within the level of skill of an ordinary artisan to appropriately apply Joo's thicknesses to Trivedi's local interconnect. *See id.* ¶ 68. "A person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421. After all, an artisan must be presumed to know something about the art apart from what the references disclose. *See In re Jacoby*, 309 F.2d 513, 516 (CCPA 1962).

On balance, we agree with Petitioner's arguments and credit the testimony of Dr. Lee because Petitioner's arguments and Dr. Lee's testimony are consistent with and supported by the evidence of record. Based on the complete record now before us, we find that Petitioner has

shown that the further recitations in claims 4, 5, 6, and 16 are taught by the proposed combination of Trivedi and Joo.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claims 4, 5, 6 and 16 are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Trivedi and Joo.

E. Obviousness over Trivedi and Yang – Claim 8

Petitioner asserts dependent claim 8 would have been obvious over the combination of Trivedi and Yang. Pet. 49–53.

1. Overview of Yang

Yang is an article titled: “A comparison of TiN processes for CVD W/TiN gate electrode on 3 nm gate oxide” published by The Institute of Electrical and Electronics Engineers (IEEE) in connection with a conference held December 10, 1997. Ex. 1006, 4. Yang describes a comparison of CVD W/CVD TiN stacks and CVD W/PVD TiN gate stacks as gate electrodes on 3nm gate oxide. *Id.* at 6. Figure 1 is reproduced below.

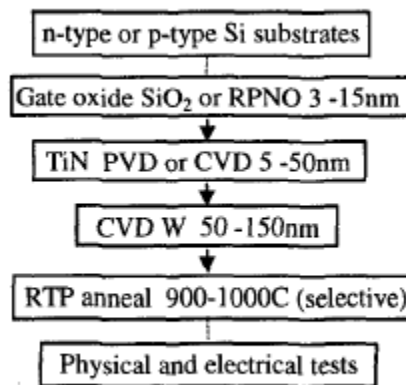


Fig.1 Key process steps with splits.

Figure 1 shows the key process steps and splits including the tungsten (W) layer. *Id.* at 8.

2. *Analysis of Claim 8*

Claim 8 depends from claim 1 and further recites “the first film and the second film form a metal stack having a sheet resistance equal to or less than about 10 Ohm/sq.” Ex. 1001, 6:23–25.

Petitioner asserts that Yang teaches sheet resistance is a physical property of a layer stack. Pet. 49. Based on this disclosure, Petitioner argues that Trivedi’s interconnect structure inherently has sheet resistance. *Id.* For the specific range recited in claim 8, Petitioner points to Yang’s Table 1 and argues that Yang’s TiN/W sheet resistance for a PVD TiN and CVD W stack is similar to Trivedi’s PVD TiN layer 30 and CVD tungsten-silicide layer 30, and that Yang’s TiN/W sheet resistance is 2.06Ω/sq. Pet. 50 (citing Ex. 1002 ¶ 198; Ex. 1006, 461, Table 1). Petitioner adds that

[a] POSITA would have understood that Trivedi’s metal stack can be readily modified to include a CVD tungsten (W) layer instead of a CVD tungsten silicide layer, and that the thicknesses of the TiN and W layers can be configured as Yang teaches to provide, in a predictable manner, a local interconnect stack having low sheet resistance.

Pet. 51 (citing Ex. 1002 ¶ 199).

In response, Patent Owner argues that Petitioner has not explained sufficiently why a POSITA would ignore the sheet resistance already disclosed in Trivedi for its tungsten silicide layer and use the sheet resistance disclosed in Yang for an elemental tungsten layer. PO Resp. 43 (citing Ex. 2009 ¶ 105). Patent Owner adds that “tungsten silicide has a resistivity that is approximately 10X larger than tungsten, to get the same resistance as a tungsten film, the tungsten silicide would have to be 10X thicker than a tungsten film used for the same purpose, assuming the width of the lines are the same.” *Id.* at 42 (citing Ex. 2009 ¶ 104).

We note that in the Petition, Petitioner asserts that

[a] POSITA would have also known that the sheet resistance of a composite layer structure is a property of the different materials forming the layers and the thicknesses of those layers, and that the sheet resistance would be independent of the purpose for which the structure is formed (e.g., whether as a gate electrode or a local interconnect.)

Pet. 52 (citing Ex. 1002 ¶ 187). As such, Petitioner takes the position that the purposes of Yang and Trivedi's layered structures do not detract from the teaching that layer thickness affects sheet resistance.

Petitioner's point is well taken, but does not address clearly how or why one of ordinary skill in the art would combine the relied upon teachings. Turning to the references, Petitioner relies upon the TiN/WSi_x stack structure in its challenge of independent claim 1 of the '033 patent, from which claim 8 depends. *See supra* sect. V.B. For this structure, Trivedi teaches a "low" sheet resistivity in the range of 100 Ohm/sq to 150 Ohm/sq for its tungsten silicide layer. Ex. 1004, 5:48–51 ("[H]ard mask 32 has low sheet resistivity. Low sheet resistivity is defined herein as a resistivity in a range from about 100 Ohm/sq to 150 Ohm/sq."). Trivedi, therefore, does not teach that the TiN/WSi_x local interconnect has "a sheet resistance equal to or less than about 10 Ohm/sq," which is required by claim 8.

Petitioner then relies upon Yang for the sheet resistivity range. Yang is directed to a comparison of TiN processes for CVD W/TiN gate electrodes. Ex. 1006, 6. Yang teaches that the TiN/W gate electrode has a sheet resistivity of 2.06 Ω/sq or 1.45 Ω/sq. Ex. 1006, 8 (Table 1: TiN/W sheet resistance and stress.). Yang observes that "[t]hough the two TiN films are quite different, their stacked properties with CVD W are similar

since the *relatively thick W film dominates these properties.*” *Id.* (emphasis added).

Because Yang employs a different TiN/W structure, Petitioner asserts “Trivedi’s metal stack can be readily modified to include a CVD tungsten (W) layer instead of a CVD tungsten silicide layer, and that the thicknesses of the TiN and W layers can be configured as Yang teaches to provide, in a predictable manner, a local interconnect stack having low sheet resistance.” Pet. 51 (citing Ex. 1002 ¶ 199). Dr. Lee’s testimony mirrors the Petition in this regard.

We determine that Patent Owner has the better position. We observe that Trivedi teaches a process that forms another local interconnect structure from titanium nitride (TiN) and tungsten, with the tungsten layer covered on opposite sides by titanium nitride. Ex. 1004, 4:39–42, 7:58–37. Referring to Figure 7, Trivedi teaches first barrier layer 30 comprises titanium nitride (TiN), first electrically conductive layer 82 is formed over first barrier layer 30. *Id.* at 7:58–63. Trivedi further teaches that “electrically conductive layer 82 preferably comprises tungsten (W), and is formed using CVD processes.” *Id.* at 7:67–8:2. Trivedi then discloses that a second barrier layer 84, TiN, is formed over layer 82, then a hard mask layer 88 and photoresist layer are formed. *Id.* at 8:8–37. Trivedi does not provide a sheet resistivity for this structure, but consistently refers to the range of 100 Ohm/sq to 150 Ohm/sq. in the written description and claims. *See* Ex. 1004, 5:48–51, claims 1, 8.

In its Reply, Petitioner argues that a POSITA would replace Trivedi’s tungsten-silicide layer with Yang’s CVD tungsten layer and adjust the layer thicknesses because “[t]he benefit of this combination modification was to provide ‘a local-interconnect stack having low sheet resistance.’” Pet. Reply

19 (citing Ex. 1020 ¶¶ 74–76, 199). But, Petitioner does not address the fact that Trivedi already teaches a “low sheet resistivity” for a TiN/W local interconnect structure. The sheet resistivity range disclosed by Trivedi, 100 Ohm/sq to 150 Ohm/sq, applies to Trivedi’s local interconnects that include TiN/W and is described by Trivedi to be “low sheet resistivity.” *See* Ex. 1004, 5:48–51, claims 1, 8, 19.

Given this disclosure, we are left then with the question of why a POSITA would have modified Trivedi with Yang’s tungsten layer to achieve an even lower sheet resistivity (e.g., 10 Ohm/sq) that is not in the range contemplated by Trivedi for “low sheet resistivity,” particularly because Trivedi already discloses a TiN/W layered structure. We are aware that there may be some distinction between the sheet resistance of Trivedi’s hard mask layer versus the sheet resistance of the entire TiN/W structure in Yang. *See* Ex. 1004, 5:48–51; Ex. 1006, 6 (Table 1). But, based on the complete record, Petitioner has failed to sufficiently address how a POSITA would consider these sheet resistivity ranges in light of the proposed combination.

Petitioner does present several arguments regarding how a POSITA could modify Trivedi with Yang’s structures and layer thicknesses. *See* Pet. Reply 19–23; *see* Ex. 1020 ¶¶ 81–85 (Dr. Lee’s testimony regarding the mathematical relationship between sheet resistivity, resistivity, and layer thickness). For example, Petitioner contends that one does not use “sheet-resistance in the sense a particular technique or temperature can be used to improve the formation of a layer. Rather, a layer structure can be designed such that its sheet-resistance does not exceed a specified limit.” *Id.* at 21 (citing Ex. 1020 ¶ 78; Ex. 2010 114:24–115:4).

We find that these arguments on the whole focus on how a POSITA *could* modify Trivedi with Yang, without answering why a POSITA would

do so. “[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Personal Web Techs., LLC, v. Apple, Inc.*, 848 F.3d 987, 993–994 (Fed. Cir. 2017) (citing *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015))).

Petitioner’s reasoning for combining Trivedi’s TiN/WSi_x local interconnect with Yang’s TiN/W gate electrode is undermined by Petitioner’s own failure to explain why a POSITA would do so when Trivedi teaches a TiN/W local interconnect structure that may have low sheet resistivity. Thus, we agree with Patent Owner that Petitioner proposed combination is proposed out of impermissible hindsight. *See Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.”).

Accordingly, for the foregoing reasons, we determine that Petitioner has not met its burden of demonstrating by a preponderance of the evidence that claim 8 would have been obvious over the cited combination of references.

F. Obviousness over Trivedi, Joo, and Yang – Claim 7

Petitioner asserts dependent claim 7 would have been obvious over the combination of Trivedi, Joo, and Yang. Pet. 53–57.

Claim 7 depends from claim 1 and further recites “each of the first film and the second film is deposited to a thickness of about 300 Angstroms.”

For these limitations, Petitioner argues that Trivedi combined with Joo and Yang discloses that each of a TiN layer (first film) and the tungsten film (second film) is deposited to a thickness of about 300 Angstroms. Pet. 54.

Petitioner asserts that Figure 1 of Yang teaches a TiN layer thickness between 5–50nm (e.g., 50–500Å) and Joo teaches a tungsten film thickness between 200–700Å. *Id.* (citing Ex. 1002 ¶¶ 84–100, 206–208). Petitioner further argues that “a POSITA would have understood that Trivedi’s process, modified and configured as Joo teaches, can be predictably improved further by configuring Trivedi’s TiN and tungsten-based layers to have thicknesses within the ranges that Yang provides, predictably facilitating the formation of functional, low resistance, high strength local interconnect structures.” *Id.* at 56 (citing Ex. 1002 ¶ 203).

Patent Owner asserts that Petitioner “never addresses why a POSITA would be motivated to combine specific features of gate electrodes with a design for a local interconnect.” PO Resp. 44–45. Patent Owner further contends that Joo teaches the “tungsten nitride layer be as thin as possible, less than 100 Å,” which Patent Owner asserts teaches away from a thickness of about 300 Angstroms. *Id.* at 45 (citing Ex. 1005, 5:15–20).

We determine first that Petitioner’s challenge does not rely upon a substitution of Yang’s tungsten layer for Trivedi’s tungsten silicide layer. Pet. 54–57. For this challenge, Petitioner relies on Trivedi’s TiN/WSi_x local interconnect structure and proposes to modify Trivedi’s layers with the thicknesses taught in Joo and Yang. *Id.* Specifically, Petitioner contends that Trivedi’s TiN/WSi_x structure can be modified with thicknesses taught by Yang’s TiN layer (e.g., 50–500Å) and Joo’s tungsten film (e.g., 200–700Å). Pet. 54.

In reviewing Petitioner’s arguments and evidence, we note that where there is a range disclosed in the prior art, and the claimed invention falls within that range, there is a presumption of obviousness. That presumption will be rebutted if it can be shown: (1) That the prior art taught away from

the claimed invention, *In re Geisler*, 116 F.3d 1465, 1471 (Fed. Cir. 1997); or (2) that there are new and unexpected results relative to the prior art, *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990). *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1322 (Fed. Cir. 2004); *see also Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985) (invention was obvious because it was close to prior art range). “Selecting a narrow range from within a somewhat broader range disclosed in a prior art reference is no less obvious than identifying a range that simply overlaps a disclosed range.” *In re Peterson*, 315 F.3d 1325, 1329–30 (Fed. Cir. 2003).

There is an overlap of Yang’s disclosed TiN thickness of 50–500Å and the recited “thickness of about 300 Angstroms” for the first film. There is also an overlap of Joo’s disclosed tungsten layer thickness of 200–700Å.

Patent Owner does not dispute that Yang and Joo teach the layer thickness ranges relied upon by Petitioner, but contends that Joo teaches away from the combination. PO Resp. 44–45. Joo teaches that the tungsten nitride layer be as thin as possible, less than 100 Angstroms. Ex. 1005, 5:15–17.

We do not find Joo’s preference for a thickness less than 100 Angstrom to criticize, discourage, discredit, or otherwise teach away from the proposed combination. Joo states “[t]he tungsten nitride barrier layer is *preferably* formed as thin as possible, less than 100 Å.” Ex. 1005, 5:15–20. Joo expresses a preference for a particular thickness, but a reference does not teach away “if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)).

Still, even if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding whether a skilled artisan would be motivated to combine that reference with another reference. *See Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 n.15 (Fed. Cir. 2016) (en banc) (noting that, even if a reference “does not teach away, its statements regarding users preferring other forms of switches are relevant to a finding regarding whether a skilled artisan would be motivated to combine the slider toggle in” that reference with the invention of a second reference).

Petitioner addresses this very issue and explains why a POSITA would have considered modifying Joo’s “less than 100 Angstroms” thickness in light of Yang’s teachings. According to Petitioner,

a thicker titanium nitride layer that Yang teaches can be beneficial, for two reasons. First, to provide better protection of the underlying silicon layers.

Second, Petitioner describes that to improve the strength and continuity and to reduce resistivity of a PVD deposited titanium nitride layer, Yang’s thicker layer is beneficial, because the step coverage of PVD is not as good as that of CVD.

Pet. Reply 24 (citing Pet. 56–57; Ex. 1002 ¶¶ 203–204). Petitioner adds a POSITA would have recognized “Yang provides a functional range of thicknesses for the titanium-nitride layer, that may allow better protection of the underlying silicon layers, and provide a strong barrier with low resistivity, taking into account relatively less conformality of PVD.” *Id.* at 25 (citing Ex. 1020 ¶¶ 91–92).

Dr. Gnade asserts that Petitioner’s arguments are confusing and complicated because it is not clear why it would be a “good” combination to use a thicker TiN layer. Ex. 2009 ¶ 110. Dr. Gnade further asserts that Petitioner does not explain why a person of ordinary skill in the art would be motivated to go from Joo’s CVD WN to Yang’s PVD TiN for a gate

electrode, and why this would be applicable to the thickness of TiN used in Trivedi as a local interconnect. *Id.*

We observe that Dr. Gnade's testimony is premised primarily on the position that a POSITA would not look to gate electrodes when considering local interconnects. *See* Ex. 2009 ¶ 108. For the reasons discussed previously, we are not persuaded that a POSITA would not look to methods of semiconductor fabrication generally given that these techniques apply broadly to many structures. *See* Ex. 1027, 27:12 – 28:7.

Further, we do not agree that Petitioner failed to explain its reasoning or that its reasoning is overly complicated or confusing. As discussed, Petitioner asserts that “a thicker [TiN] layer, e.g., as thick as 300Å, as Yang discloses, may be necessary when using PVD . . . [because] [a]s discussed above, Trivedi and Yang both describe depositing the titanium nitride layer using sputtering/PVD.” Pet. 57; Ex. 1002 ¶ 203. Dr. Lee also explains

a POSITA would have understood that Trivedi and Joo can be combined to: (i) select PVD/sputtering as a deposition process to form Trivedi's tungsten silicide layer, and (ii) to select a thickness for that layer within a functional range that Joo discloses. Trivedi describes forming a tungsten silicide layer by CVD over its titanium nitride layer and does not explicitly provide a thickness of that layer. . . . Joo teaches forming a tungsten layer over a barrier layer, and Joo explicitly discloses its barrier layer as either a tungsten nitride layer, or a titanium nitride layer as Trivedi teaches. . . . Joo also discloses that its tungsten layer can be formed by “CVD or PVD, to a thickness between 200-700 Å”, which includes the claimed thickness of 300 Å for the tungsten containing film.

Ex. 1020 ¶ 89 (citing Ex. 1002 ¶¶ 124, 134, 149–150). Dr. Lee further explains that “[a] POSITA would have been motivated to use the thickness of Joo's tungsten layer to form Trivedi's tungsten silicide layer, because Joo

informs a feasible range of thicknesses than can be achieved via PVD.” *Id.* ¶ 90.

Based on the complete record, we agree with Petitioner’s arguments and credit the testimony of Dr. Lee because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record as discussed above. We find that Petitioner has shown that the further recitations in claim 7 are taught by the proposed combination of Trivedi, Joo, and Yang.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 7 is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Trivedi, Joo, and Yang.

G. Obviousness over Trivedi and Lien – Claims 2, 11, and 12

Petitioner asserts dependent claims 2, 11, and 12 would have been obvious over the combination of Trivedi, Joo, and Yang. Pet. 53–57.

1. Overview of Lien

Lien, titled “Method for Fabricating a Tungsten Plug Structure and an Overlying Interconnect Metal Structure Without a Tungsten Etch Back or CMP Procedure,” relates to a method used to fabricate semiconductor memory devices, and more specifically to a method used to define a metal contact plug structure, and an overlying metal interconnect structure, using a two step, in situ etch procedure. Ex. 1007, code (54), 1:10–14. Lien describes a process for in situ patterning of an overlying metal interconnect structure, and an underlying metal plug structure, using a two stage, dry etching procedure, without directly exposing the metal plug structure, in a contact hole, and the adhesive and barrier layers, on the sides of the contact

hole, to either stage of the dry etch, patterning procedure. *Id.* at 2:25–31. A conductive region in a semiconductor substrate such as a source/drain region of a transfer gate transistor, is provided. *Id.* at 2:31–33. A contact hole, in an insulator layer, is formed, exposing the top surface of the source/drain region. *Id.* at 2:34–35. A chemical vapor deposition of a thin titanium, adhesive layer, and of a thin titanium nitride, barrier layer, is followed by an in situ, chemical vapor deposition of a tungsten layer, with the tungsten layer completely filling the contact hole. *Id.* at 2:35–39.

2. *Analysis of Claim 2*

With regard to claim 2, we note that Petitioner asserts that Trivedi teaches depositing a TiN layer and a tungsten silicide layer. However, as discussed above, Trivedi does not expressly teach in-situ deposition of both. For this challenge, Petitioner relies on the combination of Trivedi with Lien. Pet. 58–59.

a) *Petitioner's Contentions*

Petitioner contends that Lien discloses a “composite adhesive and barrier layer 10a, deposited via CVD procedures” that includes “an underlying titanium adhesive layer” and an “in situ deposit[ed] overlying titanium nitride, barrier layer.” Pet. 58 (quoting Ex. 1007, 4:13–20, Fig. 2). Petitioner adds that Lien teaches tungsten layer 11a is deposited via in-situ CVD procedure. *Id.* at 58–59 (citing Ex. 1007, 4:22–25, Fig. 2).

Petitioner reasons that “a POSITA would have understood that Trivedi’s process can be modified to form both the TiN and tungsten-based layers in a single CVD chamber as Lien describes, especially because there are no intervening layers to be formed between the tungsten-based and TiN layers.” Pet. 66 (citing Ex. 1007 ¶ 220). According to Petitioner, a POSITA would have recognized the predictable benefit of minimizing the time,

complexity, and/or cost of the overall manufacturing process, resulting from such a modification. *Id.* And, “[t]his combination would have been nothing more than combining prior art elements according to known methods (using different etchants at different stages of etching), or simple substitution of one known element for another (CVD for sputtering, to deposit the TiN layer), to obtain the predictable results described above.” *Id.*

b) Patent Owner’s Contentions

Patent Owner does not dispute that Lien teaches an in-situ CVD. *See, generally* PO Resp. 46–49. Rather, Patent Owner contends that a POSITA would not combine Lien and Trivedi because Lien relates to a tungsten metal plug (not a local interconnect) that is used to connect two metal layers in a semiconductor device. *Id.* at 46 (citing Ex. 2009 ¶ 70). According to Patent Owner “Figure 36 in Ex. 2013 shows an example of where a tungsten metal plug would be used in an integrated circuit . . . [as] the electrical connection between two different interconnect layers.” *Id.* at 48 (citing Ex. 2009 ¶ 112). Patent Owner contends that the plug has to be at least as thick as the interlevel dielectric (e.g., 5000–10,000 Angstroms) which separates the two interconnect layers. *Id.* (citing Ex. 2009 ¶ 112). This means, according to Patent Owner, that Lien’s tungsten layer is deposited to thickness of 4000 to 6000 Angstroms, which “is more than 10 times the thickness disclosed in the ’033 patent of its the tungsten layer for its local interconnect.” *Id.* at 47. Patent Owner adds that the process for fabricating a tungsten plug is not part of the local interconnect process, and Petitioner has not explained why a POSITA concerned about forming local interconnects would look to Lien for guidance on the material or process to use. *Id.* at 48 (citing Ex. 2009 ¶ 112).

c) Discussion

To start, we find that Lien discloses a “composite adhesive and barrier layer 10a, deposited via CVD procedures” that includes “an underlying titanium adhesive layer” and an “in situ deposit[ed] overlying titanium nitride, barrier layer.” Ex. 1007, 4:13–20, Fig. 2. Lien further teaches “[n]ext a tungsten layer 11a, is in situ deposited, via CVD procedure.” *Id.* at 4:22–25, Fig. 2. Consistent with Petitioner’s position, Lien teaches a titanium nitride layer and tungsten layer deposited via in-situ CVD.

We also agree with Petitioner that Trivedi teaches the first film (titanium nitride) and second film (tungsten silicide) that may be deposited by CVD or sputtering. Ex. 1004, 5:11–18, 5:31–39. Trivedi does not, however, explicitly teach that the films/layers are deposited in-situ. *See* Pet. 64.

Nonetheless, based on the complete record, we agree with Petitioner that a POSITA would have recognized the combination of Lien’s in-situ CVD process with Trivedi “would have been nothing more than combining prior art elements according to known methods . . . or simple substitution of one known element for another (CVD for sputtering, to deposit the TiN layer), to obtain the predictable results described above.” Pet. 66 (citing Ex. 1002 ¶ 223). *Id.*

Patent Owner does not dispute that Lien teaches in-situ deposition processes. PO Resp. 46–49. However, Patent Owner argues that a POSITA would not combine Lien’s metal plug disclosure with Trivedi’s local interconnect. *Id.*

But Lien’s and Trivedi’s disclosures are not so disparate as Patent Owner would like us to believe. Lien’s teachings generally relate to “*a method used to fabricate semiconductor memory devices, and . . . a method*

used to define a metal contact plug structure, and an overlying metal interconnect structure, using a two step in-situ etch procedure.” Ex. 1007, 1:9–14 (emphasis added). Lien discloses in-situ CVD processes in the context of fabricating metal plugs and metal interconnect structures, but also states that its disclosure applies to “source/drain regions of P channel devices, or to *other active regions in a semiconductor substrate.*” *Id.* at 3:17–21 (emphasis added).

Dr. Lee also testifies that Lien’s “processes or technique of forming layers, and in particular commonly used techniques such as CVD and PVD, are generally applicable to forming layers of various materials and dimensions.” Ex. 1020 ¶ 94. Consistent with Dr. Lee’s testimony, Trivedi refers to “sputtering” as a “conventional process” and in “The Relevant Technology” section, Trivedi teaches that “typically . . . a refractory metal film is formed by sputtering, also known as physical vapor deposition process, or by chemical vapor deposition (CVD).” Ex. 1004, 1:29–36, 5:13–18. Neither Patent Owner nor Dr. Gnade disputes that these processes were commonly used techniques. *See* Ex. 2009 ¶¶ 111–113; *see* PO Resp. 46–49; *see generally* Sur-reply.

We further note that Petitioner relies on Lien principally for the described in-situ CVD process through which a tungsten layer is deposited in-situ with a titanium nitride layer. Pet. 64 (citing Ex. 1007, 4:13–25). We observe that Petitioner relies on Trivedi for the local interconnect structure containing a TiN/WSi_x layer. *See supra* Sect. V.B.

With this in mind, we disagree with Patent Owner that a POSITA would categorically ignore Lien’s disclosure regarding layer deposition based solely on the purpose of the resulting structures. Lien expressly states that its teachings apply to “other active regions in a semiconductor

substrate.” Ex. 1007, 3:17–21. And, Petitioner’s reliance on Lien is narrow—focused on those commonly used processes of forming layers. We, therefore, agree with Petitioner that a POSITA would consider Lien’s metal plug disclosure in combination with Trivedi’s local interconnect teachings because the proposed combination relies on Lien for commonly used techniques in semiconductor fabrication.

Additionally, we are not persuaded by Dr. Gnade’s testimony that a POSITA would not be motivated to combine Lien and Trivedi because Lien’s metal plug structure has a thickness of 4000 to 6000 Angstroms and a metal plug serves a different purpose from a local interconnect. Ex. 2009 ¶ 112. Again, as discussed above, Petitioner relies on Lien for commonly used techniques in semiconductor fabrication, in-situ CVD procedures, that are not limited to metal plug fabrication. *See* Ex. 1007, 3:17–21. Moreover, Lien teaches a variety of layer thicknesses all formed by the in-situ CVD process. Ex. 1007, 4:8–26. This disclosure better supports Dr. Lee’s testimony that “a POSITA would have understood that these predictable, beneficial results can be obtained without requiring substantial changes or modifications to either Trivedi’s or Lien’s processes, and without adversely affecting the interconnect structures formed by Trivedi’s process.” Ex. 1002 ¶ 223.

Based on the complete record, we agree with Petitioner’s arguments and credit the testimony of Dr. Lee because Petitioner’s arguments and Dr. Lee’s testimony are consistent with and supported by the evidence of record. Based on the complete record now before us, we find that Petitioner has shown that the further recitations in claim 2 are taught by the proposed combination of Trivedi and Lien.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 2 is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Trivedi and Lien.

3. *Analysis of Claims 11 and 12*

Claim 11 depends from claim 1, further reciting “wherein the second film is etched with a fluorine-based etchant.” Claim 12 depends from claim 1, and further recites “wherein the first film is etched with a chlorine-based etchant.” Ex. 1001, 6:32–36.

For claim 11, Petitioner argues that Lien discloses etching a tungsten layer 11a (second film) using SF₆ as an etchant (a fluorine-based etchant). Pet. 59 (citing Ex. 1002 ¶ 230). Petitioner adds that

Lien discloses using a “photoresist ... as a mask to create an aluminum based interconnect structure, ... using a first stage of an anisotropic RIE (reactive ion etching) procedure, via the use of a chlorine based etchant” (Ex.1007, 2:42-48; Ex.1002, ¶231) and at a “second stage of the anisotropic RIE procedure,” using “SF₆ as an etchant, which removes the regions of tungsten layer 11a.” (Ex.1007, 5:1-6; Ex.1002, ¶231.) Lien discloses etching a tungsten layer 11a (second film) using SF₆ as an etchant, e.g., “etching the second film with a fluorine-based etchant.” (Ex.1002, ¶231.)

Pet. 59–60. For claim 12, Petitioner contends that

Lien further describes, with reference to FIG. 4, that a “[p]hotoresist shape 14” is “used as a mask” and then, a “first stage of an anisotropic RIE procedure is next performed, using a chlorine based etchant, resulting in the formation of titanium nitride, ARC shape 13b, and aluminum based, interconnect structure 12b, shown schematically in FIG. 4.” (*Id.* 4:43-51; FIG. 4.)

Pet. 61. Petitioner argues that a “POSITA would have recognized that Trivedi’s etching process modified according to Lien’s teachings

beneficially avoids the need for a specialized etchant that is selective to TiN and may be less easily available, more costly, and/or less efficient in removing a tungsten based layer.” *Id.* at 65 (citing Ex. 1002 ¶¶ 218–219). Petitioner reiterates that the proposed combination would have been nothing more than combining prior art elements according to known methods of using different etchants at different stages of etching. *Id.* at 66.

Patent Owner does not dispute that Lien teaches fluorine-based and chlorine-based dry etch. PO Resp. 48–49. Patent Owner contends that a POSITA would not be motivated to apply Lien’s fluorine-based dry etch and chlorine-based dry etch to Trivedi because Trivedi already discloses that its preferred chemical etch is a wet etch that is selective to hard mask layer tungsten silicide (WSi_x). *Id.* (citing Ex. 1007, 6:7–11; Ex. 2009 ¶ 113).

Based on the complete record, we agree with Petitioner. Petitioner explains why a POSITA would replace Trivedi’s wet etching with Lien’s chlorine-based etching. *See* Pet. 63–67; Ex. 1002, ¶¶ 239–243. Petitioner contends that a POSITA would have understood that using an etchant selective to tungsten-silicide would not be necessary for etching the portions of titanium nitride layer where the overlying layer of tungsten-silicide is already removed. Pet. 65 (citing Ex. 1002 ¶ 242; Ex. 1004, Fig. 4). Moreover, Petitioner explains that a POSITA would have chosen chlorine-based etching that Lien teaches over Trivedi’s wet etching because the former was known to be less corrosive than the latter. *Id.* (citing Ex. 1002 ¶¶ 240, 243; Ex. 1020 ¶¶ 99–100).

We note that Dr. Lee’s testimony supports Petitioner’s position. Dr. Lee testifies that “a POSITA would have understood that the use of an etchant selective to tungsten silicide would not be essential. A POSITA would have been motivated to use Lien’s RIE process, that uses a chlorine

based etchant, instead of Trivedi's wet etching at least because RIE was known to be less corrosive than wet etching." Ex. 1002 ¶ 243.

Dr. Gnade points to Trivedi's preference for wet etch but does not otherwise dispute Dr. Lee's testimony that REI would be less corrosive. Ex. 2009 ¶ 113. Dr. Gnade testifies that

I do not believe that a person of ordinary skill in the art would be motivated to use the fluorine-based dry etch and chlorine-based dry etch of Lien and apply it to Trivedi because Trivedi already discloses that its preferred chemical etch is a wet etch that is selective to hard mask layer tungsten silicide (WSix). (Ex. 1007 at 6:7–11). Trivedi discloses specific reasons why its wet etch is selected.

Ex. 2009 ¶ 113. Missing from his testimony is an explanation for why a POSITA would not consider Lien's alternative processes for the benefits that Dr. Lee provides. Rather, Dr. Gnade's statements are conclusory in nature, entitling his testimony to less weight in this regard. 37 C.F.R. 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Further, consistent with Petitioner's position, Lien teaches the use of "[c]onventional photolithographic and anisotropic RIE procedures" as part of the described processes. Ex. 1007, 3:46–47. We find that the conventionality and commonality of these procedures supports Petitioner's argument that "[a] POSITA would have also been able to apply known, conventional semiconductor fabrication techniques to perform the necessary modifications" to Trivedi's or Lien's processes for the proposed combination. Pet. 66.

Based on the complete record, we agree with Petitioner's arguments and credit the testimony of Dr. Lee because Petitioner's arguments and Dr. Lee's testimony are consistent with and supported by the evidence of record.

Based on the complete record now before us, we find that Petitioner has shown that the further recitations in claims 11 and 12 are taught by the proposed combination of Trivedi and Lien.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claims 11 and 12 are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Trivedi and Lien.

H. Obviousness over Trivedi and Johnson – Claim 13

1. Overview of Johnson

Johnson is titled “Systems and Methods for Measuring Properties of Conductive Layers,” and “relates to systems and methods for measuring properties of conductive layers” and “discloses embodiments that relate to a pin having a substantially planar contact surface that may be disposed within a probe and a system that may include multiple probes configured to measure a property of a conductive layer.” Ex. 1008, code (54), 1:14–19.

2. Analysis of Claim 13

Claim 13 depends from claim 1 and further recites the step of “probing the second film to electrically test the metal stack.” Ex. 1001, 6:37–38.

Petitioner argues that

FIG. 20 of Johnson depicts such an exemplary process for probing a metal stack. In particular, FIG. 20 of Johnson depicts probing (contacting) a tungsten layer (second film) to determining a sheet resistance (electrical property) of a metal stack.

Pet. 67 (citing Ex. 1002 ¶ 250; Ex. 1008, Fig. 20). Petitioner adds “that a POSITA would have understood that Trivedi’s process would be improved by monitoring the properties of the formed local interconnect structures

using Johnson’s probe, so that the processes can be adjusted as needed.” *Id.* at 70.

Patent Owner responds that Petitioner does not explain why “a POSITA would be motivated to combine the Johnson patent which relates to probing conductive layers, with the Trivedi patent which discloses a WSix layer.” PO Resp. 49. Patent Owner adds that Petitioner does not address whether tungsten silicide is probable.

Based on the complete record, we determine Petitioner has established that Johnson teaches that sheet resistance is a property of a conductive layer and that “[t]he conductive layer may also include a conductive structure formed upon a semiconductor substrate such as a gate electrode and a local interconnect.” Pet. 68 (citing Ex. 1008, 14:3–5, 14:10–13; Ex. 1002 ¶ 251). Further, although tungsten silicide is not specifically mentioned, we note Johnson expressly teaches that “the conductive layer may include silicon, polysilicon, aluminum, copper, an aluminum-copper alloy, tungsten, titanium, titanium nitride, and a titanium-tungsten alloy. The conductive layer, however, may also include any conductive layer known in the art.” *Id.* at 69 (citing Ex. 1008, 14:13–20); *see also* Ex. 1002 ¶ 251. Thus, Johnson is consistent with Petitioner’s position that a tungsten-containing compound is conductive and probable. *See also* Ex. 1035, 40–41 (discussing sheet-resistance of tungsten-silicide films). As noted above, Trivedi describes tungsten silicide as a refractory *metal* silicide layer. Ex. 1004, 4:51–56. Additionally, Dr. Lee and Dr. Gnade testify that tungsten-silicide is conductive. Ex. 2010, 87:22–25; Ex. 2009 ¶ 87.

Moreover, we find that Johnson teaches the benefits of monitoring semiconductor fabrication processes. Johnson discloses that “semiconductor fabrication processes typically involve a number of processing steps,” and

“ion implantation systems may require extensive monitoring to ensure that such systems and ion implantation processes are performing within process constraints.” Ex. 1008, 1:22–24, 1:38–41. We determine that this disclosure supports Dr. Lee’s testimony that “a POSITA would have understood that Trivedi’s process can be predictably improved by monitoring the properties of the formed local interconnect structures using Johnson’s probe, so that the processes can be adjusted as needed.” Ex. 1002 ¶ 247.

Accordingly, after consideration of the contentions and the evidence of record, we find that Petitioner has shown that the combination of Trivedi and Johnson teaches each limitation of claim 13. Also, we are persuaded that Petitioner has offered articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have combined the teachings of Trivedi and Johnson in the manner recited in claim 13.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 13 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Trivedi and Johnson.

I. Obviousness over Trivedi, Joo, and Johnson – Claim 17

Claim 17 depends from claim 15 and further recites “probing the second film to electrically test the material stack.” Ex. 1001, 6:54–56.

Similar to arguments discussed above, Petitioner combines Johnson’s teaching of metal stack probing to Trivedi’s local interconnect structure as modified by Joo’s sputtering process. *See supra* Sect. V.D (discussing claim 2); Pet. 72–75.

Patent Owner also relies on arguments previously presented and discussed above for Grounds 1 and 7. PO Resp. 50–51. Additionally, Patent Owner reiterates that “Petitioner never addresses why a POSITA

would be motivated to combine a reference [(Joo)] that relate[s] to gate electrodes with prior art that relates to a local interconnect.” *Id.* at 50.

Based on the complete record, we agree with Petitioner. *See* Pet. 72–75. For claim 15 (from which claim 17 depends), Petitioner relies on Joo’s general teaching of semiconductor manufacturing that is not specific to gate electrode fabrication. *See* Ex. 1005, 1:7–10. Moreover, as discussed above for claim 13, we agree with Petitioner’s reading of Johnson. Namely, Johnson discloses a method for probing and testing the electrical properties of a material stack. *See* Ex. 1008, 14:1–5, 14:10–20.

Based on the complete record now before us, we determine that Petitioner has proved, by a preponderance of the evidence, that claim 17 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Trivedi, Joo, and Johnson.

VI. CONCLUSION¹⁰

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–7 and 9–17 of the '033 patent are unpatentable, as summarized in the following table:

Claims Challenged	35 U.S.C. §	Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 9, 10, 14	103(a)	Trivedi	1, 9, 10, 14	
2–6, 15, 16	103(a)	Trivedi, Joo	2–6, 15, 16	
8	103(a)	Trivedi, Yang		8
7	103(a)	Trivedi, Joo, Yang	7	
2, 11, 12	103(a)	Trivedi, Lien	2, 11, 12	
13	103(a)	Trivedi, Johnson	13	
17	103(a)	Trivedi, Joo, Johnson	17	
Overall Outcome			1–7, 9–17	8

¹⁰ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

VII. ORDER

Upon consideration of the record before us, it is:

ORDERED that claims 1–7 and 9–17 of the '033 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner has not shown that challenged claim 8 of the '033 patent is unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

Sanjeet Dutta
sdutta@goodwinlaw.com

Suhrid Wadekar
swadekar@goodwinlaw.com

FOR PATENT OWNER:

Justin Oliver
joliver@venable.com

Sarah Brooks
ssbrooks@venable.com