

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-00872
Patent 7,302,619 B1

Before FRANCES L. IPPOLITO, ROBERT L. KINDER, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

KINDER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Microchip Technology Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–32 of U.S. Patent No. 7,302,619 B1 (Ex. 1001, “the ’619 patent”). HD Silicon Solutions LLC (“Patent Owner”) filed a Preliminary Response to the Petition (Paper 8,¹ “Prelim. Resp.”).

To institute an *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons set forth below, upon considering the Petition, Preliminary Response, and evidence of record, we conclude Petitioner has not established a reasonable likelihood of prevailing in demonstrating the unpatentability of any challenged claim of the ’619 patent. Accordingly, we do not institute an *inter partes* review.

A. Related Proceedings

The parties indicate that the ’619 patent has been asserted in *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092

¹ Patent Owner filed an “Unopposed Motion to Correct a Clerical Error” (Paper 9) noting that both Paper 7 (a first filed Preliminary Response) and then Paper 8 (the second filed Preliminary Response) contained small clerical errors. The Motion to Correct states that “[t]he only changes to the corrected Preliminary Response are to remove the error codes from pages 38 and 39 of the previously filed Preliminary Response [Paper 8].” Paper 9, 1. We have considered the Motion to Correct, but find it unnecessary to grant because the errors found in Paper 8 are so small (*see* Prelim. Resp. 38–39) and do not detract from the merits of the briefing. Accordingly we accept Paper 8 as the proper Preliminary Response, expunge Paper 7 for clarity, but otherwise deny Patent Owner’s Motion to Correct (Paper 9) as moot.

(W.D. Tex), filed November 30, 2020 (“District Court Litigation”). Pet. 1; Paper 3, 2. On October 25, 2021, the District Court Litigation was transferred to the Northern District of California from the Western District of Texas. Ex. 3001 (Judge Albright’s Order Granting Microchip Technology Inc.’s Motion to Transfer Venue).

On June 15, 2021, Petitioner filed a separate petition in IPR2021-01042 also challenging all claims of the ’619 patent. That proceeding will be separately addressed.

B. The ’619 Patent

The ’619 patent, titled “Error Correction in a Cache Memory,” is directed to “systems and methods for error correction of instructions in an instruction cache coupled to a processor.” Ex. 1001, codes (54), (57). The application leading to the ’619 patent was filed on July 6, 2004. *Id.* at code (22). The invention seeks to address the issue of “bit flipping due to alpha radiation,” which is a condition resulting from radiation striking a storage component such that “a logical ‘1’” may “flip into a logical ‘0’ or vice versa.” *Id.* at 1:12–20. “Such bit flipping may result in data inaccuracies and fatal errors in the operation of network traffic processors.” *Id.*

According to the ’619 patent, “a plurality of instructions stored in the instruction cache are fetched for execution by the processor, each of the instructions being fetched during a respective one of a plurality of instruction cycles of the processor.” *Id.* at code (57). The Specification describes an exemplary processor circuit as shown in Figure 1, below.



Figure 1 is a schematic that illustrates an instruction cache with error correction circuitry employed in a traffic signal processor. *Id.* at 1:30–32. Processor circuit 100 . . . includes instruction cache 103 and processor 106. *Id.* at 1:60–62. “The instruction cache 103 is a memory for the storage of instructions 109 that are accessed and executed by the processor 106.” *Id.* at 1:62–64. In relation to Figure 1 above, the ’619 patent describes “cache tag logic 116, cache read/write control logic 119, and the RAM access logic 123 facilitate the general operation of fetching instructions 109 from either the instruction cache 103 or from a random access memory 126 when such instructions 109 are requested by the processor 106.” *Id.* at 2:37–42.

The Specification describes how “processor circuit 100 also includes error correction circuitry 129 that is executed to correct any errors in instructions 109 and in the associated error correction codes 113 that can be corrected.” *Id.* at 2:43–46. Error correction circuitry 129 includes error

correction code generators 133 and 136, a comparator 139, and error correction logic 143. *Id.* at 2:49–51. According to the ’619 patent, “the error correction circuitry 129 corrects single bit errors that occur due to bit flipping caused by alpha particles.” *Id.* at 2:46–48.

C. Illustrative Claim

Petitioner challenges claims 1–32 (“challenged claims”). Pet. 1. Claims 1, 21, and 29 are independent. Claim 1 is reproduced below.

1. A method for error correction in an instruction cache that is operatively coupled to a processor, comprising the steps of:

fetching a plurality of instructions stored in the instruction cache for execution by the processor, each of the instructions being fetched during a respective one of a plurality of instruction cycles; and

performing error detection for each of the instructions concurrently with the fetching of a respective one of the instructions.

Ex. 1001, 10:39–48. Claims 21 and 29 are both independent claims and very similar in claim scope. *Id.* at 12:8–16, 12:44–53. Both claims are system claims and claim 29 has a means plus function limitation.

D. The Evidence Relied on by Petitioner

Petitioner relies on the following evidence:

Reference	Exhibit
U.S. Patent No. 7,290,179, filed on Dec. 1, 2003, and issued Oct. 30, 2007 (“Lempel”)	1006
U.S. Patent No. 7,395,489, filed on Jan. 13, 2003, and issued July 1, 2008 (“Itou”)	1007
U.S. Patent No. 7,278,083, filed on June 27, 2003 and issued on Oct. 2, 2007 (“Haswell”)	1008

E. The Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–32 would have been unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Basis
1–9, 13–32	103	Lempel, Itou
6–12, 17, 24, 25, 31, 32	103	Lempel, Itou, Haswell

See Pet. 4. In support of its unpatentability arguments, Petitioner relies on the declaration testimony of Carl Sechen, Ph.D. (Ex. 1002, the “Sechen Declaration”).

II. LEGAL STANDARDS

In *Graham v. John Deere Co.*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the Federal Circuit has “repeatedly emphasized that an obviousness inquiry requires examination of all four *Graham* factors and that an obviousness determination can be made only after consideration of each factor.” *WPIP v. Kohler*, 829 F.3d 1317, 1328 (Fed. Cir. 2016) (“A determination of whether a patent claim is invalid as obvious under § 103 requires consideration of all four *Graham* factors, and it is error to reach a conclusion of obviousness until all those factors are considered.”).

We note that, with respect to the fourth *Graham* factor, the current record in this proceeding does not include any argument or evidence directed to secondary considerations of non-obviousness.

III. LEVEL OF ORDINARY SKILL IN THE ART

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus. Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends that a person of ordinary skill in the art at the time of the invention of the '619 patent would have had the following education and experience:

at least (1) a master's degree in electrical engineering, computer science, or a related degree, and at least 3-5 years of experience in computer architecture and cache memory design; or (2) a bachelor's degree in electrical engineering, computer science, or a related degree, and at least 5-6 years of experience in computer architecture and cache memory design.

Pet. 5. Patent Owner does not dispute this level of skill. *See generally* Prelim. Resp. For purposes of this Decision, we adopt Petitioner's proposal, which is supported by Dr. Sechen's testimony. *See* Ex. 1002 ¶¶ 26–28.

IV. CLAIM CONSTRUCTION

Claims in an *inter partes* review are interpreted “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). Under that standard, the “words of a claim ‘are generally given their ordinary and

customary meaning.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citation omitted). “[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which [it] appears, but in the context of the entire patent, including the specification.” *Id.* at 1313.

Petitioner argues that “[f]or the purposes of this Petition, claim terms should be given their plain and ordinary meaning.” Pet. 9. Petitioner also recognizes that “[c]ertain claim terms are *means plus function* terms that should be interpreted under 35 U.S.C. § 112, ¶6,” and provides interpretations for these claims. *Id.*

For purposes of this Decision, we determine it is not necessary to construe any specific claim terms whereas the outcome is not impacted by any particular claim scope for any term. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. DISCRETION UNDER 35 U.S.C. § 314(A)

Patent Owner contends we should exercise our discretion under 35 U.S.C. § 314(a) to deny institution of *inter partes* review. Prelim. Resp. 40–46 (citing, e.g., *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”)). Because we determine that Petitioner fails to demonstrate that there is a reasonable likelihood that it would prevail with respect to at least one of the claims challenged in the petition, we need not address Patent Owner’s contentions concerning discretionary denial.

VI. OBVIOUSNESS OVER LEMPEL AND ITOU

Petitioner's grounds for each of claims 1–32 rely on at least the combination of Lempel and Itou. For the reasons that follow, and considering the evidence of record, Petitioner has not shown by a reasonable likelihood that a person of ordinary skill in the art would have had reason to combine these two references for the reasons set forth by Petitioner.

A. Overview of Lempel

Lempel is titled “System and Method for Soft Error Handling” and it relates to detecting and clearing a soft error in a cache memory. Ex. 1006, codes (54), (57). Lempel explains that “[s]oft error’ is a term . . . used to describe random corruption of data in computer memory [and that] [s]uch corruption may be caused, for example, by particles [e.g., alpha particles] in normal environmental radiation.” *Id.* at 1:12–17. As depicted below in the system diagram of Figure 1, “the cache 102 may be coupled to or include a soft error detection logic 104. The soft error detection logic may be configured to detect soft errors in data loaded into the cache, for example by parity checking.” *Id.* at 2:22–26.

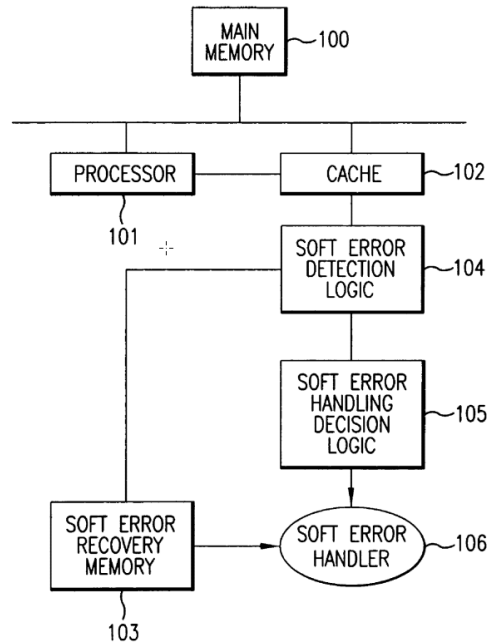


FIG. 1

Figure 1 of Lempel depicts a system diagram showing main memory 100 coupled to processor or CPU 101 and cache 102, which may also be coupled to processor 101. *Id.* at 2:13–16.

In the Background of Lempel, it discusses known methods of handling soft errors in caches, including shutting down operations and also not shutting down operations but instead using error correction circuitry (“ECC”). Ex. 1006, 1:18–45. With regard to ECC methods, Lempel describes how

ECC is additional hardware logic built into a cache; the logic is able to detect soft errors and execute a hardware algorithm to correct them. However, a disadvantage of ECC is that the additional hardware takes up space on the silicon and requires time to perform the needed computations, imposing further area and timing constraints on the overall design.

Id. Further, Lempel notes that “an additional cycle is usually added to the cache access time in order to accommodate the ECC’s soft error correction

logic, adversely impacting processor performance even when no soft errors are detected.” *Id.* Lempel notes that a distinct “approach is needed for handling soft errors in view of the foregoing considerations.” *Id.*

In Lempel’s process, when a soft error is detected, the “normal operations . . . such as instruction fetch, may be paused while microcode . . . executes to clear the soft error.” *Id.* at 2:4–12, 2:40–3:17 (“operations of the front end of the processor, which is typically involved in such pre-execution operations as instruction fetch, may be paused”). While the processor is paused, microcode is executed to clear (i.e., remove) the error from the instruction cache. *Id.*

B. Overview of Itou

Itou is titled “Control System and Memory Control Method Executing a Detection of an Error in a Formation in Parallel With Reading Operation.” Ex. 1007, code (54). The invention generally relates to control of access to a memory in order “to provide a memory control technology capable of ensuring a high reliability by having a data error correcting function and exhibiting the same performance as an architecture containing no error correcting mechanism.” *Id.* at 1:9–10, 1:40–44. Itou discloses a memory control device which, among other components, includes a memory module and an error detecting unit executing an error detection operation in parallel with a reading operation of the memory module. *Id.* at code (57). Itou explains that when an error is detected, the error detecting unit corrects the error in the information containing the detected error. *Id.*

The memory control device (circuit) of Itou is shown below in

Figure 1:

FIG. 1

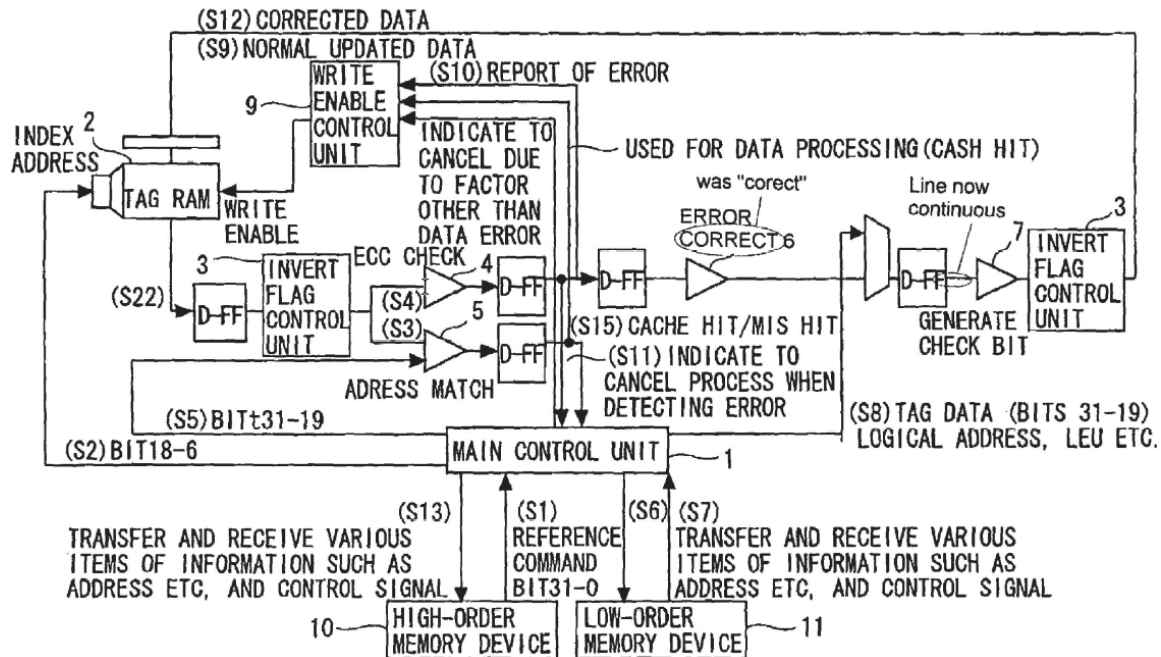


Figure 1 of Itou depicts a block diagram showing a hardware architecture of a memory control circuit. *Id.* at 2:48–50. This memory control circuit includes tag RAM 2 serving as a component of a cache memory, a data write circuit for writing data to tag RAM 2, a data read circuit for reading from tag RAM 2, and main control unit 1 that controls the data write and read to and from tag RAM 2. *Id.* at 3:9–15. As shown in Figure 1, the CPU (high-order memory device 10) is coupled to tag RAM 2 via main control unit 1.

Itou recognizes that prior methods of data protection include a parity check, but Itou states that “[t]he parity check is, though capable of detecting an error, incapable of correcting the error.” *Id.* at 1:10–17. Itou explains that according to the parity check method, “an access time is delayed to a great degree due to the error correcting process,” and invalidating the data causes the logic to become intricate in such a method. *Id.*

C. Discussion

Petitioner asserts that each of independent claims 1, 21, and 29 are unpatentable under 35 U.S.C. § 103 as obvious over Lempel and Itou. Pet. 15–28, 47–48, 54–59. In particular, Petitioner relies upon both Lempel and Itou to teach the preamble of claim 1, the limitation requiring “each of the instructions being fetched during a respective one of a plurality of instruction cycles,” and the final limitation requiring “performing error detection for each of the instructions concurrently with the fetching of a respective one of the instructions.” *See* Pet. 15–28. Claims 21 and 29 have nearly identical limitations. We consider whether Petitioner has provided sufficient explanation showing how a person of ordinary skill in the art would have combined the teachings of Lempel and Itou so as to meet the subject matter recited in claims 1, 21, and 29.

Based on the totality of the record before us, we determine that Petitioner does not provide a convincing underlying rationale as to why a person of ordinary skill in the art would be motivated to combine features of Lempel and Itou. Below, we consider Petitioner’s contentions as to this issue, Patent Owner’s response, and then provide our analysis.

1. Petitioner’s Reasons for Combining Lempel and Itou

Petitioner identifies three reasons why a person of ordinary skill in the art (POSITA) would have been motivated to combine Lempel and Itou. Pet. 66. First, Petitioner states that “both Lempel and Itou are directed to systems and methods for addressing errors in data—where data is used as a broad term that encompasses instructions as would be understood by a POSITA— stored in cache memories that are operatively coupled to respective processors.” Pet. 66–67 (citing Ex. 1002 ¶¶ 227, 228) (Dr. Sechen’s Declaration repeats the Petition nearly verbatim). Petitioner points

out that Lempel relates to a system and method for handling soft errors in cache memory and Itou concerns a memory control technology for ensuring a high reliability by having a data error correcting function and exhibiting the same performance as an architecture containing no error correcting mechanism. Pet. 67 (citing Ex. 1006, 1:6–8; Ex. 1007, 1:41–44).

Second, Petitioner contends that the POSITA would have been motivated to combine Lempel and Itou because “Lempel and Itou offer a variety of solutions to a POSITA for detecting and correcting data errors in a cache,” and “[a] POSITA would therefore be able to combine teachings from both references to achieve improved error detection and recovery solutions.” Pet. 67. Petitioner provides an example that

a POSITA could use the error detection and recovery method of Itou (*e.g.*, an ECC (Error Check Code)-based method) when a correctable error is detected, and the error detection and recovery method of Lempel (*e.g.*, targeted invalidation of the data errors in the cache and selectively replacing the invalidated data with error-free data from the main memory) when a non-correctable error is detected to reduce the latency associated with accessing the content of the main memory. (*Id.*) . . . Lempel does not address the additional computation time required by error correction circuitries (Ex. 1006, 1:35-43; Ex. 1002, ¶229). Thus, Itou will provide a clear speedup path compared to Lempel, whereas Lempel will be highly useful when the error is not correctable (*e.g.*, when two or more bits contain errors) and a cache line needs to be re-loaded from main memory in a minimum amount of time. (Ex. 1002, ¶229.)

Id. at 67–68. Petitioner reasons that Itou can be applied to other types of memories and thus, “a POSITA would understand that the methods of Itou, as a whole or partially, can be combined with the teachings of Lempel. (Ex. 1002, ¶230.).” Pet. 68.

Finally, for its third reason, Petitioner argues that “applying the teachings of Itou in Lempel, or vice versa, does not require substantial changes . . . because both Itou and Lempel disclose configurations using known hardware components.” *Id.* Thus, Petitioner alleges, “the combination of Lempel and Itou would yield predictable results.” *Id.*

2. *Patent Owner’s Contentions as to the Combination of Lempel and Itou*

Patent Owner contends that “Petitioner’s argument for combining Lempel and Itou is fatally flawed,” and “[t]here is no reasonable likelihood that Ground 1 would render unpatentable any claim of the ’619 patent.” Prelim. Resp. 22. Patent Owner questions the second motivation given by Petitioner for combining the references, and notes that “Lempel, specifically advises against using error correction circuitry (referenced in Lempel as ‘ECC’) in its specification.” *Id.* “Lempel advised avoiding ECC approaches to error detection altogether, due to the timing, performance, space, and cost limitations of then-existing ECC hardware.” *Id.* (citing Ex. 1006, 1:31–44, 1:58–61). According to Patent Owner, the approach adopted in “Lempel sought to improve upon the known method of using parity checking to detect errors by avoiding the need to shut down the processor when errors are detected.” *Id.* at 22–23 (citing Ex. 1006, 1:20–30). Patent Owner argues “Lempel did not accomplish this by performing error detection in parallel with the processor’s operation, but rather by pausing processor operations when an error is detected and allowing microcode to clear the error from the instruction cache.” *Id.* at 23 (citing Ex. 1006, 1:31–42, 2:32–39).

Patent Owner next contrasts the system in Itou, which “set out to improve upon the known strategy of adding an error-correcting circuit (referenced in Itou as ‘ECC’) to the cache memory by developing ECC

hardware that could operate in parallel with normal processor operations, thereby improving performance.” Prelim. Resp. 23 (citing Ex. 1007, 1:21–29 (“error correcting circuit is known as an error correcting mechanism on the memory”), 9:9–12 (“the ECC-based data check and the normal operation are performed in parallel”)). Patent Owner contends that Petitioner asserts that both of Lempel’s and Itou’s approaches could be combined in a single integrated circuit but Petitioner does not explain how this proposed combination would actually operate. *Id.* at 23–24. Instead, Patent Owner alleges that “[a] POSITA would not have seen the Itou and Lempel solutions as equal or compatible with each other,” and they “would have recognized that Lempel and Itou provide markedly different solutions (Lempel’s parity checking versus Itou’s ECC circuitry) to the same problem (error detection due to bit flipping).” *Id.* at 24.

Patent Owner further argues that Lempel’s consistent disparagement of ECC approaches, as carried out in Itou, teaches away from the combination. *Id.* Specifically, “a POSITA would have recognized that Lempel teaches away from ECC approaches by stating several reasons why parity checking is superior, namely, that ECC imposes area and timing constraints on the circuit design, adversely impacting processor performance, and costs more.” *Id.* (citing Ex. 1006, 1:31–44, 1:58–61). “Thus,” according to Patent Owner, “a POSITA seeking to improve upon Lempel’s parity checking system would have been dissuaded from using approaches that require ECC hardware, such as Itou’s.” *Id.* Accordingly, Patent Owner contends that “Petitioner’s argument in support of a motivation to combine Lempel and Itou thus lacks merit.” *Id.* For the reasons set forth below, we agree.

3. *Analysis*

We consider whether Petitioner has provided sufficient explanation showing how and why a person of ordinary skill in the art would have combined the teachings of Lempel and Itou so as to meet the subject matter recited in claims 1, 21, and 29.

Petitioner's first rationale for the combination is that it makes sense to combine the references because both are "directed to systems and methods for addressing errors in data." Pet. 66–67. As set forth more below, the approach that each reference takes to address errors in data is distinct. Petitioner has not shown how combining these references would be compatible to the person of ordinary skill in the art. The person of ordinary skill in the art would have recognized that Lempel and Itou provide distinct solutions (Lempel's parity checking versus Itou's ECC circuitry) to the same problem (error detection due to bit flipping). Thus, Petitioner's first contention is too conclusory and vague with respect to how a person having ordinary skill in the art would have combined the teachings of the asserted art to meet any particular element of the claims.

For instance, Petitioner does not identify persuasively the differences between either Lempel or Itou and the limitations they supposedly teach in combination, nor does Petitioner provide persuasive explanation as to how either reference would be modified to accommodate the distinct architecture of the other reference (Lempel's parity checking and Itou's ECC circuitry) in a combination. Petitioner does not explain adequately how this proposed combination would operate. Because the teachings of Lempel and Itou are somewhat contradictory, Petitioner should have provided at least some explanation as to how the resulting system operates and why a person of

ordinary skill in the art would have combined the references to operate in that manner. *See* Prelim. Resp. 24.

Petitioner next argues that

a POSITA could use the error detection and recovery method of Itou (*e.g.*, an ECC (Error Check Code)-based method) when a correctable error is detected, and the error detection and recovery method of Lempel (*e.g.*, targeted invalidation of the data errors in the cache and selectively replacing the invalidated data with error-free data from the main memory) when a non-correctable error is detected to reduce the latency associated with accessing the content of the main memory.

Pet. 67. This rationale, however, fails to address Lempel’s consistent disparagement of ECC approaches, as adopted in Itou. Based on Lempel’s teachings, adding ECC functionality to an integrated circuit already configured with parity checking functionality would increase “space on the silicon” as well as increase cost. *See* Ex. 1006, 1:31–44, 1:58–61. Yet, Petitioner does not acknowledge these drawbacks of ECC circuitry, much less explain why they would have been acceptable to a POSITA. Thus, we are not persuaded a POSITA would have been willing to combine the two references as proposed by Petitioner.

Petitioner (and its expert Dr. Sechen) argue that a POSITA would have been motivated to combine Lempel with Itou, but Petitioner’s arguments do not address Lempel’s clear disclosure of the disadvantages of using ECC hardware, nor explain why a POSITA would seek to incorporate any aspect of allegedly inferior ECC hardware, such as Itou’s, into an allegedly superior parity checking system like Lempel’s. As noted above, Lempel suggests that ECC approaches (like Itou) are not adequate and that parity checking is superior because ECC imposes area and timing constraints on the circuit design, adversely impacting processor performance, and costs

more. *See* Ex. 1006, 1:31–44, 1:58–61. Petitioner and Dr. Sechen fail to address these disadvantages and how they would impact the analysis for a person of ordinary skill in the art. Further, a person of ordinary skill in the art reading Itou would also question whether Lempel’s parity checking method was acceptable because Itou describes known parity checking techniques as “incapable of correcting” an error. Ex. 1007, 1:12–17. Thus, Petitioner has not established that a POSITA seeking to improve upon Lempel’s parity checking system would have adopted an approach that requires ECC hardware, such as Itou’s. Petitioner has not established that a person of ordinary skill in the art would have viewed the Itou and Lempel solutions as compatible.

Finally, we do not find Petitioner’s “predictable results” arguments persuasive. Pet. 68. Petitioner did not provide an adequate factual analysis of the technological differences or the compatibility of the two distinct systems of error detection. Merely characterizing that the combination yields predictable results is insufficient in this instance when information within references suggest combining them would not have been predictable. Based on the distinct approaches of error detection and correction between Lempel and Itou, Petitioner has not sufficiently established that the combination of these systems would have yielded predictable results.

In summary, Petitioner does not explain with sufficient specificity how or why a person of ordinary skill in the art would have combined Lempel with Itou. Because each ground upon which the Petition relies is based on the combination of Lempel and Itou, including each independent claim challenged, Petitioner has not proven by a reasonable likelihood that it would prevail in showing that any claim of the ’619 patent is unpatentable.

VII. CONCLUSION

For the foregoing reasons, we conclude that the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail in showing that any of claims 1–32 of the '619 patent is unpatentable.

VIII. ORDER

Upon consideration of the record before us, it is:

ORDERED that the Petition is denied, and we do not institute *inter partes* review of any claim of the '619 patent based on the grounds asserted in this Petition.

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