

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP B.V., NXP USA, INC., and
NXP SEMICONDUCTORS N.V.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2021-00966
Patent 8,049,340 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM
JULIET MITCHELL DIRBA, *Administrative Patent Judges.*

DIRBA, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Dismissing Renewed Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. § 42.122(b)

On May 17, 2021, NXP B.V., NXP USA, Inc., and NXP Semiconductors N.V. (collectively “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–19 of U.S. Patent No. 8,049,340 B2 (Ex. 1001, “the ’340 patent”). Paper 1 (“Pet.”). Bell Semiconductor, LLC¹ (“Patent Owner”) filed a Preliminary Response. Paper 13 (“Prelim. Resp.”).

Petitioner also timely filed a Motion for Joinder seeking to join IPR2021-00148 (the “148 IPR”). Paper 3. The parties to the 148 IPR subsequently filed a joint motion to terminate the 148 IPR, and Petitioner then filed a Renewed Motion for Joinder (Paper 9) pursuant to our authorization (Paper 7). Patent Owner filed an Opposition to that motion (Paper 11), and Petitioner filed a Reply in support (Paper 12).

An *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Having reviewed the parties’ papers and the evidence of record, we are not persuaded to discretionarily deny institution, and we determine that Petitioner has shown a reasonable likelihood it will prevail in establishing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review. In addition, as explained below, we dismiss Petitioner’s Renewed Motion for Joinder as moot.

¹ Patent Owner states that it “is a wholly owned subsidiary of Hilco Patent Acquisition 56, LLC.” Paper 6, 2.

I. BACKGROUND

A. Related Matters

The parties indicate that the '340 patent has been asserted in several district court lawsuits, including *Bell Semiconductor, LLC v. NXP Semiconductors N.V.*, 1:20-cv-00611 (W.D. Tex.). Pet. 91–92; Paper 6 (Patent Owner's Mandatory Notice), 2.

The parties also identify two *inter partes* review proceedings challenging the '340 patent, filed by Texas Instruments Incorporated (IPR2020-01692) and Microchip Technology Inc. and Microsemi Corporation (IPR2021-00148). Pet. 92; Paper 6, 2. Both of these proceedings have since been terminated due to the parties' settlement. *Texas Instruments Inc. v. Bell Semiconductor, LLC*, IPR2020-01692, Paper 15 (PTAB April 6, 2021); *Microchip Tech. Inc. v. Bell Semiconductor, LLC*, IPR2021-00148, Paper 25 (PTAB October 7, 2021).

In addition, Petitioner identifies IPR2021-00967, which is an *inter partes* review proceeding filed by Petitioner that challenges U.S. Patent No. 8,288,269 B2, a divisional of the '340 patent. Pet. 92. Concurrently with this Decision, we also issue a decision instituting *inter partes* review in that proceeding.

B. The Petition's Asserted Grounds

Petitioner asserts the following grounds of unpatentability (Pet. 2):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3, 4, 6–9, 12–15	103(a) ²	Chin ³
2, 4, 5, 10	103(a)	Chin, MC92600, ⁴ HighSpeed ⁵
3, 11	103(a)	Chin, Oggioni ⁶
16, 17	103(a)	Chin, MC92600
18	103(a)	Chin, MC92600, Oggioni
19	103(a)	Chin, MC92600, Oggioni, Hsu, ⁷ Barr ⁸
6–9	103(a)	Chin, HighSpeed
2, 4, 5, 10	103(a)	Chin, Shafer, ⁹ HighSpeed
16, 17	103(a)	Chin, Shafer

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the challenged patent was filed before March 16, 2013, we refer to the pre-AIA version of § 103.

³ US 6,765,298 B2, issued July 20, 2004 (Ex. 1004).

⁴ Motorola, MC92600 Quad 1.25 Gbaud SERDES User's Manual, Rev. 2 (Feb. 2003) (Ex. 1008).

⁵ Stephen H. Hall et al., *High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices* (2000) (Ex. 1009).

⁶ US 6,717,255 B2, issued Apr. 6, 2004 (Ex. 1006).

⁷ US 2005/0037601 A1, published Feb. 17, 2005 (Ex. 1007).

⁸ US 2005/0011676 A1, published Jan. 20, 2005 (Ex. 1011).

⁹ US 6,908,340 B1, filed Sept. 11, 2003, issued June 21, 2005 (Ex. 1026).

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
18	103(a)	Chin, Shafer, Oggioni

Petitioner also relies on the testimony of David Choi, Ph.D. to support its contentions. Ex. 1003. Patent Owner relies on the testimony of Mr. Peter Elenius in its Preliminary Response. Ex. 2002.

C. Summary of the '340 Patent

The '340 patent is titled “Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package.” Ex. 1001, code (54). It issued from an application filed on March 22, 2006. *Id.* at code (22).

The '340 patent is “directed to the design of an integrated circuit package that minimizes parasitic capacitance between metal layers in a ball grid array integrated circuit package.” Ex. 1001, 1:8–13. The '340 patent explains:

In integrated circuits such as serializer/deserializer (SERDES) devices that convert a serial data stream to or from a parallel data stream, high data transfer rates may require fast switching speeds that surpass 1 GHz. At such high frequencies, the parasitic capacitance between transmit (Tx) and receive (Rx) contact pads in the contact pad layer and nearby metal layers of the integrated circuit package may result in a deterioration of the signal waveform and a correspondingly reduced circuit performance.

Id. at 2:52–60. The '340 patent teaches avoiding the parasitic capacitance between the contact pads and other nearby metal layers by forming “cutouts” in the metal layers to “enclose an area that surrounds each of the contact pads.” *Id.* at 3:58–63.

The '340 patent illustrates one embodiment in Figure 5, reproduced below.

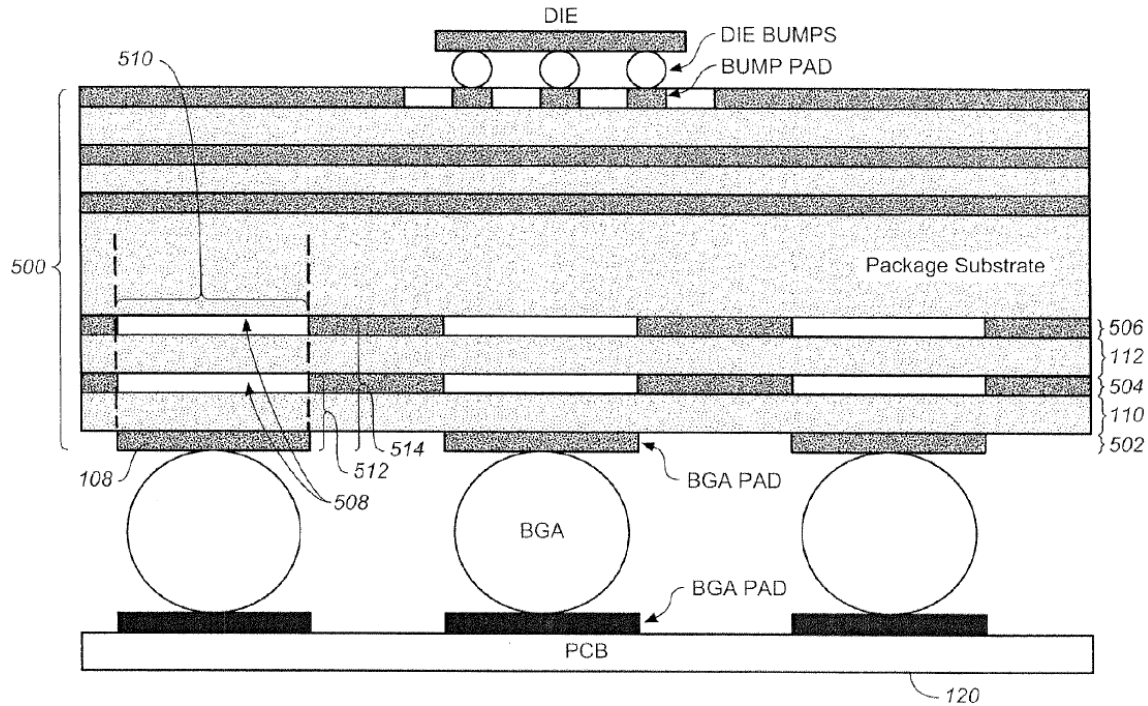


FIG. 5

As shown above, Figure 5 shows a partial side view of integrated circuit package substrate 500, which includes ball pad 108, dielectric layers 110 and 112, vias¹⁰ (not shown), printed circuit board 120, contact pad metal layer 502, routing metal layer 504, and ground return metal layer 506. Ex. 1001, 4:9–18. Figure 5 also shows cutouts 508 in routing metal layer 504 and ground return metal layer 506 above ball pad 108. *Id.* at 4:19–23.

According to the '340 patent, cutout 508 encloses cutout area 510 “so that the area enclosed by the ball pad 108 is completely surrounded by the cutout area 510,” which means that “there is no overlap between the area enclosed by the ball pad 108 and the metal in the routing metal layer 504 and in the

¹⁰ According to the '340 patent, “[c]onnections between the electrically conductive layers, typically metal layers, are made by forming vias in the electrically insulating layers, typically dielectric layers, and depositing an electrically conductive material in the vias, such as copper.” Ex. 1001, 1:18–22.

ground return metal layer 506 above the ball pad 108.” *Id.* at 4:31–36; *see id.* at 4:51–54 (explaining that the dashed lines in Fig. 5 extending upward from the sides of contact pad 108 demonstrate how contact pad 108 encloses the areas of routing metal layer 504 and ground return metal layer that are overlapped by ball pad 108).

The ’340 patent explains that parasitic capacitances 512 and 514 in Figure 5 are reduced compared to capacitances in prior art integrated circuits that are similarly constructed but lack cutouts 508, and that “[t]he reduction in parasitic capacitance advantageously extends the upper frequency limit that may be used to drive the ball pad 108 in the integrated circuit package substrate.” Ex. 1001, 4:59–65 (referring to capacitances 114 and 116 in the prior art integrated circuit shown in Fig. 1).

D. Challenged Claims

Petitioner challenges all claims of the ’340 patent. Claims 1, 7, and 12 are independent.

Independent claim 1 is illustrative:

1. An integrated circuit package substrate comprising:

[a] a first and a second electrically conductive layer separated from each other by an electrically insulating layer with no intermediate conductive layer therebetween;

[b] a plurality of rows of contact pads formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board; and

[c] a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer,

[d] wherein each cutout encloses an electrically insulating area within the second electrically conductive layer, and

[e] wherein each electrically insulating area completely overlaps a corresponding one of the contact pads formed in the first electrically conductive layer such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

Ex. 1001, 6:36–54 (line breaks and reference designations added).

Independent claims 7 and 12 are also apparatus claims with similar scope; however, claim 7 recites a “routing metal layer” rather than a “second electrically conductive layer,” and claim 12 recites three layers rather than two. *Id.* at 7:21–36, 8:7–21.

II. DISCRETION TO DENY

Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 314 and deny institution based on a district court trial scheduled to begin on April 11, 2022, involving the ’340 patent and the same parties. *See* Prelim. Resp. 1–7. Petitioner argues that discretionary denial is unwarranted. Pet. 88–90.

A. Legal Standard for Exercising Discretion under Section 314(a)

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. *See Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir.

2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

In determining whether to exercise discretion on behalf of the Director, we are guided by the Board’s precedential decision in *NHK Spring Co. v. Intri-Plex Techs, Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential). In *NHK*, the Board found that the “advanced state of the district court proceeding” was a “factor that weighs in favor of denying” the petition under § 314(a). *NHK*, Paper 8 at 20. The Board determined that “[i]nstitution of an *inter partes* review under these circumstances would not be consistent with ‘an objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.’” *Id.* (citing *Gen. Plastic Indus. Co., Ltd. v. Canon Kabushuki Kaisha*, IPR2016-01357, Paper 19, 16–17 (PTAB Sept. 6, 2017) (precedential in relevant part)).

The Board’s precedential decision in *Fintiv* sets forth six factors that we consider when determining whether to use our discretion to deny institution due to the advanced state of a parallel proceeding: *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 3 (PTAB Mar. 20, 2020) (precedential) (Order) (“*Fintiv*”). When determining whether to exercise discretion to deny institution under *NHK* due to an earlier trial date, we consider the following factors (“*Fintiv* factors”):

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;

4. overlap between issues raised in the petition and in the parallel proceeding;

5. whether the petitioner and the defendant in the parallel proceeding are the same party; and

6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 6. “These factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Id.* In evaluating these factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* (citing Patent Trial and Appeal Board Consolidated Trial Practice Guide, November 2019 (“CTPG”), 58¹¹). We address the *Fintiv* factors below.

B. Analysis of Fintiv Factors

1. Factor 1: Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted

Patent Owner argues that this factor weighs in favor of denying institution because Petitioner has not offered any evidence that the district court would grant a stay if *inter partes* review is instituted. Prelim. Resp. 1. Petitioner does not address this factor. *See* Pet. 88.

Because neither party has produced evidence that a stay was requested or that the district court considered staying the parallel litigation, we determine that Factor 1 is neutral. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) (Institution

¹¹ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

Decision) (“*Fintiv II*”) (holding that “[t]his factor does not weigh for or against discretionary denial” when neither party requested a stay).

2. *Factor 2: Proximity of the Court’s Trial Date to the Board’s Projected Statutory Deadline*

Petitioner argues that this factor is neutral, citing the Board’s decision in *Western Digital v. Kuster*, IPR2020-01410, Paper 13 at 10–11 (PTAB Feb. 17, 2021), in which the panel determined this factor is neutral when the final written decision was expected three and a half months after the expected trial date. Pet. 89. Petitioner also argues that there is some uncertainty in the trial schedule, because of the COVID-19 pandemic. *Id.*

Patent Owner argues that this factor favors denying institution because the trial in the parallel district court proceeding is scheduled for April 11, 2022, and a Final Written Decision would likely issue somewhere between 4.5 to 7.5 months later. Prelim. Resp. 2 (citing Ex. 1028, 6). Patent Owner also argues that Petitioner offers no evidence indicating the trial date will be delayed due to the COVID-19 pandemic. *Id.* at 3.

The proximity factor in *Fintiv* asks us to evaluate our discretion in light of trial dates that have been set in parallel litigations. *See Fintiv*, Paper 11 at 3, 5, 9. Where, as here, the trial date is approximately six months earlier than the projected date of our Final Written Decision, the Board has weighed this factor in favor of exercising discretion to deny institution. *See id.* at 9. Although the trial could be delayed (e.g., as a result of the COVID-19 pandemic), the record includes no evidence indicating that such a delay is likely, and we decline to speculate about the likelihood of such a delay. Therefore, we find that factor 2 weighs in favor of exercising our discretion to deny institution.

3. *Factor 3: Investment in the Parallel Proceeding by the Court and Parties*

Petitioner argues that this factor weighs against discretionary denial because “[s]ubstantial work remains in the district court” and the “district court’s Markman orders will have minimal relevance here as the only claim constructions raised by Patent Owner in this IPR do not overlap with those at issue in the district court.” Pet. 89–90.

Patent Owner argues that the investment in the parallel proceeding by the court and parties has been “immense.” Prelim. Resp. 3. Patent Owner contends the district court has already conducted a claim construction hearing and issued a Markman Order, and that fact discovery opened on April 12, 2021, and is scheduled to close on November 4, 2021. *Id.* (citing Ex. 2004 (docket entries), 12; Ex. 1028 (scheduling order), 4). Patent Owner further notes that opening expert reports are due on November 18, 2021. *Id.* Additionally, Patent Owner asserts that given the current trial schedule, the parties will have to invest a significant amount of time and resources after institution but before a Final Written Decision issues, including completion of fact and expert discovery, pre-trial motion practices, trial preparation, trial, and post-trial briefing. *Id.* at 4–5.

We, however, consider the investment “at the time of the institution decision” not at some later date (*Fintiv*, Paper 11, 9–10), and thus we do not agree with Patent Owner’s arguments about investments that will occur after this Decision, but prior to any Final Written Decision for this proceeding. In addition, the present circumstances are somewhat similar to those in *Sand Revolution II v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”),

in which the district court conducted a Markman hearing and entered an order construing claim terms. *Id.* at 10. The *Sand Revolution* panel found that “aside from the district court’s Markman Order, much of the district court’s investment relates to ancillary matters untethered to the validity issue itself” and “much work remains in the district court case as it relates to invalidity: fact discovery is still ongoing, expert reports are not yet due, and substantive motion practice is yet to come,” and determined that the parties had not invested substantially in the merits of the invalidity positions at issue. *Id.* at 10–11. Similarly, here, fact discovery is still ongoing, expert reports are not yet due, and substantive motion practice is yet to come, so “much work remains in the district court case as it relates to invalidity.” *Id.* at 11. Furthermore, although the district court has issued a Markman Order, Patent Owner does not dispute Petitioner’s assertion that the “district court’s Markman orders will have minimal relevance” in this proceeding. Pet. 90.

Fintiv also directs us to consider whether “the petitioner filed the petition expeditiously.” *Fintiv*, Paper 11 at 11. Petitioner, however, does not present any argument as to diligence. Accordingly, there is no showing of Petitioner diligence that weighs against exercising our discretion to deny.

Considering the above facts, we find this factor weighs marginally in favor of exercising our discretion to deny institution under § 314(a).

*4. Factor 4: Overlap Between Issues Raised in the Petition
and in the Parallel Proceeding*

In the Petition, Petitioner states that “[t]here should be no overlap between this IPR and the district court proceeding because Petitioners stipulate not to pursue in the district court any ground raised or that could have [been] reasonably raised in an IPR (*i.e.*, under §§ 102, 103 on the basis

of prior art patents or printed publications alone) if this IPR is instituted.”
Pet. 90.

Patent Owner argues that the same invalidity arguments raised in the Petition are also raised in the district court action. Prelim. Resp. 5. With regard to Petitioner’s stipulation, Patent Owner states that Petitioner has not submitted the stipulation in district court, and asserts that “[w]ithout seeing the actual language of the stipulation, one is left to wonder what the stipulation would indeed cover.” *Id.* at 5.

Petitioner’s stipulation here, which includes a representation that Petitioner will not pursue any ground raised or that could have been reasonably raised in the *inter partes* review, is similar to the one the petitioner made in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 18–19 (PTAB Dec. 1, 2020) (precedential as to § II.A) (“*Sotera*”). As stated in *Sotera*, this type of stipulation “mitigates any concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.” *Id.* at 19. Furthermore, as noted in *Sand Revolution*, this type of broad stipulation “better address[es] concerns regarding duplicative efforts and potentially conflicting decisions in a much more substantial way.” *Sand Revolution*, Paper 24 at 12 n.5.

Considering that Petitioner has agreed to be bound by a stipulation with substantively the same wording as the stipulation addressed in *Sotera*, we follow the *Sotera* precedent in finding that this factor weighs strongly against exercising discretion to deny. *See Sotera*, Paper 12 at 18–19.

5. *Factor 5: Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party*

“If a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution under NHK.” *Fintiv*, Paper 11 at 13–14. Here, Petitioner is the defendant in the district court action. Accordingly, *Fintiv* factor 5 weighs in favor of exercising discretion to deny institution.

6. *Factor 6: Other Circumstances that Impact the Board’s Exercise of Discretion, Including the Merits*

Petitioner argues that the “unpatentability grounds presented here are strong . . . , and this IPR will efficiently resolve issues raised in four district court cases involving the patent.” Pet. 90.

Patent Owner contends that the Petition does not meet the threshold burden for several of the challenged claims, and Petitioner will likely continue its attacks in district court on claims that it does not prevail on in this proceeding. Prelim. Resp. 6. Patent Owner further contends that this proceeding is part of Petitioner’s “serial harassment of Patent Owner.” *Id.* As to Petitioner’s assertion regarding efficiently resolving issues in four district court cases, Patent Owner notes that all other defendants in the district court cases involving the patent have settled. *Id.* at 7.

Both Petitioner’s and Patent Owner’s arguments are unavailing as to this factor. For example, with regard to the merits of the Petition, we find that Petitioner has demonstrated a reasonable likelihood it will prevail, and such a determination weighs neither for nor against the exercise of discretion to deny institution of *inter partes* review. Similarly, with regard to Patent Owner’s “serial attacks” argument, we note that the Board terminated

IPR2020-01692 and IPR2021-00148 in view of settlements. IPR2020-01692, Paper 15; IPR2021-00148, Paper 25.

Accordingly, after considering the parties' arguments with regard to this factor, we find Factor 6 does not weigh for or against exercising discretion.

7. Balancing the Fintiv Factors

We have considered the circumstances and facts before us in view of the *Fintiv* factors. Because our analysis is fact driven, no single factor is determinative of whether we exercise our discretion to deny institution under § 314(a). Further, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review” when evaluating these factors. *Fintiv*, Paper 11 at 6. Having evaluated all of the factors on this record, we do not exercise our discretion under § 314(a) to deny institution of *inter partes* review.

III. ANALYSIS

A. The Level of Ordinary Skill in the Art

Petitioner asserts that the level of ordinary skill in the art corresponds to a bachelor's degree in electrical engineering or a related field and four years of experience in “high-frequency circuit engineering and development,” or an equivalent combination of education and practical experience. Pet. 3 (citing Ex. 1003 ¶ 26).

At this stage, Patent Owner does not address the level of ordinary skill in the art. *See generally* Prelim. Resp.

We are satisfied that Petitioner's proposed definition generally comports with the level of skill necessary to understand and implement the

teachings of the '340 patent and the asserted prior art. This definition is also supported by the testimony of Dr. Choi. *See* Ex. 1003 ¶ 26. For purposes of this Decision, we adopt Petitioner's proposed level of skill.

To the extent the level of ordinary skill in the art is in dispute or makes a material difference in the obviousness analysis, the parties should brief their respective positions in this regard during trial.

B. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). Under the principles set forth by our reviewing court, the “words of a claim ‘are generally given their ordinary and customary meaning,’” as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Petitioner contends that no terms require express construction in this proceeding. Pet. 14. Patent Owner raises two claim construction arguments. Prelim. Resp. 12–16. First, Patent Owner argues that the preamble of claim 1 is limiting (*id.* at 12–13), and second, Patent Owner advances a construction of the term “contact pad” (*id.* at 14–16). For the reasons provided below, we determine that the preamble is a limitation of independent claim 1, but not the other independent claims. As for “contact pad,” we need not expressly construe this term in this Decision.

Based on the record before us, we do not find it necessary to provide express claim constructions for any terms or phrases, except the preambles of independent claims 1, 7, and 12. *See Nidec Motor Corp. v. Zhongshan*

Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Is the Preamble a Limitation?

“Generally, the preamble does not limit the claims.” *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). But, in certain situations, a preamble is limiting:

In general, a preamble limits the invention if it recites essential structure or steps, or if it is “necessary to give life, meaning, and vitality” to the claim. Conversely, a preamble is not limiting “where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.”

Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999); *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)).

Patent Owner argues that the preamble of claim 1—“[a]n integrated circuit package substrate”—is limiting because it provides antecedent basis for a limitation appearing in the body of the claim. Prelim. Resp. 12 (citing *Pitney Bowes*, 182 F.3d at 1305–06). Specifically, claim 1 recites “a plurality of rows of contact pads . . . for making a direct connection between *the* integrated circuit package substrate and a printed circuit board.” *Id.* (quoting Ex. 1001, 6:40–43) (alteration in original). Relatedly, Patent Owner submits that a person of ordinary skill would understand that an

“integrated circuit package substrate” is different than a “printed circuit board” (“PCB”). *Id.* at 13 (also citing Ex. 1001, Figs. 1, 5).

On this record, we agree with Patent Owner.¹² Claim 1 recites “[a]n integrated circuit package substrate comprising,” *inter alia*, “a plurality of rows of contact pads . . . for making a direct connection between the integrated circuit package substrate and a printed circuit board.” Ex. 1001, 6:36–43. The phrase “the integrated circuit package substrate” derives antecedent basis from the preamble. *See id.* Given the structure of this claim, we conclude that the preamble is limiting. *See Bio-Rad Labs., Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1371 (Fed. Cir. 2020) (“The fact that [two of] the terms [in preamble] . . . provide antecedent basis for these terms in the body of the claim is a strong indication that the preamble acts ‘as a necessary component of the claimed invention.’” (quoting *Eaton Corp. v. Rockwell Int’l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003))); *see also Shoes by Firebug LLC v. Stride Rite Children’s Grp., LLC*, 962 F.3d 1362, 1368 (Fed. Cir. 2020) (“While antecedent basis alone is not determinative of whether a preamble is limiting, use of preamble terms to define positive limitations in the body of claims can evince an inventor’s intent that the preamble limit the scope of the claim.”).

This conclusion, however, does not apply to the other two independent claims of the ’340 patent. While independent claims 7 and 12 recite the same preamble as claim 1, the bodies of these claims do not rely on the preamble for antecedent basis. *See* Ex. 1001, 7:22–36 (no recitation of “integrated circuit package substrate” in body of claim 7), 8:8–21 (same

¹² Petitioner has not yet had an opportunity to respond to this claim construction issue, but may do so in its reply brief at trial.

for claim 12). Patent Owner provides (and we perceive) no other reason to conclude that the preamble of either of these claims is limiting. *See* Prelim. Resp. 12–13 (addressing preamble of claim 1, but not claims 7 and 12). Accordingly, on this record, we conclude that independent claims 7 and 12 are not limited by their preambles.

Finally, although we agree that a person of ordinary skill would understand the claimed “integrated circuit package substrate” to be a different component than the claimed “printed circuit board” (Prelim. Resp. 13), this observation does not reveal any deficiency in Petitioner’s contentions.

C. Law on Obviousness

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The legal question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the

prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.¹³ *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes references covering each limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). A petitioner must also articulate a reason why a person of ordinary skill in the art would have combined or modified those references to yield the claimed invention. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination.”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”) (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

¹³ The current record does not include allegations or evidence of objective indicia of nonobviousness.

D. Summary of Prior Art

1. Chin (Ex. 1004)

Chin is directed to “the design and fabrication of printed circuits and multi-layered substrates that are suitable for carrying signals with very high data rates,” and relates to “techniques to reduce landing pad parasitic components and reduce the impedance discontinuity between the pad and the interconnect to the pad.” Ex. 1004, 1:7–13. Chin explains that “the impedance of the landing pads is generally significantly lower than that of their associated interconnect conductors,” and “[t]he substantial impedance drop of the pad causes excess parasitic capacitance, which results in a reduction in bandwidth and slowing the signal transition rate.” *Id.* at 1:46–48, 2:2–5. In view of this, Chin aims to “decrease the parasitic capacitance of substrate landing pads and to provide better impedance matching between the traces and the landing pads.” *Id.* at 2:20–23.

According to Chin, “[a] landing pad’s parasitic capacitance may be reduced by forming patterned holes in one or more reference potential layers below the landing pad,” and “[r]educing the landing pad’s parasitic capacitance creates a corresponding increase in the landing pad’s impedance.” *Id.* at 3:45–49. “A pre-determined amount of capacitance is then re-introduced to the landing pad” with compensation capacitors in order “to lower the pad’s characteristic impedance to match that of the trace.” *Id.* at 3:55–65.

Chin discloses several embodiments of printed circuit boards that include metal layers separated by dielectric material, with patterned holes formed in the metal layers. One embodiment is shown in Figure 2a, reproduced below.

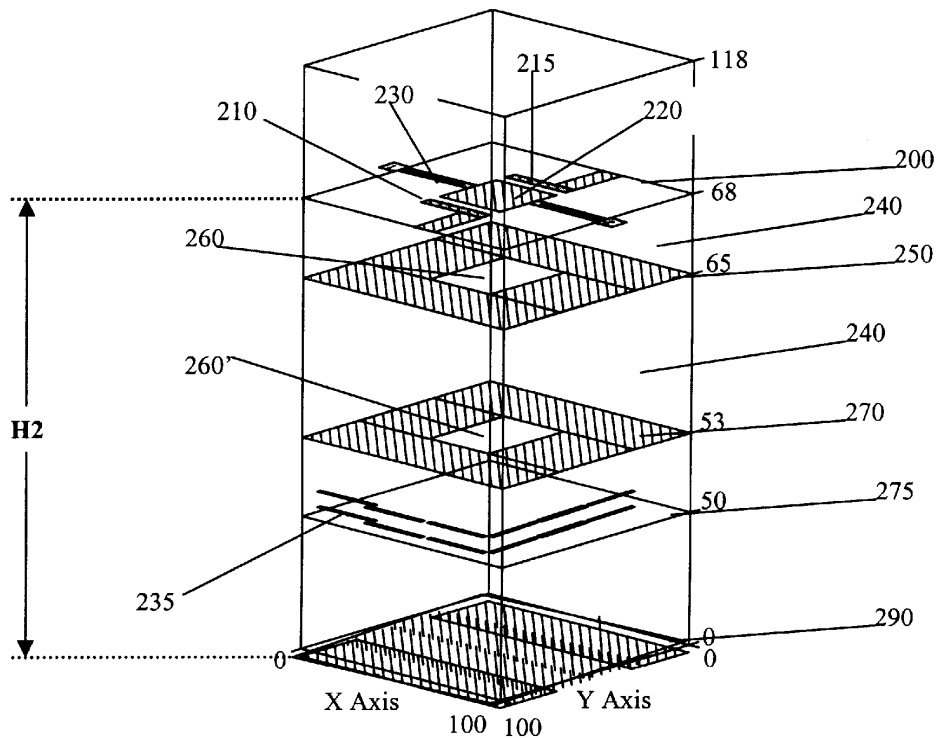


Figure 2a of Chin is an exploded isometric drawing of a segment of a printed circuit board. Ex. 1004, 4:4–5. The printed circuit board segment in Figure 2a includes: compensation capacitors 210 and 215, pad 220, and single trace 230 on surface metal layer 200; intermediate metal layers 250, 270, and 275; patterned holes 260 and 260' in layers 250 and 270, respectively; and ground reference layer 290. *Id.* at 4:4–25, 4:48–50.

2. HighSpeed (Ex. 1009)

HighSpeed is titled “High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices.” Ex. 1009, 1. In section 5.1, HighSpeed describes “vias,” which are “used to make connections between various layers of the PCB or to connect components to traces.” *Id.* at 94.

“Figure 5.1 depicts a typical through-hole via and its equivalent circuit” and is reproduced below:

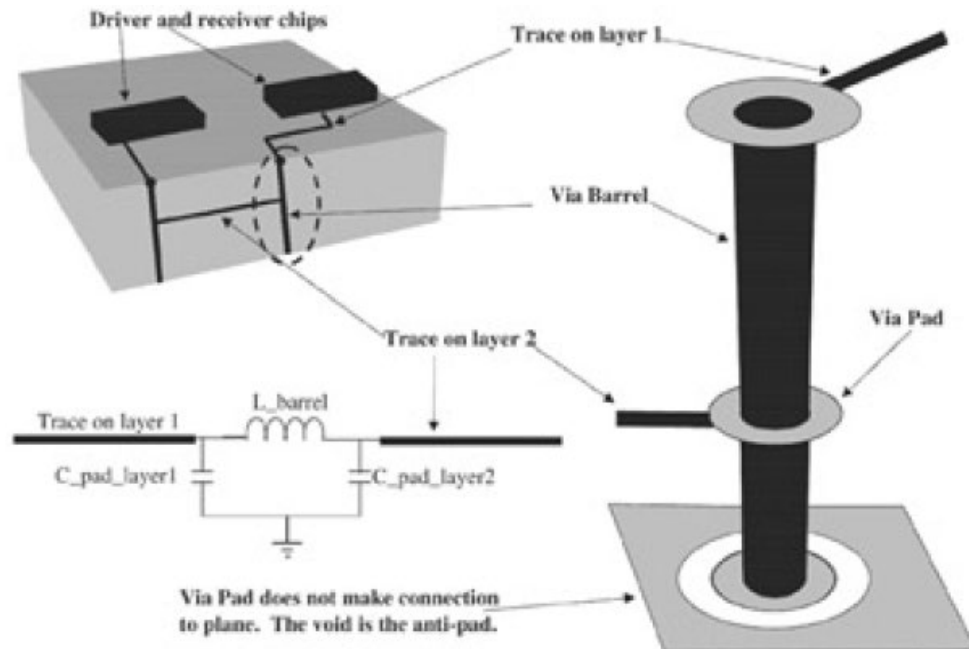


Figure 5.1: Equivalent circuit of a through-hole via.

Ex. 1009, 94. As shown above, Figure 5.1 illustrates a through-hole via connected to a trace on layer 1 and a trace on layer 2 along with its equivalent circuit. HighSpeed explains that a through-hole via “is made by drilling a hole through the board, filling it with solder, and making connections on appropriate layers via the pad.” *Id.* “Other, less common types of vias, used primarily in multichip modules (MCMs) and advanced PCBs, are blind, buried, and micro-vias.” *Id.*

3. MC92600 (Ex. 1008)

MC92600 is the User’s Manual for Motorola’s MC92600 Quad 1.25 Gbaud SERDES transceiver. Ex. 1008, 1, 17. MC92600 states that the Motorola part includes a transmitter that “takes the data byte presented at its data input . . . and serially transmits” associated information out the output pads. *Id.* at 21.

According to MC92600, the part is offered in a 196 MAPBGA package, and Figure 7-3 “provides a graphic of the package pin signal

mappings.” Ex. 1008, 67; *see id.* at 70 (showing Figure 7-3). Petitioner annotates this figure with yellow and blue highlighting, as shown below:

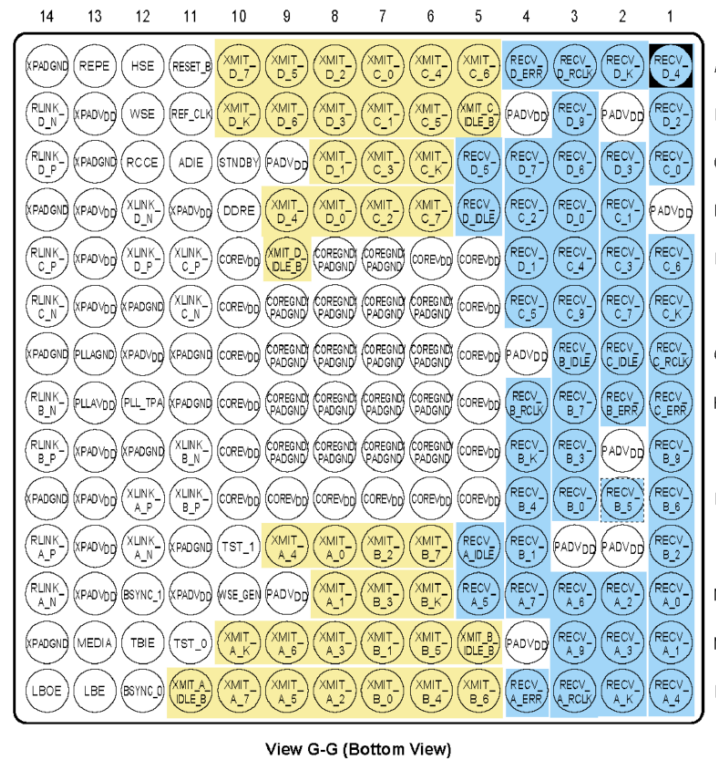


Figure 7-3. 196 MAPBGA Package

Pet. 61 (citing Ex. 1008, 70). Petitioner’s annotation of Figure 7-3, reproduced above, shows yellow-colored transmit pins (designated “XMIT”) and blue-colored receive pins (designated “RECV”). *Id.*

4. Oggioni (Ex. 1006)

Oggioni is directed to an electronic package including a chip carrier having a first conductive layer that includes at least one signal track and one contact area, and a reference structure having at least two conductive layers such that the signal track is electrically shielded by the reference structure. Ex. 1006, Abstract. Oggioni explains that the trend towards miniaturization of electronic devices has led to a reduction in the dimensions of the chip carrier conductive tracks on which the devices are

packaged, including the use of a thin dielectric layer between the conductive tracks and ground plane of the electronic package. *Id.* at 1:57–67.

According to Oggioni, “[a] shortened distance between conductive tracks and the ground plane increases the value of a corresponding stray capacitance. As a consequence, the bandwidth of the transmission line is strongly reduced.” *Id.* at 1:67–2:3.

In attempting to address this drawback, Oggioni discloses an embodiment having conductive layers that do not “intersect a shadow of the projection of” its contact areas. Ex. 1006, 4:65–5:3; Fig. 2b. Oggioni states that its invention “substantially reduces the capacitance of the stray capacitor formed between” conductive signal tracks and corresponding ground planes. *Id.* at 5:46–49.

5. *Shafer (Ex. 1026)*

Shafer is generally directed to a method and system for reducing crosstalk in backplanes, which, according to Shafer, “have become popular for providing high-speed connections between printed circuit boards.” Ex. 1026, 1:1–13. Shafer explains that as data transmission speeds increase into the gigahertz range, near-end crosstalk becomes a significant problem for certain connector pin configurations. *Id.* at 2:52–55. Shafer further explains that because transmit signals are relatively much larger than receive signals, the transmit signal couples with the receive signal. *Id.* at 2:55–57. Furthermore, “[s]ince linear equalization circuits cannot typically distinguish a signal from the crosstalk, it is difficult to correct for the crosstalk using circuitry alone.” *Id.* at 2:60–63.

To address this problem, Shafer aims to provide an improved connector pin assignment having ground shields in only one direction.

Ex. 1026, 3:11–13. Shafer describes several embodiments of a connector for connecting a circuit board to a backplane, wherein the connector includes different configurations of transmit connection positions, receive connection positions, and ground shields positioned between the transmit and receive connection positions in only one direction. *Id.* at 3:24–33. Shafer’s embodiments include receive and transmit connection elements for serializer/deserializer modules. *Id.* at 3:34–67.

6. *Hsu (Ex. 1007)*

Hsu describes a method of fabricating a semiconductor package substrate. Ex. 1007, Abstract; *see id.* ¶¶ 40, 54 (noting that “a Cavity Down Ball Grid Arrays (CDBGAs) package” can be fabricated with Hsu’s substrate). Figures 3A to 3I provide cross-sectional views of a substrate fabricated using Hsu’s method. *Id.* ¶ 38. Figure 3C is reproduced below:

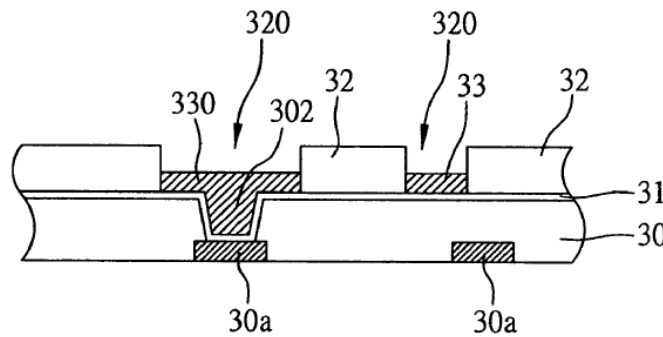


FIG. 3C

As shown above, Figure 3C is a cross-sectional view of a substrate that includes inner trace 30a, via 302, and contact pad 330, as well as insulating layer 30, conductive film 31, first resist layer 32, patterned trace layer 33, and openings 320. *Id.* ¶¶ 38, 44–46. According to Hsu, “patterned trace layer 33 has a plurality of contact pads 330 formed in the conductive vias

302 to establish connection with the inner trace 30a,” and “conductive vias 302 may be formed directly below the contact pad 330.” *Id.* ¶ 46.

7. *Barr (Ex. 1011)*

Barr teaches that “[v]ias are conductors that connect traces from one layer in a PCB to traces in another layer in a PCB.” Ex. 1011 ¶ 1. When the via passes through a ground or power plane, some of the conductive material is removed from the plane (around the via) to prevent a short: “The area that is removed creates a void called an anti-pad.” *Id.*; *see also id.* ¶ 37. In Figure 9, reproduced below, Barr shows a “via pin field of an integrated circuit 700.” *Id.* ¶ 39 (“A via pin field can exist where an integrated circuit is mounted on a PCB.”).

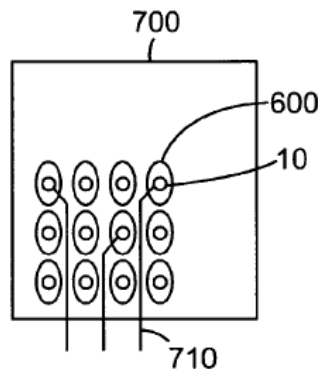


Fig. 9

As shown above, Figure 9 depicts anti-pads 600, via barrels 10, and signal traces 710. *Id.* “Signal traces 710 are illustrated on the same level as anti-pads 600 . . . for clarity,” but “are typically on a parallel signal layer.” *Id.* In addition, Barr notes that increasing the size of an anti-pad reduces the parasitic capacitance between the associated plane and via. *Id.* ¶ 2; *see id.* ¶ 40 (“Elongated anti-pads allow for signal traces 710 to be routed between anti-pads 600 while still reducing stray capacitance [].”).

E. Obviousness Ground Based on Chin Alone

Petitioner contends that the subject matter of independent claims 1, 7, and 12 and dependent claims 3, 4, 6, 8, 9, and 13–15 would have been obvious over Chin combined with the knowledge of a person of ordinary skill in the art. Pet. 18–58. Patent Owner alleges deficiencies in Petitioner’s showing for independent claim 7 and dependent claims 3, 6, 8, and 9. Prelim. Resp. 20–26, 29–33.

We begin our analysis with each of the independent claims and then turn to the dependent claims.

1. Independent Claim 1

[pre] “An integrated circuit package substrate”

Petitioner contends that, “[t]o the extent the preamble is limiting,” Chin teaches or suggests it. Pet. 20–21. Petitioner points to Chin’s reference to a “ball-grid-array (BGA) package” and “a substrate used inside a BGA package.” *Id.* at 20 (quoting Ex. 1004, 1:56–62). According to Petitioner, a person of ordinary skill in the art would know that the “substrate used inside a BGA package” is “an integrated circuit package substrate.” *Id.* at 21 (citing Ex. 1003 ¶ 85).¹⁴ Petitioner also contends “Chin

¹⁴ Petitioner also points to the application that matured into Chin. Pet. 20–21 (citing Ex. 1005, 9). We do not rely upon that evidence in this Decision. We agree that it includes a claim that is broad enough to encompass both printed circuit boards and substrates, and we agree it is prior art. *See* Ex. 1005, code (43) (published June 12, 2003), 9 (claim 1). But, contrary to Petitioner’s suggestion, the claim does not “teach the use of patterned holes (*i.e.*, cutouts) in PCBs and substrates” (Pet. 21)—it refers to neither PCBs nor substrates (*see* Ex. 1005, 9). So, even though the scope of the claim is

explains that its disclosure relates to ‘printed circuits’ *and* ‘multi-layered substrates’ and that its teachings apply broadly to ‘laminated PCB implementations’ and to ‘semiconductor implementations.’” *Id.* (quoting Ex. 1004, 1:7–10, 5:67–6:7); *see also id.* at 20 (citing Ex. 1004, 2:20–23). From this, Petitioner asserts that an ordinary artisan “would have been motivated to apply the teachings of Chin to a package substrate because both PCBs and substrates secure electronic components and route signals between components and supply reference potentials.” *Id.* at 21 (citing Ex. 1003 ¶ 86). Further, Petitioner submits that the ’340 patent includes “a typical ball grid array (BGA) integrated circuit package substrate 100 *of the prior art*” in Figure 1. *Id.* (quoting Ex. 1001, 2:1–3).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches or suggests this limitation. Although most of Chin refers specifically to printed circuit boards, we are sufficiently persuaded, at this stage, that a person of ordinary skill in the art would have understood Chin’s disclosure to include other multi-layered substrates, such as an integrated circuit package substrate. *See* Pet. 20–21. For example, Chin references an example BGA package in a printed circuit board, as well as “a substrate used inside a BGA package.” Ex. 1004, 1:56–62. Also, Chin states that “semiconductor implementations” are within the scope of the invention. *Id.* at 5:67–6:10; *see also id.* at 1:8–9 (stating that invention

consistent with Petitioner’s interpretation of Chin, we question whether this evidence is a reliable indication of the proper understanding of Chin.

“relates generally to the design and fabrication of printed circuits and multi-layered substrates”).

[a] “a first and a second electrically conductive layer separated from each other by an electrically insulating layer with no intermediate conductive layer therebetween”

Petitioner contends that Chin teaches this limitation. Pet. 22–23. In particular, Petitioner maps Chin’s surface metal layer 200 (which includes pad 220) and metal layer 250 to the claimed first and second electrically conductive layers. *Id.* (citing Ex. 1004, 4:48–57, Fig. 2a). Petitioner contends that Chin teaches that these layers are separated by dielectric material 240. *Id.* (citing Ex. 1004, 4:10–11, Fig. 2a).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches this limitation.

[b] “a plurality of rows of contact pads formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board”

Petitioner contends that Chin teaches this limitation. Pet. 23–24. As noted above, Petitioner contends that Chin teaches or suggests use of its invention in a BGA package substrate. *Id.* at 23 (citing Ex. 1004, 1:61–62); *see also supra* § III.E.1[pre] (addressing the preamble of claim 1). Petitioner further contends that a person of ordinary skill in the art “would know that a BGA package is comprised of a plurality of rows (i.e., a grid array) of contact pads.” Pet. 23–24 (emphasis omitted) (citing Ex. 1004, 1:57, 6:40–

41; Ex. 1003 ¶ 90). In support, Petitioner also cites to the '340 patent, which describes a BGA package substrate “of the prior art” that includes pads arranged in transmit and receive rows. *Id.* (citing Ex. 1001, 2:61–66, 3:27–36);¹⁵ *see* Ex. 1001, Figs. 1–2. Moreover, according to Petitioner, a person of ordinary skill in the art would understand Chin to teach contact pads (i.e., pad 220) “for making a direct connection between the integrated circuit package substrate and a printed circuit board,” as required. Pet. 24 (citing Ex. 1003 ¶¶ 91–92; Ex. 1004, 1:16–21, 1:62–65).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches this limitation.

[c] “a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer”

Petitioner contends that Chin teaches this limitation. Pet. 25–26. In particular, Petitioner submits that Chin’s invention reduces “[a] landing pad’s parasitic capacitance . . . by forming patterned holes in one or more reference potential layers below the landing pad.” *Id.* at 25 (quoting Ex. 1004, 3:45–47; citing Ex. 1004, 1:10–11, 6:44–46, Fig. 2a) (first alteration in original); *see also* Ex. 1004, Abstract (*cited by* Pet. 19). To illustrate, Petitioner annotates Chin’s Figure 2a, as shown below:

¹⁵ The pin cites provided by Petitioner do not match the material quoted, which appears a few lines away. We have considered both the cited and quoted material, and we have updated these citations to reflect those lines.

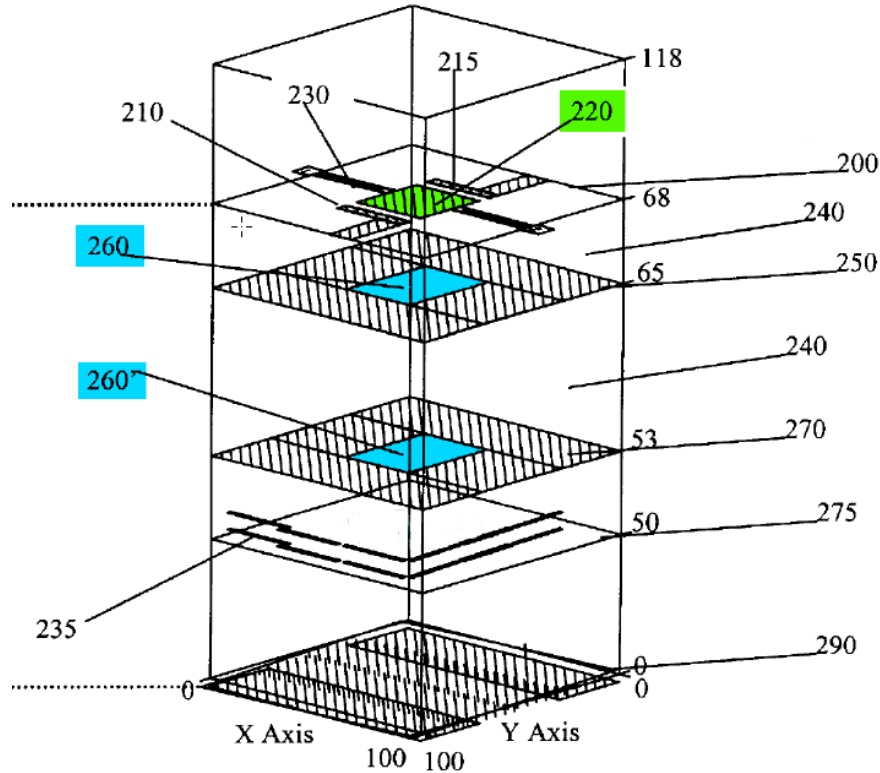


Figure 2a

As depicted above, Petitioner annotates Figure 2a to illustrate the landing pad 220 (in green) and its aligned holes 260, 260' (in blue). Pet. 26.

At this stage, Patent Owner does not dispute Petitioner's arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches this limitation.

[d] “wherein each cutout encloses an electrically insulating area within the second electrically conductive layer”

Petitioner contends that Chin teaches this limitation. Pet. 26–28. Chin states that “[p]atterned hole 260 is formed by any suitable technique that creates a prescribed region devoid of metal.” *Id.* at 26 (quoting Ex. 1004, 4:15–16) (alteration in original). Petitioner contends that an

ordinary artisan would understand this to mean that hole 260 is an electrically insulating area. *Id.* at 26–27 (citing Ex. 1003 ¶ 97). Petitioner also submits that hole 260 is within metal layer 250. *Id.* at 27–28 (citing Ex. 1004, 4:4–15, Fig. 2a).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches this limitation.

[e] “wherein each electrically insulating area completely overlaps a corresponding one of the contact pads formed in the first electrically conductive layer such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.”

Petitioner contends that Chin teaches this limitation. Pet. 28. In particular, Petitioner argues that Chin teaches that each hole completely overlaps a corresponding contact pad and is larger than the pad. *Id.* (citing Ex. 1004, 2:41–42, 3:49–55, 6:35–36, 8:6–7); *see also* Ex. 1004, 3:45–47, 6:17–22, 6:40–50. Referencing the earlier discussion that Chin’s holes are “a prescribed region devoid of metal,” Petitioner asserts that Chin inherently discloses that there is substantially no overlap of the contact pads with metal in the second electrically conductive layer (i.e., layer 250). Pet. 28 (emphasis omitted) (quoting Ex. 1004, 4:15–17; citing Pet. 26–28; Ex. 1003 ¶ 101).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this limitation. *See generally* Prelim. Resp.

On this record, Petitioner has established a reasonable likelihood of showing that Chin teaches this limitation.

Conclusion

Petitioner's assertions and explanations are consistent with and supported by the evidence cited by Petitioner. Moreover, Petitioner sufficiently explains why a person of ordinary skill in the art would have understood Chin to teach or suggest each limitation of claim 1. On the current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it will prevail in showing that the subject matter of claim 1 would have been obvious over Chin.

2. Independent Claim 7

Claim 7 differs from independent claim 1: it requires a routing metal layer comprising a plurality of routing traces. Specifically, claim 7 recites:

7. An integrated circuit package substrate,
comprising:

a first layer comprising a plurality of rows of electrical
contacts;

*a routing metal layer comprising a plurality of routing
traces, the electrical contacts in the first layer being electrically
connected with the respective routing traces;*

a dielectric layer between the first layer and the routing
metal layer with no intermediate conductive layer
therebetween; and

a plurality of *cutouts in the routing metal layer* for
reducing parasitic capacitance between the first layer and the
routing metal layer, the cutouts respectively overlapping the
electrical contacts and having the same or larger dimensions as
the electrical contacts such that there is substantially no overlap

of the rows of contact pads with metal in the routing metal layer.

Ex. 1001, 8:7–21 (emphases added). Notably, the claim specifies that the routing metal layer is separated from the “first layer” (including the electrical contacts) by a dielectric layer “with no intermediate conductive layer therebetween.” *Id.* In this Decision, we refer to this required positioning of the routing metal layer as the “routing placement limitation.”

Relying on the analysis for independent claim 1, Petitioner contends that the subject matter of independent claim 7 would have been obvious over Chin. Pet. 41–46 (citing *id.* at 20–26, 28, 35–41). For the “routing metal layer” of claim 7, Petitioner points to Chin’s metal layer 275 with traces 235. *Id.* at 42 (citing Ex. 1004, 1:22–34; Pet. 35–39). Petitioner argues that Chin renders obvious the claim’s routing placement limitation. *Id.* at 42–44 (citing Ex. 1004, 1:22–34, 4:9–10; Ex. 1003 ¶¶ 124–127; Ex. 1009, 94 (Fig. 5.1)). Specifically, Petitioner states:

Chin teaches: “Metal layer 275 . . . represents *any intermediate routing layer* with traces 235.” In other words, Chin teaches that a routing layer with traces such as 235 could be placed interchangeably with, for example, a second conductive layer such as 250, in Figure 2a

Id. at 35 (quoting Ex. 1004, 4:23–24).

A POSITA would have found it obvious to modify the layer order of Chin Figure 2a to place the routing metal layer below the contact pad layer with only a dielectric layer in between. Specifically, a POSITA would have understood the need to route possibly hundreds of signals between contact pads of the BGA substrate and integrated circuit contacts within the package. A POSITA would also have understood that the ordering of layers in the substrate needed to be flexible to accommodate those many signal lines. The placement of a

routing layer next to the contact pad layer is a design choice that a POSITA was capable of making.

Id. at 43 (citing Ex. 1003 ¶ 126). Finally, Petitioner contends that Chin teaches “cutouts” in layer 275 because Chin states that “[a]ny conductive traces 235 in metal routing layers such as layer 275, should be routed around where patterned hole 260’s projection onto that layer would be.” *Id.* at 44–46 (alteration in original) (quoting Ex. 1004, 5:3–9; citing Ex. 1004, 4:15–20, Fig. 2a; Ex. 1003 ¶¶ 129–132; Pet. 39–41 (also comparing the routing of traces 135 with traces 235 in Figures 1 and 2a of Exhibit 1004)).

Patent Owner argues that Petitioner fails to show that an ordinary artisan would have modified Chin to yield the routing placement limitation of claim 7. Prelim. Resp. 21–26. Patent Owner asserts that Petitioner’s proposed modification of Chin is “textbook hindsight” and faults Petitioner for failing to explain *why* a person of ordinary skill in the art would have made this modification. *Id.* at 21, 25–26. Patent Owner explains that “Petitioner does not explain why placing a signal layer next to the pad layer would have achieved [the proffered] objective” of accommodating many signal lines in a BGA substrate. *Id.* at 25. Patent Owner also argues that Petitioner does not explain why an ordinary artisan would have replaced power plane layer 250 with routing layer 275, where Chin describes layer 250 as “the first metal power plane layer below surface metal layer 200” followed by “intermediate” routing layer 275 and power plane layer 270. *Id.* at 22 (quoting Ex. 1004, 4:12–20). Also, citing the testimony of Mr. Peter Elenius, Patent Owner argues that Petitioner’s proposed swap of power plane layer 250 and routing layer 275 would result in two adjacent signal layers, which is contrary to “Chin’s design rule.” *Id.* at 23–24 (citing Ex. 2002 ¶ 96). In support, Patent Owner points to Chin’s statement that

“reference potential planes [] are typically interspersed between alternating signal layers” and its discussion of microstrips (which require a reference plane adjacent to a signal line). *Id.* at 22–24 (alteration in original) (quoting Ex. 1004, 1:30–32; citing Ex. 1004, 1:24–27, Figs. 1, 2a, 2b, 3c; citing Ex. 2002 ¶¶ 62, 96, 105–106).

On this record, we are persuaded by Patent Owner’s arguments regarding the routing placement limitation. Chin’s layer 200 includes pad 220, which is interconnected with other components by trace 230. Ex. 1004, 4:10–12. According to Chin, “[l]ayer 250 is the first metal power plane layer below surface metal layer 200” *Id.* at 4:12–13. Chin also describes an intermediate metal power plane layer 270 “that is below the top two metal layers” and an intermediate routing layer 275 that “represents any intermediate routing layer with traces 235.” *Id.* at 4:18–24. Even if Chin indicates that intermediate routing layer 275 can be swapped with intermediate power plane layer 270, Chin does not teach (expressly or inherently) that “intermediate” metal layer 275 can be swapped with “first” power plane layer 250. Petitioner does not provide support for its assertion to the contrary. *See* Pet. 35.

Also, on this record, we question Petitioner’s assertion that it would have been obvious to modify Chin to yield this limitation. In its background, Chin explains that reference potential planes (e.g., layers 250, 270, 290) “are typically interspersed between alternating signal layers” (e.g., layer 200, layer 275). Ex. 1004, 1:30–32; *accord id.* at Figs. 1, 2a, 2b (showing signal layers separated by reference potential planes). Similarly, Chin discusses microstrips (*id.* at 1:24–27), and we credit Mr. Elenius’s testimony, which is undisputed on this record, that “there cannot be an

intermediate signal trace metal layer between the transmission line and the reference plane” in a microstrip configuration (Ex. 2002 ¶¶ 62, 105). We disagree with Patent Owner’s assessment that this is a design rule (*see* Prelim. Resp. 22–24), and we preliminarily determine that Chin’s discussion does not preclude Petitioner’s proposed combination. But, these statements in Chin’s background tend to indicate that an ordinary artisan would *not* have replaced power plane layer 250 with routing layer 275.

Further, Petitioner fails to articulate a persuasive explanation for *why* a person of ordinary skill in the art would have modified Chin as proposed. Petitioner refers to “the need to route possibly hundreds of signals”—but, even if this would have motivated an ordinary artisan to *add* routing layers, it does not explain why routing layer 275 would have been moved, as Petitioner suggests. *See* Pet. 43; Ex. 1003 ¶ 126 (repeating the Petition). It also does not explain why the ordinary artisan would have switched the locations of a routing layer and a reference potential plane, particularly where the result is the placement of a routing layer adjacent to a trace.¹⁶ Petitioner simply states that this placement “is a design choice that a [person of ordinary skill in the art] was capable of making.” Pet. 43–44 (citing Ex. 1009, 94; Ex. 1003 ¶¶ 126–127 (repeating the Petition)). But the fact that an ordinary artisan *could* have performed the proposed modification does not show the requisite motivation to do so. *See Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018) (faulting the Board for “focus[ing] on what a skilled artisan would have been *able* to do, rather

¹⁶ In this Decision, we refer to different metal layers as “adjacent” to indicate that there are no metal layers between them; however, adjacent metal layers are separated by a dielectric layer.

than what a skilled artisan would have been *motivated* to do at the time of the invention”); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (“It was [Petitioner’s] burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” (quotations omitted)). Moreover, Petitioner’s use of generalized statements and lack of supporting explanation leaves us to wonder whether Petitioner’s proposal is the result of improper hindsight.

Ultimately, on this record, we question Petitioner’s contention that a person of ordinary skill in the art would have been motivated to modify Chin in the manner proposed; however, we invite the parties to further address this ground at trial.

3. *Independent Claim 12*

Claim 12 is different from independent claim 1 in that it requires a third layer that also includes the claimed cutouts. It recites:

12. An integrated circuit package substrate, comprising:

a first layer comprising a plurality of rows of electrical contacts;

a plurality of electrically conductive layers disposed immediately proximate the first layer;

a plurality of dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other, and

a plurality of rows of *cutouts formed in each of the plurality of the electrically conductive layers*, each of the

cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers.

Ex. 1001, 8:7–21 (emphases added).

Petitioner contends that the subject matter of independent claim 12 would also have been obvious over Chin. Pet. 51–56 (relying on discussion of independent claim 1 and dependent claim 4). For the claimed “first layer,” Petitioner points to Chin’s layer 200 (which includes pad 220), and for the “plurality of electrically conductive layers,” Petitioner points to metal layers 250, 270.¹⁷ *Id.* at 51–53 (citing Ex. 1004, Fig. 2a, 1:22–34, 4:9–11). Petitioner also contends that Chin’s layers 250, 270 each include a hole that encloses an electrically insulating area and overlaps a corresponding pad for reducing parasitic capacitance. *Id.* at 54, 56 (citing Ex. 1004, Fig. 2b, 7:1–7; Pet. 30–32, 33–34 (also citing Ex. 1004, 4:18–20, Fig. 2a)).

At this stage, Patent Owner does not dispute Petitioner’s arguments, analysis, or evidence for this claim. *See generally* Prelim. Resp.

We determine Petitioner’s assertions and explanations regarding independent claim 12 are consistent with and supported by the evidence cited by Petitioner. Moreover, Petitioner sufficiently explains why a person of ordinary skill in the art would have understood Chin to teach or suggest each limitation of this claim. On the current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it will prevail in

¹⁷ Petitioner also identifies Chin’s routing metal layer 275 and ground layer 290. Pet. 51–52, 54–55. We do not consider this aspect of the Petition here because it is incidental to Petitioner’s challenge to this claim.

showing that the subject matter of claim 12 would have been obvious over Chin.

4. Dependent Claim 3

Claim 3 depends from claim 1 and requires that “the cutouts have the same dimensions as the contact pads.” Ex. 1001, 6:62–64.

Petitioner contends that this limitation is obvious in light of Chin. *See* Pet. 29. In particular, Petitioner argues that a person of ordinary skill in the art “would understand the sizing of the cutouts to be a design decision subject to tradeoffs.” *Id.* Petitioner acknowledges that Chin teaches using cutouts that are larger than the contact pads to minimize parasitic capacitance, but argues Chin also teaches that using oversized cutouts reduces capacitance more than desired and requires reintroduction of capacitance to tune the pad impedance. *Id.* (citing Ex. 1004, Abstract). Petitioner also asserts that a person of ordinary skill in the art would understand “that larger cutouts reduce the shielding effects of ground or power metal layers and reduce the available area for routing traces in routing layers,” and, therefore, “would have found it obvious to try sizing the cutouts to have the same dimensions as the contact pads to allow for greater shielding and routing flexibility.” *Id.* (citing Ex. 1003 ¶ 103).

Patent Owner argues that Petitioner’s rationale for modifying Chin is insufficient. Prelim. Resp. 32–33. Patent Owner contends that the rationale provided by Petitioner is deficient because “Chin already proposes a solution to address the issues with Chin’s oversized cutouts.” *Id.* at 32; *see id.* at 29–32 (arguing that Petitioner fails to show that an ordinary artisan would have been motivated to modify Chin to solve the identified problem in a different way). In addition, Patent Owner submits that “Dr. Choi’s testimony adds

nothing to Petitioner’s conclusory arguments, provides no facts or data underlying the conclusory testimony and is entitled to little to no weight.” *Id.* at 33.

On this record, we question whether Petitioner has sufficiently shown that the proposed modification would have been “obvious to try.” Petitioner’s obviousness contention “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (quoting *KSR*, 550 U.S. at 418). Moreover, Petitioner relies on Dr. Choi’s testimony to support its arguments, but the cited paragraph in Dr. Choi’s declaration simply repeats the statements made in the Petition without citing the basis for the testimony. We agree with Patent Owner that unsupported statements are entitled to little or no weight. 37 C.F.R. § 42.65(a).

Ultimately, we question whether a person of ordinary skill in the art would have been motivated to modify Chin in the manner proposed by Petitioner, but we invite the parties to further address this ground at trial.

5. *Dependent Claims 6, 8, and 9*

Like independent claim 7, dependent claims 6, 8, and 9 each include the routing placement limitation.¹⁸ *See* Ex. 1001, 6:36–54 (claim 1 specifies

¹⁸ Patent Owner erroneously contends that dependent claim 4 also includes the routing placement limitation. *See* Prelim. Resp. 21 (“Claims 2 and 4–11 require the second metal layer be a routing layer.”); *but see* Ex. 1001, 6:65–8:6 (claim 4 does not recite a “routing layer,” but claims 5–11 each recite a

first and second conductive layers adjacent to each other), 7:16–20 (claim 6 depends from claim 1 and specifies the second layer is a routing layer), 7:37–50 (claims 8 and 9 depend from claim 7); *see also* Prelim. Resp. 28 (arguing these claims suffer from the same deficiency as claim 7). Consequently, we have the same concerns for these claims as those articulated above for independent claim 7. *See supra* § III.E.2.

6. *Dependent Claims 4 and 13–15*

We find that Petitioner has made an adequate showing, unchallenged by Patent Owner in its Preliminary Response (*see generally* Prelim. Resp.),¹⁹ that Chin teaches or suggests the additional limitations of dependent claims 4 and 13–15. *See* Pet. 29–34, 56–58. Accordingly, we conclude that Petitioner also has demonstrated a reasonable likelihood of prevailing in its challenge to those claims as unpatentable over Chin.

7. *Summary*

For the reasons explained above, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing in showing that the subject matter of claims 1, 4, and 12–15 would have been obvious over Chin. As a

“routing layer”). The inclusion of claim 4 appears to be a typographical error. *See* Prelim. Resp. 28 (not listing claim 4).

¹⁹ Patent Owner states, in passing, that the “challenge to claim 4 in Ground 1 also fails” (Prelim. Resp. 35–36), but this argument is insufficiently explained. The statement is included as part of Patent Owner’s contentions that the Chin-MC92600 combination is deficient. However, Petitioner does not rely on MC92600 for the limitations additionally recited by claim 4 (*see* Pet. 66, 86), and Patent Owner does not address Petitioner’s contentions that those additionally recited limitations are taught or suggested by Chin (*see* Prelim. Resp. 35–36; Pet. 32–34).

result, we institute *inter partes* review of all claims and all challenges raised in the petition.²⁰

Nevertheless, in order to further guide the parties after institution, we provide additional observations regarding the parties' arguments for the other grounds and challenged claims.

F. Obviousness Grounds Based on Chin Combined with Other References

Petitioner contends that independent claim 7 would have been obvious over Chin and HighSpeed. Pet. 78–80. Petitioner contends that dependent claims 2–6, 8–11, and 16–19 would have been obvious over Chin combined with HighSpeed, MC92600, Oggioni, Hsu, Barr, and/or Shafer. *Id.* at 58–79, 81–88; *see also id.* at 2 (listing grounds).

In addition to the arguments addressed above, Patent Owner alleges deficiencies in Petitioner's combination of Chin with HighSpeed, Oggioni, MC92600, and/or Shafer. Prelim. Resp. 26–41.

We address each of the issues raised by Patent Owner along with Petitioner's associated contentions. For each, we provide our initial observations and analysis to provide guidance to the parties for the upcoming trial. Because we do not need to resolve these issues for purposes of this Decision, and because the panel would benefit from additional arguments and evidence on these topics, we invite and encourage the parties to further address these issues during the course of the trial.

²⁰ *Guidance on the Impact of SAS on AIA Trial Proceedings*” (Apr. 26, 2018), <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>; *see also SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

1. Routing Layer Placement (Chin and HighSpeed)

As noted above, Petitioner contends that independent claim 7 would have been obvious over Chin and HighSpeed. Pet. 78–80. Petitioner relies on its allegations that Chin teaches or suggests each element of the claim (*id.* at 79 (citing *id.* at 41–46)), and Petitioner further contends that the combination of Chin and HighSpeed renders obvious the routing placement limitation (*id.* at 79–80).

As to the latter point, Petitioner contends that “HighSpeed illustrates and describes a commonly used prior art arrangement of metal layers with a routing trace on layer 2 adjacent the contact layer 1, which is coupled to an integrated circuit (‘receiver chip’).” Pet. 79–80. In support, Petitioner shows Figure 5.1 of HighSpeed, which is reproduced below:

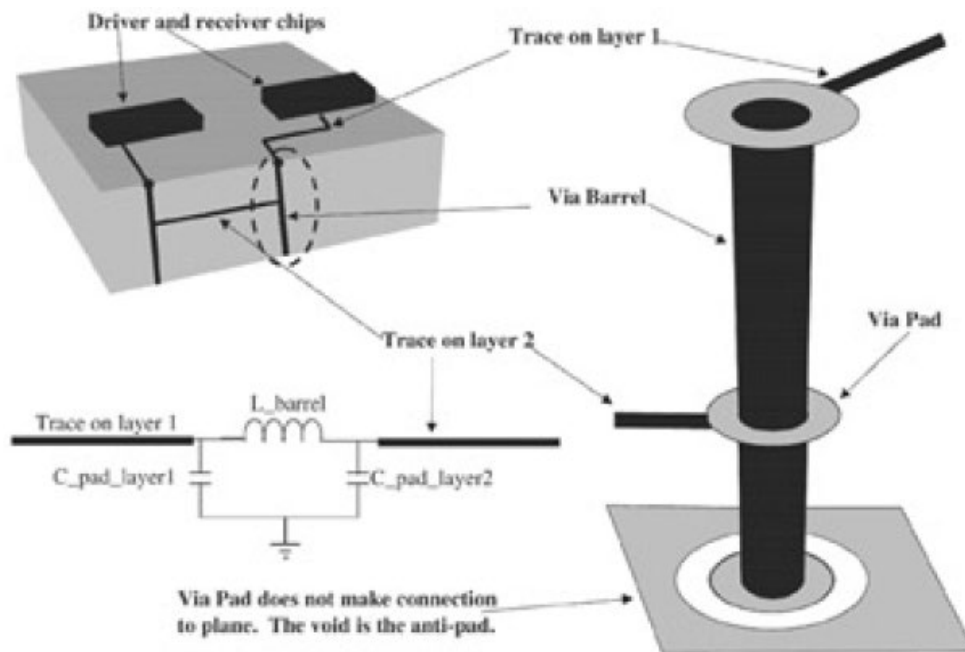


Figure 5.1: Equivalent circuit of a through-hole via.

Pet. 80 (reproducing Ex. 1009, Fig. 5.1). As shown above, Figure 5.1 illustrates a through-hole via connected to a trace on layer 1 and a trace on layer 2 along with its equivalent circuit. Ex. 1009, 94.

Petitioner asserts that a person of ordinary skill in the art would have been motivated to arrange Chin’s layers “as shown/described in HighSpeed because this is one of a finite number of possibilities and within the skill of a [person of ordinary skill in the art] to try.” Pet. 80 (citing Ex. 1003 ¶ 232); *see id.* at 65 (stating that an ordinary artisan “would be choosing from a finite number of identified, predictable solutions (ordering a finite number of metal layers within a substrate) with reasonable expectation of success”). According to Petitioner, Chin and HighSpeed are both from the same field of endeavor, and an ordinary artisan “would have looked to HighSpeed, a combinable reference describing useful structures and approaches, or would have known and understood the prior art principles detailed therein.” *Id.* at 58–60 (*cited by id.* at 78–79) (citing Ex. 1003 ¶¶ 72, 164–165, 168).

Patent Owner argues that “Petitioner’s explanation for why a [person of ordinary skill in the art] would have combined Chin and HighSpeed is legally insufficient.” Prelim. Resp. 26–29; *see also id.* at 21–26 (arguing lack of motivation to modify Chin). In particular, Patent Owner disputes Petitioner’s assertion that the references come from the same field of endeavor (*id.* at 26–27) and argues that the alleged similarity does not provide the requisite motivation to combine (*id.* at 27). Further, according to Patent Owner, Petitioner does not provide enough support to demonstrate that the modification would be obvious to try. *Id.* at 27–28 (citing Ex. 1004, 1:30–32, 3:67–4:3).

We have concerns about Petitioner’s showing regarding the routing placement limitation. Specifically, even if we were to find that HighSpeed teaches this limitation, Petitioner does not sufficiently explain *why* a person of ordinary skill in the art would have been motivated to combine Chin and

HighSpeed in the manner proposed. Petitioner asserts, without supporting explanation, that this configuration “is one of a finite number of possibilities and within the skill of a[n ordinary artisan] to try.” Pet. 80 (citing Ex. 1003 ¶ 232); *see also* Ex. 1003 ¶ 232 (repeating the Petition). Similarly, Petitioner asserts that there are a “finite number of identified, predictable solutions” because there are a finite number of metal layers within a substrate. Pet. 65. These statements contend that a person of ordinary skill in the art *could* have made the proposed combination, but do not explain sufficiently why such a person would have been *motivated* to do so. *Cf.* *KSR*, 550 U.S. at 421 (“*When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.*” (emphasis added)).

Our analysis and preliminary determinations are informed by Chin’s background, which tends to indicate that an ordinary artisan would *not* reorder the layers to swap the first power plane layer with an intermediate routing layer. *See supra* § III.E.2 (addressing Petitioner’s contention that Chin teaches or suggests the routing placement limitation). While the cited HighSpeed figure does not show a reference potential layer between the traces on layers 1 and 2, it also does not directly address the relative placement of trace layers and reference potential layers. *See* Ex. 1009, 94. Moreover, HighSpeed’s figure depicts a “*through-hole via . . . made by drilling a hole through the board.*” *Id.* (also noting that other types of vias exist). It is unclear whether a person of ordinary skill in the art would have used a through-hole via (as shown in HighSpeed) to connect a BGA package substrate’s electrical contacts and routing metal layer (as Petitioner appears

to contend). At this stage, weighing Petitioner's cursory statements against Chin's background and HighSpeed's statements (and lack thereof), we cannot say that we are persuaded it would have been obvious to modify Chin's layer order in view of HighSpeed.

Furthermore, dependent claims 2, 5, 6, and 8–11 each include the routing placement limitation. *See* Ex. 1001, 6:36–54 (claim 1 specifies first and second conductive layers adjacent to each other), 7:16–20 (claim 2 depends from claim 1 and specifies the second layer is a routing layer), 7:10–20 (same for dependent claims 5 and 6), 7:37–8:6 (claims 8–11 each depend from claim 7); *see also* Pet. 13 (noting claims 2, 5, and 6 require the second layer to be a routing layer); Prelim. Resp. 28 (arguing claims 2, 5, 6, 8, and 10 suffer from the same deficiency as claim 7), 35 (arguing combination with other references does not cure these deficiencies). Petitioner's showing for these claims presents substantially the same issue. *See* Pet. 65–67, 79, 84–86 (claims 2, 5, and 6).

In sum, our concerns regarding the routing placement limitation apply to independent claim 7 and dependent claims 2, 5, 6, and 8–11.

2. Size of Cutouts (Chin and Oggioni)

Petitioner contends that Oggioni, like Chin, is directed to “mitigating issues with high-speed signals interfacing an integrated circuit package by reducing package pad parasitic capacitance.” Pet. 68 (citing Ex. 1006, 1:57–2:3, 6:21–27). Petitioner further contends that Oggioni discloses using cutouts in a conducting layer that are the same size as the contact pad. *Id.* at 70–71 (citing Ex. 1006, 5:2–3, Fig. 2a).

Petitioner contends a person of ordinary skill in the art would have had reason to combine Chin and Oggioni because they are from the same

field of endeavor, describe nearly identical solutions, and a person of ordinary skill in the art would have looked to Oggioni “for other techniques to optimize reduction in pad parasitic capacitance.” Pet. 68. As an example, Petitioner asserts that Oggioni teaches a configuration (using cutouts in a conducting layer that are the same size as the contact pad) that addresses a problem discussed in Chin (impedance discontinuity) derived from the use of cutouts larger than the pads. *Id.* at 68–69 (citing Ex. 1004, 2:16–19; Ex. 1003 ¶ 196). Petitioner also argues:

Combining Chin and Oggioni would have been (a) a combination of prior art elements according to known methods to yield predictable results, since a [person of ordinary skill in the art] would have known how to make cutouts the same size as the pads; (b) a simple substitution of one known element (Oggioni’s cutouts the same size as the pads) for another (Chin’s cutouts larger than the pads) to obtain predictable results; (c) a predictable use of prior art elements according to their established functions (Oggioni and Chin’s cutouts in conducting layers under package contact pads to reduce parasitic capacitance); (d) applying a known technique (forming cutouts in conducting layers under package contact pads to reduce parasitic capacitance) to a known device (method or product) ready for improvement to yield predictable results; [and] (e) choosing from a finite number of identified, predictable solutions (cutouts in conducting layers under pads of the same, or different size), with a reasonable expectation of success.

Id. at 69 (citing Ex. 1003 ¶ 197).

Patent Owner acknowledges Chin’s disclosure that oversized holes potentially introduce an impedance discontinuity, but argues that Chin offers a solution to the stated problem that “ensures impedance continuity between the pad and trace.” Prelim. Resp. 30 (quoting Ex. 1004, 4:39–45). Patent Owner argues that Petitioner fails to explain why a person of ordinary skill

in the art would have looked to Oggioni to solve a problem Chin had already solved. *Id.* at 30–31. According to Patent Owner, even if a person of ordinary skill in the art could have made the proposed modification, for example according to known methods or as a simple substitution of one known element for another, “that does not mean that they **would have been** motivated to do it when there is no ‘design incentive’ or ‘market pressure’ to do so.” *Id.* at 32 (quoting *KSR*, 550 U.S. at 417, 421).

Patent Owner’s argument that a person of ordinary skill in the art would not have turned to Oggioni’s configuration to solve the impedance discontinuity issue in Chin because Chin already proposes a solution is reasonable. Moreover, Petitioner’s arguments regarding combining prior art elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, the predictable use of prior art elements according to their established functions, applying a known technique to a known device, and choosing from a finite number of identified, predictable solutions are supported only by a citation to a paragraph in Dr. Choi’s declaration that merely repeats the language in the Petition itself. Ex. 1003 ¶ 197.

3. Combination of Chin and MC92600

a. Motivation to Combine

Petitioner contends that it would have been obvious to combine Chin and MC92600. *See* Pet. 58–63 (articulating proposed combination for claim 2 in Chin-MC92600-HighSpeed ground); *see also id.* at 66–67, 72–73 (referencing discussion of claim 2).

According to Petitioner, MC92600 describes rows of transmit and receive ball pads coupled to SERDES functionality to convert parallel data

to serial data in a BGA package. Pet. 61 (citing Ex. 1008, 21, 70; Ex. 1003 ¶ 171). Petitioner also contends that Patent Owner’s infringement contentions “assert[] that the presence of SERDES functionality satisfies [the claim] limitation” requiring ball pads operable with the second layer “for converting a serial data stream to or from a parallel data stream.” *Id.* at 62–63 (citing Ex. 1010, 18).

Further, Petitioner contends that a person of ordinary skill in the art would have been motivated to combine these features of MC92600 with Chin’s BGA package because: (1) it is “a combination of prior art elements according to known methods . . . , as taught by MC92600 . . . to yield predictable results of organizing transmit and receive pins in an industry accepted arrangement” and (2) it applies “a known technique (organizing rows of transmit and receive pads as in MC92600) to a known design (such as Chin’s multi-layer BGA package) ready for improvement to yield predictable results, with a reasonable expectation of success.” Pet. 61–62 (citing Ex. 1003 ¶ 172). Petitioner also argues that an ordinary artisan would have consulted MC92600 when designing an IC package because it provides implementation details for an existing design. *Id.* at 60 (citing Ex. 1003 ¶¶ 72, 164, 168).

Patent Owner argues that “Petitioner has not presented any competent evidence that a POSITA would have combined Chin with MC92600.” Prelim. Resp. 33. Patent Owner contends that “nothing in the analysis explains *why* a POSITA would have used Chin’s PCB design for a SERDES package substrate design.” *Id.* at 33–34 (citing Pet. 60–62). Patent Owner also faults “Petitioner’s laundry list of alleged reasons to combine” as “too

generic,” arguing that the failure to include “specific reasoning . . . evinces hindsight.” *Id.* at 34.

On this record, we have some concerns regarding Petitioner’s articulated motivation to combine Chin and MC92600. Chin describes a technique for reducing parasitic capacitance and improving impedance matching on a substrate. *See* Ex. 1004, Abstract. MC92600 is a SERDES transceiver “that can be used to transmit or receive data between chips.” Ex. 1008, 17. At this stage, we understand Petitioner to propose a combination of Chin’s technique (applied to a BGA package substrate) with MC92600’s ball pads (arranged in transmit and receive rows) and IC (with SERDES functionality). *See* Pet. 61–63. But, when explaining *why* an ordinary artisan would have combined these references in this manner, Petitioner focuses its analysis on the combination of Chin’s technique with MC92600’s transmit and receive ball pads. *See id.* at 61–62. To that end, Petitioner provides the cursory assertions that the elements are in the prior art, the methods are known, the results are predictable, and there would have been a reasonable expectation of success. *See id.* (citing Ex. 1003 ¶ 172 (repeating the Petition)). This may be sufficient to show a motivation to arrange the ball pads in Chin’s BGA package substrate in transmit and receive rows, given evidence in the record regarding an ordinary artisan’s understanding of BGA packages. *See, e.g.,* Ex. 1001, 2:61–67, 3:27–30, Fig. 2 (prior art BGA package includes ball pads in transmit and receive rows). But we question whether Petitioner’s explanation is sufficient for its proposed combination that also includes MC92600’s SERDES functionality. Patent Owner argues that, “if, as Petitioner asserts, a [person of ordinary skill in the art] would have looked to MC92600 as a reference design for

SERDES packages, Petitioner does not explain why a [person of ordinary skill in the art] would not have started with MC92600's known package substrate with all its known routing." Prelim. Resp. 34. We consider this argument to have some merit.

b. Dependent Claim 16

Claim 16 depends from independent claim 12. It requires (1) "a first layer comprising a plurality of rows of electrical contacts" that "comprise transmit rows and receive rows" and (2) "a plurality of electrically conductive layers disposed immediately proximate the first layer," where (3) "the electrically conductive layers are operable to convert a serial data stream to or from a parallel data stream." Ex. 1001, 8:8–11, 8:35–39.

The Petition contends that the subject matter of claim 16 would have been obvious over the Chin-MC92600 combination. Pet. 72. To that end, Petitioner points to the analysis of claims 2 and 12 and contends that "[i]t would have been obvious to route a serial data stream to or from a SERDES IC operable to convert that data stream to or from a parallel data stream that is also routed to electrical contacts." *Id.* (citing *id.* at 51–56 (allegations for claim 12), 60–63 (allegations for claim 2)). For independent claim 12, Petitioner maps Chin's layer 200 (which includes pad 220) to the claimed "first layer" and Chin's metal layers 250, 270, 275, 290 to the "plurality of electrically conductive layers." *See id.* at 51–53. Notably, metal layer 275 is a routing layer with traces. Ex. 1004, 4:23–25.

According to Patent Owner, "[i]n Chin, the electrically conductive layers immediately proximate the first layer are two reference planes," and "Petitioner does not explain how the two reference planes 'are operable to

convert a serial data stream to or from a parallel data stream” as would be required by claim 16. Prelim. Resp. 36 (citing Pet. 72).

On this record, this argument does not reveal any additional deficiencies in the Petition. Although we agree with Patent Owner that additional explanation would be required to show that a *reference plane* “convert[s] a serial data stream to or from a parallel data stream,” as claimed, the Petition does not appear to include such a contention. Rather, the Petition points to layer 275—a *routing layer*—as one of the claimed “electrically conductive layers.” See Ex. 1004, 4:23–25. To the extent Patent Owner contends that this routing layer would need to be adjacent to the claimed “first layer” in order to satisfy claim 16, this argument is insufficiently explained. See Prelim. Resp. 36 (arguing that the Petition has not shown that “the second layer [is] a routing layer,” without explaining whether or how this relates to claim 16).

4. *Combination of Chin and Shafer*

Petitioner contends that a person of ordinary skill in the art “designing an IC package capable of handling high speed communications (as taught by Chin) would have looked at existing solutions for interconnecting that IC package with other circuits like the solution described in Shafer.” Pet. 81–82. According to Petitioner, a person of ordinary skill in the art “might, for example, recognize the value of using SERDES to reduce the number of external communication signal lines and of using the connector arrangement of Shafer [with separate rows of transmit and receive signal contacts] to reduce crosstalk between those signal lines.” *Id.* at 82 (citing Ex. 1026, 2:52–65; Ex. 1003 ¶ 237), 83–84 (citing Ex. 1026, 4:61–6:26, Ex. 1003 ¶ 241). Petitioner also argues that a person of ordinary skill in the art would

have been motivated to modify Chin in view of Shafer because “doing so is a combination of prior art elements according to known methods (transmit and receive rows of ball pads taught by Shafer), in Chin’s BGA package to yield predictable results of organizing transmit and receive pads to reduce crosstalk.” *Id.* at 84 (citing Ex. 1003 ¶ 242). Petitioner also argues the proposed modification involves applying Shafer’s known technique of organizing rows of transmit and receive connectors to Chin’s known design that was ready for improvement to yield predictable results, with a reasonable expectation of success. *Id.* Petitioner also submits that Shafer discloses that its contacts may be “connected to a BGA package such as a Xilinx Virtex II Pro FPGA.” *Id.* (citing Ex. 1026, 1:25–40).

Patent Owner asserts that the same deficiencies noted regarding the combination of MC92600 and Chin apply to the combination of Shafer and Chin. Prelim. Resp. 37. Patent Owner contends that Petitioner fails to show *why* an ordinary artisan would have combined a SERDES device and Chin’s design. *Id.* at 37–38. Patent Owner further contends that “the Petition fails to clearly articulate a rational basis, supported by evidence (and not conclusory assertions), as to why a [person of ordinary skill in the art] would have combined” Shafer and Chin. *Id.* at 40–41.

Patent Owner also argues:

[T]here is no analysis whatsoever whether Chin’s design of having a microstrip layer followed by multiple reference planes would be compatible with a SERDES design. For example, both Hall’s prior art and inventive embodiments involve SERDES packages with the second electrically conductive layer (the layer immediately adjacent the pad layer) being the routing layer. As already explained in Section A above, Petitioner has not demonstrated that a POSITA would have modified Chin by placing a routing layer next to the pad layer.

But if that is a common configuration for a SERDES device, the Petition begs the question why a POSITA would have even looked to Chin for a SERDES package.

Prelim. Resp. 38 (citing Pet. 82; Ex. 1001, 2:63–67, 4:13–18, Figs. 1, 5).

Finally, Patent Owner contends that “the deficiencies in the combinability of Chin and HighSpeed (for why the routing layer is the second electrically conductive layer adjacent the first (pad) layer) and the deficiencies in the combinability of Chin and Oggioni (for cutout size) cannot be cured by arguments regarding combinability of Chin and Shaffer.” *Id.* at 39.

To the extent the parties’ arguments regarding the combination of Shafer and Chin are the same as those made for the combination of MC92600 and Chin, we reiterate our comments above.

At this stage, we do not agree with Patent Owner’s arguments relying on the location of the routing layer. *See* Prelim. Resp. 38. Any deficiencies regarding the routing placement limitation do not appear to be relevant to claims that do not include that limitation. Further, we do not agree that a “common configuration for a SERDES device” is to have a routing layer adjacent to the pad layer because, at this stage, we perceive no evidence to support such a finding.²¹ Finally, even if this were a common design, we do not agree that the Petition necessarily should have addressed the compatibility between that design and Chin’s disclosure. For example, Patent Owner does not contend that all SERDES designs *require* a routing layer adjacent to the pad layer.

²¹ The configurations shown in the ’340 patent do not support this contention—the fact that a SERDES design *can* have that configuration does not mean that the configuration is *common* in SERDES designs. *See* Ex. 1001, 2:63–67, 4:13–18, Figs. 1, 5.

We do, however, agree with Patent Owner’s assessment that Petitioner does not rely on Shaffer for either the routing placement limitation or the size of the cutouts and, thus, that Petitioner’s contentions regarding Shaffer do not address our concerns regarding the routing placement limitation (*see supra* § III.F.2) and size of the cutouts (*see supra* § III.F.2). *See* Prelim. Resp. 39.

IV. DISMISSING RENEWED MOTION FOR JOINDER

As noted above, Petitioner filed a Renewed Motion for Joinder seeking to join IPR2021-00148 (“the 148 IPR”). Paper 9.

We dismiss Petitioner’s motion for joinder as moot because the 148 IPR was terminated on October 7, 2021. IPR2021-00148, Paper 25. Section 315(c) provides that “[i]f the Director institutes an inter partes review, the Director, in his or her discretion, may join as a party to that inter partes review any person who properly files a petition . . . that the Director . . . determines warrants the institution of an inter partes review under section 314.” 35 U.S.C. § 315(c). Thus, there necessarily must be an instituted proceeding to join for a motion for joinder to be granted.

V. CONCLUSION

As explained above, we determine that Petitioner has established a reasonable likelihood of prevailing in its challenge to at least one claim of the ’340 patent. Accordingly, we institute an *inter partes* review of all challenged claims on all asserted grounds.

This Decision is not a final determination on either the patentability of any challenged claims or the construction of any claim term. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016)

("[T]here is a significant difference between a petitioner's burden to establish a reasonable likelihood of success at institution, and actually proving invalidity by a preponderance of the evidence at trial." (quotations omitted)).

VI. ORDER

It is:

ORDERED that an *inter partes* review is instituted on all of the challenged claims, i.e., claims 1–19 of the '340 patent, on all corresponding grounds of unpatentability as specified in the Petition and identified in the Table in Section I.B. of this Decision;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '340 patent shall commence on the entry date of this Decision, and notice is hereby given of the institution of a trial; and

FURTHER ORDERED that Petitioner's Renewed Motion for Joinder (Paper 9) is *dismissed* as moot.

IPR2021-00966
Patent 8,049,340 B2

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