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Paper 34
Date: October 6, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP B.V., NXP USA, INC., and
NXP SEMICONDUCTORS N.V.,
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2021-00966
Patent 8,049,340 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM
JULIET MITCHELL DIRBA, *Administrative Patent Judges*.

DIRBA, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318

On October 8, 2021, we instituted an *inter partes* review of claims 1–19 of U.S. Patent No. 8,049,340 B2 (Ex. 1001, "the '340 patent"). Paper 14 ("Inst. Dec."). Having considered the full record at trial, and for the reasons explained below, we determine that Petitioner has shown that claims 1, 4, and 12–17 of the '340 patent are unpatentable, but Petitioner has not shown that claims 2, 3, 5–11, 18, and 19 of the '340 patent are unpatentable.

I. BACKGROUND

A. History of this Proceeding

On May 17, 2021, NXP B.V., NXP USA, Inc., and NXP Semiconductors N.V. (collectively, "Petitioner") filed a Petition requesting *inter partes* review of claims 1–19 of the '340 patent. Paper 1 ("Pet."). Bell Semiconductor, LLC[1] ("Patent Owner") filed a Preliminary Response. Paper 13 ("Prelim. Resp."). Petitioner submitted a declaration from David Choi, Ph.D., in support of its Petition (*see* Ex. 1003), and Patent Owner submitted a declaration from Peter Elenius to support its Preliminary Response (*see* Ex. 2002). After reviewing the preliminary record, we determined that Petitioner had demonstrated a reasonable likelihood that it would prevail in establishing the unpatentability of at least one challenged claim, and we instituted an *inter partes* review of all challenged claims on all grounds asserted in the Petition. Inst. Dec. 58–59.

During trial, Patent Owner filed a Response (Paper 19, "PO Resp."), and a supporting declaration from Charles E. Bauer, Ph.D. (*see* Ex. 2030). In addition, Petitioner filed a Reply (Paper 23, "Pet. Reply"), and Patent

[1] Patent Owner states that it "is a wholly owned subsidiary of Hilco Patent Acquisition 56, LLC." Paper 6, 2.

Owner filed a Sur-reply (Paper 25, "PO Sur-reply"). Moreover, Patent Owner deposed Dr. Choi and filed the corresponding transcript (*see* Exs. 2031, 2032), and Petitioner deposed Dr. Bauer and filed the corresponding transcript (*see* Ex. 1110).

A combined oral hearing for this proceeding and a related proceeding (IPR2021-00967) was held on July 13, 2022, and a transcript of the hearing is included in the record. Paper 33 ("Tr."). Patent Owner objects to several slides in Petitioner's hearing demonstratives (Paper 30), and Petitioner objects to one slide in Patent Owner's demonstratives (Paper 31).

B. Related Matters

The parties indicate that the '340 patent has been asserted in several district court lawsuits, including *Bell Semiconductor, LLC v. NXP Semiconductors N.V.*, 1:20-cv-00611 (W.D. Tex.). Pet. 91–92; Paper 6 (Patent Owner's Mandatory Notice), 2.

The parties also identify two other *inter partes* review proceedings that challenged the '340 patent: IPR2020-01692 and IPR2021-00148. Pet. 92; Paper 6, 2. Both of these proceedings were terminated due to settlement. *Texas Instruments Inc. v. Bell Semiconductor, LLC*, IPR2020-01692, Paper 15 (PTAB April 6, 2021); *Microchip Tech. Inc. v. Bell Semiconductor, LLC*, IPR2021-00148, Paper 25 (PTAB October 7, 2021). Prior to settlement, the Board entered an institution decision in IPR2021-00148 ("148 IPR"). *Microchip Tech.*, IPR2021-00148, Paper 19 ("148 DI"). In this Final Written Decision, we reference one portion of the 148 DI that includes relevant analysis. Notably, the 148 DI was entered before we instituted trial in this proceeding, the petition in the 148 IPR was identical to this Petition in all relevant respects, and the 148 DI addressed some

arguments advanced by Patent Owner in this proceeding. *Compare* Pet., PO Resp., *with Microchip Tech*, IPR2021-00148, Papers 2, 11; *see also* Paper 9 (Petitioner's motion for joinder).

In addition, Petitioner identifies IPR2021-00967, which is an *inter partes* review proceeding filed by Petitioner that challenges U.S. Patent No. 8,288,269 B2, a divisional of the '340 patent. Pet. 92. Concurrently with this Decision, we also enter a final written decision in that proceeding.

C. The Grounds

We instituted trial on the following grounds of unpatentability:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 3, 4, 6–9, 12–15	103(a)[2]	Chin[3]
2	2, 4, 5, 10	103(a)	Chin, MC92600,[4] HighSpeed[5]
3	3, 11	103(a)	Chin, Oggioni[6]
4	16, 17	103(a)	Chin, MC92600
5	18	103(a)	Chin, MC92600, Oggioni

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the challenged patent was filed before March 16, 2013, we refer to the pre-AIA version of § 103.

[3] US 6,765,298 B2, issued July 20, 2004 (Ex. 1004).

[4] Motorola, MC92600 Quad 1.25 Gbaud SERDES User's Manual, Rev. 2 (Feb. 2003) (Ex. 1008).

[5] Stephen H. Hall et al., *High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices* (2000) (Ex. 1009).

[6] US 6,717,255 B2, issued Apr. 6, 2004 (Ex. 1006).

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
6	19	103(a)	Chin, MC92600, Oggioni, Hsu,[7] Barr[8]
7	6–9	103(a)	Chin, HighSpeed
8	2, 4, 5, 10	103(a)	Chin, Shafer,[9] HighSpeed
9	16, 17	103(a)	Chin, Shafer
10	18	103(a)	Chin, Shafer, Oggioni

D. Summary of the '340 Patent

The '340 patent is titled "Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package." Ex. 1001, code (54). It issued from an application filed on March 22, 2006. *Id.* at code (22).

The '340 patent is "directed to the design of an integrated circuit package that minimizes parasitic capacitance between metal layers in a ball grid array integrated circuit package." Ex. 1001, 1:8–13. The '340 patent explains:

> In integrated circuits such as serializer/deserializer (SERDES) devices that convert a serial data stream to or from a parallel data stream, high data transfer rates may require fast switching speeds that surpass 1 GHz. At such high frequencies, the parasitic capacitance between transmit (Tx) and receive (Rx) contact pads in the contact pad layer and nearby metal layers of the integrated circuit package may result in a deterioration of the signal waveform and a correspondingly reduced circuit performance.

[7] US 2005/0037601 A1, published Feb. 17, 2005 (Ex. 1007).

[8] US 2005/0011676 A1, published Jan. 20, 2005 (Ex. 1011).

[9] US 6,908,340 B1, filed Sept. 11, 2003, issued June 21, 2005 (Ex. 1026).

Id. at 2:52–60. The '340 patent teaches avoiding the parasitic capacitance between the contact pads and other nearby metal layers by forming "cutouts" in the metal layers to "enclose an area that surrounds each of the contact pads." *Id.* at 3:58–63.

The '340 patent illustrates one embodiment in Figure 5, reproduced below.

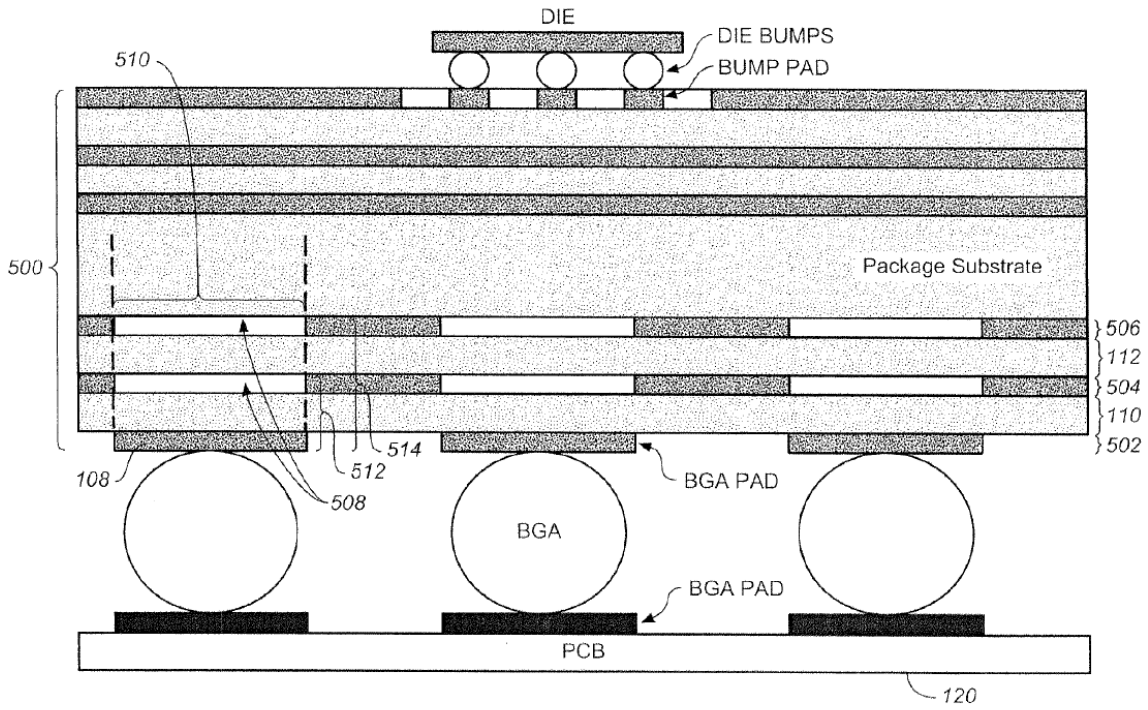


FIG. 5

As shown above, Figure 5 shows a partial side view of integrated circuit package substrate 500, which includes ball pad 108, dielectric layers 110 and 112, vias[10] (not shown), printed circuit board 120, contact pad metal layer 502, routing metal layer 504, and ground return metal layer 506.

[10] According to the '340 patent, "[c]onnections between the electrically conductive layers, typically metal layers, are made by forming vias in the electrically insulating layers, typically dielectric layers, and depositing an electrically conductive material in the vias, such as copper." Ex. 1001, 1:18–22.

Ex. 1001, 4:9–18. Figure 5 also shows cutouts 508 in routing metal layer 504 and ground return metal layer 506 above ball pad 108. *Id.* at 4:19–23. According to the '340 patent, cutout 508 encloses cutout area 510 "so that the area enclosed by the ball pad 108 is completely surrounded by the cutout area 510," which means that "there is no overlap between the area enclosed by the ball pad 108 and the metal in the routing metal layer 504 and in the ground return metal layer 506 above the ball pad 108." *Id.* at 4:31–36; *see id.* at 4:51–54 (explaining that the dashed lines in Fig. 5 extending upward from the sides of contact pad 108 demonstrate how contact pad 108 encloses the areas of routing metal layer 504 and ground return metal layer that are overlapped by ball pad 108).

The '340 patent explains that parasitic capacitances 512 and 514 in Figure 5 are reduced by cutouts 508, and that "[t]he reduction in parasitic capacitance advantageously extends the upper frequency limit that may be used to drive the ball pad 108 in the integrated circuit package substrate." Ex. 1001, 4:59–65 (referring to capacitances 114 and 116 in the prior art integrated circuit shown in Figure 1).

E. Challenged Claims

Petitioner challenges all claims of the '340 patent. Claims 1, 7, and 12 are independent, and independent claim 1 is illustrative:

> 1. An integrated circuit package substrate comprising:
>
> [a] a first and a second electrically conductive layer separated from each other by an electrically insulating layer with no intermediate conductive layer therebetween;
>
> [b] a plurality of rows of contact pads formed in the first electrically conductive layer for making a direct connection

> between the integrated circuit package substrate and a printed circuit board; and
>
> [c] a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer,
>
> [d] wherein each cutout encloses an electrically insulating area within the second electrically conductive layer, and
>
> [e] wherein each electrically insulating area completely overlaps a corresponding one of the contact pads formed in the first electrically conductive layer such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

Ex. 1001, 6:36–54 (line breaks and reference designations added). Independent claims 7 and 12 are also apparatus claims with similar scope; however, claim 7 recites a "routing metal layer" rather than a "second electrically conductive layer," and claim 12 recites three layers rather than two. *Id.* at 7:21–36, 8:7–21.

II. ANALYSIS

A. Legal Standards

In an *inter partes* review, the petitioner has the burden of proving unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e). That burden never shifts to the patentee. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The legal question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of obviousness or nonobviousness.[11] *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966). One seeking to establish obviousness based on more than one reference also must articulate sufficient reasoning with rational underpinnings to combine teachings. *See KSR*, 550 U.S. at 418.

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). "This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, 550 U.S. at 418–419.

On the other hand, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, a petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d

[11] The record does not include allegations or evidence of objective indicia of obviousness or nonobviousness.

1364, 1380 (Fed. Cir. 2016). Instead, a petitioner must articulate a reason why a person of ordinary skill in the art would have combined or modified the prior art references. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) ("In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination."); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.") (citing *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. The Level of Ordinary Skill in the Art

Our reviewing court has explained that "the level of skill in the art is a prism or lens through which a judge, jury, or the Board views the prior art and the claimed invention." *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (citing *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999)). "This reference point prevents these factfinders from using their own insight or, worse yet, hindsight, to gauge obviousness." *Id.*

Petitioner asserts that the level of ordinary skill in the art corresponds to a bachelor's degree in electrical engineering or a related field and four

years of experience in "high-frequency circuit engineering and development," or an equivalent combination of education and practical experience. Pet. 3 (citing Ex. 1003 ¶ 26). For purposes of the Institution Decision, we adopted Petitioner's proposal (Inst. Dec. 16–17), and neither party addresses the level of ordinary skill in the post-institution briefs (*see* PO Resp.; Pet. Reply).

In this Decision, we again adopt the level of ordinary skill proposed by Petitioner. This level of skill is consistent with the Specification of the '340 patent and the asserted prior art, and it is supported by the testimony of Dr. Choi. *Accord* Inst. Dec. 16–17.

C. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b). Under the principles set forth by our reviewing court, the "words of a claim 'are generally given their ordinary and customary meaning,'" as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Below, we address two claim construction disputes. Based on the record before us, we do not find it necessary to provide any other express claim constructions. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that "we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

1. Is the Preamble a Limitation?

Patent Owner argues that the preamble of claim 1 is limiting. PO Resp. 10–12; PO Sur-reply 1–2. Petitioner disagrees. Pet. Reply 6. But, because we find that Petitioner has shown that Chin satisfies the recitations in the preamble (*infra* § II.E.1[pre]), we need not resolve this dispute. *See Nidec*, 868 F.3d at 1017.

However, if we needed to substantively address this dispute, we would conclude that the preamble of claim 1 is limiting, and the preamble of claims 7 and 12 are not limiting, for the reasons previously explained. *See* Inst. Dec. 18–20. We disagree with Petitioner's contention that "the preamble merely states an intended use and does not impact additional structure" (Pet. Reply 6) because the preamble of claim 1 recites "[a]n integrated circuit package substrate"—i.e., a structure. Petitioner misses the mark by relying on language in the *body* of the claim to allege that the *preamble* recites an intended use. *See id.* Moreover, Patent Owner provides no basis for concluding that the preambles of claims 7 and 12 are limiting. *See* PO Resp. 10–11 (addressing only claim 1); Pet. Reply 6.

2. "contact pads"

Patent Owner argues "that the term 'contact pads' refers to the pads on an integrated circuit package substrate for connecting with a printed circuit board." PO Resp. 12–14; PO Sur-reply 2–4. Petitioner disagrees. Pet. Reply 6–8. But, because we find that Petitioner has shown that Chin suggests implementing its invention in an IC package substrate as Patent Owner's proposed construction would require (*infra* § II.E.1[pre]), we need not resolve this dispute. *See Nidec*, 868 F.3d at 1017.

However, if we needed to substantively address this dispute, we would reject Patent Owner's proposed construction. Patent Owner advocates limiting the scope of this claim term to include only the contact pads in a particular location (i.e., the PCB-side of the IC package substrate),[12] but the intrinsic record does not support importing such a limitation into the claim. Patent Owner identifies (and we perceive) no passage in the intrinsic record that redefines the term "contact pads" or disavows part of its scope. *See Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365, 1367 (Fed. Cir. 2012) (explaining that a term should be given its plain and ordinary meaning unless a patentee acted as his own lexicographer or disavowed claim scope). Rather, Patent Owner's argument is that the term should be limited because the Specification only discusses "contact pads" in that particular location and does not apply its invention to other pads shown in its figures. *See* PO Resp. 12–14; PO Sur-reply 3–4. But claims are not limited to the embodiments disclosed. *See Phillips*, 415 F.3d at 1323. Moreover, we agree with Petitioner (*see* Pet. Reply 6–7) that adoption of Patent Owner's proposal would render superfluous the phrase in claim 1 that requires contact pads to be "for making a direct connection between the integrated circuit package substrate and a printed circuit board," which is disfavored. *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

[12] The testimony of Patent Owner's declarant, Dr. Bauer, confirms that the term "contact pad" has a plain and ordinary meaning that includes pads located on an IC package substrate as well as those located on a PCB or an IC. Ex. 1110, 143:21–144:1 (agreeing Chin's PCB includes a "contact pad"); Ex. 2030 ¶ 46 (referencing "contact pads (I/O) on the ICs").

D. Summary of Prior Art

1. Chin (Ex. 1004)

Chin is directed to "the design and fabrication of printed circuits and multi-layered substrates that are suitable for carrying signals with very high data rates," and relates to "techniques to reduce landing pad parasitic components and reduce the impedance discontinuity between the pad and the interconnect to the pad." Ex. 1004, 1:7–13. Chin explains that "the impedance of the landing pads is generally significantly lower than that of their associated interconnect conductors," and "[t]he substantial impedance drop of the pad causes excess parasitic capacitance, which results in a reduction in bandwidth and slowing the signal transition rate." *Id.* at 1:46–48, 2:2–5. In view of this, Chin aims to "decrease the parasitic capacitance of substrate landing pads and to provide better impedance matching between the traces and the landing pads." *Id.* at 2:20–23.

According to Chin, "[a] landing pad's parasitic capacitance may be reduced by forming patterned holes in one or more reference potential layers below the landing pad," and "[r]educing the landing pad's parasitic capacitance creates a corresponding increase in the landing pad's impedance." *Id.* at 3:45–49. "A pre-determined amount of capacitance is then re-introduced to the landing pad" with compensation capacitors in order "to lower the pad's characteristic impedance to match that of the trace." *Id.* at 3:55–65.

Chin discloses several embodiments of printed circuit boards that include metal layers separated by dielectric material, with patterned holes formed in the metal layers. One embodiment is shown in Figure 2a, reproduced below.

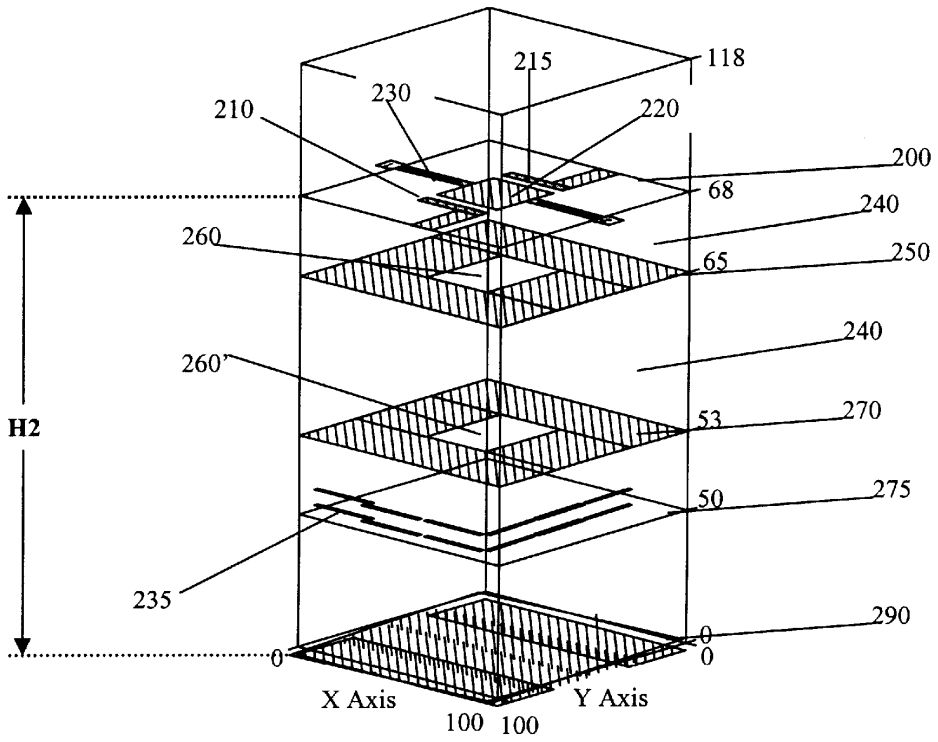


Figure 2a of Chin is an exploded isometric drawing of a segment of a printed circuit board. Ex. 1004, 4:4–5. The printed circuit board segment in Figure 2a includes: compensation capacitors 210 and 215, pad 220, and single trace 230 on surface metal layer 200; intermediate metal layers 250, 270, and 275; patterned holes 260 and 260' in layers 250 and 270, respectively; and ground reference layer 290. *Id.* at 4:4–25, 4:48–50.

2. HighSpeed (Ex. 1009)

HighSpeed is titled "High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices." Ex. 1009, 1. In section 5.1, HighSpeed describes "vias," which are "used to make connections between various layers of the PCB or to connect components to traces." *Id.* at 94.

"Figure 5.1 depicts a typical through-hole via and its equivalent circuit" and is reproduced below:

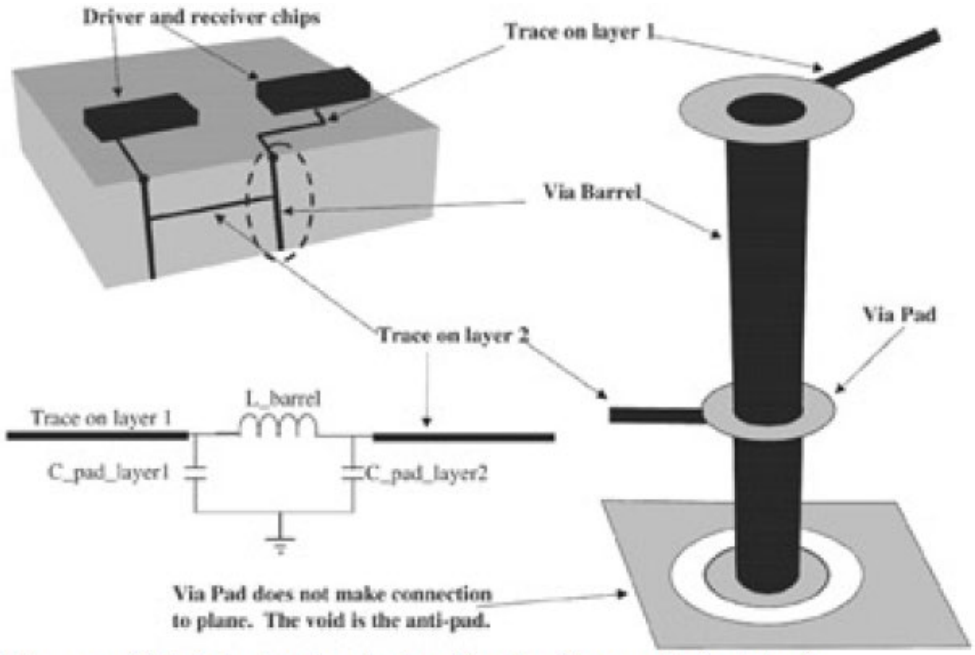


Figure 5.1: Equivalent circuit of a through-hold via.

Ex. 1009, 94. As shown above, Figure 5.1 illustrates a through-hole via connected to a trace on layer 1 and a trace on layer 2 along with its equivalent circuit. HighSpeed explains that a through-hole via "is made by drilling a hole through the board, filling it with solder, and making connections on appropriate layers via the pad." *Id.* "Other, less common types of vias, used primarily in multichip modules (MCMs) and advanced PCBs, are blind, buried, and micro-vias." *Id.*

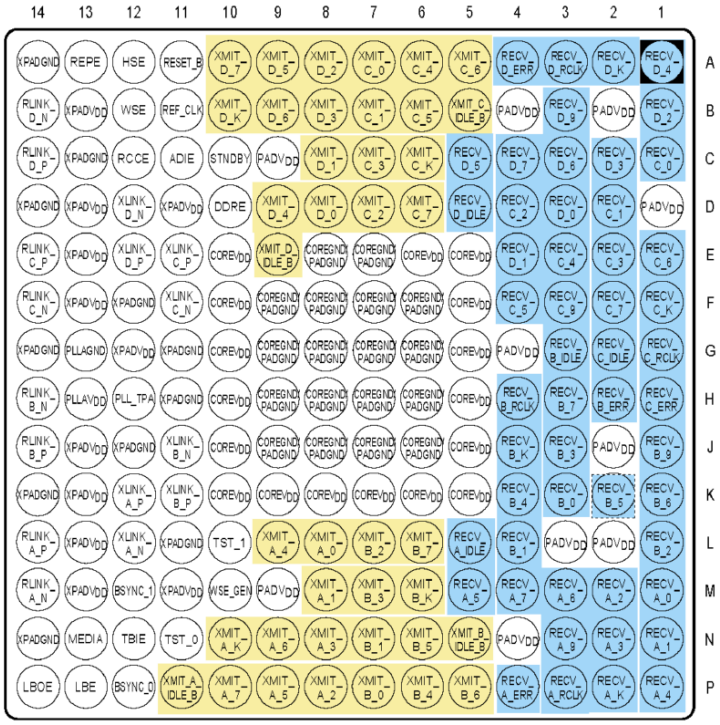
3. MC92600 (Ex. 1008)[13]

MC92600 is the User's Manual for Motorola's MC92600 Quad 1.25 Gbaud SERDES transceiver. Ex. 1008, 1, 17. MC92600 states that the

[13] Petitioner has established, by a preponderance of the evidence, that MC92600 was accessible to the public in 2003 and that persons interested in

Motorola part includes a transmitter that "takes the data byte presented at its data input . . . and serially transmits" associated information out the output pads. *Id.* at 21.

According to MC92600, the part is offered in a 196 MAPBGA package, and Figure 7-3 "provides a graphic of the package pin signal mappings." Ex. 1008, 67; *see id.* at 70 (showing Figure 7-3). Petitioner annotates this figure with yellow and blue highlighting, as shown below:



View G-G (Bottom View)

Figure 7-3. 196 MAPBGA Package

Pet. 61 (citing Ex. 1008, 70). Petitioner's annotation of Figure 7-3, reproduced above, shows yellow-colored transmit pins (designated "XMIT") and blue-colored receive pins (designated "RECV"). *Id.*

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the subject matter could have located it with reasonable diligence. *See* Pet. 59–60; Ex. 1003 ¶¶ 72, 168; Ex. 1013; Ex. 1027 ¶¶ 6–11, 16–17.

4. Oggioni (Ex. 1006)

Oggioni is directed to an electronic package including a chip carrier having a first conductive layer that includes at least one signal track and one contact area, and a reference structure having at least two conductive layers such that the signal track is electrically shielded by the reference structure. Ex. 1006, Abstr. Oggioni explains that the trend towards miniaturization of electronic devices has led to a reduction in the dimensions of the chip carrier conductive tracks on which the devices are packaged, including the use of a thin dielectric layer between the conductive tracks and ground plane of the electronic package. *Id.* at 1:57–67. According to Oggioni, "[a] shortened distance between conductive tracks and the ground plane increases the value of a corresponding stray capacitance. As a consequence, the bandwidth of the transmission line is strongly reduced." *Id.* at 1:67–2:3.

In attempting to address this drawback, Oggioni discloses an embodiment having conductive layers that do not "intersect a shadow of the projection of" its contact areas. Ex. 1006, 4:65–5:3, Fig. 2b. Oggioni states that its invention "substantially reduces the capacitance of the stray capacitor formed between" conductive signal tracks and corresponding ground planes. *Id.* at 5:46–49.

E. Obviousness Ground Based on Chin Alone (Ground 1)

Petitioner contends that the subject matter of independent claims 1, 7, and 12 and dependent claims 3, 4, 6, 8, 9, and 13–15 would have been obvious over Chin. Pet. 18–58.

Patent Owner disagrees, arguing that an ordinary artisan would not have extended Chin's design to IC package substrates (PO Resp. 14–23) and

that Chin fails to disclose cutouts "for reducing parasitic capacitance" between the first and second conductive layers (*id.* at 23–31). In addition, Patent Owner argues that Petitioner fails to show why an ordinary artisan would have modified Chin to yield the routing placement limitation (found in claims 6–9) (*id.* at 43–54), and Patent Owner separately addresses dependent claim 3 (*id.* at 41–42) and dependent claim 4 (*id.* at 70).

We begin our analysis with each independent claim and then turn to the dependent claims.[14]

1. Independent Claim 1

[pre] "An integrated circuit package substrate . . . ."

Petitioner contends that, "[t]o the extent the preamble is limiting," Chin teaches or suggests it. Pet. 20–21. Petitioner points to Chin's reference to a "ball-grid-array (BGA) package" and "a substrate used inside a BGA package." *Id.* at 20 (quoting Ex. 1004, 1:56–62). According to Petitioner, a person of ordinary skill in the art would know that the "substrate used inside a BGA package" is "an integrated circuit package

[14] The parties raised untimely, new arguments in the Reply, Sur-reply, and during the oral hearing, and such arguments are forfeited. *See* 37 C.F.R. § 42.23(b) (limiting scope of replies and sur-replies); Paper 15 (Scheduling Order), 8 (cautioning Patent Owner that "any arguments not raised in the response may be deemed waived"); Tr. 4:16–18 (instructing parties to limit oral hearing presentation to arguments in the briefs); *see also* Patent Trial and Appeal Board Consolidated Trial Practice Guide ("CTPG") 73–74, 85–86 (Nov. 2019), *available at* https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf. We have identified these arguments below when they are relevant to our analysis. Nevertheless, even if the parties had raised these arguments in a timely manner, they would not change the outcome here, as discussed below.

substrate." *Id.* at 21 (citing Ex. 1003 ¶ 85; Ex. 1001, 1:8–14, 2:1–3). Petitioner also contends "Chin explains that its disclosure relates to 'printed circuits' ***and*** 'multi-layered substrates' and that its teachings apply broadly to 'laminated PCB implementations' and to 'semiconductor implementations.'" *Id.* (quoting Ex. 1004, 1:7–10, 5:67–6:7); *see also id.* at 20 (citing Ex. 1004, 2:20–23). In addition, Petitioner asserts that an ordinary artisan "would have been motivated to apply the teachings of Chin to a package substrate because both PCBs and substrates secure electronic components and route signals between components and supply reference potentials." *Id.* at 21 (citing Ex. 1003 ¶ 86). Further, Petitioner submits that although Chin describes its invention using a PCB embodiment, "Chin also explains the concepts apply equally to a package substrate." *Id.* at 19 (citing Ex. 1003 ¶ 78); *see also* Pet. Reply 8.

Patent Owner disagrees. PO Resp. 14–23. According to Patent Owner, Petitioner's identified similarity between PCBs and IC packages (*see* Pet. 21) is too generic and "does not explain why POSITAs[15] would have considered Chin for the ball pad layer" as the majority of routing takes place near the contacts that connect to the IC. PO Resp. 14–16 (citing Ex. 2030 ¶¶ 152–154). Patent Owner also contends that "the Petition must, but does not, show that the BGA packages . . . would have benefited from Chin's designs." *Id.* at 16. Patent Owner contends that, unlike Chin, high-frequency BGA packages did not have microstrips connected to the ball pad layer (*id.* at 16–18 (citing Ex. 2030 ¶¶ 50–52, 145)) and did not have room for compensation capacitors (*id.* at 18–19 (citing Ex. 2030 ¶¶ 71 & n.7, 143–

[15] The acronym "POSITA" refers to a person of ordinary skill in the art.

144)). Finally, Patent Owner argues that, despite Petitioner's contention that parasitic capacitance was a known problem with known solutions, the state of the art did not suggest applying Chin's design to IC package substrates because the PCBs cited by Petitioner are "vastly different from high-frequency BGA package substrates." *Id.* at 19–23 (citing Pet. 10–12; Exs. 1021, 1022, 1024; Ex. 2030 ¶¶ 50–51, 160–164).

Having considered the parties' arguments, we are persuaded that Petitioner has established that Chin teaches the recitations in the preamble. In particular, we find that Chin discloses an IC package substrate, as recited by the preamble. *See* Ex. 1004, 1:61–62 ("a substrate used inside a BGA package"); Ex. 1003 ¶ 85 (Dr. Choi testifying that an ordinary artisan would know that a BGA substrate qualifies as an IC package substrate); *see also* Ex. 1003 ¶¶ 28–30 (Dr. Choi explaining that a BGA is a type of IC package). We credit Dr. Choi's testimony on this point because it is logical and supported by cited evidence. *See*, *e.g.*, Ex. 1014, 45;[16] Ex. 1016, 5–7.

We are also persuaded that Chin expressly suggests implementing its invention in an IC package substrate. Chin begins its description by stating that "[t]he present invention relates generally to the design and fabrication of printed circuits *and multi-layered substrates*." Ex. 1004, 1:7–8 (emphasis added). Similarly, Chin's final paragraph states that alternative implementations "will be apparent to those skilled in the art," and it states that "semiconductor implementations . . . are contemplated as within the scope of the present invention" as they use "similar layered printed circuit

[16] Unless otherwise noted, our citations refer to page numbers added to an exhibit by Petitioner or Patent Owner rather than the document's native page numbers.

routing techniques." *Id.* at 5:54–6:10. Moreover, as background for its invention, Chin addresses problems encountered as signal speed increases and explains that "excess parasitics that limit the bandwidth" are caused by an impedance mismatch between landing pads and their associated interconnect conductors. *Id.* at 1:35–56. Chin then states:

> One example is the use of a ball-grid-array (BGA) package in a multi-gigahertz printed circuit board. The landing pads of current state of the art BGAs are typically 25–30 mils in diameter, which is significantly larger than the typically 5 mil microstrips used in interconnecting conductors. *Another example is a substrate used inside a BGA package.* Typical solder ball landing pad sizes for current technology BGA substrates are on the order of 20–25 mil, significantly larger than the typically 3 mil traces used in microstrip interconnects.

Id. at 1:56–65 (emphasis added). Accordingly, given the context provided by Chin (*see id.* at 1:7–8, 5:54–6:10), we find that a person of ordinary skill in the art would have understood this passage (*see id.* at 1:61–65) to suggest applying Chin's disclosure to an IC package substrate. *Accord* Inst. Dec. 30–31; 148 DI, 42–43.

Patent Owner's arguments regarding this element are unavailing. *See* PO Resp. 14–23; PO Sur-reply 8–16. Patent Owner provides no alternative understanding of the salient passage of Chin (*cf.* PO Resp. 16, 18; Tr. 47:16–22), and it does not argue that an ordinary artisan would have been discouraged from following Chin's suggestion. *See* Pet. Reply 8–9. Instead, Patent Owner contends that "despite the statement in Chin 1:60–65, there is no evidence that microstrips would be present on the pad layer in a high-frequency BGA package substrates that allegedly would have benefited from Chin's design." PO Resp. 18; *see also id.* at 16. There are several flaws with this argument (which we address below), but most importantly, it

appears to be premised on the erroneous assumption that Chin's disclosure does not provide the requisite motivation.[17] As a result, the argument is inapposite because, as explained above, we find that Chin itself suggests the modification proposed by Petitioner.

Nevertheless, we have considered Patent Owner's arguments and evidence and weighed them against Chin's disclosure, but ultimately we credit Chin's statements over Patent Owner's arguments and evidence. Patent Owner presents arguments regarding Chin's microstrips (*see* PO Resp. 16–18) and Chin's compensation capacitors (*id.* at 18–19). We address these in turn.

As for the microstrips, Patent Owner's Response assumes (without explanation) that any implementation of Chin would necessarily include Chin's microstrips; however, we do not assume that microstrips are required simply because Chin's preferred embodiment includes microstrips. *See KSR*, 550 U.S. at 421 ("A person of ordinary skill is also a person of ordinary creativity, not an automaton."); *In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) ("[W]e do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art."); *see also Lear Siegler Inc. v. Aeroquip Corp.*, 733 F.2d 881, 889 (Fed. Cir. 1984) (The ordinary artisan is not "compelled to adopt

[17] *See, e.g.*, PO Resp. 16 ("To establish a motivation to apply Chin's design concepts to the BGA package(s) the Petition relies on, the Petition must, but does not, show that the BGA packages relied on by Petitioner would have benefited from Chin's designs."); PO Sur-reply 9 (arguing that "even if a POSITA *could* apply Chin's method to more than PCBs, that does not mean that they *would* have done so"), 10 ("Petitioner has not presented sufficient evidence that a POSITA would have considered the BGA pads had the impedance mismatch problem to apply Chin's method.").

every single aspect of [a reference's] teaching without the exercise of independent judgment."). In addition, Chin's claims indicate that a microstrip is *not* a necessary part of its invention. *See*, *e.g.*, Ex. 1004, 6:12–8:13 (most claims include no such requirement). *But see id.* at 6:57–64 (dependent claim 6 requires "interconnect lines" in the pad layer), 8:8–13 (dependent claim 13 requires "traces extending from" the contact pads). Consequently, even if Patent Owner were correct that an ordinary artisan would not have included microstrips coupled to the pads in a BGA package substrate, then we would determine that an ordinary artisan would not have included that aspect of Chin when adapting its invention to a BGA package substrate. *See* Pet. Reply 14.

In its Sur-reply, Patent Owner also argues that "if no surface transmission lines (microstrips) existed, then there would be no impedance mismatch or the need for Chin's modification at all." PO Sur-reply 14. To the extent Patent Owner advances this as a justification for its assumption that Chin's microstrips are required, this argument is untimely because it was not raised in Patent Owner's Response and is not fairly responsive to Petitioner's Reply. *See* PO Resp. 16–18; Pet. Reply 14–15; *supra* n.14. But, even if this argument had been properly raised, Patent Owner does not sufficiently explain why an ordinary artisan would have understood Chin's disclosure to only be applicable for impedance matching between a microstrip and a pad. *See* PO Sur-reply 14 (citing Ex. 2030, 91 n.12); *see also id.* at 8 (citing Ex. 2031, 45:17–46:23), 10 (citing Ex. 1110, 115:13–116:1). In particular, Patent Owner cites testimony regarding transmission

lines, but even assuming *arguendo* that Chin requires a transmission line,[18] we cannot agree that it requires a microstrip. Patent Owner's evidence shows that a microstrip is one type (but not the only type) of transmission line, and Patent Owner fails to sufficiently explain why this specific type of transmission line is allegedly required by Chin. *See* Ex. 2031, 45:17–46:23; *see also* Ex. 2030 ¶¶ 96 ("A transmission line is a signal trace with a controlled impedance."), 97 (identifying microstrip, stripline, and coplanar wave guide as types of transmission lines). In addition, to the degree Patent Owner argues that Chin should be ignored because its purpose is different than the '340 patent's purpose, this argument is inapposite. *See KSR*, 550 U.S. at 420–421 (explaining that an ordinary artisan would not ignore a reference simply because its "primary purpose" was different).

As for the compensation capacitors, Patent Owner contends that Chin would not have been implemented in a BGA substrate because Chin's

[18] Incidentally, we cannot agree that Chin requires a transmission line. Chin describes matching the impedance between an interconnecting conductor and a pad (Ex. 1004, 2:2–19), but Chin's disclosure does not state that it is limited to the situation where that interconnecting conductor is a transmission line (*see id.* at 1:39–43 (explaining that interconnecting conductor and adjacent reference plane for a transmission line with a predetermined impedance)). *Cf.* PO Sur-reply 10 (arguing that "Chin's method stemmed from the need to match the impedance at the pad *with the impedance of a signal line* (*typically a transmission line* in PCBs due to signal lengths) . . ." (emphasis added)). Dr. Bauer testifies that an ordinary artisan would not have applied Chin's method when "impedance and capacitance are not of concern" (Ex. 2030, 91 n.12), but does not testify that Chin requires a transmission line. Moreover, Dr. Bauer's other testimony indicates that impedance was, in fact, a concern at the interface between the PCB and the IC package. *See* Ex. 2030 ¶ 104 (testifying that impedance is controlled "at the interface(s) to the next packaging level or device"); *see also id.* ¶ 24 (explaining packaging levels).

compensation capacitors would not have fit (*see* PO Resp. 18–19; PO Sur-reply 13–15); however, Chin states that its invention is applicable in BGA substrates as well as larger-scale devices (i.e., PCBs) and smaller-scale devices (i.e., semiconductor applications). Ex. 1004, 1:56–65, 5:67–6:7; *see* Ex. 2030 ¶ 16 (identifying geometries of ICs, IC packages, and PCBs). Although Patent Owner relies on Dr. Bauer's testimony to support its contention (*see* PO Resp. 18–19), we assign little weight to that testimony because Dr. Bauer fails to provide sufficient analysis or evidence on these specific points (*see* 37 C.F.R. § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.")). In particular, Dr. Bauer testifies that "there is simply not enough substrate area" to include Chin's compensation capacitors on an IC package substrate due to "wiring line and space requirements" (Ex. 2030 ¶ 71), and because "IC package substrates tended to use SMD [(solder mask defined)] BGA ball pads" that "tend to be larger than NSMD PCB landing pads (the type frequently used on PCBs)" (*id.* ¶ 71 n.7; *see also id.* ¶ 143). This explanation is insufficient for three reasons.

First, Dr. Bauer fails to connect the dots between the BGA substrate's "wiring line and space requirements" and his conclusion that "there is simply not enough substrate area" on the pad layer for Chin's compensation capacitors. *See* Ex. 2030 ¶ 71 & n.7; *see also id.* ¶¶ 69–70 (explaining that wiring line widths and spaces are different in BGA substrates and PCBs and require different manufacturing techniques). Although we agree that PCBs have different wiring line and spacing requirements than IC substrates, we cannot find that this difference would prevent inclusion of compensation capacitors in the latter. Dr. Bauer's testimony could be read to suggest that

the problem lies in the fact that different manufacturing processes are used for PCBs and BGA substrates (*see id.* ¶ 70), but this is insufficiently explained.[19]

Second, Dr. Bauer fails to sufficiently explain why the alleged size differences between the PCB pads and the BGA substrate pads would have had a material effect on a designer's ability to fit compensation capacitors. *See* Ex. 2030 ¶ 71 n.7. In fact, at deposition, Dr. Bauer testified that the differences in pad sizes between PCBs and IC package substrates are "relatively immaterial." Ex. 1110, 88:20–89:13; *see also* Ex. 2019, 17–18 (illustrating the benefit of using PCB and BGA pads that are similarly sized). Also, Chin's disclosure contradicts Dr. Bauer's testimony by instead stating that BGA substrate pads are slightly *smaller* than PCB pads. *See* Ex. 1004, 1:58–65 (20–25 mils versus 25–30 mils). Moreover, Dr. Bauer does not testify that an ordinary artisan would not have used the larger NSMD landing pads on a BGA package, but rather that the smaller SMD pads were more common. Ex. 2030 ¶ 71 n.7.

Third, Dr. Bauer fails to reconcile his conclusions with Chin's disclosure of a BGA substrate example. *See* Ex. 1004, 1:56–65.

Ultimately, we credit Chin's statements (which suggest applying Chin's invention in an IC package substrate) over Patent Owner's evidence (which does not squarely contradict those statements, as explained above). Consequently, we disagree with Patent Owner's argument that an ordinary

[19] There is insufficient evidence on this record suggesting that the manufacturing techniques used at the time would prevent inclusion of Chin's compensation capacitors in a BGA substrate. Chin's compensation capacitors are simply metal strips in the pad layer (*see* Ex. 1004, 4:26–38), not standalone capacitors that are mounted on a PCB (*cf.* Ex. 2030 ¶ 19).

artisan would not have been motivated to include Chin's invention in a BGA substrate.

Finally, we address Patent Owner's argument that Petitioner fails to sufficiently show a rationale to include Chin's invention on the correct side of the IC package substrate. *See* Tr. 67:2–73:2, 96:11–100:10. This argument is untimely because it was raised for the first time at the oral hearing. *See supra* n.14; *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016) (vacating Board decision that relied on assertion first introduced at the oral hearing). Patent Owner asserts that the argument was made in its Response (Tr. 70:6–11, 96:11–97:10), but we do not agree that the Response fairly makes this argument—the cited pages instead contend that this issue is not addressed by Petitioner's reasoning regarding similarities between PCBs and IC substrates (PO Resp. 15–16). But, even if this argument were timely, we would disagree with it. We find that an ordinary artisan would understand the salient passage of Chin to expressly suggest applying its invention to the PCB-side of the BGA substrate. *See* Ex. 1004, 1:61–65 (identifying pads "on the order of 20–25 mil");[20] *see also* Ex. 2030 ¶¶ 30 (testifying that "the BGA ball pads on a BGA package substrate for connecting with a PCB generally used a pitch of .65–1.0 millimeters [(i.e., 25–39 mils)]"), 37 (testifying that BGA balls were typically 375–600 microns in diameter (i.e., 14.8–23.6 mils), where bump

[20] During the oral hearing, Patent Owner argued that Petitioner's identification of this passage during its rebuttal presentation was procedurally improper. Tr. 98:5–10 (referencing *id.* at 93:5–21). We disagree. At a minimum, we did not discern this argument from Patent Owner's briefs and, thus, cannot fault Petitioner for not responding to it earlier.

pads were 95–115 microns (i.e., 3.7–4.5 mils) in diameter (*cited in* PO Sur-reply 9)). During the hearing, Patent Owner argued that Dr. Bauer testified that Chin's microstrips would have meant that Chin would be implemented on the IC-side of the substrate (Tr. 100:14–101:2); however, Patent Owner's assertion is not supported by the evidence it cites (*see* Ex. 2030 ¶¶ 142–154). Dr. Bauer testifies that the IC-side of the BGA substrate included the majority of the routing, but does not sufficiently explain why this would have affected an ordinary artisan's implementation of Chin. *See id.* ¶¶ 152–154.

Patent Owner's other arguments are inapposite. Patent Owner disputes Petitioner's contention that parasitic capacitance was a known problem with known solutions (PO Resp. 19–23 (citing Pet. 10–12)), but we do not rely upon that contention. Patent Owner also disputes Petitioner's contention that the similarities between PCBs and IC packages would motivate an ordinary artisan to apply Chin to an IC package substrate (PO Resp. 14–16 (citing Pet. 22)), but we also do not rely upon that contention. Similarly, we do not rely on the parties' subsequent debate on these topics.[21] *See* Pet. Reply 9–11, 15–16; PO Sur-reply 8–10, 15–16. Finally, we do not address Patent Owner's allegation that Petitioner's Reply includes new

[21] We note that these arguments stray from the salient issues. For example, Patent Owner argues that a person of ordinary skill in the art would not have been motivated to apply Chin to the "bump pads" of an IC package (PO Sur-reply 9) in response to Petitioner's statement that Chin could apply "within an IC, within an IC substrate, and within a PCB" (Pet. Reply 9). However, the "bump pads" referenced by Patent Owner are not the pads at issue. *See*, *e.g.*, Ex. 1001, Fig. 1 (showing "bump pads" on the *IC-side* of the substrate).

arguments (PO Sur-reply 11–13 (citing Pet. Reply 11–13)) because we do not reach those arguments.

> *[a] "a first and a second electrically conductive layer separated from each other by an electrically insulating layer with no intermediate conductive layer therebetween"*

Petitioner contends that Chin teaches this limitation. Pet. 22–23. In particular, Petitioner maps Chin's surface metal layer 200 (which includes pad 220) and metal layer 250 to the claimed first and second electrically conductive layers. *Id.* (citing Ex. 1004, 4:48–57, Fig. 2a). Petitioner contends that Chin teaches that these layers are separated by dielectric material 240. *Id.* (citing Ex. 1004, 4:10–11, Fig. 2a).

Patent Owner does not dispute these contentions. *See* PO Resp.

We are persuaded that Chin teaches element 1[a]. Chin's metal layers 200 and 250 are electrically conductive layers that are separated from each other by an electrically insulating layer (i.e., dielectric material 240). Ex. 1004, 4:9–15, Fig. 2a.

> *[b] "a plurality of rows of contact pads formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board"*

Petitioner contends that Chin teaches this limitation. Pet. 23–24. As noted above, Petitioner contends that Chin suggests use of its invention in a BGA package substrate. *Id.* at 23 (citing Ex. 1004, 1:61–62); *see also supra* § II.E.1[pre] (addressing the preamble of claim 1). Petitioner contends that "a POSITA would know that a BGA package is comprised of a plurality of rows (i.e., a grid array) of contact pads." Pet. 23–24 (emphasis omitted)

(citing Ex. 1004, 1:57, 5:62–65, 6:40–41; Ex. 1003 ¶ 90). In support, Petitioner also cites to the '340 patent, which describes a BGA package substrate "of the prior art" that includes pads arranged in transmit and receive rows. *Id.* (citing Ex. 1001, 2:61–66, 3:27–36);[22] *see* Ex. 1001, Figs. 1–2. Moreover, according to Petitioner, a person of ordinary skill in the art would understand Chin to teach contact pads (i.e., pad 220) "for making a direct connection between the integrated circuit package substrate and a printed circuit board," as required. Pet. 24 (citing Ex. 1003 ¶¶ 91–92; Ex. 1004, 1:16–21, 1:62–65).

Patent Owner does not dispute these contentions. *See* PO Resp.

We are persuaded that Chin teaches or suggests element 1[b]. Chin describes "a substrate used inside a BGA package" (Ex. 1004, 1:61–62), and a person of ordinary skill in the art would understand that a BGA package substrate includes a plurality of rows of contact pads. Ex. 1003 ¶ 90; Ex. 1004, 1:56–58 ("ball-grid-array (BGA)"). Moreover, while Chin describes its invention using a single contact pad (pad 220) in metal layer 200, a person of ordinary skill in the art would understand Chin to describe use of its invention with several contact pads in that layer. *See*, *e.g.*, Ex. 1004, 1:16–23 (background suggesting application to several signals on different landing pads), 4:4–13 (explaining that Figure 2a shows "a segment of a PCB that for illustrative purposes, includes a single trace 230 and pad 220"), 6:40–41 (stating that conductive layer on surface includes "a plurality of contact pads"). In addition, we find that an ordinary

[22] The pin cites provided by Petitioner do not match the material quoted, which appears a few lines away. We have considered both the cited and quoted material, and we have updated these citations to reflect those lines.

artisan would understand Chin's contact pads to be used for directly connecting the package substrate and a printed circuit board. Ex. 1003 ¶¶ 91–92 (citing Ex. 1004, 1:16–21, 1:62–65); *see also* Ex. 1004, 6:40–43 (reciting a circuit board comprising "contact pads [that are] suitable for electrical connection to components mounted on the circuit board"); § II.E.1[pre] (finding that Chin suggests using his invention in the BGA package substrate). We credit Dr. Choi's testimony regarding element 1[b] because it is logical and consistent with the evidence of record.

> *[c] "a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer"*

Petitioner contends that Chin teaches this limitation. Pet. 25–26. In particular, Petitioner submits that Chin's invention reduces "[a] landing pad's parasitic capacitance . . . by forming patterned holes in one or more reference potential layers below the landing pad." *Id.* at 25 (quoting Ex. 1004, 3:45–47; citing Ex. 1004, 1:10–11, 6:44–46, Fig. 2a) (first alteration in original); *see also* Ex. 1004, Abstract (*cited in* Pet. 19). To illustrate, Petitioner annotates Chin's Figure 2a, as shown below:

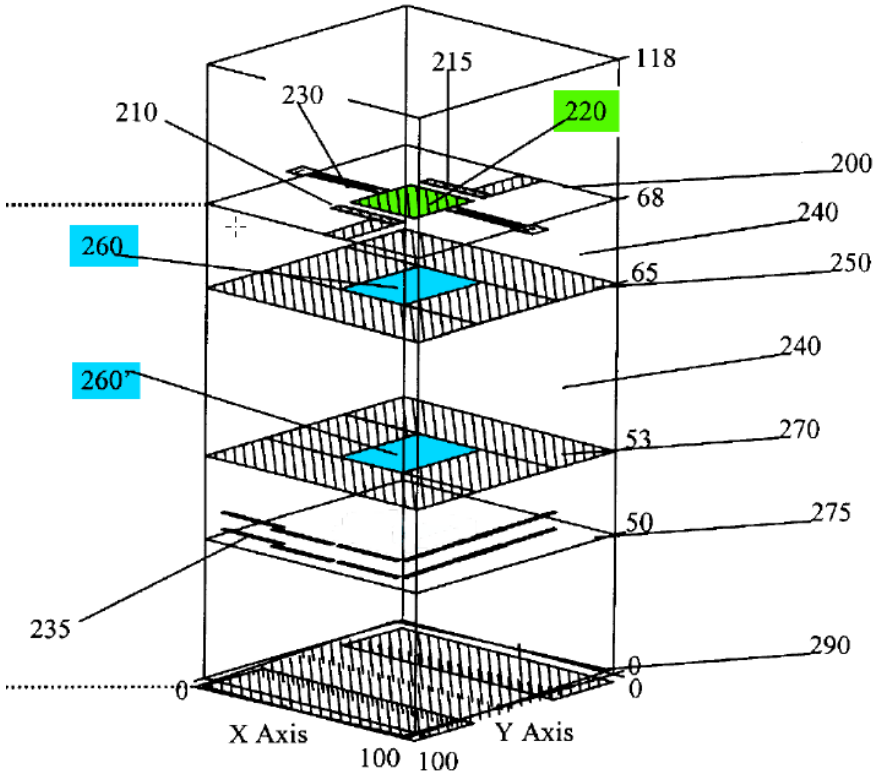


Figure 2a

As depicted above, Petitioner annotates Figure 2a to illustrate the landing pad 220 (in green) and its aligned holes 260, 260' (in blue). Pet. 26.

Patent Owner disagrees. PO Resp. 23–31. According to Patent Owner, Petitioner's analysis "does not account for the second half of Chin's methodology," which adds metal strips to layer 200 (forming compensation capacitors 210, 215) in order to lower the pad's impedance to match that of the trace by adding a controlled amount of parasitic capacitance. *Id.* at 24–25 (citing Ex. 1004, Abstr., 2:48–50, 2:64–67, 3:16–18, 3:56–64, 4:26–28, 4:39–41, 4:56–60, 6:51–55). Patent Owner contends that, by adding these metal strips to the first layer, "[t]his second step . . . result[s] in an increase in the capacitance between the first and second layers." *Id.* at 25 (citing Ex. 2030 ¶¶ 129–130). Patent Owner further contends that, as a result, the capacitance between the pad layer and the reference plane (the "Final

Capacitance") "can [be] the same . . . as the Original Capacitance (or even greater)." *Id.* at 26–28 (citing Ex. 2030 ¶ 130). According to Patent Owner, Petitioner fails to show that Chin teaches element 1[c] because Petitioner "has not explained why the Final Capacitance . . . is reduced as compared to the Original Capacitance." *Id.* at 28–29. Patent Owner submits that Petitioner fails to "explain why a POSITA would be motivated to ignore half of the Chin technique," given Chin's desire to eliminate an impedance discontinuity. *Id.* at 29–30 (citing Ex. 1004, 4:1–3, 5:48–53).

Having considered the parties' arguments, we are persuaded that Chin teaches "a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer," as required by element 1[c]. Chin describes forming hole 260 in metal layer 250, and this teaches the claimed "cutout[] formed in the second electrically conductive layer." *See*, *e.g.*, Ex. 1004, 3:45–47, 4:13–17, Fig. 2a. Chin also discloses that the layer can include a plurality of these cutouts. Ex. 1004, 6:44–46; *see also supra* § II.E.1[b] (addressing requirement for rows of contact pads). In addition, Chin expressly states that it includes these holes to reduce the corresponding pad's parasitic capacitance. Ex. 1004, 3:45–47, 6:46–50. Moreover, the pads are found in layer 200 (*e.g.*, *id.* at 4:11–13, Fig. 2a), and capacitance exists between adjacent metal layers 200 and 250.[23] Thus, we find that Chin's holes reduce parasitic capacitance between layer 200 ("the first electrically conductive layer") and layer 250 ("the second electrically conductive layer").

[23] We refer to different metal layers as "adjacent" when there are no metal layers between them, but these layers are separated by a dielectric layer.

Patent Owner's arguments regarding the "second half of Chin's methodology" are misplaced. *See* PO Resp. 24–29. Patent Owner appears to assume that claim 1 requires a device with reduced capacitance—rather than holes for reducing capacitance—but Patent Owner identifies (and we perceive) no such limitation in the claim. The claim recites "*cutouts . . . for reducing parasitic capacitance* between the second electrically conductive layer and the first electrically conductive layer," and *Chin's holes* satisfy this limitation because they *reduce parasitic capacitance*. It does not matter whether Chin includes other components that increase parasitic capacitance (such as Chin's compensation capacitors), as the claim does not preclude the addition of those components. *See Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997) (stating that, with a "comprising" claim, "other elements may be added and still form a construct within the scope of the claim"). Ultimately, Patent Owner does not propose a construction of this claim that would require a net reduction in parasitic capacitance (*see* PO Resp. 23–31),[24] and we perceive no support for such a construction in the

[24] To the degree Patent Owner urges a particular construction of the claim, this argument was first raised at the oral hearing (*see* Tr. 53:1–4, 55:7–11, 61:14–17), and Patent Owner forfeited any such argument by not timely raising it in its Response (*see supra* n.14). Indeed, Patent Owner's delay is not justifiable because Patent Owner was (or should have been) aware of this issue several months before it filed its Response. In the 148 IPR, Patent Owner made substantially similar arguments in response to a substantially similar petition, and we explained: "The compensation capacitors are not germane to our inquiry because the claim neither precludes such capacitors nor requires the claimed device to provide a net reduction in parasitic capacitance." IPR2021-00148, Paper 19 at 47 (emphasis added); *see also id.* at 45–47 (summarizing parties' arguments).

Moreover, even if this argument had been timely presented, it would not have been persuasive. Patent Owner argues that claim 1 requires a

record. As a result, Patent Owner's evidence (which compares capacitance between those layers with and without Chin's hole *and compensation capacitors*) is misplaced. *See* Ex. 2030 ¶¶ 129–132.

In addition, Patent Owner's proposed requirement is untenable because it is unclear how that requirement would be evaluated. Although Patent Owner contends that the "final" device (as manufactured) must have less parasitic capacitance than an "original" device (*see*, *e.g.*, PO Resp. 25–26), Patent Owner does not clearly identify what qualifies as the "original" device. Patent Owner assumes that Chin's cutouts and compensation capacitors are not present in the "original" device, but Patent Owner does not state whether the "original" also excludes pad 220 and traces 230 (in metal layer 200) and/or reference plane 250. To the degree an "original" includes some (but not all) components, Patent Owner provides no rationale to explain which components should be omitted (and why).

Moreover, even if we agreed with Patent Owner's premise (and assumed, as Patent Owner does, that the claim requires a device with overall reduced capacitance even considering Chin's compensation capacitors), we would still find this limitation to be taught by Chin's description of a device with reduced capacitance. *See* Pet. Reply 16. Chin describes an experimental prototype board with cutouts and compensation capacitors.

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completed device (*see* Tr. 55:7–11)—and we agree—but Patent Owner fails to explain why the claim requires that the completed device have reduced capacitance (*see id.* at 60:24–61:26). The claim does not require an integrated circuit package substrate with reduced capacitance between the first and second layers, but rather requires "cutouts . . . for reducing parasitic capacitance" between those layers. *See* Ex. 1001, 6:36–54. In addition, Patent Owner fails to substantiate its proposal with analysis or citations to the intrinsic record.

See Ex. 1004, 5:38–53. After Chin's modifications, the pad's impedance was 46.4 ohms (instead of 36 ohms), which more closely matches the 50-ohm microstrip, and Chin states that "[t]his improvement in impedance mismatch *and removal of excess capacitance* enhanced the bandwidth of the interconnect from 3.8 GHz to 7.2 GHz." *Id.* (emphasis added).[25] Moreover, Patent Owner's argument that the original parasitic capacitance is "caused by impedance mismatch" (PO Sur-reply 16 (citing Ex. 1004, 2:2–5)) misses the mark because the *cause* of the parasitic capacitance is not germane to our inquiry. *See KSR*, 550 U.S. at 420–421 (explaining that an ordinary artisan would not ignore a reference simply because its "primary purpose" was different).

Finally, at the oral hearing, Patent Owner argued that Chin's reference to reducing capacitance *at the pad* does not disclose the claim's requirement of reducing capacitance *between the two layers*. *See*, *e.g.*, Tr. 47:23–48:14, 51:19–21, 63:26–64:14; *see also id.* at 96:6–9 (citing Ex. 2030 ¶¶ 127–133). We determine that Patent Owner did not fairly present this argument in its briefs,[26] and thus, the argument is untimely. But, even if it had been

[25] Our understanding of this passage is consistent with Dr. Bauer's testimony. Dr. Bauer explains that the final capacitance depends upon the dimensions of the compensation capacitors, and compensation capacitors will compensate the loss in capacitance from the hole if the total area of overlap for those capacitors is the same as the pad area. *See* Ex. 2030 ¶¶ 129–130. Thus, if the total area of overlap for the compensation capacitors were *less* than the total pad area, then the capacitance in the "final" device would be reduced.

[26] There is only one sentence that even arguably advances this argument. *See* PO Resp. 29 ("Additionally, because the claims recite 'a plurality of cutouts . . . for reducing parasitic *capacitance between the second* electrically conductive *layer and the first* electrically conductive *layer*' in an

properly presented, we would disagree with it because consideration of the physics involved shows that Chin's holes reduce the capacitance between layer 200 and layer 250. These layers each include metal structures, and a parallel plate capacitor is formed between the layers. *See* Ex. 1003 ¶ 35; Ex. 1020, 4; *cf.* Ex. 2030 ¶¶ 92, 129. The capacitance between the layers is directly proportional to the overlapping area between their metal structures. *See* Ex. 1003 ¶ 35; Ex. 1020, 4; Ex. 2030 ¶ 130. Because Chin's holes remove metal from layer 250, those holes reduce the amount of overlapping area between the metal structures, which reduces the capacitance between the layers. Furthermore, although the capacitance between the metal layers may be different than the capacitance locally at the pad (*see* Ex. 2030 ¶ 132), *reducing* the capacitance between the pad and layer 250, as Chin discloses (*see* Tr. 49:2–7), will *reduce* the capacitance between layers 200 and 250.

> *[d] "wherein each cutout encloses an electrically insulating area within the second electrically conductive layer"*

Petitioner contends that Chin teaches this limitation. Pet. 26–28. Chin states that "[p]atterned hole 260 is formed by any suitable technique that creates a prescribed region devoid of metal." *Id.* at 26 (quoting Ex. 1004, 4:15–16) (alteration in original). Petitioner contends that an

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IC package substrate, it is not enough for Petitioner to merely argue that the capacitance at the pad is reduced."). In the Response, Patent Owner explains the argument in one way, which suffers from the deficiencies identified above. *See id.* However, at the oral hearing, Patent Owner instead provides a different explanation of it. *See* Tr. 47:23–66:7. We find the oral hearing argument to be new and not presented in the briefs. Indeed, Patent Owner's extensive elaboration of a single sentence from its brief unfairly deprives Petitioner of its opportunity to substantively respond.

ordinary artisan would understand this to mean that hole 260 is an electrically insulating area. *Id.* at 26–27 (citing Ex. 1003 ¶ 97). Petitioner also submits that hole 260 is within metal layer 250. *Id.* at 27–28 (citing Ex. 1004, 4:4–15, Fig. 2a).

Patent Owner does not dispute these contentions. *See* PO Resp.

We are persuaded that Chin teaches element 1[d]. Chin states that hole 260 (in metal layer 250) is a "region devoid of metal," which means it is an electrically insulating area. Ex. 1004, 4:13–17; *see also* Ex. 1003 ¶ 97.

> *[e] "wherein each electrically insulating area completely overlaps a corresponding one of the contact pads formed in the first electrically conductive layer such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer."*

Petitioner contends that Chin teaches this limitation. Pet. 28. In particular, Petitioner argues that Chin teaches that each hole completely overlaps a corresponding contact pad and is larger than the pad. *Id.* (citing Ex. 1004, 2:41–42, 3:49–55, 6:35–36, 8:6–7); *see also* Ex. 1004, 3:45–47, 6:17–22, 6:40–50. Referencing the earlier discussion that Chin's holes are "a prescribed region devoid of metal," Petitioner asserts that Chin inherently discloses that there is substantially no overlap of the contact pads with metal in the second electrically conductive layer (i.e., layer 250). Pet. 28 (emphasis omitted) (quoting Ex. 1004, 4:15–17; citing Pet. 26–28; Ex. 1003 ¶ 101).

Patent Owner does not dispute these contentions. *See* PO Resp.

We are persuaded that Chin teaches element 1[e]. Chin's holes are larger than and located below the corresponding pad (e.g., holes 260, 260'

are aligned below pad 220). *E.g.*, Ex. 1004, 2:41–42, 3:45–4:3, 8:6–7, Fig. 2a; *see also id.* at 5:38–47, Figs. 3a–3c.

Conclusion

For the reasons provided above, we are persuaded that Chin teaches or suggests each limitation of independent claim 1. We are also persuaded that a person of ordinary skill in the art would have been motivated to modify Chin's disclosure to yield the subject matter of claim 1. Accordingly, we conclude that Petitioner has shown, by a preponderance of the evidence, that the subject matter of claim 1 would have been obvious over Chin.

2. Independent Claim 7

Claim 7 differs from independent claim 1: it requires a routing metal layer comprising a plurality of routing traces. Specifically, claim 7 recites:

> 7. An integrated circuit package substrate, comprising:
>
> a first layer comprising a plurality of rows of electrical contacts;
>
> *a routing metal layer comprising a plurality of routing traces, the electrical contacts in the first layer being electrically connected with the respective routing traces*;
>
> a dielectric layer between the first layer and the routing metal layer with no intermediate conductive layer therebetween; and
>
> a plurality of cutouts in the routing metal layer for reducing parasitic capacitance between the first layer and the routing metal layer, the cutouts respectively overlapping the electrical contacts and having the same or larger dimensions as the electrical contacts such that there is substantially no overlap of the rows of contact pads with metal in the routing metal layer.

Ex. 1001, 8:7–21 (emphasis added). The claim also requires the routing metal layer to be adjacent to the claimed "first layer." *Id.* In this Decision, we refer to this required positioning as the "routing placement limitation."

Relying on the analysis for independent claim 1, Petitioner contends that the subject matter of independent claim 7 would have been obvious over Chin. Pet. 41–46 (citing *id.* at 20–26, 28, 35–41). For the "routing metal layer" of claim 7, Petitioner points to Chin's metal layer 275 with traces 235, and Petitioner argues that Chin renders obvious the routing placement limitation. *Id.* at 42–44 (citing *id.* at 35–39; Ex. 1004, 1:22–34, 4:23–24). Specifically, Petitioner states:

> Chin teaches: "Metal layer 275 . . . represents **any intermediate routing layer** with traces 235." In other words, Chin teaches that a routing layer with traces such as 235 could be placed interchangeably with, for example, a second conductive layer such as 250, in Figure 2a . . . .
>
> A POSITA would have found it obvious, and likely necessary, to modify the layer order of Chin Figure 2a to place the routing metal layer below the contact pad layer with only a dielectric layer in between because common BGA designs must route hundreds of signals between contact pads of the BGA substrate and integrated circuit contacts within the package. A POSITA would also have understood that the ordering of layers in the substrate needed to be flexible to accommodate those many signal lines. The placement of a routing layer next to the contact pad layer is a design choice that a POSITA was capable of making.

Id. at 35–36 (quoting 1004, 4:23–24; citing Ex. 1003 ¶¶ 114–115); *see also id.* at 43 (citing Ex. 1003 ¶ 126); Pet. Reply 26 (stating that "the large number of signals to be routed through the substrate would require routing signals in the layer immediately adjacent to the contact pad layer"). In addition, as evidence that a person of ordinary skill in the art would have

been aware of the design choice of putting a routing layer next to a contact layer, Petitioner contends that HighSpeed discloses "a commonly used prior art arrangement of metal layers with a routing trace on layer 2 immediately adjacent to the contact on layer 1." Pet. 38 (citing Ex. 1009, 94; Ex. 1030, 6; Ex. 1003 ¶ 117); *see also id.* at 43–44 (citing Ex. 1003 ¶ 127).

Patent Owner argues that Petitioner fails to show that an ordinary artisan would have modified Chin to yield the routing placement limitation of claim 7. PO Resp. 43–54. Patent Owner asserts that Petitioner's proposed modification of Chin is "textbook hindsight" and faults Petitioner for failing to explain *why* a person of ordinary skill in the art would have made this modification. *Id.* at 43 (citing *Princeton Biochemicals, Inc. v. Beckman Coulter, Inc.*, 411 F.3d 1332, 1337 (Fed. Cir. 2005)). In particular, Patent Owner argues that Petitioner does not explain why an ordinary artisan would have replaced power plane layer 250 with routing layer 275, where Chin describes layer 250 as "the first metal power plane layer below surface metal layer 200" followed by "intermediate" routing layer 275 and power plane layer 270. *Id.* at 44 (quoting Ex. 1004, 4:12–20); *see also* PO Sur-reply 22 (arguing that Petitioner ignores Chin's "express differentiation between intermediate routing layer 275 and power planes 250 (first) and 270 (intermediate)"). Additionally, Patent Owner submits that there was no teaching in the prior art of patterning holes in an adjacent metal routing layer as claimed. PO Resp. 44, 49–51.

We are not persuaded by Petitioner's arguments regarding interchanging Chin's routing layer 275 and first power plane 250. Chin's layer 200 includes pad 220, which is interconnected with other components by trace 230. Ex. 1004, 4:10–12. According to Chin, "[l]ayer 250 is the

first metal power plane layer below surface metal layer 200 . . . ." *Id.* at 4:12–13. Chin also describes an intermediate metal power plane layer 270 "that is below the top two metal layers" and an intermediate routing layer 275 that "represents any intermediate routing layer with traces 235." *Id.* at 4:18–24. Even if Chin indicates that intermediate routing layer 275 can be swapped with intermediate power plane layer 270, Chin does not teach (expressly or inherently) or suggest that "intermediate" metal layer 275 can be swapped with "first" power plane layer 250. Petitioner does not provide adequate support for its assertion to the contrary. *See* Pet. 35.

Also, Petitioner does not adequately support its assertion that it would have been obvious to modify Chin to replace layer 250 with layer 275. Petitioner refers to "the need to route possibly hundreds of signals" and "be flexible to accommodate [the] many signal lines"—but, even if this would have motivated an ordinary artisan to *add* routing traces or layers, it does not sufficiently explain why routing layer 275 would have been moved, as Petitioner suggests. *See* Pet. 43; Ex. 1003 ¶ 126 (repeating the Petition). Petitioner simply states that this placement "is a design choice that a POSITA was capable of making." Pet. 43 (citing Ex. 1003 ¶ 126 (repeating the Petition)). But the fact that an ordinary artisan *could* have performed the proposed modification does not show the requisite motivation to do so. *See Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018) (faulting the Board for "focus[ing] on what a skilled artisan would have been *able* to do, rather than what a skilled artisan would have been *motivated* to do at the time of the invention"); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) ("It was [Petitioner's] burden to demonstrate both that a skilled artisan would have

been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." (internal quotation marks omitted)). Petitioner's use of generalized statements and lack of supporting explanation suggests that Petitioner's proposal invokes improper hindsight.

Moreover, Patent Owner is correct that the additional prior art Petitioner relies upon (e.g., HighSpeed) does not show an arrangement of metal layers with a routing trace and cutouts on a second layer adjacent to a first layer with contacts. *See* PO Resp. 49. This further suggests Petitioner's proposal is the result of improper hindsight.

Ultimately, on this record, we find Petitioner has not established by a preponderance of evidence that a person of ordinary skill in the art would have been motivated to modify the layer order of Chin by moving routing layer 275 below contact pad layer 200, as Petitioner proposes.

In its Reply, Petitioner argues that Chin's metal layers satisfy this limitation because the term "routing layer" is "merely a label, *i.e.*, a non-limiting intended use." *See* Pet. Reply 21–28. However, this argument is untimely and forfeited. *See supra* n.14. Specifically, Petitioner presents a new claim construction argument (i.e., the term "routing layer" is non-limiting) that departs from the approach taken in the Petition and does not fairly respond to Patent Owner's Response or the Institution Decision. *See* Pet. 42 (contending that "routing layers are layers comprising metal traces"); CTPG 45 ("The petitioner may respond to any such new claim construction issues raised by the patent owner, but cannot raise new claim construction issues that were not previously raised in its petition."), 74 ("'Respond,' in the context of 37 C.F.R. § 42.23(b), does not mean proceed in a new

direction with a new approach as compared to the positions taken in a prior filing.").

However, even if the argument had been properly presented, it would not have been persuasive because we would conclude that the term "routing layer" is limiting and requires at least one routing trace. To support its argument to the contrary, Petitioner argues that some metal layers include both routing traces and reference planes and, as a result, it "is impossible" to clearly differentiate between routing layers and reference layers. Pet. Reply 23–25. But, this argument is a red herring. Even if Petitioner were correct that an ordinary artisan would be unable to reliably determine the proper classification for a layer with both routing traces and reference planes, this would show that the scope of the term "routing layer" is somewhat unclear,[27] but not that it is non-limiting. Indeed, both parties agree that a "routing layer" must at least include a routing trace. *See* Tr. 36:17–20, 77:19–25. Moreover, we agree with Patent Owner that the '340 patent differentiates between routing layers and reference potential layers. *See also* PO Sur-reply 22 (citing Ex. 1001, 2:61–67, 4:35–36). And, to the extent Petitioner contends that Chin's reference layer 250 qualifies as a "routing layer," we discern no basis for that contention.

[27] We determine that the term is sufficiently clear for us to evaluate Petitioner's contentions, and we need not (and cannot) evaluate whether the scope of the term would survive an indefiniteness challenge. *Cf. Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 813 (Fed. Cir. 2021) ("[I]t is not always impossible to adjudicate a prior-art challenge, one way or the other, just because some aspect of a claim renders the claim indefinite."). Moreover, we do not delimit the precise contours of the term "routing layer" because it is unnecessary for this proceeding. *See Nidec*, 868 F.3d at 1017.

Petitioner's Reply argument that Chin discloses the "routing layer" limitation appears to be premised on its untimely and erroneous contention that this term is non-limiting (*see* Pet. Reply 26–28), but even setting that aside, none of these arguments are persuasive. At best, these arguments show: Chin discloses cutouts in its routing and reference layers (*see id.* at 26), that it was possible to route signals in two adjacent metal layers (*see id.* at 26–27), and that it was possible to include signal traces on the second layer of an IC substrate (*see id.* at 27–28). However, we are not persuaded that this shows that Chin teaches or suggests the routing placement limitation. Also, even if this shows that a person of ordinary skill in the art *could* have modified Chin to include a signal trace in first power layer 250, as required by the routing placement limitation, we are not persuaded of any reason *why* the ordinary artisan would have done so. Thus, Petitioner's arguments remain deficient for the reasons explained above. This is especially problematic considering Chin differentiates between its first power layer and intermediate power layers, does not disclose signal traces on its first power layer, and only refers to signal traces on its intermediate power layers.

Accordingly, we find Petitioner has not established, by a preponderance of the evidence, that the subject matter of claim 7 would have been obvious over Chin.

3. Independent Claim 12

Claim 12 is different from independent claim 1 in that it requires a third layer that also includes the claimed cutouts. It recites:

> 12. An integrated circuit package substrate, comprising:

> *a first layer* comprising a plurality of rows of electrical contacts;
>
> *a plurality of electrically conductive layers* disposed immediately proximate the first layer;
>
> a plurality of dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other, and
>
> a plurality of rows of *cutouts formed in each of the plurality of the electrically conductive layers*, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers.

Ex. 1001, 8:7–21 (emphases added).

Petitioner contends that the subject matter of independent claim 12 would also have been obvious over Chin. Pet. 51–56 (relying on discussion of independent claim 1 and dependent claim 4). For the claimed "first layer," Petitioner points to Chin's layer 200 (which includes pad 220), and for the "plurality of electrically conductive layers," Petitioner points to metal layers 250, 270, 275, 290. *Id.* at 51–53 (citing Ex. 1004, Fig. 2a, 1:22–34, 4:9–11); *see also id.* at 55 (citing Ex. 1004, 4:52–53, 7:8–11). Petitioner also contends that Chin discloses that its metal layers each include a hole that encloses an electrically insulating area and overlaps a corresponding pad for reducing parasitic capacitance. *Id.* at 54–56 (citing Ex. 1004, Fig. 2b, 7:1–11; Pet. 25–28, 30–32, 33–34).

Patent Owner contends that Chin fails to teach "cutouts . . . for reducing parasitic capacitance" for the same reasons argued with respect to the corresponding limitation in claim 1 (*see* PO Resp. 1, 23–31), but, as we explained above, this argument is unavailing (*supra* § II.E.1[c] (addressing

corresponding limitation in claim 1)). Patent Owner does not otherwise dispute Petitioner's showing for this claim. *See* PO Resp.

On this record, Petitioner's contentions are persuasive. Petitioner shows that Chin teaches or suggests each limitation of claim 12. In particular, Chin's layer 200 teaches the claimed "first layer," metal layers 250 and 270 teach the "plurality of electrically conductive layers," and dielectric material 240 teaches the "dielectric layers." Ex. 1004, 4:4–25, Fig. 2a; *see also supra* § II.E.1[a]–[b] (addressing similar limitations in claim 1). Chin discloses that layers 250, 270 include respective holes 260, 260' that each overlap the corresponding pad and reduce parasitic capacitance between the layers. Ex. 1004, 4:13–20, 7:1–7, Fig. 2a; *see also supra* § II.E.1[c]–[e] (addressing similar limitations in claim 1).

Accordingly, we conclude that Petitioner has shown, by a preponderance of the evidence, that the subject matter of claim 12 would have been obvious over Chin.

4. Claim 3

Claim 3 depends from claim 1 and requires that "the cutouts have the same dimensions as the contact pads." Ex. 1001, 6:62–64.

For this claim, Petitioner argues that "[a] POSITA would understand the sizing of the cutouts to be a design decision subject to tradeoffs." Pet. 29. Petitioner acknowledges that Chin teaches using cutouts that are larger than the contact pads to minimize parasitic capacitance, but argues Chin also teaches that using oversized cutouts reduces capacitance more than desired and requires reintroduction of capacitance to tune the pad impedance. *Id.* (citing Ex. 1004, Abstr.). Petitioner also asserts that "[a] POSITA would understand that larger cutouts reduce the shielding effects of

ground or power metal layers and reduce the available area for routing traces in routing layers," and, therefore, "would have found it obvious to try sizing the cutouts to have the same dimensions as the contact pads to allow for greater shielding and routing flexibility." *Id.* (citing Ex. 1003 ¶ 103).

Patent Owner argues that Petitioner fails to provide sufficient evidence supporting its assertions. PO Resp. 41–42. For example, Patent Owner contends that "Petitioner has not shown any example in the prior art where the cutouts were of the same dimension as the contact pads." *Id.* at 41. Patent Owner also argues that neither Petitioner nor Dr. Choi performed a "tradeoff analysis" to support its claims that different sized cutouts would "allow for greater shielding and routing flexibility." *Id.* at 41–42.

We agree with Patent Owner. The only evidence Petitioner cites in the Petition to support this argument is paragraph 103 of Dr. Choi's declaration. Pet. 29. That paragraph, however, simply parrots the language in the Petition, without offering the underlying facts on which the opinion is based. *Compare* Ex. 1003 ¶ 103, *with* Pet. 29. Such testimony is conclusory and entitled to little or no weight. 37 C.F.R § 42.65(a).

We also agree with Patent Owner that Petitioner has not directed us to any disclosure in the prior art where the cutouts were the same size as the contact pads. *See infra* § II.F (discussing grounds relying on a combination of Chin and Oggioni); PO Resp. 41–42. Instead, Petitioner relies only on references that teach the use of holes larger than the contact pads. Additionally, Dr. Bauer explains that the prior art shows "even with a hole larger than the contact area, excellent shielding and routing flexibility were achieved." Ex. 2030 ¶¶ 139–140; PO Resp. 42. Furthermore, we note that Dr. Choi does not provide any evidence or further explanation of the

purported tradeoff between cutout size and greater shielding and routing flexibility. *See* PO Resp. 41 (noting that Petitioner and Dr. Choi fail to analyze "how much (if any) additional shielding could be provided, or how much routing density could be increased"). As a result, we are not persuaded that additional space for shielding or routing would have motivated an ordinary artisan to make the proposed modification to Chin.

Additionally, we are not persuaded by Petitioner's argument that a person of ordinary skill in the art "would have found it *obvious to try* sizing the cutouts to have the same dimensions as the contact pads." Pet. 29 (emphasis added). The Supreme Court set forth the standard for when something may be obvious to try: "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. In the Petition, Petitioner does not address whether there are a finite number of identified solutions, and Petitioner does not persuasively show that the proposed modification would have solved a problem.

We, therefore, agree with Patent Owner that Petitioner offers insufficient evidence with the Petition to show a rationale to modify Chin in the manner proposed. PO Resp. 41–42.

Petitioner does not cure this deficiency in its Reply.[28] For example, in its Reply, Petitioner argues that the "sizing of the cutouts is a clear example

[28] Patent Owner contends that Petitioner's Reply injects "five pages of improper new arguments." PO Sur-reply 18. We agree that Petitioner presents arguments in its Reply that do not appear in its Petition. *See supra* n.14. Nevertheless, we have addressed these arguments to explain why we find them to be unpersuasive.

of a predictable variation that cannot render a claim non-obvious," and that "sizing a known structure is simply the 'application of a known technique' with predictable results." Pet. Reply 16–17. According to Petitioner, a person of ordinary skill in the art would have understood the effect of resizing the patterned hole to be smaller, the same size, or larger than the pad size. *Id.* at 17. To support this, Petitioner directs us to an IBM publication (Ex. 1111) purportedly "confirming a predictable improvement in signal performance as the cut-out size in an IC substrate was increased." Pet. Reply 17.[29] As Petitioner acknowledges, however, the IBM publication includes no actual data for cutouts that were the same size as the pads. Instead, as Patent Owner explains, "the newly submitted IBM reference tested one configuration with cutouts (400μm) significantly smaller than and another with cutouts (800μm) significantly larger than the pads (650μm)." PO Sur-reply 18. Nor does Dr. Choi address the predictability purportedly demonstrated by the IBM reference.

Petitioner also contends that the IBM publication "discusses the well-known design trade-offs like reduced shielding and difficulty routing around the large cutouts" (Pet. Reply 17 (citing Ex. 1111, 1)), but the IBM publication does not indicate that any such tradeoffs would have motivated an ordinary artisan to make the proposed modification to Chin (*cf.* Ex. 1111, 1 (instead stating that "wider plane opening[s]" provide "better electrical performance" but "may compromise . . . wireability" and mechanical

[29] Petitioner did not offer this exhibit with its Petition, and Dr. Choi did not cite to this exhibit in his declaration submitted with the Petition. *See* CTPG 73; *Intelligent Bio-Sys.*, 821 F.3d at 1369. Additionally, Dr. Choi did not provide a supplemental declaration addressing this reference.

reliability)). Additionally, Dr. Choi does not address the purported trade-offs in the IBM reference.

As such, we are not persuaded by Petitioner's reliance on the IBM reference, and agree with Patent Owner that Petitioner's attorney arguments are insufficient to support its obviousness challenge. *See, e.g.,* PO Sur-reply 19 (arguing "Petitioner presents no analysis whatsoever on the achievable variability caused by fringe capacitance and how that variability affects the performance").

Petitioner additionally argues that "[a] POSITA would not have blindly recreated the exact size structures disclosed in Chin but would have employed ordinary creativity to explore a range of sizes that suited a particular application." Pet. Reply 18. According to Petitioner, hole size is a common engineering tradeoff that could be modeled and tested to determine what size worked for a particular purpose. *Id.* Petitioner states:

> With reports from Chin (and Oggioni) of significant bandwidth increases resulting from cutouts in metal layers below contact pads, a POSITA would have been motivated to model, simulate, and prototype a range of cutout sizes including the simplest size, that equal in size to the ball pad. Equally sized cutouts are the easiest to draw in a layered CAD tool because one can trace the ball pad in an overlay view. . . . Because Chin provided only one testing datapoint, a POSITA would have been motivated to model variations on the Chin design to determine the optimal pattern hole size . . . .

Id. at 20–21.

Petitioner's arguments are unpersuasive. In support of these arguments, Petitioner relies on deposition testimony from Dr. Bauer, but our review of that cited testimony reveals Dr. Bauer testified that there are "tools for modeling the performance of a transmission line in a lot of different

situations," but those tools "have limits in capabilities." Ex. 1110, 21:8–22:3. Dr. Bauer also testified that generally in 2006 "there would be a prototyping phase," and agreed that a person of ordinary skill in the art "reading Oggioni or Chin and trying to determine the size of the cutout that [he/she] wanted to use, could . . . try four different cutout sizes." Ex. 1110, 28:20–29:4, 190:25–191:10. Absent from this testimony is any indication that a person of ordinary skill in the art would consider using cutout sizes other than those disclosed in Chin and Oggioni, which teach using cutouts that are larger than the pads.

Additionally, we are not persuaded by Petitioner's argument that "[e]qually sized cutouts are the easiest to draw in a layered CAD tool." Pet. Reply 20. Petitioner does not provide any support for this statement. Additionally, even if it is true, Petitioner fails to demonstrate or explain sufficiently any correlation between the ease of creating drawings using a layered CAD tool and what a person of ordinary skill in the art would have considered or done when sizing cutouts. As a result, Petitioner is left to rely on primarily attorney argument to support its contention that "a POSITA would have been motivated to model variations on the Chin design to determine the optimal pattern hole size, the number of layers in which to include the pattern holes, and other design aspects." *Id.* at 20–21. Attorney argument, however, cannot take the place of evidence. *E.g.*, *In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974).

Nor does Petitioner cure the deficiency in its "obvious to try" argument, as it fails to adequately address whether there are a finite number of identified solutions. During the oral hearing, counsel for Petitioner argued that "a person of ordinary skill in the art making cutouts would make

them either smaller, the same size or larger. There are only three options and so the same size ones would simply be a choice that would be right in the middle." Tr. 45:17–22; *see also* Pet. Reply 17 (referring to "resizing the patterned hole to be smaller, the same size, or larger than the pad size"). Petitioner's attempt to characterize the sizing options as being limited to three *categories* of sizes—smaller, the same size, or larger—is unavailing because two of those categories comprise a range with a virtually infinite number of size values. Moreover, Petitioner's argument that there are a limited number of sizing options seems inconsistent with its arguments based on "design trade-offs" such as routing *flexibility*. Pet. 29; Pet. Reply 17.

Accordingly, we conclude that Petitioner has not shown, by a preponderance of the evidence, that the subject matter of claim 3 would have been obvious over Chin.

5. Claim 4

Claim 4 depends from claim 1 and further recites:

> a third electrically conductive layer separated from the second electrically conductive layer by a second electrically insulating layer, the third electrically conductive layer including a plurality of cutouts each of which encloses an electrically insulating area and completely overlaps one of the contact pads, *the contact pads forming transmit and receive rows*, the cutouts in the second and third electrically conductive layers being arranged in rows corresponding to the transmit and receive rows such that there is substantially no overlap of the rows of contact pads with metal in the third electrically conductive layer.

Ex. 1001, 6:65–7:9 (emphasis added to disputed limitation).

Petitioner contends that Chin teaches or suggests these additionally-recited limitations. *See* Pet. 29–34. In particular, Petitioner asserts that Chin's metal layer 270 (which includes hole 260') teaches the "third electrically conductive layer" that includes the claimed cutouts. *Id.* (citing Ex. 1004, 4:18–20, 7:1–7, Fig. 2a; Pet. 26–28). Petitioner argues that Chin teaches or suggests pads that "form[] transmit and receive rows," as also required, because "[a] POSITA would know that a BGA package would have rows of ball pads that serve to transmit and receive signals." *Id.* at 32 (citing Ex. 1003 ¶ 110; Pet. 23–24 (addressing "rows of contact pads" in claim 1)). Petitioner also submits that "the '340 patent admits such an arrangement was known to a POSITA." *Id.* at 32–33 (citing Ex. 1001, Fig. 2 (items 202, 204)).

Patent Owner argues that it is improper to rely on the '340 patent to argue obviousness. PO Resp. 70. According to Patent Owner, because the '340 patent does not show microstrips in its pad layer, "Petitioner has not shown that a POSITA would realize that the [patent's illustrated] layout would suffer from excessive capacitance or impedance mismatch to benefit from Chin's method." *Id.* (citing Ex. 2030 ¶¶ 50, 52, 125; Ex. 1001, Fig. 2). In addition, Patent Owner contends that, even though Figure 2 is identified as prior art, "there is no evidence that this was a publicly known arrangement," as the label "could just refer to an earlier iteration of a confidential design over which the inventors improved." *Id.* (citing Ex. 2030 ¶ 54; Ex. 2031, 18:4–10).

Having considered the parties' arguments, we are persuaded that Petitioner has established that the additionally-recited limitations of claim 4 would have been obvious over Chin.

As explained above, Chin's metal layer 270 teaches the claimed "third electrically conductive layer," which is separated from layer 250 by dielectric material 240, and Chin discloses that layer 270 includes hole 260' that overlaps the corresponding pad. Ex. 1004, 4:4–25, 7:1–7, Fig. 2a; *see also supra* § II.E.3 (addressing similar limitations in claim 12). In addition, Chin suggests implementing its invention in a BGA package substrate. Ex. 1004, 1:61–65; *see also supra* § II.E.1[pre] (addressing claim 1).

We are persuaded that an ordinary artisan would have understood that a BGA package substrate includes "contact pads forming transmit and receive rows," as required by claim 4.[30] Dr. Choi testifies that an ordinary artisan would know that a BGA package "would have rows of ball pads that serve to transmit and receive signals." Ex. 1003 ¶ 110. We credit this testimony because it is logical and consistent with the evidence of record. In addition, we perceive no contradictory testimony from Dr. Bauer on this point. *See* PO Resp. 70.

In addition, the Specification of the '340 patent admits that, in "a typical ball grid array (BGA) integrated circuit package substrate of the prior art," the contact pad metal layer includes transmit rows and receive rows. Ex. 1001, 2:1–5, 2:61–67, 3:27–30, Fig. 2 (labeled "prior art"). From this, we find that the applicant admitted that "contact pads forming transmit and

[30] In its Reply, Petitioner argues that this claim phrase does not present a "structural limitation." Pet. Reply 29. We need not (and do not) address that contention because we find that this phrase would have been obvious even applying Patent Owner's understanding of it. *See* PO Sur-reply 7 (contending that "transmit and receive rows" of pads "refer to I/O pads for transmitting and receiving [data]," as opposed to "ones used to connect to . . . power, ground, and control signals").

receive rows" is prior art. *See Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988) ("A statement in a patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness."); *In re Nomiya*, 509 F.2d 566, 571 (C.C.P.A. 1975) ("By filing an application containing Figs. 1 and 2, labeled prior art, ipsissimis verbis, and statements explanatory thereof appellants have conceded what is to be considered as prior art in determining obviousness of their improvement." (footnote omitted)); *see also Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1339 (Fed. Cir. 2020) (stating that "it is appropriate to rely on admissions in a patent's specification when assessing whether that patent's claims would have been obvious" in an *inter partes* review proceeding).[31] For this additional reason, we find that this limitation would have been obvious in light of Chin.

Patent Owner's contrary arguments are unavailing. Although admissions regarding prior art are not held against an inventor "when the subject matter at issue is the inventor's own work" (*Riverwood Int'l Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1354 (Fed. Cir. 2003)), we have no reason to believe that this subject matter was the inventors' work. Indeed, Patent

[31] The Director of the Patent and Trademark Office recently issued a Memorandum addressing the use of "applicant-admitted-prior-art" ("AAPA") in an *inter partes* review proceeding. *See* USPTO Memorandum, Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311 (June 9, 2022), *available at* https://www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf. That Memorandum states that AAPA is evidence of an ordinary artisan's knowledge and "must be considered in an IPR, notwithstanding the provisions of § 311(b)." *Id.* at 3. Moreover, because the Petition relies on AAPA in combination with Chin, the AAPA does not form "the basis" of a ground. *See id.* at 4.

Owner does not assert that the inventors of the '340 patent invented this subject matter; instead, Patent Owner simply posits that it "could" be true. *See* PO Resp. 70. Also, even if the specific layer ordering depicted was unusual, as Patent Owner contends (*id.* (citing Ex. 2030 ¶ 54)), this fails to indicate that the subject matter relevant to our inquiry (i.e., contact pads forming transmit and receive rows) was the inventors' work.

Accordingly, we conclude that Petitioner has shown, by a preponderance of the evidence, that the subject matter of claim 4 would have been obvious over Chin.

6. Claims 6, 8, and 9

Claim 6 depends from claim 1, and includes the routing placement limitation. *See* Ex. 1001, 6:36–54 (claim 1 specifies first and second conductive layers adjacent to each other), 7:16–20 (claim 6 depends from claim 1 and specifies the second layer is a routing layer); *accord* Inst. Dec. 49. Claims 8 and 9 also include the routing placement limitation by virtue of their dependency from independent claim 7. *See* Ex. 1001, 7:37–50.

For the reasons explained above, Petitioner has not shown that the routing placement limitation would have been obvious in light of Chin. *Supra* § II.E.2 (addressing claim 7). Consequently, Petitioner has not shown, by a preponderance of the evidence, that the subject matter of claims 6, 8, or 9 would have been obvious over Chin.

7. Claims 13–15

Claims 13–15 depend from independent claim 12. Ex. 1001, 8:22–34. Petitioner contends that the subject matter of each of these claims is

rendered obvious by Chin because Chin teaches or suggests each claim's additionally-recited limitations. Pet. 56–58. Patent Owner does not dispute these contentions. *See* PO Resp. Having considered the record, we are persuaded that Petitioner has shown that Chin teaches or suggests each limitation of claims 13–15.

As for claims 13 and 15, we are persuaded by Petitioner's undisputed showing (*see* Pet. 56 (citing *id.* at 28, 30–32), 58) that Chin teaches that holes 260, 260' each completely overlap (and are larger than) the corresponding pad. *See* Ex. 1004, 3:45–55, 6:44–48, 7:1–7, 8:5–7, Fig. 2a; *supra* § II.E.1[e] (addressing similar limitation in claim 1).

As for claim 14, we are persuaded by Petitioner's undisputed showing (*see* Pet. 56–58 (citing *id.* at 44–46, 47–51)) that Chin teaches or suggests that the claimed "electrically conductive layers" include "a routing layer" (i.e., Chin's layer 275) that is electrically connected to the pads and "a ground return metal layer" (i.e., Chin's layer 290). *See* Ex. 1004, 4:23–24, 4:48–50, 5:3–9, 6:56–64, 7:8–11, Fig. 2b; Ex. 1003 ¶ 162.

Accordingly, we conclude that Petitioner has shown, by a preponderance of the evidence, that the subject matter of claims 13–15 would have been obvious over Chin.

F. Obviousness Grounds Based on Chin and Oggioni (Grounds 3, 5, 6, and 10)

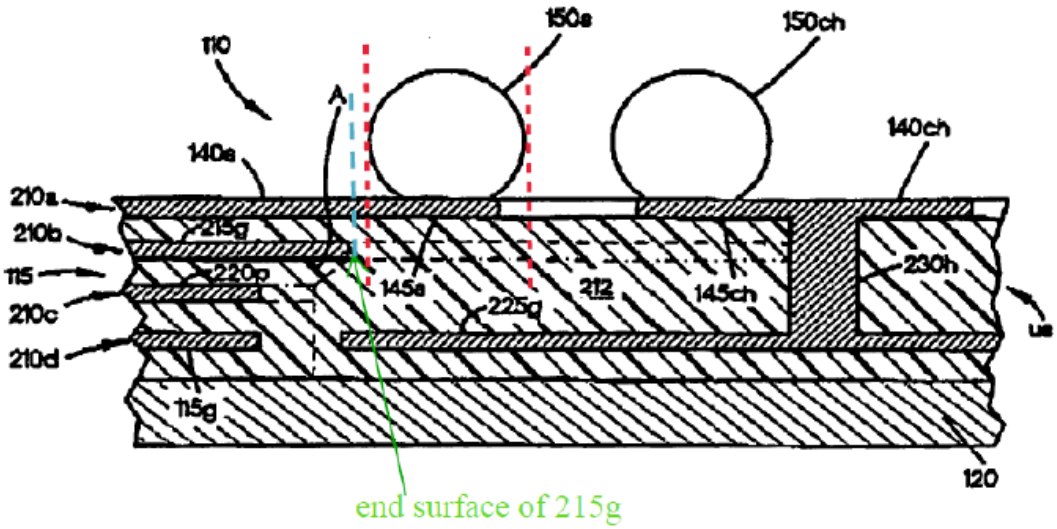
Petitioner contends that dependent claims 3 and 11 would have been obvious over Chin and Oggioni. Pet. 68–71. Petitioner also contends that dependent claim 18 would have been obvious over Chin and Oggioni in combination with either MC92600 or Shafer. *Id.* at 73, 87–88. In addition, Petitioner contends that dependent claim 19 would have been obvious over

Chin and Oggioni in combination with MC92600, Hsu, and Barr. *Id.* at 73–78.

As noted above, dependent claim 3 requires the claimed cutouts to be the same size as the corresponding contact pads. Ex. 1001, 6:63–64 (claim 3: "cutouts have the same dimensions as the contact pads"). Claims 11, 18, and 19 include commensurate limitations. *See id.* at 8:5–6 (claim 11: "electrical contacts . . . having the same dimensions as the cutouts"), 8:44–45 (claim 18: "cutouts having the same dimensions as the ball pads"), 8:46 (claim 19: depending from claim 18).

Petitioner contends that Oggioni, like Chin, is "directed to mitigating issues with high-speed signals interfacing an integrated circuit package by reducing package pad parasitic capacitance." Pet. 68. Petitioner further contends that Oggioni discloses using cutouts in a conducting layer that are the same size as the contact pad based on Oggioni's statement that "[g]round plane 215g does not intersect a shadow of the projection of contact area 145s." *Id.* at 70–71 (quoting Ex. 1006, 5:2–3).

Patent Owner disputes that Oggioni teaches using cutouts that are the same size as the contact pad. PO Resp. 34–35. To support its position, Patent Owner provides an annotated version of Oggioni Figure 2b, reproduced below from the Patent Owner Response. *Id.* at 35.



Annotated Figure 2b of Oggioni shows a partial sectional view of a chip carrier, including ground plane layer 215g formed in conductive layer 210b, solder balls 150, and contact area 145s. Ex. 1006, Fig. 2b, 3:55–4:38. Patent Owner's annotations include dotted red lines on the right and left sides of solder ball 150s, a dotted blue line on the left of the left-side red dotted line, and a green line pointed to the end of the blue dotted line labeled "end surface of 215g." Patent Owner explains that "[a]s illustrated in Figure 2b, the 'end surface of ground plane 215g' is to the left of solder ball 150s' projection. EX1006, Fig. 2b, 5:9–15. This indicates that the opening is larger than 150s in at least one dimension. EX2030, ¶180." PO Resp. 34.

Petitioner does not directly dispute Patent Owner's argument based on Figure 2b, asserting only that a person of ordinary skill in the art would "not find certainty in the figures." Pet. Reply 21. Rather, Petitioner maintains that Oggioni's statement defining a keep-out region as "a shadow of the projection of contact area 145s" demonstrates Oggioni discloses equal-sized cutouts. *Id.* (quoting Ex. 1006, 5:2–3).

We find that Oggioni's statement does not disclose equal-sized cutouts. Oggioni states that "ground plane 215g does not intersect a shadow of the projection of contact area 145s." Ex. 1006, 5:2–3. This statement does not clearly speak to the salient issue, despite Petitioner's contention to the contrary. Indeed, Dr. Choi acknowledges that this statement will be satisfied if the opening in ground plane 215g is *larger* than the shadow of contact area 145s. Ex. 2031, 121:22–122:16, 165:11–166:4; Ex. 2030 ¶ 178 (*cited in* PO Resp. 35–36). As a result, given Figure 2b, which depicts an opening larger than the contact pad in at least one dimension, Oggioni's statement does not teach sizing a cutout to be equal in size to contact area 145s. In addition, as Patent Owner points out, "Dr. Choi testified that 'a shadow of the projection of contact area 145s' does not necessarily mean a normal projection of the contact area 145s," and "[a] shadow of contact pad 145s could depend on the angle of the projection." PO Resp. 36 n.2 (quoting Ex. 2031, 169:17–24, 171:23–25). We agree with Patent Owner's assertion that this testimony from Dr. Choi indicates that a cutout corresponding to a shadow of 145s that is not projected perpendicularly to layer 210b would have a different size to the pad size.

After considering the evidence of record, we find Petitioner has failed to demonstrate persuasively that Oggioni discloses cutouts having the same dimensions as the contact pads, as required by these claims. Accordingly, we conclude that Petitioner has not shown, by a preponderance of the evidence, that the subject matter of claims 3, 11, 18, or 19 would have been obvious over Chin and Oggioni.

G. Obviousness Grounds Based on Chin and HighSpeed (Grounds 2, 7, and 8)

Petitioner contends that independent claim 7 and dependent claims 6, 8, and 9 would have been obvious over Chin and HighSpeed. Pet. 78–81. Petitioner also contends that dependent claims 2, 4, 5 and 10 would have been obvious over Chin and HighSpeed in combination with either MC92600 or Shafer. Pet. 58–67, 81–86. Patent Owner argues that Petitioner fails to show the routing placement limitation required by claims 2 and 5–10. PO Resp. 43–59.

We begin our analysis with independent claim 7 and then turn to the dependent claims.

1. Independent Claim 7

Petitioner contends that independent claim 7 would have been obvious over Chin and HighSpeed. Pet. 78–80. Petitioner relies on its allegations that Chin teaches or suggests each element of the claim (*id.* at 79 (citing *id.* at 41–46)), and Petitioner further contends that the combination of Chin and HighSpeed renders obvious the routing placement limitation (*id.* at 79–80).

As to the latter point, Petitioner contends that "HighSpeed illustrates and describes a commonly used prior art arrangement of metal layers with a routing trace on layer 2 adjacent the contact layer 1, which is coupled to an integrated circuit ('receiver chip')." Pet. 79–80. In support, Petitioner shows Figure 5.1 of HighSpeed, which is reproduced below:

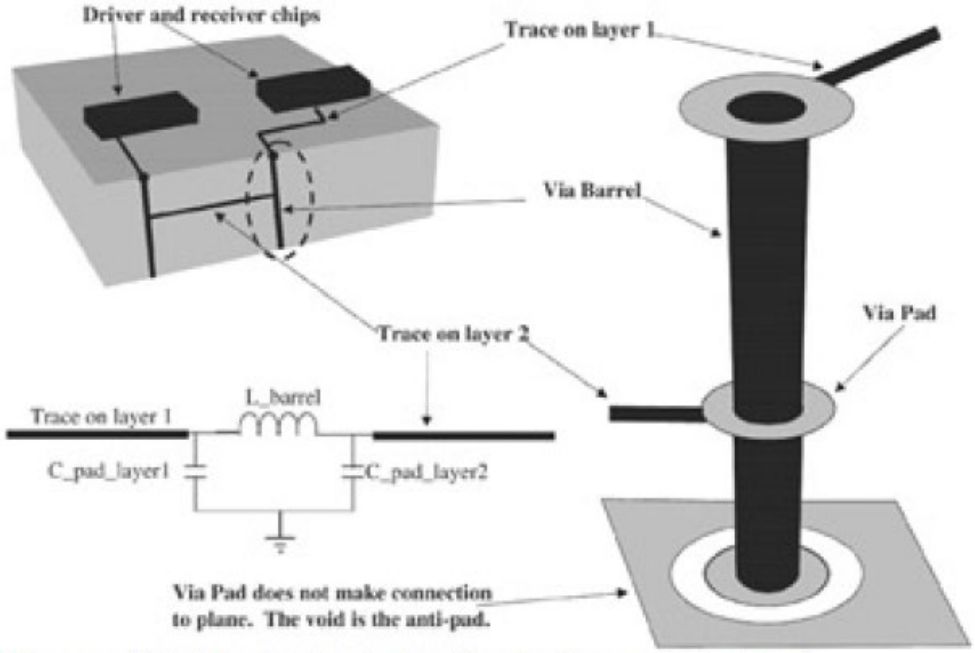


Figure 5.1: Equivalent circuit of a through-hold via.

Pet. 80 (reproducing Ex. 1009, Fig. 5.1). As shown above, Figure 5.1 illustrates a through-hole via connected to a trace on layer 1 and a trace on layer 2 along with its equivalent circuit. Ex. 1009, 94.

Petitioner asserts that a person of ordinary skill in the art would have been motivated to arrange Chin's layers "as shown/described in HighSpeed because this is one of a finite number of possibilities and within the skill of a POSITA to try." Pet. 80 (citing Ex. 1003 ¶ 232); *see id.* at 65 (stating that an ordinary artisan "would be choosing from a finite number of identified, predictable solutions (ordering a finite number of metal layers within a substrate) with reasonable expectation of success"). According to Petitioner, Chin and HighSpeed are both from the same field of endeavor, and an ordinary artisan "would have looked to HighSpeed, a combinable reference describing useful structures and approaches, or would have known and understood the prior art principles detailed therein." *Id.* at 58–60 (*cited in id.* at 78–79) (citing Ex. 1003 ¶¶ 72, 164–165, 168).

Patent Owner relies on the same arguments discussed above regarding obviousness in view of Chin alone, and further argues that Petitioner's analysis as to why a person of ordinary skill in the art would have combined Chin and HighSpeed is "legally insufficient." PO Resp. 43–44, 55–56. In particular, Patent Owner argues that simply characterizing references as being from the same field of endeavor is not sufficient to support an obviousness conclusion. *Id.* at 56 (citing *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017)). Further, according to Patent Owner, Petitioner's argument that the references are combinable does not demonstrate why a person of ordinary skill in the art would have combined them. *Id.* Patent Owner also challenges Petitioner's argument based on a finite number of possibilities, arguing that Petitioner's own declarant, Dr. Choi, testified that there were many different ways to achieve the results desired in Chin. *Id.* at 57 (citing Ex. 2032, 196:20–23).

We are not persuaded by Petitioner's arguments regarding the combination of Chin and HighSpeed. Petitioner does not sufficiently explain *why* a person of ordinary skill in the art would have been motivated to combine Chin and HighSpeed in the manner proposed. We agree with Patent Owner that simply characterizing references as being from the same field of endeavor is not sufficient to support an obviousness conclusion. PO Resp. 56; *see ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.,* 694 F.3d 1312, 1327–28 (Fed. Cir. 2012). Furthermore, Petitioner's analysis that it would have been obvious to arrange Chin in view of HighSpeed to have the second layer be a routing layer because the arrangement "is one of a finite number of possibilities and within the skill of a POSITA to try" is incomplete. Pet. 80. The Supreme Court in *KSR* held that "*[w]hen there is*

a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421 (emphasis added). Petitioner, however, never addresses, or otherwise presents evidence showing, a design need or market pressure to solve a problem. *See* Pet. 58–59, 65, 80; Ex. 1003 ¶¶ 165, 177, 232 (repeating material in the Petition). Additionally, testimony from Dr. Choi that "there are many ways to achieve the same result" of an impedance match in Chin, undermines Petitioner's "finite number" argument.[32] Ex. 2032, 196:20–23.

For these reasons, as well as those discussed in Section II.E.2 *supra*, we find Petitioner fails to establish, by a preponderance of the evidence, that the subject matter of claim 7 would have been obvious over Chin and HighSpeed.

2. Dependent Claims 2, 5, 6, 8–10

Petitioner contends that dependent claims 6, 8, and 9 would have been obvious over Chin and HighSpeed. Pet. 78–81. Petitioner also contends that dependent claims 2, 5 and 10 would have been obvious over Chin and HighSpeed in combination with either MC92600 or Shafer. Pet. 58–67, 81–86.

Claims 2, 5, and 6 each depend from claim 1 and include the routing placement limitation. *See* Ex. 1001, 6:36–54 (claim 1 specifies first and second conductive layers adjacent to each other), 6:55–61 (claim 2 depends

[32] Petitioner did not address this testimony, or Patent Owner's argument based on it, in its Reply.

from claim 1 and specifies the second layer is a routing layer), 7:10–20 (same for claims 5 and 6); *accord* Inst. Dec. 49.

Claims 8, 9, and 10 include the routing placement limitation by virtue of their dependency from independent claim 7. *See* Ex. 1001, 7:37–8:3.

For the reasons explained above, Petitioner has not shown that the routing placement limitation would have been obvious in light of Chin alone or in combination with HighSpeed. *Supra* §§ II.E.2 (addressing claim 7 and Chin alone), II.G.1 (addressing claim 7 and Chin-HighSpeed). Petitioner's allegations regarding MC92600 and Shafer do not remedy those deficiencies. *See* Pet. 65, 66–67, 84–85. Consequently, Petitioner has not shown, by a preponderance of the evidence, that the subject matter of claims 2, 5, 6, or 8–10 would have been obvious over Chin and HighSpeed.

3. Dependent Claim 4

Petitioner contends that dependent claim 4 would have been obvious over Chin and HighSpeed in combination with either MC92600 or Shafer. Pet. 66, 86.

We already found claim 4 to be unpatentable based on Chin alone (*see supra* § II.E.5), so we do not reach Petitioner's contentions that this claim is unpatentable over Chin in combination with other references. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner "is entitled to a final written decision addressing all of the claims it has challenged"); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (non-precedential) (recognizing that the "Board need not address issues that are not necessary to the resolution of the proceeding" and, thus, agreeing that the Board has "discretion to decline to decide additional

instituted grounds once the petitioner has prevailed on all its challenged claims").

H. Obviousness Ground Based on Chin and MC92600 (Ground 4)

Petitioner contends that dependent claims 16 and 17 would have been obvious over Chin and MC92600. Pet. 72. Patent Owner argues that Petitioner fails to show a sufficient rationale to combine these references as proposed. PO Resp. 60–65.

We address the limitations of these claims, and then we analyze the parties' arguments regarding the rationale to combine these references.

1. Dependent claims 16 and 17

Claim 16 depends from independent claim 12 and recites:

> wherein the electrical contacts comprise transmit rows and receive rows, and the electrically conductive layers are operable to convert a serial data stream to or from a parallel data stream.

Ex. 1001, 8:35–39. Claim 17 depends from claim 16 and further requires that "each cutout completely overlaps a corresponding one of the electrical contacts." *Id.* at 8:40–42.

Petitioner contends that the additionally-recited limitations of claim 16 would have been obvious over the Chin-MC92600 combination. Pet. 72 (citing *id.* at 60–63 (addressing commensurate limitations in claim 2)). In particular, Petitioner contends that MC92600 discloses a BGA package with rows of transmit ball pads and receive ball pads, which are

coupled to SERDES[33] functionality to convert parallel data to serial data. *Id.* at 61 (citing Ex. 1008, 21, 70; Ex. 1003 ¶ 171). In addition, Petitioner explains that a BGA package is used to connect an IC with an external system. *Id.* at 63 (citing Ex. 1003 ¶ 174).

Petitioner further contends that Chin teaches the additionally-recited limitations of claim 17. Pet. 72 (indirectly citing *id.* at 28).[34] Specifically, Petitioner contends that Chin teaches that each hole completely overlaps a corresponding contact pad and is larger than the pad. *Id.* at 28 (citing Ex. 1004, 2:41–42, 3:49–55, 6:35–36, 8:6–7).

Patent Owner does not dispute these contentions. *See* PO Resp. 60–65.

We are persuaded by Petitioner's undisputed showing that MC92600 discloses the additionally-recited limitations of claim 16.[35] MC92600 describes a BGA package with transmit rows and receive rows, and because it has SERDES function, its layers are operable to convert a serial data

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[33] SERDES (Serializer/Deserializer) refers to a method of sequencing parallel data bits into a stream of serial bits, transmitting the serial bits, and converting the bits back to parallel at the receiver. Ex. 1003 ¶ 33.

[34] The Petition refers to the discussion of claim 8, but that simply refers back to this portion of the Petition. *See* Pet. 47, 72.

[35] In its Reply, Petitioner argues that the recitation of "electrically conductive layers [that] are operable to convert a serial data stream to or from a parallel data" is a "non-limiting intended use[]." Pet. Reply 29–30. We need not (and do not) address this argument. Patent Owner states that this phrase would be satisfied by a package substrate for an integrated circuit that performs the SERDES function (Tr. 81:5–9, 83:3–18), and the Petition relies on a substantially similar contention (*see* Pet. 62–63). We are persuaded that such a substrate would satisfy the claim language, and as we explain, we are also persuaded that MC92600 teaches such a substrate.

stream to or from a parallel data stream. Ex. 1008, 21, 67, 70; *see also* Ex. 1003 ¶ 171 (annotating figure from reference to show transmit pads in yellow and receive pads in blue).

In addition, we are persuaded by Petitioner's undisputed showing that Chin discloses the additionally-recited limitations of claim 17, as Chin's holes are larger than and located below the corresponding pad (e.g., holes 260, 260' are aligned below pad 220). *E.g.*, Ex. 1004, 2:41–42, 3:45–4:3, 8:6–7, Fig. 2a; *see also supra* § II.E.1.[e] (addressing commensurate limitation in claim 1).

2. Rationale to Combine Chin and MC92600

Petitioner contends that an ordinary artisan would have been motivated to combine Chin with MC92600 to "arrange electrical contacts as transmit rows and receive rows" and "route a serial data stream to or from a SERDES IC operable to convert that data stream to or from a parallel data stream that is also routed to electrical contacts," as required by claim 16. Pet. 72 (citing *id.* at 58–63). Petitioner asserts that "[a] POSITA designing an IC package capable of handling high-speed communications would have looked at existing designs for common processors like the one described in MC92600," for example, "to build compatibility or to study best practices." *Id.* at 60 (citing Ex. 1003 ¶¶ 72, 164, 168). Petitioner contends that an ordinary artisan would have been motivated "to modify Chin's BGA package to use an arrangement of transmit and receive ball pad rows like the one disclosed in MC92600." Pet. 62. In support, Petitioner submits that this would be a combination of prior art elements according to known methods to yield predictable results. *Id.* (citing Ex. 1003 ¶ 172).

Patent Owner argues that Petitioner fails to address "why a POSITA would have applied Chin's approach to a SERDES package substrate." PO Resp. 60; *see also id.* at 63–64 (arguing that Petitioner's reasons to combine are "too generic" and "lack . . . specific reasoning," which evinces hindsight). Patent Owner submits that Petitioner fails to show that MC92600 had an impedance mismatch between a trace and a pad, which was the problem solved by Chin. *Id.* at 60–61. Patent Owner also argues that "Petitioner does not explain why a POSITA would not have started with MC92600's existing package substrate." *Id.* at 62 (citing Ex. 2030 ¶ 169). In addition, according to Patent Owner, "Petitioner may argue that SERDES often involved high frequency data and a POSITA would therefore 'seek to reduce parasitic capacitance by employing cutouts in metal layers adjacent to substrate contact pads,'" but this does not explain why the holes should be aligned with the contacts. *Id.* at 62–63 (citing Pet. 13; Ex. 1001, 8:18–21). Patent Owner also contends that, in Chin, the two metal layers adjacent to the contacts are reference planes, and "Petitioner does not explain how the two reference planes 'are operable to convert a serial data stream to or from a parallel data stream.'" *Id.* at 64–65.

In the Reply, Petitioner contends that "a POSITA would have applied Chin to a SERDES substrate because Chin addresses 'the design and fabrication of printed circuits and multi-layered substrates that are suitable for carrying signals with very high data rates' such as those attained with SERDES chips." Pet. Reply 30 (quoting Ex. 1004, 1:7–10; citing Pet. 8, 13 (citing Ex. 1003 ¶ 48)). Petitioner responds to Patent Owner's arguments by asserting that Chin is directed to reducing excess parasitic capacitance in addition to matching impedance (*id.* at 30 (citing PO Resp. 60–61)), and that

the MC92600's substrate design was not publicly accessible like the pinout (*id.* (citing PO Resp. 61–62)). Petitioner also contends that the MC92600 pinout was valuable. *Id.* at 30–31 (citing Ex. 2032, 369:3–370:22).

In the Sur-reply, Patent Owner responds that "Chin only discusses the problem of excess parasitic capacitance in connection with impedance mismatch," "Chin does not suggest the need for a cutout when there is no microstrip," and "Chin does not suggest SERDES packages suffered from excess parasitic capacitance." PO Sur-reply 26 (citing Ex. 1004, 2:2–5). Patent Owner also responds that an ordinary artisan could have reverse engineered the MC92600 to reveal the layer structure and layout, and it "makes no sense to start from Chin's design when the goal is to create a package compatible with MC92600." *Id.* at 27.

Having considered the parties' arguments and evidence, we are persuaded that Petitioner has shown, by a preponderance of the evidence, that a person of ordinary skill in the art would have been motivated to combine Chin with MC92600. *See* Pet. 7–9 (*cited in* Pet. Reply 30) (providing technology background), 59–62; Pet. Reply 30.

We find that an ordinary artisan would have been aware of SERDES and would have known that it used high data rates. Ex. 1003 ¶¶ 33–35 (*cited in* Pet. 7–9) (Dr. Choi testifying that SERDES "was ubiquitous and was known . . . at least as early as 1966" and explaining that the serial data was eight times faster than the IC's internal clock frequency). In addition, on this record, we find that the ordinary artisan would have understood that parasitic capacitance was a problem for SERDES packages. In particular, Dr. Choi testifies that a high-frequency SERDES data stream was "impeded by the parasitic capacitance between a substrate contact pad and other metal

layers within the substrate." Ex. 1003 ¶ 35. Dr. Choi also testifies that, given this problem, a person of ordinary skill in the art would have sought to reduce this parasitic capacitance. *Id.* ¶ 48. We credit this testimony because it includes a logical explanation and is corroborated by evidence. *See* Ex. 1004, 1:66–2:5; Ex. 1020, 4; *see also* Ex. 1016, 5, 9 (*cited in* Pet. 6–7).

Chin states that its invention is applicable to "substrates that are suitable for carrying signals with very high data rates," and it describes techniques for reducing landing pad parasitic components. Ex. 1004, 1:7–10. In addition, Chin explains that "increasing signal speed requires improvements in the signal fidelity," and states that signal fidelity is degraded (and excess parasitic capacitance is caused) by the impedance mismatch associated with the "relatively large landing pad geometry." *Id.* at 1:36–37, 1:66–2:5. Further, Chin states that a "technique believed to be used by some engineers" to solve that problem is to include a hole in the reference plane directly underneath the pad. *Id.* at 2:13–16.

MC92600 describes a Motorola product with SERDES functionality (*see* Ex. 1008), and Motorola was a well-known provider of communications technologies and integrated circuits (Ex. 1003 ¶ 168). Dr. Choi testifies that "[a] POSITA designing an IC package capable of handling high-speed communications would have looked at existing designs for common processors like the one described in MC92600." Ex. 1003 ¶ 168. Dr. Choi identifies two exemplary motivations for this: "to build compatibility or to study best practices." *Id.* Dr. Choi further testifies that

> [a] POSITA would be motivated to modify Chin's BGA package to use an arrangement of transmit and receive ball pad rows like the one disclosed in MC92600 to form a combination of prior art elements according to known methods (forming rows of transmit and receive pads in a BGA package for a

> SERDES IC, as taught by MC92600), in Chin's BGA package to yield predictable results of organizing transmit and receive pins in an industry accepted arrangement.

Id. ¶ 172. Dr. Choi also testifies that the ordinary artisan would have had a reasonable expectation of success in making the proposed combination. *Id.* We credit this testimony from Dr. Choi because it is logical and consistent with the evidence of record.

Given these findings, we are persuaded by Petitioner's argument that a person of ordinary skill in the art would have been motivated to modify a BGA package substrate implementing Chin's invention so that, as taught by MC92600, it includes rows of transmit and receive pads for a SERDES IC.[36] *See* Pet. 62; *see also* Pet. Reply 30 (explaining that "a POSITA would have applied Chin to a SERDES substrate because Chin addresses 'the design and fabrication of printed circuits and multi-layered substrates that are suitable for carrying signals with very high data rates' such as those attained with SERDES chips"). Indeed, as explained above, an ordinary artisan would have understood parasitic capacitance to be a problem for SERDES (given its high data rates), and Chin describes a technique for reducing the parasitic capacitance between a substrate's contact pad and its metal layers. *See KSR*, 550 U.S. at 420 (stating that "any need or problem known in the field of endeavor at the time of invention . . . can provide a reason for combining the elements in the manner claimed").

[36] We note that, during trial, the parties explained that the substrate includes the wiring to route signals (and is agnostic to the type of signal carried), and a corresponding IC performs the serialization/deserialization. *See* Pet. Reply 29 (citing Ex. 1110, 18:3–10); *see also* Tr. 81:5–9, 83:3–18.

Patent Owner's arguments to the contrary are unavailing. Patent Owner argues that MC92600 was not shown to have an impedance mismatch between a trace and a pad (*see* PO Resp. 60–61; PO Sur-reply 26), but this argument is inapposite because Petitioner does not rely on an impedance mismatch to propose a modification of MC92600 with Chin (*cf.* PO Resp. 62 (recognizing that, instead, Petitioner proposes to modify Chin with MC92600)). Patent Owner also appears to argue that Chin is only applicable when a substrate includes a microstrip (PO Sur-reply 26), but we disagree for the reasons previously explained (*see supra* § II.E.1[pre] (rejecting similar arguments)). Moreover, although Petitioner did not explain "why a POSITA would not have started with MC92600's existing package substrate" (PO Resp. 62; *see* PO Sur-reply 27), we do not agree that such an explanation is required. Our focus is on evaluating whether Petitioner's proposal demonstrates obviousness, not whether other combinations were also possible and obvious.[37]

Finally, we disagree with Patent Owner's argument that "Petitioner does not explain how the two reference planes 'are operable to convert a serial data stream to or from a parallel data stream.'" PO Resp. 64–65. The parties agree that an ordinary artisan would know that the IC package substrate itself does not actually convert serial data to and from parallel data,

[37] Even if some of Petitioner's statements suggest a different combination of these references, the existence of other combinations, without more, would not indicate that this combination fails to render the claimed invention obvious. *See Dome Patent L.P. v. Lee*, 799 F.3d 1372, 1381 (Fed. Cir. 2015) ("[J]ust because 'better alternatives' may exist in the prior art 'does not mean that an inferior combination is inapt for obviousness purposes.'" (quoting *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012))).

but an IC performs the SERDES function and the IC package substrate routes the data from that IC to a PCB. *See* Pet. Reply 29; Tr. 81:5–9, 83:3–18. As a result, Petitioner sufficiently addresses these aspects of the claim. In particular, Petitioner persuasively shows: an ordinary artisan would understand that a BGA package connects an IC with an external system (*see* Pet. 63 (citing Ex. 1003 ¶ 174)); MC92600 describes a BGA package with transmit and receive pads that connect to SERDES functionality (*see* Pet. 61–63 (citing Ex. 1008, 18, 21, 70; Ex. 1003 ¶¶ 171–173)); and Chin discloses holes in the routing layer and each reference plane that are aligned with the contact pad (*see* Pet. 51–52, 54–57 (citing Ex. 1004, 5:3–4, 7:1–11, Fig. 2b)).

3. Conclusion

For the reasons provided above, we are persuaded that the Chin-MC92600 combination teaches or suggests each limitation of dependent claims 16 and 17. We are also persuaded that a person of ordinary skill in the art would have been motivated to combine Chin and MC92600, as proposed. Accordingly, we conclude that Petitioner has shown, by a preponderance of the evidence, that the subject matter of claims 16 and 17 would have been obvious over Chin and MC92600.

I. Obviousness Ground Based on Chin and Shafer (Ground 9)

Petitioner contends that dependent claims 16 and 17 would have been obvious over Chin and Shafer. Pet. 86–87.

We already found claims 16 and 17 to be unpatentable (*see supra* § II.H.3), so we do not reach this ground. *See SAS*, 138 S. Ct. at 1359

(holding a petitioner "is entitled to a final written decision addressing all of the claims it has challenged"); *Boston Sci.*, 809 F. App'x at 990 (recognizing that the "Board need not address issues that are not necessary to the resolution of the proceeding" and, thus, agreeing that the Board has "discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims").

III. OBJECTIONS TO DEMONSTRATIVES

Patent Owner objects to slides 25–30, 33–35, and 41–46 of Petitioner's hearing demonstratives, arguing that these slides include new arguments and/or evidence not present in the Petition and/or Reply (Paper 30), and Petitioner objects to slide 32 of Patent Owner's hearing demonstratives, arguing that it presents a new argument and claim construction position that is not found in the record (Paper 31). We dismiss these objections as moot because, even considering any alleged new arguments, the outcome here would not change. *See supra* n.14.

IV. CONCLUSION[38]

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner

[38] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*, 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

has shown by a preponderance of the evidence that claims 1, 4, and 12–17 are unpatentable, but has not shown by a preponderance of the evidence that claims 2, 3, 5–11, 18, and 19 are unpatentable.

In summary:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 3, 4, 6–9, 12–15	103(a)	Chin	1, 4, 12–15	3, 6–9
2, 4, 5, 10	103(a)	Chin, MC92600, HighSpeed[39]		2, 5, 10
3, 11	103(a)	Chin, Oggioni		3, 11
16, 17	103(a)	Chin, MC92600	16, 17	
18	103(a)	Chin, MC92600, Oggioni		18
19	103(a)	Chin, MC92600, Oggioni, Hsu, Barr		19
6–9	103(a)	Chin, HighSpeed		6–9
2, 4, 5, 10	103(a)	Chin, Shafer, HighSpeed		2, 5, 10
16, 17	103(a)	Chin, Shafer[40]		
18	103(a)	Chin, Shafer, Oggioni		18
Overall Outcome			**1, 4, 12–17**	**2, 3, 5–11, 18, 19**

[39] Because we determine that claim 4 is unpatentable as obvious based on Chin alone, we decline to address the patentability of claim 4 based on Chin in combination with other references. *See supra* § II.G.3.

[40] Because we determine that claims 16 and 17 are unpatentable as obvious based on Chin and MC92600, we decline to address this ground. *See supra* § II.I.

V. ORDER

Accordingly, it is

ORDERED that claims 1, 4, and 12–17 of U.S. Patent No. 8,049,340 B2 are determined to be unpatentable, and claims 2, 3, 5–11, 18, and 19 are not determined to be unpatentable;

FURTHER ORDERED that Patent Owner's Objections to Petitioner's Demonstratives (Paper 30) are *dismissed* as moot;

FURTHER ORDERED that Petitioner's Objections to Patent Owner's Demonstratives (Paper 31) are *dismissed* as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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