

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP B.V., NXP USA, INC., and
NXP SEMICONDUCTORS N.V.
Petitioner,

v.

BELL SEMICONDUCTOR, LLC,
Patent Owner.

IPR2021-00967
Patent 8,288,269 B2

Before JO-ANNE M. KOKOSKI, JEFFREY W. ABRAHAM, and
JULIET MITCHELL DIRBA, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318

I. INTRODUCTION

NXP, B.V., NXP USA, Inc., and NXP Semiconductors N.V., (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–20 of U.S. Patent No. 8,288,269 (“the ’269 patent,” Ex. 1001). Paper 1 (“Pet.”). Bell Semiconductor, LLC. (“Patent Owner”) filed a Patent Owner Preliminary Response to the Petition. Paper 11 (“Prelim. Resp.”).

Petitioner also filed a Motion for Joinder to IPR2021-00147. Paper 3. On June 10, 2021, we issued an Order Dismissing Petitioner’s Motion for Joinder as Moot because the parties in IPR2021-00147 filed a joint motion to terminate IPR2021-00147, and we determined that the Board would benefit from revised briefing on Petitioner’s Motion for Joinder in view of this development. Paper 7, 2–3. Petitioner subsequently filed a Renewed Motion for Joinder (Paper 8), Patent Owner filed an Opposition to Petitioner’s Renewed Motion for Joinder (Paper 9), and Petitioner filed a Reply in Support of its Renewed Joinder Motion (Paper 10).

On October 8, 2021, we instituted *inter partes* review of claims 1–20, and dismissed Petitioner’s Renewed Motion for Joinder as moot. Paper 12 (“Institution Decision” or “Inst. Dec.”). After institution, Patent Owner filed a Response to the Petition (Paper 17, “PO Resp.”), Petitioner filed a Reply to Patent Owner’s Response (Paper 21, “Reply”), and Patent Owner filed a Sur-reply (Paper 23, “Sur-reply”).

On July 13, 2022, the parties presented arguments at an oral hearing for this proceeding. We have entered a transcript of the hearing into the record. Paper 31 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Based on the record before us, we conclude that Petitioner has shown by a preponderance of the evidence that

claims 1, 4, 7, and 9–20 of the ’269 patent are unpatentable, but has not shown by a preponderance of the evidence that claims 2, 3, 5, 6, and 8 are unpatentable.

II. BACKGROUND

A. *Related Matters*

The parties indicate that the ’269 patent is or was involved in the following proceedings: *Bell Semiconductor, LLC v. Microchip Technology, Inc.*, No. 6:20-cv-00296 (W.D. Tex. Apr. 16, 2020); *Bell Semiconductor, LLC v. Integrated Device Technology Inc.*, No. 1:19-cv-02155 (D. Del. Nov. 18, 2019); *Bell Semiconductor, LLC v. Texas Instruments Incorporated*, No. 2:20-cv-00048 (E.D. Tex. Feb. 21, 2020); and *Bell Semiconductor, LLC v. NXP Semiconductors, N.V.*, No. 1:20-cv-00611 (W.D. Tex. Mar. 23, 2020). Pet. 94; Paper 6, 2.

Additionally, the parties identify IPR2020-01693 and IPR2021-00147, involving the ’269 patent, and Petitioner identifies IPR2020-01692 and IPR2021-00148, involving related U.S. Patent No. 8,049,340 B2 (“the ’340 patent”). Pet. 94; Paper 6, 2.¹ In addition, Petitioner identifies IPR2021-00966, which is an *inter partes* review proceeding filed by Petitioner that challenges claims of the ’340 patent. Pet. 95. Concurrently with this Decision, we also enter a final written decision in that proceeding.

B. *The ’269 Patent*

The ’269 patent, titled “Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package,” issued on October 16, 2012. Ex. 1001, codes (45), (54). The ’269 patent is “directed to the design of an integrated

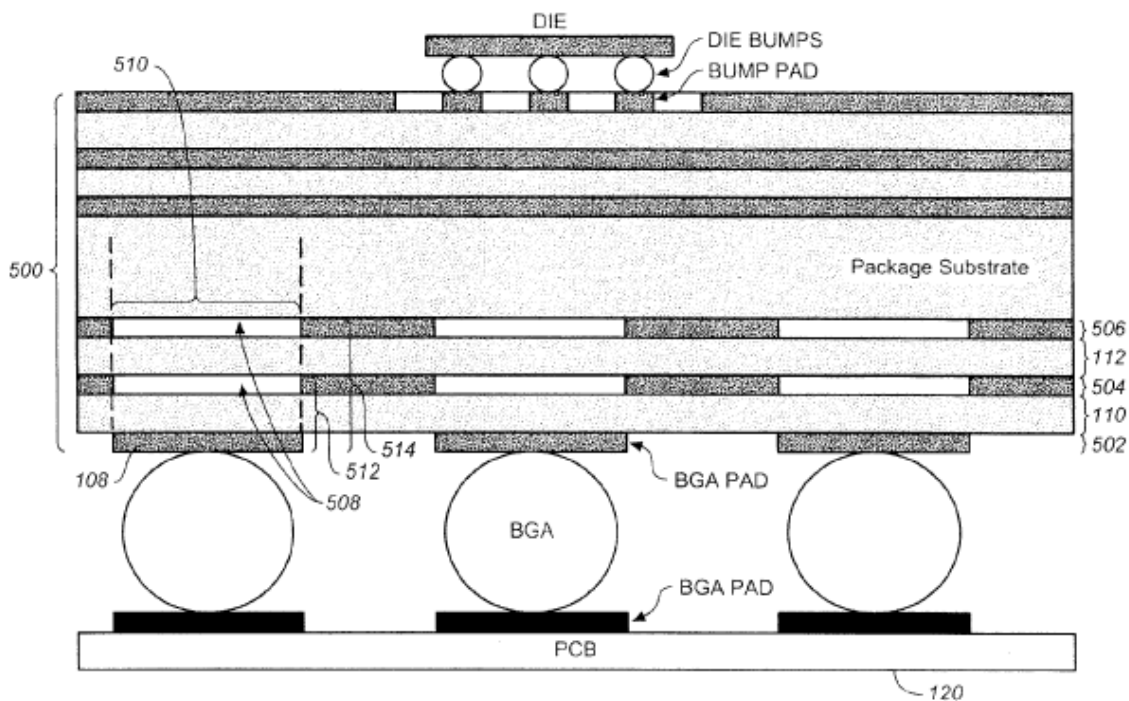
¹ On April 6, 2021, the Board terminated IPR2020-01692 and IPR2020-01693 at the request of the parties. On October 7, 2021, the Board terminated IPR2021-00147 and IPR2021-00148 at the request of the parties.

circuit package that minimizes parasitic capacitance between metal layers in a ball grid array integrated circuit package.” Ex. 1001, 1:15–20. The ’269 patent explains:

In integrated circuits such as serializer/deserializer (SERDES) devices that convert a serial data stream to or from a parallel data stream, high data transfer rates may require fast switching speeds that surpass 1 GHz. At such high frequencies, the parasitic capacitance between transmit (Tx) and receive (Rx) contact pads in the contact pad layer and nearby metal layers of the integrated circuit package may result in a deterioration of the signal waveform and a correspondingly reduced circuit performance.

Ex. 1001, 2:55–63. The ’269 patent teaches avoiding the parasitic capacitance between the contact pads and other nearby metal layers by forming “cutouts” in the metal layers to “enclose an area that surrounds each of the contact pads.” Ex. 1001, 3:62–67.

The ’269 patent illustrates one embodiment in Figure 5, reproduced below.



As shown above, Figure 5 shows a partial side view of integrated circuit package substrate 500, which includes ball pad 108, dielectric layers 110 and 112, vias² (not shown), printed circuit board 120, contact pad metal layer 502, routing metal layer 504, and ground return metal layer 506.

Ex. 1001, 4:14–23. Figure 5 also shows cutouts 508 in routing metal layer 504 and ground return metal layer 506 above ball pad 108. Ex. 1001, 4:24–28. According to the '269 patent, cutout 508 encloses cutout area 510 “so that the area enclosed by the ball pad 108 is completely surrounded by the cutout area 510,” which means that “there is no overlap between the area enclosed by the ball pad 108 and the metal in the routing metal layer 504 and in the ground return metal layer 506 above the ball pad 108.” Ex. 1001, 4:36–41, 4:56–59 (explaining that the dashed lines in Fig. 5 extending upward from the sides of contact pad 108 demonstrate how contact pad 108 encloses the areas of routing metal layer 504 and ground return metal layer that are overlapped by ball pad 108).

The '269 patent explains that parasitic capacitances 512 and 514 in Figure 5 are reduced by cutouts 508, and that “[t]he reduction in parasitic capacitance advantageously extends the upper frequency limit that may be used to drive the ball pad 108 in the integrated circuit package substrate.” Ex. 1001, 4:64–5:3 (referring to capacitances 114 and 116 in the prior art integrated circuit shown in Figure 1).

² According to the '269 patent, “[c]onnections between the electrically conductive layers, typically metal layers, are made by forming vias in the electrically insulating layers, typically dielectric layers, and depositing an electrically conductive material in the vias, such as copper.” Ex. 1001, 1:24–28.

In addition to describing an integrated circuit package substrate that avoids parasitic capacitance, the '269 patent also discloses a method of avoiding parasitic capacitance in an integrated circuit package substrate that includes forming electrically conductive layers separated from each other by electrically insulating layers, forming a contact pad in the first electrically conductive layer, and forming cutouts in the additional electrically conductive layers. Ex. 1001, 5:54–6:26, Fig. 9.

C. Challenged Claims

Petitioner challenges claims 1–20 of the '269 patent. Claims 1 and 10 are the only independent claims. Independent claim 1 is illustrative, and is reproduced below.

1. A method, comprising steps of:
forming a first electrically conductive layer including a plurality of rows of contact pads;
forming an electrically insulating layer on the first electrically conductive layer; and
forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

Ex. 1001, 6:39–55.

D. Reviewed Unpatentability Challenges

We review the following challenges from the Petition:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3–20	103	Chin ³
5, 8, 14–16, 19	103	Chin, HighSpeed ⁴
2	103	Chin, MC92600 ⁵
2	103	Chin, Shafer ⁶
3	103	Chin, Oggioni ⁷

Petitioner relies on the declaration of David Choi, Ph.D. (Ex. 1003). Patent Owner deposed Dr. Choi, and filed the transcript of the deposition as Exhibits 2031 and 2032 in this proceeding.

Patent Owner relies on the declaration of Charles E. Bauer, Ph.D. (Ex. 2030). Petitioner deposed Dr. Bauer, and filed the transcript of the deposition as Exhibit 1110 in this proceeding.

III. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l*

³ US 6,765,298 B2, issued July 20, 2004 (Ex. 1004).

⁴ Stephen H. Hall, et. al., *High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices*, Copyright 2000 by John Wiley & Sons, Inc. (Ex. 1009).

⁵ Motorola, MC92600 Quad 1.25 Gbaud SERDES User’s Manual, Mar. 2003, Rev. 2 (Ex. 1008).

⁶ US 6,908,340 B1, issued June 21, 2005 (Ex. 1026).

⁷ US 6,717,255 B2, issued Apr. 6, 2004 (Ex. 1006).

Graphics, Inc., 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). “This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR*, 550 U.S. at 418–419.

On the other hand, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, a

⁸ The parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, a petitioner must articulate a reason why a person of ordinary skill in the art would have combined or modified the prior art references. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination.”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”) (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art would have possessed “a bachelor’s degree in electrical engineering or a related field as well as at least four years of experience in high-frequency circuit engineering and development.” Pet. 3 (citing Ex. 1003 ¶¶ 26–27). For purposes of the Institution Decision, we adopted Petitioner’s proposal (Inst. Dec. 17–18), and neither party addresses the level of ordinary skill in the post-institution briefs (*see generally* PO Resp.; Reply; Sur-reply).

In this Decision, we again adopt the level of ordinary skill proposed by Petitioner. This level of skill is consistent with the Specification of the '269 patent and the asserted prior art, and it is supported by the testimony of Dr. Choi. *Accord* Inst. Dec. 17–18.

C. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). Under the principles set forth by our reviewing court, the “words of a claim ‘are generally given their ordinary and customary meaning,’” as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

In the Petition, Petitioner does not offer specific constructions for any claim terms, and instead contends the claim terms should be given their plain and ordinary meaning. Pet. 16. In the Patent Owner Response, Patent Owner offers a construction for the term “contact pads” in independent claims 1 and 10. PO Resp. 9–12. Patent Owner also provides a discussion of the claim phrase “vias connecting the contact pads with one of the electrically conductive layers” in dependent claims 14–16 and 19. PO Resp. 12–13.

1. “contact pads”

Patent Owner argues that “the term ‘contact pads’ refers to the pads on an integrated circuit package substrate for connecting with a printed circuit board.” PO Resp. 9–12; Sur-reply 1–2. Petitioner disagrees. Reply 6. But, because we find that Petitioner has shown that Chin suggests

implementing its invention in an IC⁹ package substrate as Patent Owner’s proposed construction would require (*infra* § III.D.2.), we need not resolve this dispute. See *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

However, if we needed to substantively address this dispute, we would reject Patent Owner’s proposed construction. Patent Owner advocates limiting the scope of this claim term to include only the contact pads in a particular location (i.e., the PCB-side of the IC package substrate),¹⁰ but the intrinsic record does not support importing such a limitation into the claim. Patent Owner identifies (and we perceive) no passage in the intrinsic record that redefines the term “contact pads” or disavows part of its scope. See *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365, 1367 (Fed. Cir. 2012) (explaining that a term should be given its plain and ordinary meaning unless a patentee acted as his own lexicographer or disavowed claim scope). Rather, Patent Owner’s argument is that the term should be limited because the Specification only discusses “contact pads” in that location and does not apply its invention to other pads

⁹ We follow the parties’ use of IC as an abbreviation for “integrated circuit.” Similarly, we use PCB as an abbreviation for “printed circuit board,” and use BGA as an abbreviation for “ball grid array.”

¹⁰ The testimony of Patent Owner’s declarant, Dr. Bauer, confirms that the term “contact pads” has a plain and ordinary meaning that includes pads located on an IC package substrate as well as those located on a PCB or an IC. Ex. 1110, 143:21–144:1 (agreeing Chin’s PCB includes a “contact pad”); Ex. 2030 ¶ 46 (referencing “contact pads (I/O) on the ICs”).

shown in its figures. *See* PO Resp. 10–12; Sur-reply 1–2. But claims are not limited to the embodiments disclosed. *See Phillips*, 415 F.3d at 1323. Moreover, as Petitioner points out, claim 9 expressly requires connecting the first electrically conductive layer to a printed circuit board, whereas claim 1 does not. Reply 6; Ex. 1001, 6:39–55, 7:42–44.

2. *“vias connecting the contact pads with one of the electrically conductive layers”*

In its discussion of this claim phrase, Patent Owner directs us to the language in the '269 patent explaining that vias are holes filled with an electrically conductive material used to make connections between contact pad metal layer 102, routing metal layer 104, and ground return metal layer 106. PO Resp. 12 (quoting Ex. 1001, 3:9–16). Patent Owner then argues that “when it comes to connecting the ball pads 108 specifically to a trace in an upper metal layer, [the '269 patent] describes that with respect to the via-in-pad 118.” PO Resp. 13. Patent Owner cites to portions of the '269 patent in support of this statement, but, as Petitioner points out, none of those portions of the '269 patent refer to a “via-in-pad.” Reply 7; *see, e.g.*, Ex. 1001, 3:42–43 (“In FIG. 3, the vias 118 connect the ball pads 108 in the contact pad metal layer 102 in FIG. 1 to the routing traces 302.”). Petitioner also argues that Patent Owner fails to ask for a specific construction of this claim phrase.

In its Sur-reply Patent Owner states that “the plain language dictates that what to be connected [sic] are an electrically conductive layer and the previously recited transmit and receive rows of contact pads with associated contacts.” Sur-reply 2–3.

We agree with Patent Owner’s ultimate assertion that the plain language of the claim is informative of its proper meaning, such that “vias connecting the contact pads with one of the electrically conductive layers” means that vias are used to connect the recited contact pads with an electrically conductive layer. *See Phillips*, 415 F.3d at 1312.

After considering the parties’ arguments, we determine that no other claim terms require an express construction. *See Nidec*, 868 F.3d at 1017.

D. Claims 1 and 3–20 — Obviousness in view of Chin

Petitioner contends claims 1 and 3–20 are unpatentable as obvious in view of Chin. Pet. 20–71. Patent Owner disagrees, arguing, *inter alia*, that an ordinary artisan would not have extended Chin’s design to IC package substrates. PO Resp. 13–24.

We begin with a discussion of Chin, followed by our analysis of the claims.¹¹

1. Chin (Ex. 1004)

Chin is directed to “the design and fabrication of printed circuits and multi-layered substrates that are suitable for carrying signals with very high data rates,” and relates to “techniques to reduce landing pad parasitic

¹¹ The parties raised untimely, new arguments in the Reply, Sur-reply, and during the oral hearing, and such arguments are forfeited. *See* 37 C.F.R. § 42.23(b) (limiting scope of replies and sur-replies); Paper 13 (Scheduling Order), 8 (cautioning Patent Owner that “any arguments not raised in the response may be deemed waived”); Tr. 4:16–18 (instructing parties to limit oral hearing presentation to arguments in the briefs); *see also* Consolidated Trial Practice Guide (“CTPG”) 73–74, 85–86 (Nov. 2019), *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>. We have identified these arguments below when they are relevant to our analysis. Nevertheless, even if the parties had presented these arguments in a timely manner, they would not change the outcome here, as discussed below.

components and reduce the impedance discontinuity between the pad and the interconnect to the pad.” Ex. 1004, 1:7–13. Chin explains that “the impedance of the landing pads is generally significantly lower than that of their associated interconnect conductors,” and “[t]he substantial impedance drop of the pad causes excess parasitic capacitance, which results in a reduction in bandwidth and slowing the signal transition rate.” Ex. 1004, 1:46–48, 2:2–5. In view of this, Chin aims to “decrease the parasitic capacitance of substrate landing pads and to provide better impedance matching between the traces and the landing pads.” Ex. 1004, 2:20–23.

According to Chin, “[a] landing pad’s parasitic capacitance may be reduced by forming patterned holes in one or more reference potential layers below the landing pad,” and “[r]educing the landing pad’s parasitic capacitance creates a corresponding increase in the landing pad’s impedance.” Ex. 1004, 3:45–49. “A pre-determined amount of capacitance is then re-introduced to the landing pad” with compensation capacitors in order “to lower the pad’s characteristic impedance to match that of the trace.” Ex. 1004, 3:55–65.

Chin discloses several embodiments of printed circuit boards that include metal layers separated by dielectric material, with patterned holes formed in the metal layers. One embodiment is shown in Figure 2a, reproduced below.

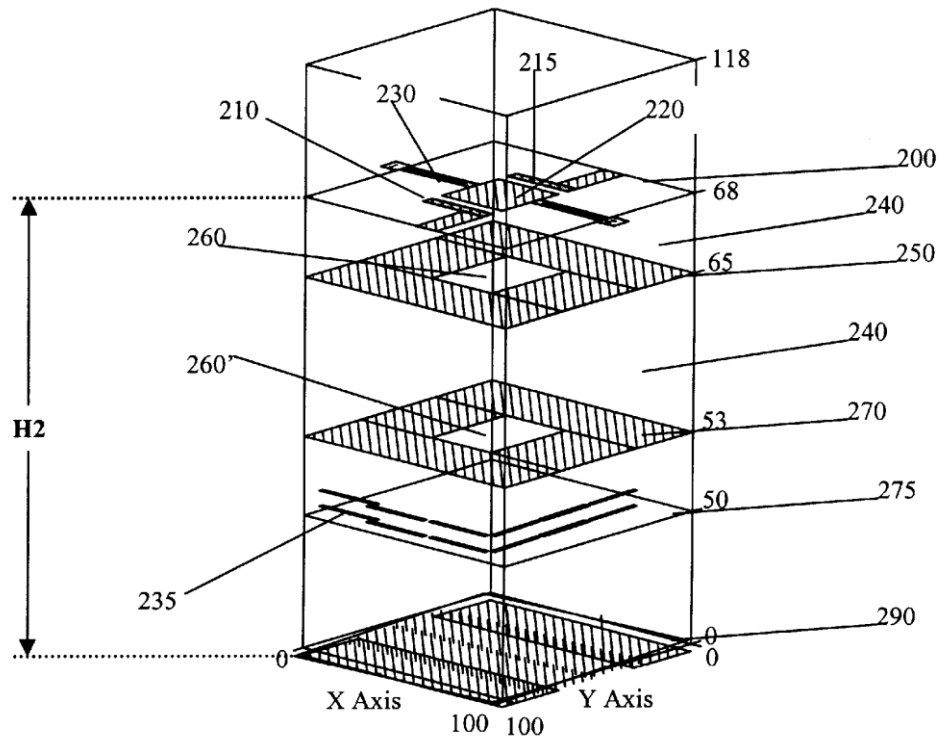


Figure 2a of Chin is an exploded isometric drawing of a segment of a printed circuit board. Ex. 1004, 4:4–5. The printed circuit board segment in Figure 2a includes compensation capacitors 210 and 215, pad 220, and single trace 230 on surface metal layer 200; intermediate metal layers 250, 270, and 275; patterned holes 260 and 260' in layers 250 and 270, respectively; and ground reference layer 290. Ex. 1004, 4:4–25, 4:48–50.

2. Claim 1

Claim 1 recites “[a] method, comprising steps of: forming a first electrically conductive layer including a plurality of rows of contact pads.” Ex. 1001, 6:39–41.

Petitioner characterizes the challenged claims of the '269 patent as “method claims relating generally to ‘the design of an integrated circuit package,’” and notes that each claim “recites ‘forming’ one or more structures that are part of an IC package.” Pet. 22 (citing Ex. 1001, 6:39–

8:45). Petitioner acknowledges that Chin’s specific descriptions are directed to forming printed circuit board embodiments, but asserts that Chin explains that “the concepts apply equally to an integrated circuit package.” Pet. 22. In support of this position, Petitioner notes that “Chin discloses ‘fabrication of printed circuits and multi-layered substrates’ (Ex. 1004, 1:8) and ‘methods of implementing’ these structures (*Id.*, 5:54-59), including ‘form[ing]’ alternating layers of metal and dielectric (*Id.*, 1:22-24).” Pet. 22 (alteration in original). Petitioner also directs us to the portion of Chin stating that “[h]aving fully described several embodiments and applications of the present invention, other **equivalent or alternative methods** of implementing printed circuit pad compensation according to the present invention will be apparent to those skilled in the art.” Pet. 22–23 (quoting Ex. 1004, 5:54–59). In view of this, Petitioner contends Chin relates broadly to semiconductor circuits and multilayer structures, and methods of fabricating those structures. Pet. 23 (citing Ex. 1003 ¶ 78).

Petitioner contends that surface metal layer 200 in Chin Figure 2 corresponds to the first electrically conductive layer recited in claim 1, noting that Chin states that “[l]ayer 200 is the surface metal layer where a component lead is electrically bonded to pad 220 and interconnected with other components by trace 230.” Pet. 23 (quoting Ex. 1004, 4:10–12). Petitioner further contends that Chin teaches “a substrate used inside a BGA package,” and that “BGA” means ball grid array. Pet. 24 (citing Ex. 1004 1:57, 1:61–62). Petitioner argues that a person of ordinary skill in the art would know that a BGA package is necessarily comprised of a plurality of rows of contact pads. Pet. 24 (citing Ex. 1003 ¶ 80; Ex. 1001, 2:64–66, 3:31–33, 3:35–36).

Claim 1 next recites “forming an electrically insulating layer on the first electrically conductive layer.” Ex. 1001, 6:42–43. For this limitation, Petitioner directs us to dielectric material 240 in Chin Figure 2a, which is formed on layer 200. Pet. 25–26 (citing Ex. 1004, 1:22–24). Petitioner argues that even though Figure 2a shows dielectric layer 240 below first layer 200, Chin teaches that landing pads can be “formed on the bottom PCB surface,” in which case Figure 2a would be flipped upside down. Pet. 26 (citing Ex. 1004, 5:62–65, Figure 2a).

Claim 1 further recites “forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers.” Ex. 1001, 6:44–47. Petitioner contends that layer 250 in Chin Figure 2a corresponds to the second electrically conductive layer, and that, as shown in the figure, there is no intermediate conductive layer between first layer 200 and second layer 250. Pet. 27–28 (citing Ex. 1004, 4:12–14, Fig. 2a). Rather, Petitioner submits that layers 200 and 250 are separated by insulating dielectric layer 240. Pet. 27.

Claim 1 additionally requires “the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer.” Ex. 1001, 6:47–51. Petitioner contends that patterned hole 260 in second metal layer 250 of Chin Figure 2a corresponds to the recited cutout. Pet. 28–29. According to Petitioner, because layer 250 is sandwiched between two dielectric (insulating) layers, removing metal in layer 250 to form hole 260 leaves only dielectric material, which creates an electrical insulating area enclosed by the cutout. Pet. 28 (citing Ex. 1003 ¶ 87). Petitioner further contends that Chin discloses a plurality of cutouts because

Chin states that the Figure 2a pad and patterned holes can be used in BGA applications. Pet. 29.

Lastly, claim 1 requires that “each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.” Ex. 1001, 6:51–55. Petitioner contends that Chin discloses this limitation based on its disclosure that “[t]he reference potential plane has an opening directly under or above the pad and is larger than the pad” and “the area of said patterned hole is larger than the area of said selected pad.” Pet. 30 (quoting Ex. 1004, 2:40–42, 6:36–37) (alteration in original).

Patent Owner argues that the claimed “contact pads” refer to pads in an IC substrate (PO Resp. 9), and Petitioner relies entirely on Chin’s disclosures regarding PCBs, which are not IC substrates, in its analysis. PO Resp. 13–14. Patent Owner contends that contrary to Petitioner’s assertions otherwise, Chin does not expressly disclose using a BGA substrate, which is an IC substrate. PO Resp. 14. According to Patent Owner, a person of ordinary skill in the art would not have extended Chin’s design to IC package substrates as evidenced by Petitioner’s failure to establish a motivation to apply Chin’s device to a BGA package. PO Resp. 14–20. Patent Owner does not dispute Petitioner’s arguments or evidence regarding Chin’s disclosure of any other limitation in claim 1.

After considering the parties’ arguments and evidence, we are persuaded by Petitioner’s arguments and evidence that Chin teaches or suggests the method steps recited in claim 1.

Although we recognize that much of Chin, including the specific embodiments disclosed therein, refers specifically to printed circuit boards,

we agree with Petitioner that Chin explains that its “concepts apply equally to an integrated circuit package substrate.” Pet. 22. In particular, we find that Chin discloses an IC package substrate. See Ex. 1004, 1:61–62 (referring to “a substrate used inside a BGA package”); see also Ex. 1003 ¶¶ 28–30 (Dr. Choi explaining that a BGA is a type of IC package). We credit Dr. Choi’s testimony on this point because it is logical and supported by cited evidence. See, e.g., Ex. 1014, 45;¹² Ex. 1016, 5–7.

We are also persuaded that Chin expressly suggests implementing its invention in an IC package substrate. Chin begins its description by stating that “[t]he present invention relates generally to the design and fabrication of printed circuits *and multi-layered substrates*.” Ex. 1004, 1:7–8 (emphasis added). Chin also states that its invention “is illustrated by way of example, and not by way of limitation,” in its figures. Ex. 1004, 3:26–27. Similarly, Chin’s final paragraph states that alternative implementations “will be apparent to those skilled in the art,” and it states that “semiconductor implementations . . . are contemplated as within the scope of the present invention” as they use “similar layered printed circuit routing techniques.” Ex. 1004, 5:54–6:10. Moreover, as background for its invention, Chin addresses problems encountered as signal speed increases and explains that “excess parasitics that limit the bandwidth” are caused by an impedance mismatch between landing pads and their associated interconnect conductors. Ex. 1004, 1:35–56. Chin then states:

One example is the use of a ball-grid-array (BGA) package in a multi-gigahertz printed circuit board. The landing pads of current state of the art BGAs are typically 25–30 mils in

¹² Unless otherwise noted, our citations refer to page numbers added to an exhibit by Petitioner or Patent Owner rather than the document’s native page numbers.

diameter, which is significantly larger than the typically 5 mil microstrips used in interconnecting conductors. *Another example is a substrate used inside a BGA package.* Typical solder ball landing pad sizes for current technology BGA substrates are on the order of 20–25 mil, significantly larger than the typically 3 mil traces used in microstrip interconnects.

Ex. 1004, 1:56–65 (emphasis added). Accordingly, given the context provided by Chin (*see* Ex. 1004, 1:7–8, 5:54–6:10), we find that a person of ordinary skill in the art would have understood this passage (*see* Ex. 1004, 1:61–65) to suggest applying Chin’s disclosure to an IC package substrate. *Accord* Inst. Dec. 23–24.

Patent Owner’s arguments to the contrary are unavailing. *See* PO Resp. 14–20; Sur-reply 6–14. Patent Owner provides no alternative understanding of the salient passage of Chin (*cf.* PO Resp. 17, 19), and it does not argue that an ordinary artisan would have been discouraged from following Chin’s suggestion. *See* Sur-reply 8. Instead, Patent Owner contends that “despite the statement in Chin 1:60–65, there is no evidence that at the time of the invention, a [person of ordinary skill in the art] would have used such a design in IC package substrates, especially for high-frequency applications that allegedly would have benefited from Chin’s design.” PO Resp. 19. There are several flaws with this argument (which we address below), but most importantly, it appears to be premised on the erroneous assumption that Chin’s disclosure does not provide the requisite motivation.¹³ As a result, the argument is inapposite because, as explained

¹³ *See, e.g.*, PO Resp. 17 (“To establish a motivation to apply Chin’s design concepts to the BGA package(s) the Petition relies on, the Petition must, but does not, show that the BGA packages relied on by Petitioner would have benefited from Chin’s designs.”); Sur-reply 7 (arguing that “even if a [person of ordinary skill in the art] *could* apply Chin’s method to more than

above, we find that Chin itself suggests its concepts apply to IC package substrates.

Nevertheless, we have considered Patent Owner’s arguments and evidence and weighed them against Chin’s disclosure, but ultimately we credit Chin’s statements over Patent Owner’s arguments and evidence. Patent Owner presents arguments regarding Chin’s microstrips (*see* PO Resp. 17–19) and Chin’s compensation capacitors (*see* PO Resp. 19–20). We address these in turn.

As for the microstrips, Patent Owner’s Response assumes (without explanation) that any implementation of Chin would necessarily include Chin’s microstrips; however, we do not assume that microstrips are required simply because Chin’s preferred embodiment includes microstrips. *See KSR*, 550 U.S. at 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”); *In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) (“[W]e do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art.”); *see also Lear Siegler Inc. v. Aeroquip Corp.*, 733 F.2d 881, 889 (Fed. Cir. 1984) (The ordinary artisan is not “compelled to adopt every single aspect of [a reference’s] teaching without the exercise of independent judgment.”). In addition, Chin’s claims indicate that a microstrip is *not* a necessary part of its invention. *See, e.g.*, Ex. 1004, 6:12–8:13 (most claims include no such requirement). *But see* Ex. 1004, 6:57–64 (dependent claim 6 requires “interconnect lines” in the pad layer), 8:8–13

PCBs, that does not mean that they *would* have done so”), 9 (“Petitioner has not presented sufficient evidence that a [person of ordinary skill in the art] would have considered the BGA pads had the impedance mismatch problem to apply Chin’s method.”).

(dependent claim 13 requires “traces extending from” the contact pads). Consequently, even if Patent Owner were correct that an ordinary artisan would not have included microstrips coupled to the pads in a BGA package substrate, then we would determine that an ordinary artisan would not have included that aspect of Chin when adapting its invention to a BGA package substrate. See Reply 13–14.

In its Sur-reply, Patent Owner also argues that “if no surface transmission lines (microstrips) existed, then there would be no impedance mismatch or the need for Chin’s modification at all.” Sur-reply 12–13. To the extent Patent Owner advances this as a justification for its assumption that Chin’s microstrips are required, this argument is untimely because it was not raised in Patent Owner’s Response and is not fairly responsive to Petitioner’s Reply. See PO Resp. 16–18; Reply 14–15; *supra* n.11. But, even if this argument had been properly raised, Patent Owner does not sufficiently explain why an ordinary artisan would have understood Chin’s disclosure to only be applicable for impedance matching between a microstrip and a pad. See Sur-reply 12–13 (citing Ex. 2030, 91 n.12); *see also* Sur-reply 7 (citing Ex. 2031, 45:17–46:23), 8–9 (citing Ex. 1110, 115:13–116:1). In particular, Patent Owner cites testimony regarding transmission lines, but even assuming *arguendo* that Chin requires a transmission line,¹⁴ we cannot agree that it requires a microstrip. Patent

¹⁴ Incidentally, we cannot agree that Chin requires a transmission line. Chin describes matching the impedance between an interconnecting conductor and a pad (Ex. 1004, 2:2–19), but Chin’s disclosure does not state that it is limited to the situation where that interconnecting conductor is a transmission line (Ex. 1004, 1:39–43 (explaining that interconnecting conductor and adjacent reference plane for a transmission line with a predetermined impedance)). *Cf.* Sur-reply 9 (arguing that “Chin’s method

Owner’s evidence shows that a microstrip is one type (but not the only type) of transmission line, and Patent Owner fails to sufficiently explain why this specific type of transmission line is allegedly required by Chin. See Ex. 2031, 45:17–46:23; see also Ex. 2030 ¶¶ 96 (“A transmission line is a signal trace with a controlled impedance.”), 97 (identifying microstrips, striplines, and coplanar wave guides as types of transmission lines). In addition, to the degree Patent Owner argues that Chin should be ignored because its purpose is different than the ’269 patent’s purpose, this argument is inapposite. See *KSR*, 550 U.S. at 420–421 (explaining that an ordinary artisan would not ignore a reference simply because its “primary purpose” was different).

As for the compensation capacitors, Patent Owner contends that Chin would not have been implemented in a BGA substrate because Chin’s compensation capacitors would not have fit (see PO Resp. 19–20; Sur-reply 12–14); however, Chin states that its invention is applicable in BGA substrates as well as larger-scale devices (i.e., PCBs) and smaller-scale devices (i.e., semiconductor applications). Ex. 1004, 1:56–65, 5:67–6:7; see Ex. 2030 ¶ 16 (identifying geometries of ICs, IC packages, and PCBs). Although Patent Owner relies on Dr. Bauer’s testimony to support its

stemmed from the need to match the impedance at the pad *with the impedance of a signal line (typically a transmission line in PCBs due to signal lengths) . . .*” (emphasis added)). Dr. Bauer testifies that an ordinary artisan would not have applied Chin’s method when “impedance and capacitance are not of concern” (Ex. 2030, 91 n.12), but does not testify that Chin requires a transmission line. Moreover, Dr. Bauer’s other testimony indicates that impedance was, in fact, a concern at the interface between the PCB and the IC package. See Ex. 2030 ¶¶ 104 (testifying that impedance is controlled “at the interface(s) to the next packaging level or device”); see also *id.* ¶ 24 (explaining packaging levels).

contention (*see* PO Resp. 19–20), we assign little weight to that testimony because Dr. Bauer fails to provide sufficient analysis or evidence on these specific points (*see* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”)). In particular, Dr. Bauer testifies that “there is simply not enough substrate area” to include Chin’s compensation capacitors on an IC package substrate due to “wiring line and space requirements” (Ex. 2030 ¶ 71), and because “IC package substrates tended to use SMD [(solder mask defined)] BGA ball pads” that “tend to be larger than NSMD PCB landing pads (the type frequently used on PCBs)” (Ex. 2030 ¶ 71 n.7; *see also* Ex. 2030 ¶ 143). This explanation is insufficient for three reasons.

First, Dr. Bauer fails to connect the dots between the BGA substrate’s “wiring line and space requirements” and his conclusion that “there is simply not enough substrate area” on the pad layer for Chin’s compensation capacitors. *See* Ex. 2030 ¶ 71 & n.7; *see also* Ex. 2030 ¶¶ 69–70 (explaining that wiring line widths and spaces are different in BGA substrates and PCBs and require different manufacturing techniques). Although we agree that PCBs have different wiring line and spacing requirements than IC substrates, we cannot find that this difference would prevent inclusion of compensation capacitors in the latter. Dr. Bauer’s testimony could be read to suggest that the problem lies in the fact that different manufacturing processes are used for PCBs and BGA substrates (*see* Ex. 2030 ¶ 70), but this is insufficiently explained.¹⁵

¹⁵ There is insufficient evidence on this record suggesting that the manufacturing techniques used at the time would prevent inclusion of Chin’s compensation capacitors in a BGA substrate. Chin’s compensation

Second, Dr. Bauer fails to sufficiently explain why the alleged size differences between the PCB pads and the BGA substrate pads would have had a material effect on a designer's ability to fit compensation capacitors. *See* Ex. 2030 ¶ 71 n.7. In fact, at deposition, Dr. Bauer testified that the differences in pad sizes between PCBs and IC package substrates are "relatively immaterial." Ex. 1110, 88:20–89:13; *see also* Ex. 2019, 17–18 (illustrating the benefit of using PCB and BGA pads that are similarly sized). Also, Chin's disclosure contradicts Dr. Bauer's testimony by instead stating that BGA substrate pads are slightly *smaller* than PCB pads. *See* Ex. 1004, 1:58–65 (20–25 mils versus 25–30 mils). Moreover, Dr. Bauer does not testify that an ordinary artisan would not have used the larger NSMD landing pads on a BGA package, but rather that the smaller SMD pads were more common. Ex. 2030 ¶ 71 n.7.

Third, Dr. Bauer fails to reconcile his conclusions with Chin's disclosure of a BGA substrate example. *See* Ex. 1004, 1:56–65.

Ultimately, we credit Chin's statements (which suggest applying Chin's invention in an IC package substrate) over Patent Owner's evidence (which does not squarely contradict those statements, as explained above). Consequently, we disagree with Patent Owner's argument that an ordinary artisan would not have been motivated to include Chin's invention in a BGA substrate.

Finally, we address Patent Owner's argument that Petitioner fails to sufficiently show a rationale to include Chin's invention on the correct side of the IC package substrate. *See* Tr. 67:2–73:2, 96:11–100:10; PO Resp. 15.

capacitors are simply metal strips in the pad layer (*see* Ex. 1004, 4:26–38), not standalone capacitors that are mounted on a PCB (*cf.* Ex. 2030 ¶ 19).

To the extent this is not a new, untimely argument, we disagree with Patent Owner’s argument because, as explained above, we find that an ordinary artisan would understand the salient passage of Chin to expressly suggest applying its invention to the PCB-side of the BGA substrate. *See* Ex. 1004, 1:61–65 (identifying pads “on the order of 20–25 mil”);¹⁶ *see also* Ex. 2030 ¶¶ 30 (testifying that “the BGA ball pads on a BGA package substrate for connecting with a PCB generally used a pitch of .65–1.0 millimeters [(i.e., 25–39 mils)]”), 37 (testifying that BGA balls were typically 375–600 microns in diameter (i.e., 14.8–23.6 mils), where bump pads were 95–115 microns (i.e., 3.7–4.5 mils) in diameter (*cited in* Sur-reply 9)). During the hearing, Patent Owner argued that Dr. Bauer testified that Chin’s microstrips would have meant that Chin would be implemented on the IC-side of the substrate (Tr. 100:14–101:2); however, Patent Owner’s assertion is not supported by the evidence it cites (*see* Ex. 2030 ¶¶ 142–154). Dr. Bauer testifies that the IC-side of the BGA substrate included the majority of the routing, but does not sufficiently explain why this would have affected an ordinary artisan’s implementation of Chin. Ex. 2030 ¶¶ 152–154.

Patent Owner’s other arguments are inapposite. Patent Owner disputes Petitioner’s contention that parasitic capacitance was a known problem with known solutions (PO Resp. 20–24 (citing Pet. 11–13)), but we do not rely upon that contention. Patent Owner also disputes Petitioner’s contention that the similarities between PCBs and IC packages would

¹⁶ During the oral hearing, Patent Owner argued that Petitioner’s identification of this passage during its rebuttal presentation was procedurally improper. Tr. 98:5–10 (referencing Tr. 93:5–21). We disagree. At a minimum, we did not discern this argument from Patent Owner’s briefs and, thus, cannot fault Petitioner for not responding to it earlier.

motivate an ordinary artisan to apply Chin to an IC package substrate (PO Resp. 14–16 (citing Pet. 22)), but we also do not rely upon that contention. Similarly, we do not rely on the parties’ subsequent debate on these topics.¹⁷ See Reply 9–11, 15–16; Sur-reply 8–10, 15. Finally, we do not address Patent Owner’s allegation that Petitioner’s Reply includes new arguments (Sur-reply 11–13 (citing Pet. Reply 11–13)) because we do not reach those arguments.

In view of the foregoing, we are persuaded by Petitioner’s argument that a person of ordinary skill in the art would have understood Chin’s disclosure to relate to more than just the formation of printed circuit boards, and would include other multi-layered substrates, such as an integrated circuit package substrate. Pet. 22–23; see *In re Wesslau*, 353 F.2d 238, 241 (CCPA 1965) (holding that a reference should be considered in its entirety for what it fairly teaches one skilled in the art).

We are also persuaded by Petitioner’s arguments and evidence that Chin teaches or suggests the specific limitations in claim 1, including forming a first electrically conductive layer including a plurality of rows of contact pads (depicted as layer 200 and pad 220 in Chin Figure 2a), forming an electrically insulating layer on the first conductive layer (depicted as layer 240 in Figure 2a), and forming a second electrically conducting layer over the electrically insulating layer having a plurality of cutouts that enclose an

¹⁷ We note that these arguments stray from the salient issues. For example, Patent Owner argues that a person of ordinary skill in the art would not have been motivated to apply Chin to the “bump pads” of an IC package (PO Sur-reply 9) in response to Petitioner’s statement that Chin could apply “within an IC, within an IC substrate, and within a PCB” (Pet. Reply 9). However, the “bump pads” referenced by Patent Owner are not the pads at issue. See, e.g., Ex. 1001, Fig. 1 (showing “bump pads” on the *IC-side* of the substrate).

electrically insulating area, wherein each electrically insulating area completely overlaps a corresponding contact pad (depicted as patterned hole 260 in layer 250 in Figure 2a). Pet. 22–30; Ex. 1004, 1:22–24, 1:61–62, 2:40–42, 3:49–56, 4:9–14, 4:61–64, 5:62–65, 6:36–37, 6:40–41, 8:5–7.

Patent Owner does not dispute the specific teachings of Chin Petitioner relies upon. As such, we consider Chin’s teachings regarding the formation of a first electrically conductive layer with a landing pad, a first insulating layer, and a second electrically conductive layer with cutouts of a particular size and configuration, in general, to be undisputed.

For the reasons provided above, we are persuaded that Chin teaches or suggests each limitation of independent claim 1. We are also persuaded that a person of ordinary skill in the art would have been motivated to modify Chin’s disclosure to yield the subject matter of claim 1. Accordingly, we determine Petitioner has established by a preponderance of evidence that claim 1 is unpatentable as obvious in view of Chin.

3. *Claim 10*

Independent claim 10 contains limitations similar to those in claim 1, with the main difference being that claim 10 requires a plurality of electrically conductive layers proximate to the first electrically conductive layer, wherein each of the electrically conductive layers includes “a plurality of electrically insulating areas such that there is substantially no overlap of the rows of contact pads with metal in the plurality of electrically conductive layers.” Ex. 1001, 7:45–8:10. Petitioner directs us to portions of Chin disclosing all of the limitations recited in claim 10, often relying on the same portions of Chin it relies on for its challenge of claim 1. Pet. 59–62. Patent Owner does not separately address claim 10.

We have reviewed the information and arguments Petitioner provides, including the relevant portions of Chin and Dr. Choi's declaration, and are persuaded, based on the arguments and evidence presented in the Petition and Dr. Choi's declaration, that Petitioner has established by a preponderance of the evidence that claim 10 is unpatentable as obvious in view of Chin. Pet. 59–62; Ex. 1004, Fig. 2a, 1:22–34, 4:10–11; Ex. 1003 ¶¶ 142–147.

4. *Claims 4, 7, 9, 11–13, 17, 18, and 20*

Claims 4, 7, and 9 depend from claim 1, and claims 11–13, 17, 18, and 20 depend directly or indirectly from claim 10. Petitioner directs us to portions of Chin disclosing all of the limitations recited in claims 4, 7, 9, 11–13, 17, 18, and 20. Pet. 31–36, 49–59, 62–66, 70–71. Patent Owner does not separately address these claims.

We have reviewed the information and arguments Petitioner provides, including the relevant portions of Chin and Dr. Choi's declaration, and are persuaded, based on the undisputed arguments and evidence presented in the Petition and Dr. Choi's declaration, that Petitioner has established by a preponderance of the evidence that claims 4, 7, 9, 11–13, 17, 18, and 20 are unpatentable as obvious in view of Chin. Pet. 31–71; Ex. 1003 ¶¶ 92–99, 122–130, 134–141, 149–155, 163–164, 168; Ex. 1004, Fig. 2a, 1:7–10, 1:17–20, 1:61–62, 12:40–42, 2:40–41, 2:64–66, 3:49–56, 4:4–26, 4:61–62, 5:62–69, 6:1–10, 6:35–37, 7:3–5, 8:6–7.

5. *Claims 2, 5, 6, and 8*

Claims 2, 5, 6, and 8, depend directly or indirectly from claim 1 and require, *inter alia*, forming the second electrically conductive layer as a routing layer. Ex. 1001, 6:56–65, 7:12–22; 7:39–41. Petitioner notes that because these claims depend from claim 1, the routing layer “must be

formed ‘such that there is no intermediate conductive layer between the first and second . . . layers.’” Pet. 39 (providing the analysis for claim 5); *see also* Pet. 47, 56, 80, and 86 (referring back to the analysis of claim 5 for each of claims 6, 8, and 2, respectively). In this Decision, we refer to this required positioning of the routing metal layer as the “routing placement limitation.”

In the Petition, Petitioner contends “routing metal layer 275” in Chin corresponds to the routing metal layer recited in the claims of the ’269 patent, and argues that Chin renders obvious the routing placement limitation in claims 2, 5, 6, and 8. Pet. 39–47 (citing Ex. 1004, 2:52–53, 4:15–20, 4:23–24, 4:29–32, 5:3–9, Fig. 2a; Ex. 1003 ¶¶ 104–117; Ex. 1009, 94 (Fig. 5.1)), 56, 72–73, 80, 86. Specifically, Petitioner states:

Chin teaches: “Metal layer 275 . . . represents **any intermediate routing layer** with traces 235.” . . . In other words, Chin teaches that a routing layer with traces (e.g., traces 235) could be placed interchangeably with, for example, a second conductive layer such as 250, in Figure 2a

Alternatively, a [person of ordinary skill in the art] would have found it obvious, and likely necessary, to modify the layer order of Chin Figure 2a to place the routing metal layer 275 below the contact pad layer 200 (first metal layer) because common BGA designs must route hundreds of signals between contact pads of the BGA substrate and integrated circuit contacts within the package. A [person of ordinary skill in the art] would also have understood that the ordering of layers in the substrate needed to be flexible to accommodate the many signal lines present in a BGA package The placement of a routing layer next to the contact pad layer is a design choice that a [person of ordinary skill in the art] was capable of making.

Pet. 39–41 (citing Ex. 1003 ¶ 106; Ex. 1004, 4:23–24, Fig. 2a); *see also* Reply 27 (again stating that the “large number of signals to be routed

through the substrate would require routing signals in the layer immediately adjacent to the contact pad layer”).

Petitioner also contends that HighSpeed discloses a “prior art arrangement of metal layers with a routing trace on layer 2 immediately adjacent to the contact on layer 1,” and is evidence that a person of ordinary skill in the art would have been aware of “the design choice of putting a routing layer next to the contact layer, of the predictability of that design choice, and of the expectation of the success of that design choice.” Pet. 41–42 (citing Ex. 1009, 94; Ex. 1003 ¶¶ 107–108).

Patent Owner argues that Petitioner fails to show that an ordinary artisan would have modified Chin to yield the routing placement limitation of claims 2, 5, 6, and 8. PO Resp. 34. Patent Owner asserts, *inter alia*, that Petitioner’s proposed modification of Chin is “textbook hindsight” and faults Petitioner for failing to explain *why* a person of ordinary skill in the art would have made this modification. PO Resp. 35 (citing *Princeton Biochemicals, Inc. v. Beckman Coulter, Inc.*, 411 F.3d 1332, 1337 (Fed. Cir. 2005)).

In particular, Patent Owner argues that Petitioner does not explain why an ordinary artisan would have replaced power plane layer 250 with routing layer 275, where Chin describes layer 250 as “the first metal power plane layer below surface metal layer 200” followed by “intermediate” routing layer 275 and power plane layer 270. PO Resp. 35 (quoting Ex. 1004, 4:12–20); *see also* Sur-reply 23 (arguing that Petitioner ignores Chin’s “express differentiation between intermediate routing layer 275 and power planes 250 (first) and 270 (intermediate)”). Additionally, Patent Owner submits that there is no teaching in the prior art of patterning holes in

an adjacent metal routing layer as claimed. PO Resp. 35, 41–42; Sur-reply 23–24.

We are not persuaded by Petitioner’s arguments regarding interchanging Chin’s routing layer 275 and first power plane 250. Chin’s layer 200 includes pad 220, which is interconnected with other components by trace 230. Ex. 1004, 4:10–12. According to Chin, “[l]ayer 250 is the first metal power plane layer below surface metal layer 200.” Ex. 1004, 4:12–13. Chin also describes an intermediate metal power plane layer 270 “that is below the top two metal layers” and an intermediate routing layer 275 that “represents any intermediate routing layer with traces 235.” Ex. 1004, 4:18–24. Even if Chin indicates that intermediate routing layer 275 can be swapped with intermediate power plane layer 270, Chin does not teach (expressly or inherently) or suggest that “intermediate” metal layer 275 can be swapped with “first” power plane layer 250. Petitioner does not provide adequate support for its assertion to the contrary. See Pet. 40.

Also, Petitioner does not support adequately its assertion that it would have been obvious to modify Chin to replace layer 250 with layer 275. Petitioner refers to “the need to route possibly hundreds of signals” and “be flexible to accommodate the many signal lines present”—but, even if this would have motivated an ordinary artisan to *add* routing traces or layers, it does not explain sufficiently why routing layer 275 would have been *moved*, as Petitioner suggests. See Pet. 40–41; Ex. 1003 ¶ 106 (repeating the Petition). Petitioner simply states that this placement “is a design choice that a [person of ordinary skill in the art] was capable of making.” Pet. 41 (citing Ex. 1003 ¶¶ 106 (repeating the Petition)). But the fact that an ordinary artisan *could* have performed the proposed modification does not show the

requisite motivation to do so. *See Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018) (faulting the Board for “focus[ing] on what a skilled artisan would have been *able* to do, rather than what a skilled artisan would have been *motivated* to do at the time of the invention”); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (“It was [Petitioner’s] burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” (internal quotation marks omitted)). Petitioner’s use of generalized statements and lack of supporting explanation suggests that Petitioner’s proposal invokes improper hindsight.

Moreover, Patent Owner is correct that the additional prior art Petitioner relies upon (e.g., HighSpeed) does not show an arrangement of metal layers with a routing trace and cutouts on a second layer immediately adjacent to the contact on the first layer. PO Resp. 35, 41–42; Sur-reply 23–24. This further suggests Petitioner’s proposal is the result of improper hindsight.

Ultimately, on this record, we find Petitioner has not established by a preponderance of evidence that a person of ordinary skill in the art would have been motivated to modify the layer order of Chin by moving routing layer 275 below contact pad layer 200, as Petitioner proposes.

In its Reply, Petitioner argues that Chin’s metal layers satisfy this limitation because the term “routing layer” is “merely a label, *i.e.*, a non-limiting intended use.” *See* Reply 23–27. However, this argument is untimely and forfeited. *See supra* n.11. Specifically, Petitioner presents a new claim construction argument (*i.e.*, the term “routing layer” is non-

limiting) that departs from the approach taken in the Petition and does not fairly respond to Patent Owner’s Response or the Institution Decision. *See* Pet. 39–40 (contending that Chin discloses a routing layer with traces); CTPG 45 (“The petitioner may respond to any such new claim construction issues raised by the patent owner, but cannot raise new claim construction issues that were not previously raised in its petition.”), 74 (“‘Respond,’ in the context of 37 C.F.R. § 42.23(b), does not mean proceed in a new direction with a new approach as compared to the positions taken in a prior filing.”).

However, even if the argument had been properly presented, it would not have been persuasive because we conclude that the term “routing layer” is limiting and requires at least one routing trace. To support its argument to the contrary, Petitioner argues that some metal layers include both routing traces and reference planes and, as a result, it “is impossible” to clearly differentiate between routing layers and reference layers. Reply 23–25. But, this argument is a red herring. Even if Petitioner were correct that an ordinary artisan would be unable to reliably determine the proper classification for a layer with both routing traces and reference planes, this would show that the scope of the term “routing layer” is somewhat unclear,¹⁸ but not that it is non-limiting. Indeed, both parties agree that a “routing

¹⁸ We determine that the term is sufficiently clear for us to evaluate Petitioner’s contentions, and we need not (and cannot) evaluate whether the scope of the term would survive an indefiniteness challenge. *Cf. Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 813 (Fed. Cir. 2021) (“[I]t is not always impossible to adjudicate a prior-art challenge, one way or the other, just because some aspect of a claim renders the claim indefinite.”). Moreover, we do not delimit the precise contours of the term “routing layer” because it is unnecessary for this proceeding. *See Nidec*, 868 F.3d at 1017.

layer” must at least include a routing trace. *See* Tr. 36:17–20, 77:19–25. Moreover, we agree with Patent Owner that the ’269 patent differentiates between routing layers and reference potential layers. Sur-reply 22 (citing Ex. 1001, 2:64–3:3, 4:40–41). And, to the extent Petitioner contends that Chin’s reference layer 250 qualifies as a “routing layer,” we discern no basis for that contention.

Additionally, for the sake of completeness, we have considered Petitioner’s argument that regardless of the label assigned to a particular metal layer or whether the layer contains traces for signal routing, Chin teaches that the area in any metal layer over the contact pads, including first metal layer 250 (corresponding to the claimed “second layer”) should be devoid of metal. Reply 27–29. Petitioner further argues that Chin discloses routing signal traces around where patterned holes would be in its metal layers, when such traces are present. Reply 28 (citing Ex. 1004, 5:3–8). Additionally, Petitioner relies on Highspeed as showing a “common approach of routing a signal through the second layer of a substrate.” Reply 28. Petitioner also directs us to additional references in support of its argument that a person of ordinary skill in the art knew how to run routing traces through the layer immediately adjacent the ball pads in a BGA substrate. Reply 29 (citing Ex. 1112). Based on these teachings, Petitioner contends that “Chin discloses the structural limitations of the ‘routing layer’ claims.” Pet. 27 (emphasis omitted).

We disagree. Even giving Petitioner the full credit of its arguments, Petitioner has at best shown that Chin discloses cutouts in its metal layers, Chin discloses routing signal traces around holes in some metal layers, and that it was known in the art to include signal traces on the second layer of a substrate that does not contain cutouts. We are not persuaded that this

establishes “Chin discloses the structural limitations of the ‘routing layer’ claims” as Petitioner suggests, because there is no disclosure of signal traces on Chin’s second layer (power plane layer 250). Furthermore, as Patent Owner argues, Petitioner’s evidence demonstrates only that a person of ordinary skill in the art *could have* modified Chin to include signal routing in the second layer. As noted above, however, obviousness requires more than a showing of what a person of ordinary skill in the art could have done.

Polaris, 882 F.3d at 1068; *Intelligent Bio-Sys.*, 821 F.3d at 1367–68.

Petitioner’s arguments in its reply thus remain deficient for failing to demonstrate why a person of ordinary skill in the art *would have* modified Chin to include signal traces in first power layer 250. This is especially problematic considering Chin differentiates between its first power layer and intermediate power layers, does not disclose signal traces on its first power layer, and only refers to signal traces on its intermediate power layers.

For all of the reasons discussed above, we find Petitioner has not established, by a preponderance of the evidence, that claims 2, 5, 6, and 8 are unpatentable as obvious in view of Chin.

6. *Claim 3*

Claim 3 depends from claim 1 and requires that “the cutouts have the same dimensions as the contact pads.” Ex. 1001, 6:66–67. Petitioner argues the subject matter of claim 3 would have been obvious in view of Chin.

Pet. 30–31. Patent Owner challenges Petitioner’s arguments. PO Resp. 24–34.

Petitioner argues that a person of ordinary skill in the art “would understand the sizing of the cutouts to be a design decision subject to tradeoffs.” Pet. 30. Petitioner acknowledges that Chin teaches using cutouts that are larger than the contact pads to minimize parasitic capacitance, but

argues Chin also teaches that using oversized cutouts reduces capacitance more than desired and requires reintroduction of capacitance to tune the pad impedance. Pet. 31 (citing Ex. 1004, Abstr.). Petitioner also asserts that a person of ordinary skill in the art would understand “that larger cutouts reduce the shielding effects of ground or power metal layers and reduce the available area for routing traces in routing layers,” and, therefore, “would have found it obvious to try sizing the cutouts to have the same dimensions as the contact pads to allow for greater shielding and routing flexibility.” Pet. 31 (citing Ex. 1003 ¶ 91).

Patent Owner argues that Petitioner fails to provide sufficient evidence supporting its assertions. PO Resp. 32–34. For example, Patent Owner contends that Petitioner has not shown any example in the prior art where the cutouts were of the same size as the contact pads.” PO Resp. 32. Patent Owner also argues that neither Petitioner nor Dr. Choi performed a “tradeoff analysis” to support its claims that different sized cutouts would “allow for greater shielding and routing flexibility.” PO Resp. 33.

We agree with Patent Owner. The only evidence Petitioner cites in the Petition to support this argument is paragraph 91 of Dr. Choi’s declaration. Pet. 30–31. That paragraph, however, simply parrots the language in the Petition, without offering the underlying facts on which the opinion is based. *Compare* Ex. 1003 ¶ 91, *with* Pet. 30–31. Such testimony is conclusory and entitled to little or no weight. 37 C.F.R § 42.65(a).

We also agree with Patent Owner that Petitioner has not directed us to any disclosure in the prior art where the cutouts were the same size as the contact pads. PO Resp. 33–34; *see* Section III.G.2., *infra*. Instead, Petitioner relies only on references that teach the use of holes larger than the contact pads. Additionally, Dr. Bauer explains that the prior art shows “even

with a hole larger than the contact area, excellent shielding and routing flexibility were achieved.” Ex. 2030 ¶¶ 139–140; PO Resp. 34.

Furthermore, we note that Dr. Choi does not provide any evidence or further explanation of the purported tradeoff between cutout size and greater shielding and routing flexibility. See PO Resp. 33 (noting that Petitioner and Dr. Choi fail to analyze “how much additional shielding could be provided (or even shielding between which elements), or how much routing could be added”). As a result, we are not persuaded that additional space for shielding or routing would have motivated an ordinary artisan to make the proposed modification to Chin.

Additionally, we are not persuaded by Petitioner’s argument that a person of ordinary skill in the art “would have found it *obvious to try* sizing the cutouts to have the same dimensions as the contact pads.” Pet. 31 (emphasis added). The Supreme Court set forth the standard for when something may be obvious to try: “When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.” *KSR*, 550 U.S. at 421. In the Petition, Petitioner does not address whether there are a finite number of identified solutions, and Petitioner does not persuasively show that the proposed modification would have solved a problem.

We, therefore, agree with Patent Owner that Petitioner offers insufficient evidence with the Petition to show a rationale to modify Chin in the manner proposed. PO Resp. 32–34.

Petitioner does not cure this deficiency in its Reply.¹⁹ For example, in its Reply, Petitioner argues that the “sizing of the cutouts is a clear example of a predictable variation that cannot render a claim non-obvious,” and that “sizing a known structure is simply the ‘application of a known technique’ with predictable results.” Reply 18–19. According to Petitioner, a person of ordinary skill in the art would have understood the effect of resizing the patterned hole to be smaller, the same size, or larger than the pad size. Reply 19. To support this, Petitioner directs us to an IBM publication (Ex. 1111) purportedly “confirming a predictable improvement in signal performance as the cut-out size in an IC substrate was increased.” Reply 19.²⁰ As Petitioner acknowledges, however, the IBM publication includes no actual data for cutouts that were the same size as the pads. Instead, as Patent Owner explains, “the newly submitted IBM reference tested one configuration with cutouts (400µm) significantly smaller than and another with cutouts (800µm) significantly larger than the pads (650µm).” Sur-reply 18. Nor does Dr. Choi address the predictability purportedly demonstrated by the IBM reference.

Petitioner also contends that the IBM publication “discusses the well-known design trade-offs like reduced shielding and difficulty routing around

¹⁹ Patent Owner contends that Petitioner’s Reply “injects over five pages of new arguments that should have been made in the Petition,” and that we should not consider these new arguments. Sur-reply 17. We agree that Petitioner presents arguments in its Reply that do not appear in its Petition. *See supra* n.11. Nevertheless, we have addressed these arguments to explain why we find them to be unpersuasive.

²⁰ Petitioner did not offer this exhibit with its Petition and Dr. Choi did not cite to this exhibit in his declaration submitted with the Petition. *See* CTPG 73; *Intelligent Bio-Sys.*, 821 F.3d at 1369. Additionally, Dr. Choi did not provide a supplemental declaration addressing this reference.

the large cutouts” (Reply 19 (citing Ex. 1111, 1)), but the IBM publication does not indicate that any such tradeoffs would have motivated an ordinary artisan to make the proposed modification to Chin (*cf.* Ex. 1111, 1 (instead stating that “wider plane opening[s]” provide “better electrical performance” but “may compromise . . . wireability” and mechanical reliability))). Additionally, Dr. Choi does not address the purported trade-offs in the IBM reference.

As such, we are not persuaded by Petitioner’s reliance on the IBM reference, and agree with Patent Owner that Petitioner’s attorney arguments are insufficient to support its obviousness challenge. *See, e.g.*, Sur-reply 18 (arguing “Petitioner presents no analysis whatsoever on the achievable variability caused by fringe capacitance and how that variability affects the performance”).

Petitioner additionally argues that a person of ordinary skill in the art “would not have blindly recreated the exact size structures disclosed in Chin but would have employed ordinary creativity to explore a range of sizes that suited a particular application.” Reply 20. According to Petitioner, hole size is a common engineering tradeoff that could be modeled and tested to determine what size worked for a particular purpose. Reply 20. Petitioner states:

With reports from Chin (and Oggioni) of significant bandwidth increases resulting from cutouts in metal layers below contact pads, a [person of ordinary skill in the art] would have been motivated to model, simulate, and prototype a range of cutout sizes including the simplest size, that equal in size to the ball pad. Equally sized cutouts are the easiest to draw in a layered CAD tool because one can trace the ball pad in an overlay view. . . . Because Chin provided only one testing datapoint, a [person of ordinary skill in the art] would have been motivated to model

variations on the Chin design to determine the optimal pattern hole size

Reply 22.

Petitioner's arguments are unpersuasive. In support of these arguments, Petitioner relies on deposition testimony from Dr. Bauer, but our review of that cited testimony reveals Dr. Bauer testified that there are "tools for modeling the performance of a transmission line in a lot of different situations," but those tools "have limits in capabilities." Ex. 1110, 21:8–22:3. Dr. Bauer also testified that generally in 2006 "there would be a prototyping phase," and agreed that a person of ordinary skill in the art "reading Oggionni or Chin and trying to determine the size of the cutout that [he/she] wanted to use, could . . . try four different cutout sizes." Ex. 1110, 28:20–29:4, 190:25–191:10. Absent from this testimony is any indication that a person of ordinary skill in the art would consider using cutout sizes other than those disclosed in Chin and Oggionni, which teach using cutouts that are larger than the pads.

Additionally, we are not persuaded by Petitioner's argument that "[e]qually sized cutouts are the easiest to draw in a layered CAD tool." Reply 22. Petitioner does not provide any support for this statement. Additionally, even if it is true, Petitioner fails to demonstrate or explain sufficiently any correlation between the ease of creating drawings using a layered CAD tool and what a person of ordinary skill in the art would have considered or done when sizing cutouts. As a result, Petitioner is left to rely on primarily attorney argument to support its contention that "a [person of ordinary skill in the art] would have been motivated to model variations on the Chin design to determine the optimal pattern hole size, the number of layers in which to include the pattern holes, and other design aspects."

Reply 22. Attorney argument, however, cannot take the place of evidence. *E.g., In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974).

Nor does Petitioner cure the deficiency in its “obvious to try” argument, as it fails to adequately address whether there are a finite number of identified solutions. During the oral hearing, counsel for Petitioner argued that “a person of ordinary skill in the art making cutouts would make them either smaller, the same size or larger. There are only three options and so the same size ones would simply be a choice that would be right in the middle.” Tr. 45:17–22; *see also* Reply 19 (referring to “resizing the patterned hole to be smaller, the same size, or larger than the pad size”). Petitioner’s attempt to characterize the sizing options as being limited to three *categories* of sizes—smaller, the same size, or larger—is unavailing because two of those categories comprise a range with a virtually infinite number of size values. Moreover, Petitioner’s argument that there are a limited number of sizing options seems inconsistent with its arguments based on “design trade-offs” such as routing *flexibility*. Pet. 30–31; Reply 19–20.

In view of the foregoing, we find Petitioner has failed to demonstrate by a preponderance of the evidence that claim 3 is unpatentable as obvious in view of Chin.

7. *Claims 14–16 and 19*

Petitioner argues claims 14–16 and 19 are unpatentable as obvious in view of Chin. Petitioner directs us to the portions of Chin that disclose or suggest the limitations recited in each claim. Pet. 66–70; Reply 16–18; Ex. 1004, 4:29–32. Petitioner also relies on testimony from Dr. Choi to support its assertions. Ex. 1003 ¶¶ 156–162, 165–167. Patent Owner contends that Chin fails to disclose or suggest “forming vias connecting the

contact pads with one of the electrically conductive layers,” as dependent claims 14–16 and 19 each require. PO Resp. 51–52; Sur-reply 15–17; Ex. 1001, 8:22–42.

With regard to this limitation, Petitioner argues that vias are well-known structures used as connections between metal layers. Pet. 68; Reply 16; Ex. 1009, 94. Petitioner further argues Chin teaches or suggests that the routing metal layer is electrically connected to the first layer, and also discloses the use of vias to connect metal layers. Pet. 68 (citing Ex. 1004, 4:29–32). According to Petitioner, a person of ordinary skill in the art would have known that vias are used to electrically connect the contacts in the first layer with routing traces on a different layer. Pet. 68–69 (citing Ex. 1003 ¶ 160).

Patent Owner notes that the cited portion of Chin, column 4, lines 29–32, refers to the use of a via to connect a compensation capacitor to a reference plane, not Chin’s landing pad to the reference plane. PO Resp. 51. Patent Owner thus argues that “there is no basis in Petitioner’s assertion that 4:29–32 discloses the limitation under any reasonable interpretation of the limitation.” PO Resp. 51–52.

Patent Owner, however, does not dispute Petitioner’s assertion and evidence that vias were well-known structures used as connections between metal layers. Nor does Patent Owner dispute Petitioner’s assertion that Chin teaches or suggests that the routing metal layer is electrically connected to the first layer. It is also undisputed that Chin itself discloses the use of vias to make electrical connections between two components on different layers. Ex. 1004, 4:29–32. Although Patent Owner is correct that this language in Chin itself does not disclose the disputed limitation in claims 14–16 and 19, Petitioner does not rely on this information alone. Rather, in addition to this

language in Chin, Petitioner directs us to additional undisputed evidence that Chin discloses electrical connections between its first layer and its routing metal layers and to undisputed evidence that vias were well-known in the art as structures used to form connections between metal layers. Pet. 68; Reply 16; Ex. 1009, 94; Ex. 1004, 4:29–32. The evidence of record thus supports Petitioner’s assertion that it would have been obvious to a person of ordinary skill in the art to use vias to electrically connect the pads in Chin’s first layer with the respective routing traces on routing layer 275. Pet. 68–69.

In view of the foregoing, we find Petitioner has demonstrated, by a preponderance of the evidence, that claims 14–16 and 19 are unpatentable as obvious in view of Chin.

8. Conclusion

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of the evidence that claims 1, 4, 7, and 9–20 are unpatentable as obvious in view of Chin, but has not demonstrated by a preponderance of the evidence that claims 2, 3, 5, 6, and 8 are unpatentable as obvious in view of Chin.

E. Claims 5, 8, 14–16, and 19 – Obviousness in view of Chin and HighSpeed

Petitioner contends claims 5, 8, 14–16, and 19 are unpatentable as obvious in view of Chin and Highspeed. Pet. 71–76. Patent Owner challenges Petitioner’s arguments.

1. HighSpeed (Ex. 1009)

HighSpeed is titled “High-Speed Digital System Design—A Handbook of Interconnect Theory and Design Practices.” Ex. 1009, 1. In section 5.1, HighSpeed describes “vias,” which are “used to make

connections between various layers of the PCB or to connect components to traces.” Ex. 1009, 94.

“Figure 5.1 depicts a typical through-hole via and its equivalent circuit” and is reproduced below:

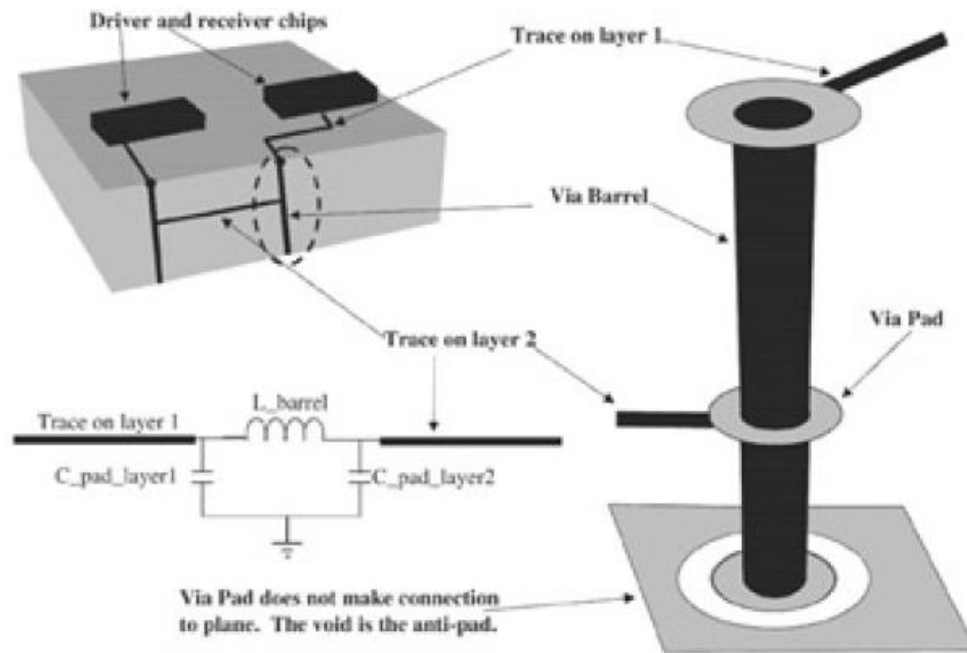


Figure 5.1: Equivalent circuit of a through-hole via.

Ex. 1009, 94. As shown above, Figure 5.1 illustrates a through-hole via connected to a trace on layer 1 and a trace on layer 2 along with its equivalent circuit. HighSpeed explains that a through-hole via “is made by drilling a hole through the board, filling it with solder, and making connections on appropriate layers via the pad.” Ex. 1009, 94. “Other, less common types of vias, used primarily in multichip modules (MCMs) and advanced PCBs, are blind, buried, and micro-vias.” Ex. 1009, 94.

2. Analysis

Petitioner contends claims 5, 8, 14–16, and 19 would have been unpatentable as obvious in view of Chin and HighSpeed. Pet. 71–76. According to Petitioner, a person of ordinary skill in the art would have been motivated to combine HighSpeed and Chin because Chin and HighSpeed are

both from the same field of endeavor, and an ordinary artisan “would have looked to HighSpeed, a combinable reference describing useful structures and approaches, or would have known and understood the prior art principles detailed therein.” Pet. 71–72.

a) Claims 5 and 8

With regard to claims 5 and 8, Petitioner again argues that Chin alone renders obvious the routing placement limitation. Pet. 72 (referring to its earlier analysis of the unpatentability of claim 5 based on Chin alone). Petitioner alternatively argues that HighSpeed discloses “a commonly used prior art arrangement of metal layers with a routing trace on layer 2 immediately adjacent to the contact on layer 1 coupled to an integrated circuit.” Pet. 72–73 (citing Ex. 1009, 94). Petitioner asserts that using HighSpeed’s arrangement of layers “would have been a routine design choice that a [person of ordinary skill in the art] was capable of making” and “one of a finite number of possibilities and within the skill of a [person of ordinary skill in the art] to try.” Pet. 73.

Patent Owner relies on the same arguments discussed above regarding obviousness in view of Chin alone, and further argues that Petitioner’s analysis as to why a person of ordinary skill in the art would have combined Chin and HighSpeed is “legally insufficient.” PO Resp. 34–35, 47–48. In particular, Patent Owner argues that simply characterizing references as being from the same field of endeavor is not sufficient to support an obviousness conclusion. PO Resp. 48 (citing *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017)). Further, according to Patent Owner, Petitioner’s argument that the references are combinable does not demonstrate why a person of ordinary skill in the art would have combined them. PO Resp. 49. Patent Owner also challenges

Petitioner's argument based on a finite number of possibilities, arguing that Petitioner's own declarant, Dr. Choi, testified that there were many different ways to achieve the results desired in Chin. PO Resp. 49–50 (citing Ex. 2032, 196:20–23).

We are not persuaded by Petitioner's arguments regarding the combination of Chin and HighSpeed. Petitioner does not sufficiently explain *why* a person of ordinary skill in the art would have been motivated to combine Chin and HighSpeed in the manner proposed. We agree with Patent Owner that simply characterizing references as being from the same field of endeavor is not sufficient to support an obviousness conclusion. PO Resp. 48; *see ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1327–28 (Fed. Cir. 2012). Furthermore, Petitioner's analysis that it would have been obvious to arrange Chin in view of HighSpeed to have the second layer be a routing layer because the arrangement “is one of a finite number of possibilities and within the skill of a[n ordinary artisan] to try” is incomplete. Pet. 73 (citing Ex. 1003 ¶ 175). The Supreme Court in *KSR* held that “[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.” *KSR*, 550 U.S. at 421 (emphasis added). Petitioner, however, never addresses, or otherwise presents evidence showing, a design need or market pressure to solve a problem. *See* Pet. 73; Ex. 1003 ¶ 175 (repeating material in the Petition). Additionally, testimony from Dr. Choi that “there are many ways to achieve the same result” of an

impedance match in Chin, undermines Petitioner’s “finite number” argument.²¹ Ex. 2032, 196:20–23.

For these reasons, as well as those discussed in Section III.D.2., *supra*, we find Petitioner fails to establish, by a preponderance of the evidence, that claims 5 and 8 are unpatentable as obvious in view of Chin and HighSpeed.

b) Claims 14–16 and 19

In view of our finding that Petitioner establishes by a preponderance of the evidence that claims 14–16 and 19 are unpatentable as obvious in view of Chin alone, we do not address Petitioner’s additional ground challenging claims 14–16 and 19 in view of Chin and Highspeed.

F. Claim 2 – Obviousness in view of Chin and either MC92600 or Shafer

Petitioner argues the subject matter of claim 2 would have been obvious in view of the combined teachings of Chin and MC92600, and in view of the combined teachings of Chin and Shafer. Pet. 77–87.

1. MC92600 (Ex. 1008)

MC92600 is the User’s Manual for Motorola’s MC92600 Quad 1.25 Gbaud SERDES transceiver. Ex. 1008, 1, 17. MC92600 states that the Motorola part includes a transmitter that “takes the data byte presented at its data input . . . and serially transmits” associated information out the output pads. Ex. 1008, 21.

According to MC92600, the part is offered in a 196 MAPBGA package, and Figure 7-3 “provides a graphic of the package pin signal

²¹ Petitioner did not address this testimony, or Patent Owner’s argument based on it, in its Reply.

mappings.” Ex. 1008, 67, 70 (showing Figure 7-3). Petitioner annotates this figure with yellow and blue highlighting, as shown below:

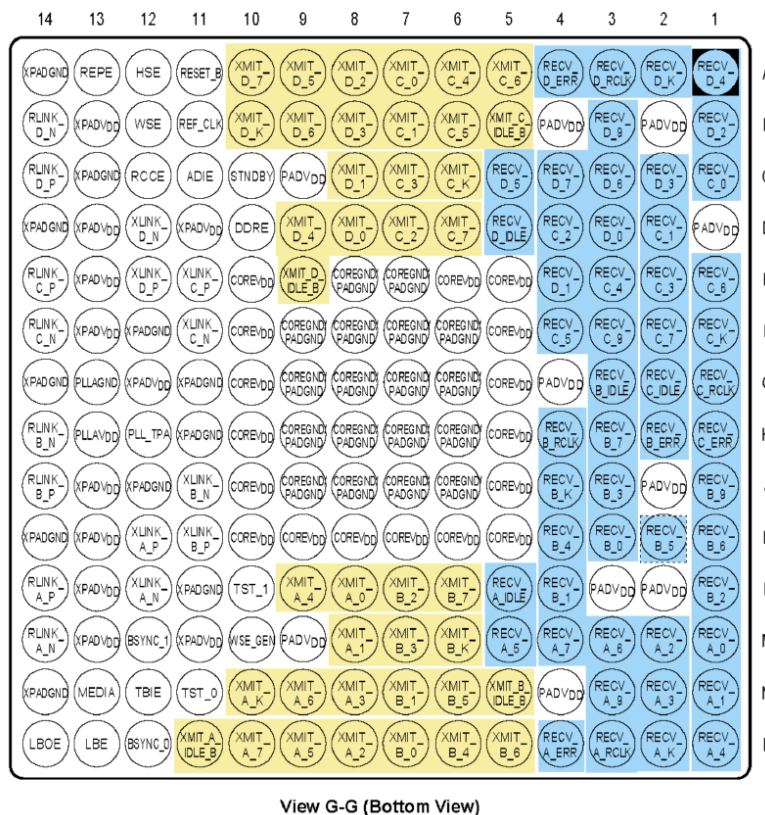


Figure 7-3. 196 MAPBGA Package

Pet. 79 (citing Ex. 1008, 70). Petitioner’s annotation of Figure 7-3, reproduced above, shows yellow-colored transmit pins (designated “XMIT”) and blue-colored receive pins (designated “RCV”). Pet. 78.

2. Shafer (Ex. 1026)

Shafer is generally directed to a method and system for reducing crosstalk in backplanes, which, according to Shafer, “have become popular for providing high-speed connections between printed circuit boards.” Ex. 1026, 1:1–13. Shafer explains that as data transmission speeds increase into the gigahertz range, near-end crosstalk becomes a significant problem for certain connector pin configurations. Ex. 1026, 2:52–55. Shafer further explains that because transmit signals are relatively much larger than receive

signals, the transmit signal couples with the receive signal. Ex. 1026, 2:55–57. Furthermore, “[s]ince linear equalization circuits cannot typically distinguish a signal from the crosstalk, it is difficult to correct for the crosstalk using circuitry alone.” Ex. 1026, 2:60–63.

To address this problem, Shafer aims to provide an improved connector pin assignment having ground shields in only one direction. Ex. 1026, 3:11–14. Shafer describes several embodiments of a connector for connecting a circuit board to a backplane, wherein the connector includes different configurations of transmit connection positions, receive connection positions, and ground shields positioned between the transmit and receive connection positions in only one direction. Ex. 1026, 3:24–33. Shafer’s embodiments include receive and transmit connection elements for serializer/deserializer modules. Ex. 1026, 3:34–67.

3. *Analysis*

For each of these challenges, Petitioner relies on its previous arguments that Chin teaches or suggests the routing placement limitation in claim 2. Pet. 78 (“As explained above for elements 5[b] and 6[a] in Ground 1, Chin combined with the [person of ordinary skill in the art]’s knowledge renders obvious a routing metal layer as a second layer having routing traces electrically connected to the contact pads.”), 85–86 (same). For the reasons discussed above, we are not persuaded by Petitioner’s arguments that Chin combined with the knowledge of a person of ordinary skill in the art renders obvious a routing metal layer as a second layer. See Section III.D.5., *supra*. Petitioner does not direct us to any portion of MC92600 or Shafer, or to any arguments based on the teachings of those references, that cure the deficiencies in Petitioner’s prior analysis of the routing layer limitation. See *generally* Pet. 77–87. Accordingly, for the same reasons discussed above,

Petitioner has not demonstrated, by a preponderance of the evidence, that claim 2 is unpatentable as obvious in view of the combined teachings of Chin and MC92600 or the combined teachings of Chin and Shafer.

G. Claim 3 – Obviousness in view of Chin and Oggioni

Petitioner argues the subject matter of claim 3 would have been obvious in view of Chin in combination with Oggioni. Pet. 87–90. Patent Owner disputes Petitioner’s contentions. PO Resp. 24–32.

1. Oggioni (Ex. 1006)

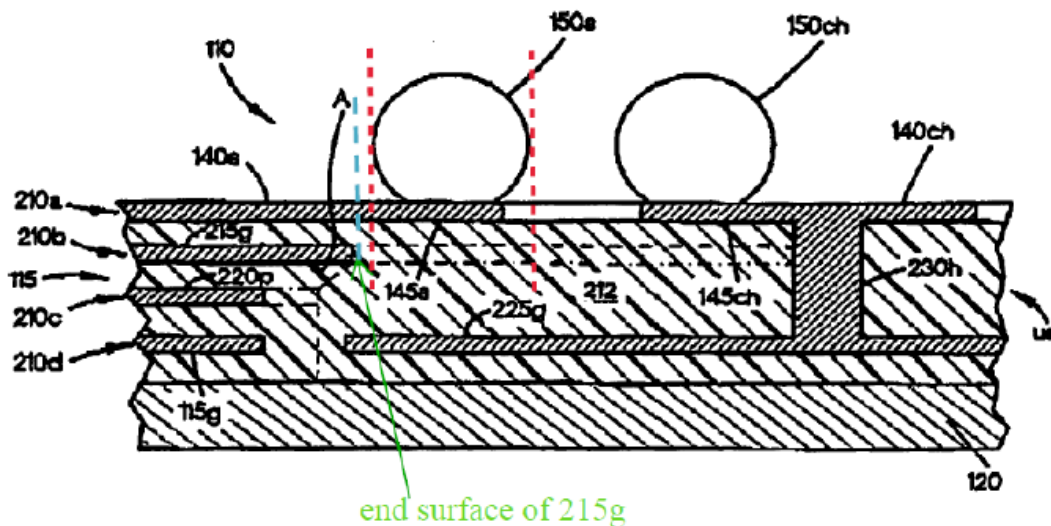
Oggioni is directed to an electronic package including a chip carrier having a first conductive layer that includes at least one signal track and one contact area, and a reference structure having at least two conductive layers such that the signal track is electrically shielded by the reference structure. Ex. 1006, Abstr. Oggioni explains that the trend towards miniaturization of electronic devices has led to a reduction in the dimensions of the chip carrier conductive tracks on which the devices are packaged, including the use of a thin dielectric layer between the conductive tracks and ground plane of the electronic package. Ex. 1006, 1:57–67. According to Oggioni, “[a] shortened distance between conductive tracks and the ground plane increases the value of a corresponding stray capacitance. As a consequence, the bandwidth of the transmission line is strongly reduced.” Ex. 1006, 1:67–2:3.

In attempting to address this drawback, Oggioni discloses an embodiment having conductive layers that do not “intersect a shadow of the projection of” its contact areas. Ex. 1006, 4:65–5:3; Fig. 2b. Oggioni states that its invention “substantially reduces the capacitance of the stray capacitor formed between” conductive signal tracks and corresponding ground planes. Ex. 1006, 5:46–49.

2. Analysis

Petitioner contends that Oggioni, like Chin, is directed to “mitigating issues with high-speed signals interfacing an integrated circuit package by reducing package pad parasitic capacitance.” Pet. 87. Petitioner further contends that Oggioni discloses using cutouts in a conducting layer that are the same size as the contact pad based on Oggioni’s statement that “[g]round plane 215g does not intersect a shadow of the projection of contact area 145s.” Pet. 89–90 (quoting Ex. 1006, 5:2–3).

Patent Owner disputes that Oggioni teaches using cutouts that are the same size as the contact pad. PO Resp. 25. To support its position, Patent Owner provides an annotated version of Oggioni Figure 2b, reproduced below from the Patent Owner Response (PO Resp. 26).



Annotated Figure 2b of Oggioni shows a partial sectional view of a chip carrier, including ground plane layer 215g formed in conductive layer 210b, solder balls 150, and contact area 145s. Ex. 1006, Fig. 2b, 3:55–4:38. Patent Owner’s annotations include dotted red lines on the right and left sides of solder ball 150s, a dotted blue line on the left of the left-side red

dotted line, and a green line pointed to the end of the blue dotted line labeled “end surface of 215g.” Patent Owner explains that “[a]s illustrated in Figure 2b, the ‘end surface of ground plane 215g’ is to the left of solder ball 150s’ projection. EX1006, Fig. 2b, 5:9–15. This indicates that the opening is larger than 150s in at least one dimension. EX2030, ¶180.” PO Resp. 25.

Petitioner does not directly dispute Patent Owner’s argument based on Figure 2b, asserting only that a person of ordinary skill in the art would “not find certainty in the figures.” Reply 23. Rather, Petitioner maintains that Oggioni’s statement defining a keep-out region as “a shadow of the projection of contact area 145s” demonstrates Oggioni discloses equal-sized cutouts. Reply 23 (quoting Ex. 1006, 5:2–3).

We find that Oggioni’s statement does not disclose equal-sized cutouts. Oggioni states that “ground plane 215g does not intersect a shadow of the projection of contact area 145s.” Ex. 1006, 5:2–3. This statement does not clearly speak to the salient issue, despite Petitioner’s contention to the contrary. Indeed, Dr. Choi acknowledges that this statement will be satisfied if the opening in ground plane 215g is *larger* than the shadow of contact area 145s. Ex. 2031, 121:22–122:16, 165:11–166:4; Ex. 2030 ¶ 178 (*cited in* PO Resp. 27). As a result, given Figure 2b, which depicts an opening larger than the contact pad in at least one dimension, Oggioni’s statement does not teach sizing a cutout to be equal in size to contact area 145s. In addition, as Patent Owner points out, Dr. Choi testified that “a shadow of the projection of contact area 145s’ does not necessarily mean a normal projection of the contact area 145s,” and “[a] shadow of contact pad 145s could depend on the angle of the projection.” PO Resp. 27 n.1 (quoting Ex. 2031, 169:17–24, 171:23–25). We agree with Patent Owner’s assertion that this testimony from Dr. Choi indicates that a cutout corresponding to a

shadow of 145s that is not projected perpendicularly to layer 210b would have a different size than the pad size.

After considering the evidence of record, we find Petitioner has failed to demonstrate persuasively that Oggioni discloses cutouts having the same dimensions as the contact pads, as claim 3 requires. In view of the foregoing, we are not persuaded Petitioner has demonstrated, by a preponderance of the evidence, that claim 3 is unpatentable as obvious in view of Chin and Oggioni.

IV. OBJECTIONS TO DEMONSTRATIVES

Patent Owner objects to slides 25–30, 33–35, and 41–46 of Petitioner’s hearing demonstratives, arguing that these slides include new arguments and/or evidence not present in the Petition and/or Reply (Paper 28), and Petitioner objects to slide 32 of Patent Owner’s hearing demonstratives, arguing that it presents a new argument and claim construction position that is not found in the record (Paper 29). We dismiss these objections as moot because, even considering any alleged new arguments, the outcome here would not change. *See supra* n.11.

V. CONCLUSION

For the reasons discussed above, we find Petitioner has demonstrated by a preponderance of the evidence that claims 1, 4, 7, and 9–20 of the ’269 patent are unpatentable.²² Petitioner, however, has not demonstrated by a preponderance of the evidence that claims 2, 3, 5, 6, and 8 are unpatentable.

²² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or*

In summary:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 3–20	103	Chin	1, 4, 7, 9–20	3, 5, 6, 8
5, 8, 14– 16, 19	103	Chin, HighSpeed ²³		5, 8
2	103	Chin, MC92600		2
2	103	Chin, Shafer		2
3	103	Chin, Oggioni		3
Overall Outcome			1, 4, 7, 9–20	2, 3, 5, 6, 8

Reexamination During a Pending AIA Trial Proceeding. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

²³ As explained above, with the exception of claims 5 and 8, we do not reach this ground, in view of our determination that Petitioner has otherwise established claims 14–16 and 19 are unpatentable.

VI. ORDER

In consideration of the foregoing, it is hereby

ORDERED that Petitioner has established by a preponderance of the evidence that claims 1, 4, 7, and 9–20 of the '269 patent are unpatentable;

FURTHER ORDERED that Petitioner has not established by a preponderance of the evidence that claims 2, 3, 5, 6, and 8 of the '269 patent are unpatentable;

FURTHER ORDERED that Patent Owner's Objections to Petitioner's Demonstratives (Paper 28) are dismissed as moot;

FURTHER ORDERED that Petitioner's Objections to Patent Owner's Demonstratives (Paper 29) are dismissed as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2021-00967
Patent 8,288,269 B2

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