

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-01089
Patent 7,154,299 B2

Before FRANCES L. IPPOLITO, NATHAN A. ENGELS, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

ENGELS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Petitioner Microchip Technology, Inc. filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–25 of U.S. Patent No. 7,154,299 B2 (Ex. 1001, “the ’299 patent”). Patent Owner HD Silicon Solutions LLC filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition and any response thereto shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon consideration of the Petition and the evidence of record, we determine Petitioner has demonstrated a reasonable likelihood of prevailing in establishing unpatentability of at least one claim of the ’299 patent. Accordingly, we institute *inter partes* review.

A. Real Parties in Interest

Petitioner identifies Microchip Technology Incorporated as the real party-in-interest. Pet. 1. Patent Owner identifies HD Silicon Solutions LLC (“HDSS”) as the real party-in-interest. Paper 4, 2.

B. Related Matters

The parties state that the ’299 patent was asserted in *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092 (W.D. Tex.). Pet. 1; Paper 4, 2. That case has been transferred to *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 3:21-cv-08295-SK (N.D. Cal.). Paper 7, 2.

C. The ’299 Patent

Titled “Architecture for Programmable Logic Device,” the ’299 patent describes an improved programmable logic device architecture that provides more efficient utilization of resources by enabling access to defined circuit

elements in the domain of any Programmable Logic Block (PLB) from any other PLB in the device. Ex. 1001, codes (54), (57). Among other things, the '299 patent describes a device that incorporates a routing means that selectively connects the input or output of the circuit element in the domain of the PLB to a common interconnect matrix connecting all the PLBs together. *Id.* at 1:56–64. The '299 patent states that the routing means may be a controlled gate structure that selectively enables the input or output of the circuit element to the interconnect matrix, based on the value of a selection input. *Id.* at 1:65–2:1.

D. Illustrative Claims

The Petition challenges all 25 claims of the '299 patent. Of the challenged claims, claims 1, 5, 7, 9, 13, 14, 16, 19, 21, and 23 are independent claims. Independent claims 1, 8, 9, 13, 14, 19, and 21 are apparatus claims, independent claims 5, 7, and 23 are method claims, and independent claim 16 is a system claim. Claim 1, reproduced below with bracketed labels added corresponding to the numbering in the Petition, is illustrative.

1. An improved programmable logic device architecture that provides more efficient utilization of resources

[a] by enabling access to a defined sequential circuit element in a routing domain associated with a programmable logic block from any other programmable logic block in the device,

[b] by incorporating a connecting means in the routing structure operable to selectively connect an input of the defined sequential circuit element in the routing domain to a first signal-pass node of a common interconnect matrix connecting all the programmable logic blocks together

[c] via no circuit element other than one or more switch elements and

[d] to simultaneously connect an output of the logic circuit element to a second signal-pass node of the common interconnect matrix.

Ex. 1001, 5:27–40.

E. Alleged Grounds of Unpatentability

Petitioner asserts that claims 1–25 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–18, 23–25	103	Ting, ¹ Knowledge of a Person of Ordinary Skill in the Art
19–22	103	Ting, Pani ²

II. ANALYSIS

A. Discretionary Denial of Institution Under 35 U.S.C. § 314(a)

With arguments premised on the original trial schedule set in the parties’ district-court litigation, Patent Owner asserts that we should exercise our discretion under 35 U.S.C. § 314(a) to deny institution. Prelim. Resp. 32–37 (citing *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020)). The original trial schedule no longer applies, however, because the parties’ litigation has been transferred to a new venue with no scheduling order in place and no trial date set. *See* Paper 7, 2 (Petitioner’s Updated Mandatory Notices). As such, the parties’ arguments premised on the earlier schedule are no longer applicable, and the record does not otherwise contain sufficient evidence to support discretionary denial. Accordingly, we decline to exercise discretion under 35 U.S.C. § 314(a) to deny institution of *inter partes* review.

¹ U.S. Patent No. 5,457,410, issued October 10, 1995 (Ex. 1005).

² U.S. Patent No. 6,034,547, issued March 7, 2000 (Ex. 1006).

B. Discretionary Denial of Institution Under 35 U.S.C. § 325(d)

Arguing that the Board should exercise its discretion to deny the Petition under 35 U.S.C. § 325(d), Patent Owner asserts “[w]hile the same prior art was not cited [during prosecution], Petitioner fails to discuss the lengthy file history of the ’299 patent nor that similar prior art and arguments were already considered by the Examiner.” Prelim. Resp. 27. Specifically, Patent Owner contends that Petitioner did not address three references that “fail to disclose or suggest the limitation of ‘via no circuit element other than’” one or more switch elements, and Patent Owner contends Ting and Pani also fail to disclose that limitation, which the Examiner cited in the Notice of Allowance. Prelim. Resp. 27 (citing Ex. 1004, 78 (Notice of Allowance)).

On this record, we are not apprised of sufficient overlap between Ting and Pani and the references cited in the prosecution history to warrant discretionary denial under 35 U.S.C. § 325(d). *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper No. 6, at 8 (P.T.A.B. Feb. 13, 2020) (precedential) (describing a two-part framework for § 325(d) considerations, including consideration of the extent of overlap between a petitioner’s art and arguments and the prosecution history).

C. Level of Ordinary Skill in the Art

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends a person of ordinary skill in the art at the time of the invention would have been a person with (1) “a master’s degree in electrical engineering, materials science, physics, or related degree, and 3-5 years of experience in semiconductors, specifically Field Programmable Gate Arrays (‘FPGA’)” or (2) “a bachelor’s degree in electrical engineering, materials science, physics, or related degree, and 5-6 years of experience in semiconductor devices, specifically FPGAs.” Pet. 5 (citing Ex. 1002, ¶ 29).

Patent Owner does not address the level of skill in the art in its Preliminary Response. For the purposes of this Decision, we apply the level of ordinary skill advanced by Petitioner, which is consistent with the evidence of record.

D. Claim Construction

We construe claims using the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc) and related cases. 37 C.F.R. § 42.100(b) (2020). Under that precedent, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips*, 415 F.3d at 1312–13.

Petitioner states that, at this stage, all claim terms should be accorded their plain and ordinary meanings. Pet. 11. Patent Owner responds that it “takes no position” in its Preliminary Response regarding Petitioner’s proposal that the claim terms should be given their plain and ordinary meaning. Prelim. Resp. 16. Patent Owner further argues that “while the Petition acknowledges that certain claims of the ’299 patent contain means-plus-function language that should be interpreted under 35 U.S.C. § 112, ¶ 6,

[the Petition] does not construe these terms, as required by 37 C.F.R. § 42.104(b)(3).” *Id.* at 19–20 (citing Pet. 11–12).

Claim element [1.b] recites “by incorporating a connecting means in the routing structure operable to selectively connect an input of the defined sequential circuit element in the routing domain to a first signal-pass node of a common interconnect matrix connecting all the programmable logic blocks together,” and Petitioner identifies this element as including a means-plus-function limitation. Pet. 24. Dependent claim 2 provides that “wherein said connecting means is a controlled gate structure that selectively enables the input of the defined sequential circuit element to the interconnect matrix, based on the value of a selection input.”

For the purposes of this Decision, we determine it is sufficient to note that the “connecting means” of claim 1 includes at least the “controlled gate structure” defined in claim 2. *See* Ex. 1001, 1:65–67 (“The routing means may be a controlled gate structure that selectively enables the input or output of the circuit element to the interconnect matrix, based on the value of a selection input.”). We note that in its comparison of Ting to element [1.b], Petitioner identifies structures from the ’299 patent’s specification that correspond to the claimed “connecting means,” including switches which Petitioner contends are controlled gate structures. Pet. 24 (quoting Ex. 1001, 3:57–64); Ex. 1002 ¶ 113 (Dr. Sechen testifying that “A person of ordinary skill in the art would understand that a controlled gate structure is the same thing as a switch; both a controlled gate structure and a switch are transistors that can be programmed to selectively allow or disallow a signal to pass along the interconnect.”); *cf.* Prelim. Resp. 21 (Patent Owner asserting “Petitioner does not argue [Ting’s switches 309, 314, 316, 324, and 330]

meet the limitation ‘controlled gate structure.’ Instead, Petitioner argues that switches 483 and 486 *act* as controlled gate structures.”).

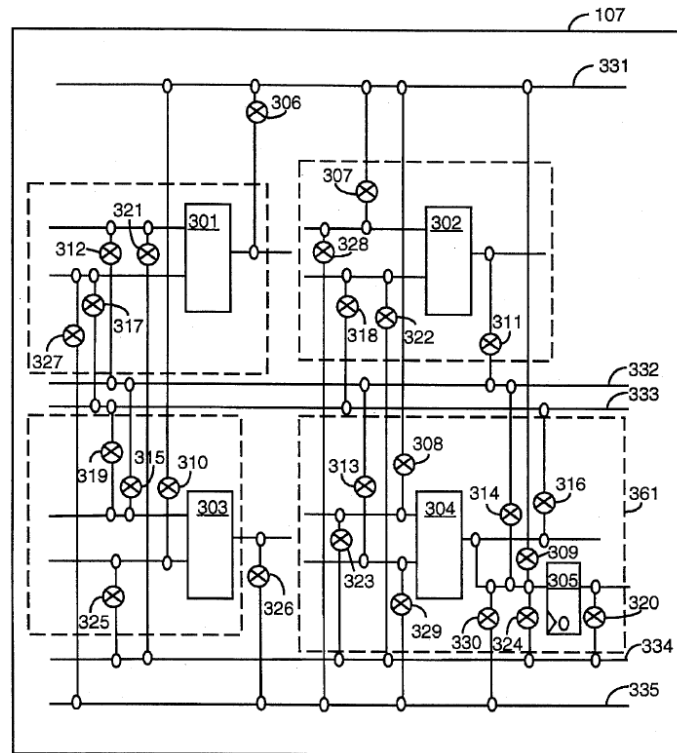
At this stage we determine Petitioner’s identification of structures satisfies the requirements of 37 C.F.R. § 42.104(b)(3). Although Patent Owner bears no burden of proof, to the extent that Patent Owner contends a switch does not fall within the scope of the claimed “connecting means” and/or the claimed “controlled gate structures” of claim 2, Patent Owner is encouraged to explain those positions in Patent Owner’s Response.

E. Summary of Prior Art References

1. Ting

Titled “Architecture and Interconnect Scheme for Programmable Logic Circuits,” Ting “pertains to the field of programmable logic circuits.” Ex. 1005, code (54), 1:8–9. Ting explains that a “programmable logic circuit is comprised of a number of cells which perform digital functions on input signals” and “[d]epending on user’s specific design, certain cells are programmably interconnected to a particular configuration for realizing the desired logic functions.” *Id.* at 3:64–4:4. Ting describes a preferred embodiment wherein “four logic cells (four two-input one-output logic gates and one D flip-flop) form a logical cluster (i.e. a 2x2 cell array) and four sets of clusters form a logical block (i.e. a 4x4 cell array).” *Id.* at 4:5–8. “Within each cluster, there is a set of five intraconnection lines, called Intraconnection Matrix (I-Matrix), one associated with the output of each one of the four gates and the D flip-flop that is connectable to the input of the other cells” and “[w]ithin each logical block, the I-Matrix within each cluster can be extended to an adjacent cluster through a passgate to form connections within the logical block (to extend the intraconnection range).” *Id.* at 4:8–16.

Figure 3A of Ting, reproduced below, depicts a logic cluster. Ex. 1005, 5:31.



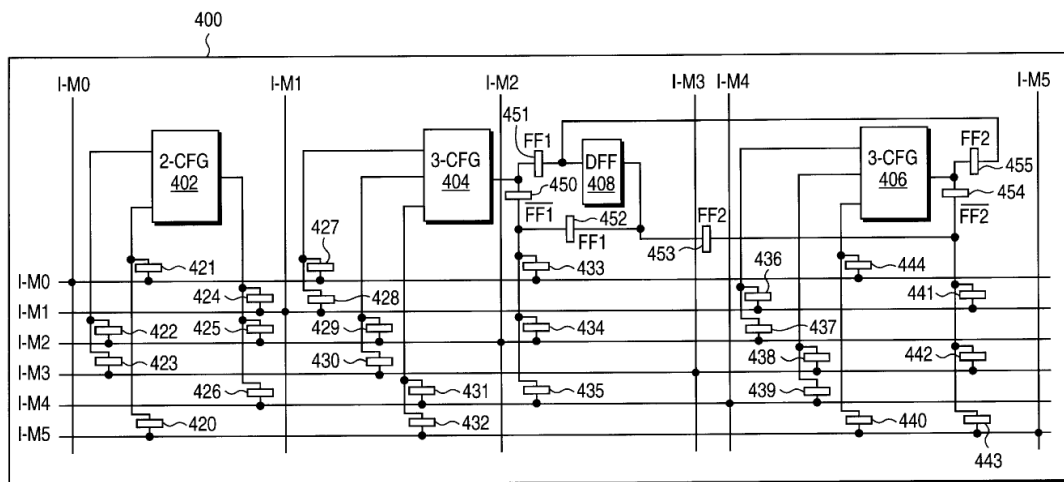
Ting's Figure 3A depicts logical cluster 107 comprised of four cells 301–304, D flip-flop 305, twenty five switches 306–330, and five intraconnection lines 331–335. Ex. 1005, 6:66–7:3. Intraconnection lines 331–335 and switches 306–330 form the I-Matrix, which “provides connectability of the output, X, of each of the four cells 301–304, and the output X of the D flip-flop 305 to at least one input of each of the other three cells and the D flip-flop.” *Id.* at 7:4–9.

2. Pani

Titled “Method and Apparatus for Universal Program Controlled Bus,” Pani “is directed to a programmable, configurable bus system of lines to interconnect electrical components for an electrical/electronics system.” Ex. 1006, code (54), 1:7–9. Pani’s “invention provides an innovative bus system of lines which can be programmed to provide data, control and

address information to the logic circuits interconnected by the bus system in the context of an electrical/electronics system.” *Id.* at 1:43–47. Pani discloses “a configurable system” that can “programmably connect one or more logic circuits such as megacells to external logic devices and other megacells.” *Id.* at 1:47–50.

Figure 4A of Pani, reproduced below, depicts a “logic cluster” that “can be formed of other elements such as logic gates and flip-flops.” *Ex.* 1006 at 5:46–49.



Pani’s Figure 4A depicts logic cluster 400, which is formed of four logic elements including one 2 input combinational logic or configurable function generator (CFG) 402, two three input CFGs 404, 406, and D flip-flop 408. *Id.* at 5:50–54. In one embodiment, Pani’s logic cluster “is used to selectively couple bus signal lines to input/outputs of a megacell and to input/output logic.” *Id.* at 5:66–6:1. According to Pani, “this combination of elements provides a fine granularity without the addition of redundant elements which add to the die size and speed of processing.” *Id.* at 6:1–4.

F. Ground 1: Ting and the Knowledge of a Person of Ordinary Skill in the Art

The Petition includes a limitation-by-limitation comparison of Ting and the purported knowledge of a person of ordinary skill in the art to claims 1–18 and 23–25. Pet. 18–91. As noted in the Petition, various claims recite essentially equivalent limitations, and the Petition cites essentially the same evidence for the corresponding limitations of each claim. Patent Owner likewise notes that its arguments apply to groups of claims having equivalent limitations. Prelim. Resp. 17–26.

1. Claim 1

[1.p] “An improved programmable logic device architecture that provides more efficient utilization of resources”

For these elements, Petitioner cites Ting as disclosing an architecture and distributed hierarchical interconnect scheme for field programmable gate arrays (FPGA) that maximizes utilization of the FPGA. Pet. 18–19 (citing Ex. 1005, code (57), 3:45–47; Ex. 1002 ¶¶ 73–74). Patent Owner does not address Petitioner’s showing for these elements. Neither party addresses whether the preamble is limiting, and we determine it is unnecessary to decide that issue at this stage.

[1.a] “by enabling access to a defined sequential circuit element in a routing domain associated with a programmable logic block from any other programmable logic block in the device”

For this limitation, Petitioner cites Ting’s disclosures of a defined sequential circuit element such as flip flop 305 in a routing domain associated with a programmable logic block 107. Pet. 19–20. According to Petitioner, Ting’s routing domain is part of the common interconnect which connects the programmable logic block with any other programmable logic

block in the device such that Ting's flip flop can be associated with any programmable logic block via intraconnection lines. Pet. 19–24. (citing Ex. 1002 ¶ 77).

According to Patent Owner, the portion of Ting cited by Petitioner “is an intraconnection line—a line that connects elements within [a programmable logic block] and not an element that enables access of a sequential circuit element in a routing domain associated with one PLB by another PLB” as claimed. Prelim. Resp. 17 (citing Ex. 1005, 7:4–9). Thus, Patent Owner argues Petitioner failed to identify a routing domain and therefore failed to identify a sequential circuit element within a routing domain. Prelim. Resp. 17–18. Patent Owner further argues that Ting describes using resources within a logic block, and Patent Owner argues that Petitioner failed to establish that “Ting enables access of the sequential circuit element in a routing domain associated with one PLB by another PLB or that Ting relates to the utilization of underutilized resources.” Prelim. Resp. 18.

On the current record, we determine that Petitioner has sufficiently shown that Ting teaches element [1.a] for the purposes of institution. As an initial matter, we do not read claim 1 to require “utilization of underutilized resources.” Further, Petitioner's arguments are consistent with the teachings of Ting and are supported by the testimony of Dr. Sechen, while at this stage, Patent Owner's arguments amount to unsupported attorney argument. Further, Patent Owner's arguments regarding “intraconnection” and Ting's statement that “[w]ith the judicious use of I-Matrix and block connectors within the same logical block, a set of signals can be internally connected “without using any resources outside the logical block” (Ex. 1005, 4:22–25)

take Ting's teachings out of context and are not consistent with Ting's teachings as a whole.

[1.b] "by incorporating a connecting means in the routing structure operable to selectively connect an input of the defined sequential circuit element in the routing domain to a first signal-pass node of a common interconnect matrix connecting all the programmable logic blocks together"

As noted above, Petitioner claim element includes a means-plus-function limitation. Pet. 24–25. Petitioner identifies corresponding structures that include "switches, which can be programmed to direct a signal through certain paths and perform certain logic functions." Pet. 24–25 (citing Ex. 1001, 3:57–64, 4:27–35, Fig. 9; Ex. 1002 ¶¶ 88–89).

Petitioner contends Ting discloses switches that act as connecting means to selectively connect the input of a flip flop to a first signal-pass node of a common interconnect matrix that connects all programmable logic blocks together. Pet. 25–30 (citing Ex. 1005, 7:4–6, 7:51–55, 7:61–62, 9:1–41, Figs. 3A, 3B, 4A, 5A; Ex. 1002 ¶¶ 87, 90, 92–95)

Patent Owner contends Petitioner failed to properly identify structures corresponding to the claimed "connecting means." Prelim. Resp. 19. As noted above, we disagree with that argument.

Patent Owner also argues Petitioner is inconsistent in identifying Ting's switches as the "connecting means" (Prelim. Resp. 20 (citing Pet. 24–25)) while later identifying Ting's intraconnection lines 331–335 as the "connecting means" (Prelim. Resp. 20 (citing Pet. 32)). Patent Owner's arguments mischaracterize Petitioner's arguments, and we determine for the purposes of institution that Petitioner has sufficiently shown that Ting teaches element [1.b], including Petitioner's citation to Ting's switches as the claimed connecting means.

[1.c] via no circuit element other than one or more switch elements and

For this element, Petitioner argues Ting teaches that “each connection between logic elements includes programmable switches.” Pet. 31; *accord* Pet. 30–34.

Patent Owner argues “Petitioner only discusses that Ting discloses switches used in the routing structure,” and “[t]he Petition contains no discussion of the limitation ‘via no circuit element other than’ one or more switch elements, as claimed. Prelim. Resp. 22–23. According to Patent Owner, “just because Ting has switches does not mean that the programmable logic blocks are connected ‘*via no circuit element other than*’” those switches, and Patent Owner notes that Petitioner additionally cites Ting’s teachings that “PLBs are connected in Ting via the intraconnection lines 331–335 and not only through switches.” Prelim. Resp. 23

On the current record, we determine Petitioner has made a sufficient showing that Ting teaches element [1.c] for the purposes of institution. Patent Owner’s arguments take Petitioner’s arguments out of context and mischaracterize those arguments. To the extent that Patent Owner reads this limitation to require switches with no connection lines, Patent Owner is encouraged to address that argument as one of claim interpretation and to identify support in the ’299 patent for such an argument; on the current record, we see no support for such an argument.

[1.d] “to simultaneously connect an output of the logic circuit element to a second signal-pass node of the common interconnect matrix.”

For this element, Petitioner contends the “logic circuit element” lacks antecedent basis and that the term could be interpreted as the claimed

“sequential circuit element.” Under that interpretation, Petitioner contends Ting satisfies this limitation with its teachings of selectively connecting an input of the defined sequential circuit element to all other programmable logic blocks with a connecting means, citing switch 320 in Figure 3A as the second signal-pass node. Pet. 35–36. According to Petitioner, the output of Ting’s flip flop (the logic circuit element) can be simultaneously connected to the second signal pass node (switch 320) to any other logic block in the common interconnect matrix via routing lines 331–335. Pet. 37–39.

Patent Owner does not address Petitioner’s showing for this element.

2. Conclusion Regarding Claim 1

Based on the current record, we determine Petitioner has made a sufficient showing for each element of claim 1 for the purposes of institution. Accordingly, Petitioner has established that it is likely to prevail in showing that claim 1 is unpatentable in view of Ting in combination with the knowledge of a person of ordinary skill in the art.

3. Claims 13 and 14

Among other limitations, claims 13 and 14 require that the routing resources are operable to allow bi-directional communication between the logic block coupled to the input of the sequential logic element and the logic block coupled to the output of the sequential logic element. Among other things, Petitioner contends Ting discloses bi-directional communication “because the signal can travel in reverse.” Pet. 78 (citing Ex. 1002 ¶ 185).

Patent Owner argues “traveling in ‘reverse’ is not the same as bi-directional. Bi-directional means capable of traveling both forward *and* in reverse.” Prelim. Resp. 24. Patent Owner additionally argues Petitioner “shows the weakness of Petitioner’s arguments” by the fact that Petitioner presents a modified version of Ting’s Figure 3A, and Patent Owner contends

that in Petitioner's modified Figure 3A, the sequential logic element is bypassed. Prelim. Resp. 24–26.

Patent Owner's argument regarding the meaning of “bi-directional” appears to take Petitioner's arguments out of context, but to the extent that the parties disagree regarding the meaning of that claim term, the parties are encouraged to address the scope and meaning of the claim limitations in future briefing. On the current record, Patent Owner's arguments regarding Ting's communication amount to unsupported attorney argument, while Petitioner supports its arguments with the testimony of Dr. Sechen. For the purposes of institution, we determine Petitioner has made a sufficient showing for these limitations, as well as the remaining limitations of claims 13 and 14.

4. Claims 2–12, 15–18, and 23–25

Petitioner provides a claim-by-claim, element-by-element comparison of each of claims 2–12, 15–18, and 23–25. Pet. 29–90. Patent Owner does not substantively address these claims beyond the arguments presented above. For the purposes of institution, we determine Petitioner has made sufficient showings for each of these claims.

G. Ground 2: Ting and Pani

1. Claims 19–22

Petitioner cites Ting for most of claims 19–22 and additionally cites Pani for its teachings regarding a similar programmable logic device. Pet. 91–127. Petitioner also presents reasons for combining the teachings of Ting and Pani. Pet. 128–129.

Patent Owner contends Petitioner improperly cites Ting's intraconnection lines as “simultaneously satisfy[ing] the ‘routing domain’ limitation, ‘common interconnect matrix’, and also the ‘circuit node input’

limitation of claim 19–22.” Prelim. Resp. 29–31. Patent Owner also argues that Petitioner fails to explain what element in Pani meets the ‘circuit node input’ limitation and that Petitioner misrepresents Pani. Prelim. Resp. 31.

On the current record, Patent Owner’s arguments take Petitioner’s arguments out of context and misrepresent Petitioner’s arguments. Patent Owner’s arguments also currently amount to unsupported attorney argument.

Based on the current record, we find Petitioner’s arguments and evidence sufficient for the purposes of institution.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail with respect to at least one claim of the ’299 patent. Accordingly, we institute an *inter partes* review as to all challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted as to claims 1–25 of the ’299 patent on all grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is given of the institution of a trial, which commences on the entry date of this Decision.

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