

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-01089
Patent 7,154,299 B2

Before FRANCES L. IPPOLITO, NATHAN A. ENGELS, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

ENGELS, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Petitioner Microchip Technology, Inc. filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–25 of U.S. Patent No. 7,154,299 B2 (Ex. 1001, “the ’299 patent”). Patent Owner HD Silicon Solutions LLC filed a Preliminary Response. Paper 6. Pursuant to 35 U.S.C. § 314, we issued a Decision instituting this *inter partes* review as to all of the challenged claims and all grounds raised in the Petition. Paper 8 (“Dec.”).

After institution, Patent Owner filed a Response (Paper 16 (“PO Resp.”)), Petitioner filed a Reply (Paper 18 (“Reply”)), and Patent Owner filed a Sur-Reply (Paper 23 (“Sur-Reply”)). Petitioner filed two Declarations of Carl Sechen, Ph.D.: Ex. 1002 in support of the Petition (“Petition-Declaration”) and Ex. 1020 in support of Petitioner’s Reply (“Reply-Declaration”). Patent Owner filed the Declaration of Dr. Steven Preyzybski in support of Patent Owner’s Response. Ex. 2002.

Each party presented oral arguments at a hearing on October 12, 2022. A transcript of the hearing has been entered into the record. Paper 27.

Based on the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 19–22 are unpatentable in view of Tang and Pani, but Petitioner has not proven the unpatentability of any of claims 1–18 or claims 23–25.

A. *Real Parties in Interest*

Petitioner identifies Microchip Technology Incorporated as the real party-in-interest. Pet. 1. Patent Owner identifies HD Silicon Solutions LLC (“HDSS”) as the real party-in-interest. Paper 4, 2.

B. Related Matters

The parties state that the '299 patent was asserted in *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092 (W.D. Tex.). Pet. 1; Paper 4, 2. That case has been transferred to *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 3:21-cv-08295-SK (N.D. Cal.). Paper 7, 2. Petitioner additionally states that the following U.S. patents are also asserted in the parties' litigation and that Petitioner has challenged those patents in the *inter partes* review proceedings identified below:

7,260,731—IPR2021-01420

7,810,002—IPR2021-01567

7,870,404—IPR2021-01265

7,302,619—IPR2021-00872 & IPR2021-01042

6,774,033—IPR2021-00752

Paper 7, 2–3.

C. The '299 Patent

Titled “Architecture for Programmable Logic Device,” the '299 patent describes an improved programmable logic device architecture that provides more efficient utilization of resources by enabling access to defined circuit elements in the domain of any Programmable Logic Block (“PLB”) from any other PLB in the device. Ex. 1001, codes (54), (57). Among other things, the '299 patent describes a device that incorporates a routing means that selectively connects the input or output of the circuit element in the domain of the PLB to a common interconnect matrix connecting all the PLBs together. *Id.* at 1:56–64. The '299 patent states that the routing means may be a controlled gate structure that selectively enables the input or output

of the circuit element to the interconnect matrix, based on the value of a selection input. *Id.* at 1:65–2:1.

D. Illustrative Claims

The Petition challenges all 25 claims of the '299 patent. Of the challenged claims, claims 1, 5, 7, 8, 9, 13, 14, 16, 19, 21, and 23 are independent claims. Independent claims 1, 8, 9, 13, 14, 19, and 21 are apparatus claims, independent claims 5, 7, and 23 are method claims, and independent claim 16 is a system claim. Claim 1, reproduced below with bracketed labels added corresponding to the numbering in the Petition, is illustrative.

1. An improved programmable logic device architecture that provides more efficient utilization of resources

[a] by enabling access to a defined sequential circuit element in a routing domain associated with a programmable logic block from any other programmable logic block in the device,

[b] by incorporating a connecting means in the routing structure operable to selectively connect an input of the defined sequential circuit element in the routing domain to a first signal-pass node of a common interconnect matrix connecting all the programmable logic blocks together

[c] via no circuit element other than one or more switch elements and

[d] to simultaneously connect an output of the logic circuit element to a second signal-pass node of the common interconnect matrix.

Ex. 1001, 5:27–40.

E. Alleged Grounds of Unpatentability

Petitioner asserts that claims 1–25 would have been unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–18, 23–25	103	Ting ¹²
19–22	103	Ting, Pani ³

F. Summary of Prior Art References

1. Ting

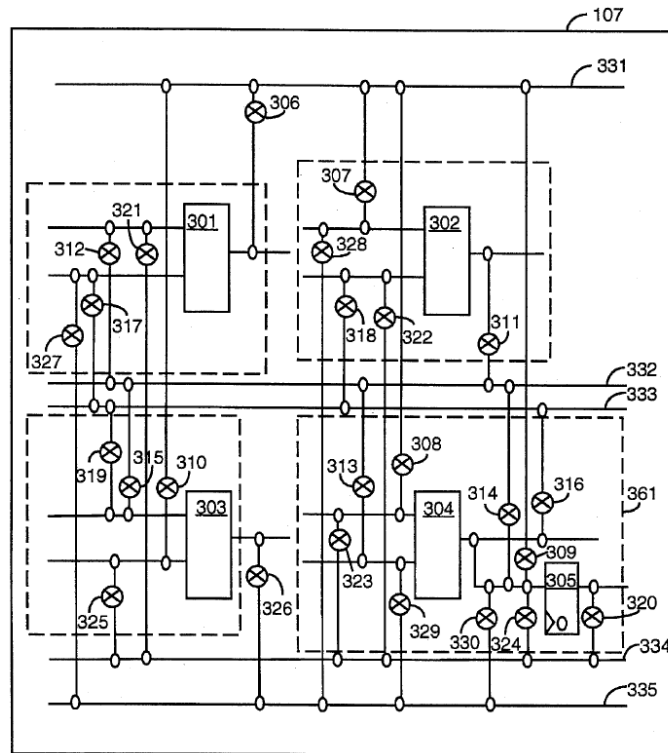
Titled “Architecture and Interconnect Scheme for Programmable Logic Circuits,” Ting “pertains to the field of programmable logic circuits.” Ex. 1005, code (54), 1:8–9. Ting explains that a “programmable logic circuit is comprised of a number of cells which perform digital functions on input signals” and “[d]epending on user’s specific design, certain cells are programmably interconnected to a particular configuration for realizing the desired logic functions.” *Id.* at 3:64–4:4. Ting describes a preferred embodiment wherein “four logic cells (four two-input one-output logic gates and one D flip-flop) form a logical cluster (i.e. a 2x2 cell array) and four sets of clusters form a logical block (i.e. a 4x4 cell array).” *Id.* at 4:5–8. “Within each cluster, there is a set of five intraconnection lines, called Intraconnection Matrix (I-Matrix), one associated with the output of each one of the four gates and the D flip-flop that is connectable to the input of the other cells” and “[w]ithin each logical block, the I-Matrix within each cluster can be extended to an adjacent cluster through a passgate to form connections within the logical block (to extend the intraconnection range).” *Id.* at 4:8–16.

¹ U.S. Patent No. 5,457,410, issued October 10, 1995 (Ex. 1005).

² Petitioner expressly lists Ting “in view of the knowledge of a Person of Ordinary Skill in the Art.” *E.g.*, Pet. 4, 18. Because the knowledge of a person of ordinary skill is implicit in every obviousness determination, we refer to this ground simply as “Ting.”

³ U.S. Patent No. 6,034,547, issued March 7, 2000 (Ex. 1006).

Figure 3A of Ting, reproduced below, depicts a logic cluster.
Ex. 1005, 5:31.



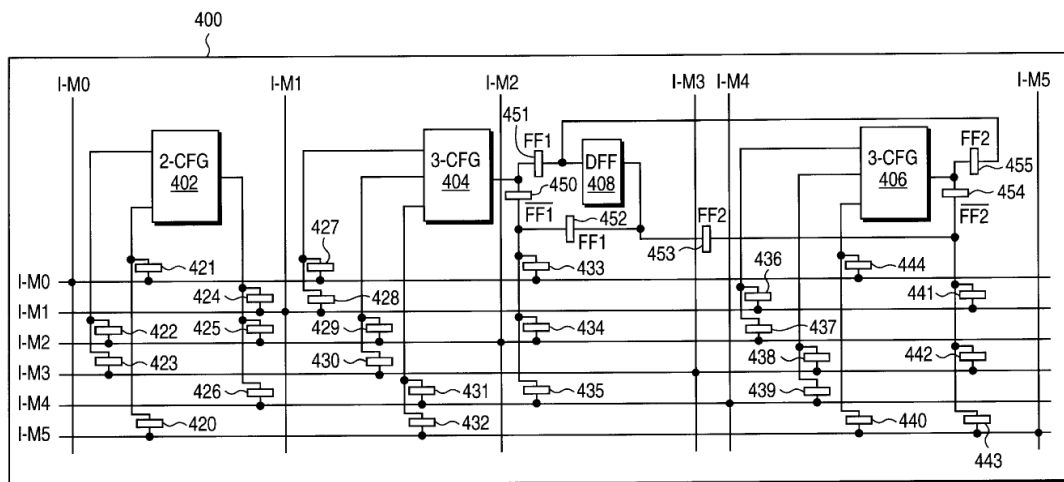
Ting's Figure 3A depicts logical cluster 107 comprised of four cells 301–304, D flip-flop 305, twenty five switches 306–330, and five intraconnection lines 331–335. Ex. 1005, 6:66–7:3. Intraconnection lines 331–335 and switches 306–330 form the I-Matrix, which “provides connectability of the output, X, of each of the four cells 301–304, and the output X of the D flip-flop 305 to at least one input of each of the other three cells and the D flip-flop.” *Id.* at 7:4–9.

2. Pani

Titled “Method and Apparatus for Universal Program Controlled Bus,” Pani “is directed to a programmable, configurable bus system of lines to interconnect electrical components for an electrical/electronics system.” Ex. 1006, code (54), 1:7–9. Pani’s “invention provides an innovative bus system of lines which can be programmed to provide data, control and

address information to the logic circuits interconnected by the bus system in the context of an electrical/electronics system.” *Id.* at 1:43–47. Pani discloses “a configurable system” that can “programmably connect one or more logic circuits such as megacells to external logic devices and other megacells.” *Id.* at 1:47–50.

Figure 4A of Pani, reproduced below, depicts a “logic cluster” that “can be formed of other elements such as logic gates and flip-flops.” *Ex. 1006* at 5:46–49.



Pani’s Figure 4A depicts logic cluster 400, which is formed of four logic elements including one 2 input combinational logic or configurable function generator (CFG) 402, two three input CFGs 404, 406, and D flip-flop 408. *Id.* at 5:50–54. In one embodiment, Pani’s logic cluster “is used to selectively couple bus signal lines to input/outputs of a megacell and to input/output logic.” *Id.* at 5:66–6:1. According to Pani, “this combination of elements provides a fine granularity without the addition of redundant elements which add to the die size and speed of processing.” *Id.* at 6:1–4.

II. ANALYSIS

A. Legal Standards

The Supreme Court set out a framework for assessing obviousness under § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long felt but unsolved needs, failure of others, etc.” *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).⁴ When evaluating obviousness based on a combination of prior art, we also “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Level of Ordinary Skill in the Art

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends a person of ordinary skill in the art at the time of the invention would have been a person with (1) “a master’s degree in electrical engineering, materials science, physics, or related degree, and 3-5 years of experience in semiconductors, specifically Field Programmable Gate Arrays (‘FPGA’)” or (2) “a bachelor’s degree in electrical engineering,

⁴ The record does not include any evidence of secondary considerations.

materials science, physics, or related degree, and 5-6 years of experience in semiconductor devices, specifically FPGAs.” Pet. 5 (citing Ex. 1002 ¶ 29).

Patent Owner does not address the level of skill in the art. We apply the level of ordinary skill advanced by Petitioner, which is consistent with the evidence of record.

C. Claim Construction

We construe claims using the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc), and related cases. 37 C.F.R. § 42.100(b) (2020). Under that precedent, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips*, 415 F.3d at 1312–13.

Petitioner states that all claim terms should be accorded their plain and ordinary meanings (Pet. 11), but the parties address the meanings of “switch/switch element” and “bi-directional” in subsequent briefing, among other terms. PO Resp. 28–39; Reply 1–4; Sur-Reply 3–5. The parties’ dispute regarding these claim terms does not affect our analysis below, and we, thus, determine that it is unnecessary to expressly interpret any claim terms for the purposes of this Decision. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Petitioner’s Burden

A petition for *inter partes* review must identify “with particularity, each claim challenged, the grounds on which the challenge to each claim is

based, and the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3). As stated by the Court of Appeals for the Federal Circuit, “[i]n an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (emphasis added) (citing 35 U.S.C. § 312(a)(3)); *see also* *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’”) (quoting 35 U.S.C. § 312(a)(3)). The Board’s *Trial Practice Guide* further advises that a petitioner should “focus on concise, well-organized, easy-to-follow arguments supported by readily identifiable evidence of record.” Patent Trial and Appeal Board Consolidated Trial Practice Guide, at 39 (Nov. 2019).⁵ Moreover, a petitioner “may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a *prima facie* case of unpatentability” (*id.* at 73), and “[i]t is also improper for a reply to present new evidence (including new expert testimony) that could have been presented in a prior filing” (*id.* at 74).

As explained below, Petitioner does not present an identifiable, consistent, and cohesive theory of unpatentability and thus failed to satisfy its burden. We also determine the arguments and evidence advanced in Petitioner’s Reply and Reply-Declaration exceed the proper scope of a reply brief under 37 C.F.R. § 42.23(b).

⁵Available at <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>

E. Ground 1: Ting

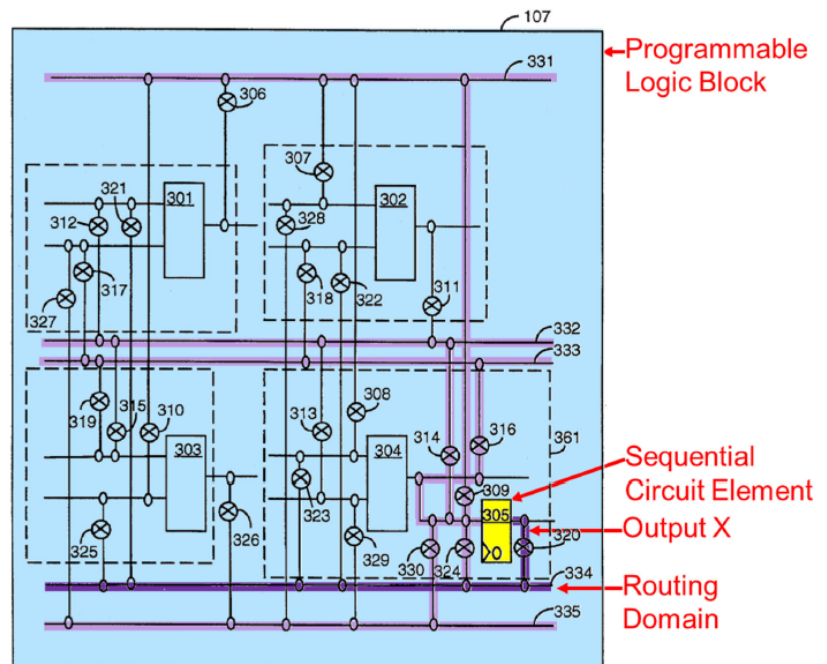
1. Ground 1 Is Unclear and Inconsistent

The Petition alleges obviousness with claim-by-claim, limitation-by-limitation comparisons of claims 1–18 and 23–25 to disclosures in Ting (Pet. 18–90), followed by a three-sentence subsection titled “Motivation to Combine Ting with the Knowledge of a Person of Ordinary Skill in the Art” (Pet. 91). Petitioner’s “Motivation” subsection states “it would have been obvious to a POSITA to take the disclosures of Ting, and apply his or her knowledge to integrate the [Field Programmable Gate Arrays] into conventional electronic systems” Pet. 91. Yet, the Petition lacks any specific discussion of where or how Petitioner contends Ting would have been combined with the knowledge of a person of ordinary skill to arrive at the challenged claims. Moreover, it is unclear in the Petition where and how Petitioner relies on evidence of the POSITA’s knowledge, a problem made worse by the extensive reliance on a POSITA’s knowledge in Petitioner’s Reply and Reply-Declaration.

The Petition’s deficiencies are most evident in Petitioner’s analysis of limitations directed to a sequential element (e.g., flip-flop) that is located outside of a PLB and in a routing domain associated with the PLB, in routing resources adjacent to the PLB, or within a routing matrix. *See* Reply 9 (“claims 1–18 and 23–25 recite that the sequential circuit/logic element be placed in the routing domain/resources/matrix”). More specifically, claims 1–4 of the ’299 patent recite “a defined sequential circuit element in a routing domain associated with a programmable logic block.” Claims 5–7 recite “a defined sequential circuit element in the domain of any programmable logic block.” Claims 8–18 recite “routing resources adjacent to one of the programmable logic blocks and including a sequential circuit

element.” And claims 23–25 recite “a sequential logic element disposed within a routing matrix.”

Patent Owner contends that “[i]n Ting . . . the sequential circuit element or flip-flop is not located in the routing domain, routing resources, or routing matrix. Instead it is located within the logic cluster.” PO Resp. 41. The Petition addresses these limitations with reference to the annotated version of Ting’s Figure 3A, reproduced below.



Pet. 20.

The Petition’s annotated version of Figure 3A labels Ting’s “logic cluster 107” as “Programmable Logic Block,” and states “Figure 3A of Ting discloses a defined sequential circuit element 305 (yellow) in a routing domain (purple) associated with a programmable logic block 107 (blue).” Pet. 19 (emphasis added); *see* Pet. 59 (stating Ting’s Figure 3A “shows routing lines 331–335 (purple) that connect to the input and output of the sequential logic element (flip-flop 305, yellow) within a logic block”). The

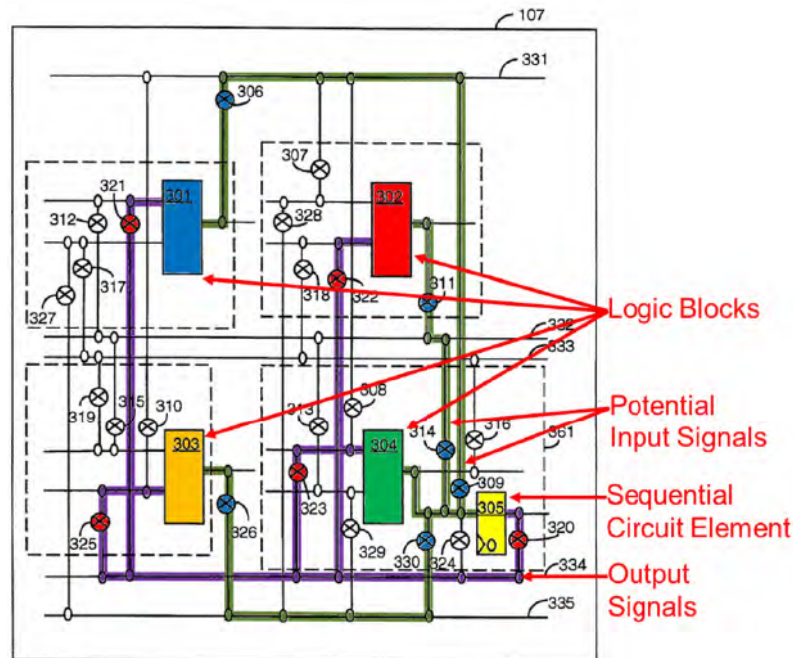
Petition similarly equates Ting's "logic cluster" to a PLB, stating "Ting discloses a logic cluster, or programmable logic block, comprised of four pass-gates 301–304 . . . and one D flip-flop 305." Pet. 12.

Contradicting that position, though, Petitioner's Reply draws a distinction between a logic block and a logic cluster. Reply 5–13. Petitioner's Reply argues "a POSITA would have understood that a logic *block*, or a PLB may include only the cells 301–304 within a logical cluster 107, and that the other components within the cluster 107, i.e., the intraconnection lines 331–335, the switches 306–330, and the D flip-flop 305, form an associated routing domain." Reply 6 (citing Ex. 1020 ¶ 21). The Reply also states, "in his Petition-Declaration Dr. Sechen identified the cells 301–304 of a logical cluster 107 as 'Logic Blocks,' which together can be understood as a PLB." Reply 6 (citing Ex. 1002 ¶ 223; Ex. 1020 ¶ 21).

But these arguments are inconsistent with the positions presented in the Petition. First, the Reply's reliance on a single paragraph in the Petition-Declaration—paragraph 223, which addresses only claim 25—seems cherry-picked in the face of numerous statements in the Petition-Declaration that do not support Petitioner's Reply arguments. *E.g.*, Ex. 1002 ¶¶ 64 ("As illustrated in Figure 3A . . ., Ting discloses a logic cluster, or programmable logic block, comprised of four logic cells having four pass-gates 301–304 . . . and one D flip-flop 305 . . . organized in a 2x2 cell array."), 77 (reproducing the annotated version of Ting's Figure 3A; referring to "programmable logic block 107 (blue)"), 80 (referring to "programmable logic block 107 (blue)" and "logic cluster 107"), 108 (referring to "logic cells within the logic block 107"), 169 (referring to "logic block 107"). In particular, the structure relied upon as teaching the programmable logic

block in the Petition is not the same as that annotated and relied upon in the Reply.

Second, Petitioner’s citation to paragraph 223 of the Petition-Declaration apparently refers only to the “Logic Block” label added to a second annotated version of Ting’s Figure 3A, copied below.



Ex. 1002 ¶ 22. This second annotated version of Ting’s Figure 3A labels cells 301–304 as “Logic Blocks” without labeling element 107, unlike the previous annotated version that labeled the entire blue rectangle 107 as the “Programmable Logic Block.” Moreover, counter to Petitioner’s reliance on paragraph 223, the textual discussion in the paragraph itself refers to element 107 as the logic block: “Figure 3A of Ting discloses routing resources that couple the input and output of the sequential logic element, flip-flop 305 (yellow) to different input and output of logic cells 301–304 *within that logic block 107*, which are adjacent to the routing resources (purple and green).” Ex. 1002 ¶ 223 (emphasis added).

Petitioner's positions are further confused by arguing that Petitioner does not have to show that Ting's flip-flop is in the routing domain because the Petition asserts obviousness and not anticipation. Reply 8–9. In support of this, Petitioner argues that “[m]oving the sequential element from the PLB to the routing domain entails nothing more than redrawing the boundary between the two.” *Id.* at 10 (citing Ex. 1020 ¶ 26). Be that as it may, it still begs the question of where the boundary is being drawn by Petitioner. It was Petitioner who drew that original boundary in the Petition where the “Sequential Circuit Element” 305 is inside the “Programmable Logic Block” to satisfy claim element 1.b. Pet. 20. Now, in response to Patent Owner's arguments (PO Resp. 41), Petitioner switches gears, abandons the boundary of the Programmable Logic Block it drew in the Petition, and apparently abandons its contention that the “programmable logic block” corresponds to the everything inside the box labeled “107” in Figure 3A of Ting. Pet. Reply 7.

Petitioner's Reply argues for the first time that “the Board may apply the ‘new or different function’ test to determine obviousness” and that “[a]lthough claims 1–18 and 23–25 recite that the sequential circuit/logic element be placed in the routing domain/resources/matrix, the arrangement does not cause the sequential element and the overall architecture to perform a ‘new or different function.’” Reply 9–10 (citing *Lincoln Eng'g Co. v. Stewart-Warner Corp.*, 303 U.S. 545, 549 (1938); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 60 (1969); and three PTAB decisions). Although we recognize that the Petition asserts obviousness, neither the new boundary nor the “new or different function test” arguments are advanced in the Petition and are improper in Petitioner's Reply. Moreover, Petitioner's “new or different function test” arguments relies

entirely on conclusory statements from Dr. Sechen that merely parrot the arguments in Petitioner's Reply (Ex. 1020 ¶¶ 24–25); even if these arguments were timely, the arguments are not supported by sufficient evidence to be persuasive.

2. Conclusion Regarding Ground 1

For the reasons explained above, we determine Petitioner's Reply includes improper arguments and Petitioner has not presented clear and cohesive challenges to claims 1–18 and 23–25. Based on the complete record, we determine Petitioner has not satisfied its burden to show by a preponderance of the evidence that claims 1–18 and 23–25 are unpatentable.

F. Ground 2: Ting and Pani

The Petition includes a claim-by-claim, limitation-by-limitation comparison of claims 19–22 to the teachings of Ting and Pani. Pet. 91–128. Petitioner also presents reasons to combine Ting and Pani. Pet. 128–129. Patent Owner did not specifically address Petitioner's showings regarding claims 19–22 in Patent Owner's Response. Counsel for Patent Owner stated during oral arguments that “[w]e are not contesting Ground 2 or [claims 19–22].” Paper 27, 60:2–5. Nonetheless, the burden remains on Petitioner to establish the unpatentability of claims 19–22 by a preponderance of the evidence.

1. Reasons to Combine Ting and Pani

Petitioner contends both Ting and Pani are directed to FPGAs, have a common inventor, and have a common assignee. Pet. 128 (citing Ex. 1002 ¶ 228). Further Petitioner contends “Pani even indicates that it is meant to be combined with the disclosures of Ting” because Pani's specification twice refers to Ting as examples of compatible disclosures. Pet. 128 (citing Ex. 1006, 5:17–20, 8:31–35; Ex. 1002 ¶ 228). According to Petitioner, Ting

and Pani disclose different components of the same logic device, with “Pani disclos[ing] improvements over a conventional bus system because Pani’s programmable connections between multiple cells without permanent wiring increases the versatility of a programmable logic device.” Pet. 129 (citing Ex. 1006, 2:19–33, 5:6–20; Ex. 1006 ¶ 230). Further, Petitioner states that “[i]t would have been obvious to a POSITA to take the configuration disclosed by Ting, and apply the slight variation disclosed by Pani, in order to create an FPGA that could perform different logic functions.” Pet. 129 (citing Ex. 1002 ¶ 231).

Based on the evidence of record, including the testimony of Dr. Sechen, we determine Petitioner has articulated adequate reasons for combining the teachings of Ting and Pani. In particular, we agree with Petitioner that the references describe complimentary technology and that Pani provides an express suggestion to combine its teachings with Ting’s teachings.

2. Claim 19

19.pre: An electronic circuit, comprising:

Although neither party addresses whether the preamble is limiting, Petitioner contends that Ting discloses an integrated circuit, which a POSITA would understand to be an electronic circuit. Pet. 56, 91 (citing Ex. 1002 ¶ 233).

19.a: a circuit node input operable to receive a logic signal;

Petitioner contends Ting discloses a circuit node input capable of receiving a logic signal from elsewhere in the circuit. Pet. 91–92 (citing Ex. 1002 ¶ 236; Ex. 1005 Fig. 3A). Petitioner also contends Pani discloses a circuit node input capable of receiving a logic signal from a configurable

function generator. Pet. 92–93 (citing Ex. 1006 5:46–53, Fig. 4A; Ex. 1002 ¶ 237).

19.b: a flip-flop having an input node and an output node, the input node coupled with the circuit input node via no circuit element other than one or more first switches;

Petitioner states that “[t]he term ‘circuit input node’ lacks an antecedent basis and therefore renders claim [19] ambiguous,” but the Petition treats “circuit input node” as a reference to the claimed “circuit node input.” Pet. 93. Petitioner states that Ting discloses a flip-flop with an input node and an output node with the input node coupled with the interconnect matrix that provides an input to the sequential circuit element, which could be a circuit input node via no circuit element other than one or more first switches. Pet. 93 (citing Ex. 1002 ¶ 240). Petitioner also states that Pani discloses a flip-flop with an input node and an output node, the input node coupled with the circuit input node via no circuit element other than one or more first switches. Pet. 94 (citing Ex. 1002 ¶ 241). Further, Petitioner quotes Pani’s disclosure that “[t]o ensure minimal signal delays during processing, separate, direct connections are provided between the D flip flop 408 and the three input CFGs 404, 406,” and those connections include no circuit element other than switches 450–455. Pet. 95 (quoting Ex. 1006, 6:24–28) (emphasis omitted).

19.c: a second switch operable to couple the circuit input node with a distribution node;

Petitioner contends Ting discloses a switch operable to couple the circuit input node with the distribution node. Pet. 95 (citing Ex. 1002 ¶ 245; Ex. 1005, Fig. 3A). Petitioner also cites Pani as disclosing a second switch operable to couple the circuit input node with the distribution node. Pet. 96

(citing Ex. 1002 ¶ 246, Fig. 4A). Petitioner also quotes Pani's disclosure that "[t]o ensure minimal signal delays during processing, separate, direct connections are provided between the D flip flop 408 and the three input CFGs 404, 406," including switches 450–455. Pet. 97 (quoting Ex. 1006, 6:24–28) (emphasis omitted).

19.d: a third switch operable to couple the flip-flop output node with the distribution node; and

Petitioner contends Ting discloses a third switch operable to couple the flip-flop output node with the distribution node. Pet. 97–98 (citing Ex. 1002 ¶ 250, Ex. 1005, Fig. 3A). Petitioner also contends Pani discloses a third switch operable to couple the flip-flop output node with the distribution node. Pet. 98–99 (citing Ex. 1002 ¶ 251; Ex. 1006, Fig. 4A). Petitioner further contends that Pani's Figure 4A discloses that switches 450–455 and connected lines provide connections between the input and output of the three CFGs 404, 406 and the register 408 to provide a one bit multiplexing function. Pet. 99 (citing Ex. 1006 6:26–33; Ex. 1002 ¶ 252). Petitioner also quotes Pani's disclosure that "the output signal of the D flip-flop is also programmable through switches 452 and 453" and "[b]y selectively enabling switches 452 or 453 and selective switches of the I-Matrix, the output signal can be routed to any one of the elements of the cluster or of other clusters." Pet. 99 (quoting Ex. 1006, 6:46–54 (emphasis omitted); citing Ex. 1002 ¶ 253).

19.e: a plurality of distribution switches, each distribution switch operable to couple the distribution node to a respective distribution output node.

Petitioner contends Ting's Figure 3A shows that the distribution node includes interconnect line 334 as part of the intraconnect matrix. Pet. 100

(citing Ex. 1002 ¶ 255; Ex. 1005, Fig. 3A). Petitioner also contends Ting's Figure 3B discloses a plurality of distribution switches 339, 344, 349, and 354 operable to couple the distribution node with the respective distribution output nodes. Pet. 100–101 (citing Ex. 1002 ¶ 256; Ex. 1005, Fig. 3B). Petitioner also cites Pani as disclosing a plurality of distribution switches 441–443 operable to couple the distribution node with the respective distribution output nodes. Pet. 101–102 (citing Ex. 1002 ¶ 257; Ex. 1006, Fig. 4A). Petitioner also quotes Pani's disclosure that "[t]he routing of the output signal of the D flip-flop is also programmable through switches 452 and 453" and that "[b]y selectively enabling switches 452 or 453 and selective switches of the I-Matrix, the output signal can be routed to any one of the elements of the cluster or of other clusters. . . . The signal output is selectively routed through the switches 433–435 adjacent to the CFG 204 or to switches 441, 442 and 443 adjacent to CFG 406." Pet. 102 (quoting Ex. 1006, 6:46–53 (emphasis omitted); citing Ex. 1002 ¶ 253).

3. Conclusion Regarding Claim 19

Based on the evidence of record, we determine Petitioner has shown by a preponderance of the evidence that claim 19 is unpatentable based on the combined teachings of Ting and Pani.

4. Claim 20

The electronic circuit of claim 19 wherein: the second and third switches each have a respective couple state and a respective decouple state; and the couple/decouple states of the second switch and the third switch are mutually exclusive.

With reference to Ting's Figure 3A, Petitioner contends Ting discloses second switch 321 and third switch 320 which can be coupled and decoupled to allow for differing logic functions. Pet. 102–105 (citing

Ex. 1002 ¶¶ 260–262, 267; Ex. 1005, 7:41–46, Fig. 3A). Petitioner also states that Pani discloses second switch 454 and third switch 453 which are mutually exclusive because they are inverse to each other. Pet. 104–106 (citing Ex. 1002 ¶¶ 264, 268, 269; Ex. 1006, 6:35–40, Fig. 4A).

5. Conclusion Regarding Claim 20

Based on the evidence of record, we determine Petitioner has shown by a preponderance of the evidence that claim 20 is unpatentable based on the combined teachings of Ting and Pani.

6. Claim 21

21.pre: An electronic circuit, comprising:

Although neither party addresses whether the preamble is limiting, Petitioner contends that Ting discloses an integrated circuit, which a POSITA would understand to be an electronic circuit. Pet. 56, 106–107 (citing Ex. 1002 ¶ 272)

21.a: a circuit node input operable to receive a logic signal;

Petitioner contends Ting and Pani both disclose a circuit node input operable to receive a logic signal. Pet. 107–109 (citing Ex. 1002 ¶¶ 273, 274; Ex. 1005, Fig. 3A; Ex. 1006, 4A).

21.b: a flip-flop having an input node and an output node, the input node coupled with the circuit input node;

Petitioner contends Ting and Pani both disclose a flip-flop having an input node and an output node, with the input node coupled to the circuit input node. Pet. 109–111 (citing Ex. 1002 ¶¶ 275, 276; Ex. 1005, Fig. 3A; Ex. 1006, Fig. 4A).

21.c: a first switch operable to couple the circuit input node with a distribution node;

Petitioner contends Ting and Pani both disclose a first switch operable to couple the circuit input node with the distribution node. Pet. 111–113 (citing Ex. 1002 ¶¶ 277–279; Ex. 1005, Fig. 3A; Ex. 1006, 6:24–28, Fig. 4A).

21.d: a second switch operable to couple the flip-flop output node with the distribution node;

Petitioner contends Ting and Pani both disclose a second switch operable to couple the flip-flop output node with the distribution node. Pet. 114–115 (citing Ex. 1002 ¶¶ 280–282; Ex. 1005, Fig. 3A; Ex. 1006, 6:26–33, 6:46–50, Fig. 4A).

21.e: a plurality of distribution switches, each distribution switch operable to couple the distribution node to a respective distribution output node;

Petitioner contends that Ting and Pani both discloses a plurality of distribution switches that are operable to couple the distribution node with the respective distribution output nodes. Pet. 116–118 (citing Ex. 1002 ¶¶ 283–286; Ex. 1005, Fig. 3A, 3B; Ex. 1006, 6:46–53, Fig. 4A).

21.f: a third switch operable to couple the circuit input node to the first switch; and

Petitioner contends that Ting and Pani both disclose a third switch operable to couple the circuit input node to the first switch. Pet. 119–120 (citing Ex. 1002 ¶¶ 288–291; Ex. 1005, 7:13–15, Fig. 3A; Ex. 1006, 6:24–28, 6:40–41, Fig. 4A).

21.g: a fourth switch operable to couple the circuit input node to the second switch.

Petitioner contends Ting and Pani both disclose a fourth switch operable to couple the input node to the second switch. Pet. 121–122 (citing

Ex. 1002 ¶¶ 294–297; Ex. 1005 7:41–46, Fig. 3A; Ex. 1006, 6:24–28, 6:35–37, Fig. 4A).

7. Conclusion Regarding Claim 21

Based on the evidence of record, we determine Petitioner has shown by a preponderance of the evidence that claim 21 is unpatentable based on the combined teachings of Ting and Pani.

8. Claim 22

The electronic circuit of claim 21 wherein: the third and fourth switches each have a respective couple state and a respective decouple state; and the couple/decouple states of the third switch and the fourth are mutually exclusive.

Petitioner contends Ting discloses third and fourth switches that can be turned on or off (in a couple or decouple state) to perform different logic functions. Pet. 122–124, 125–127 (citing Ex. 1005, 7:13–15, 7:41–46, Fig. 3A; Ex. 1002 ¶¶ 300, 301, 306, 307). Petitioner also contends Pani discloses third and fourth switches that can be turned on or off (in a couple or decouple state). Pet. 124–125 (citing Ex. 1006, 6:24–28, Fig. 4A; Ex. 1002 ¶¶ 302, 303). Petitioner also states that Pani expressly discloses that the couple/decouple states of the third and fourth switches are mutually exclusive. Pet. 127–128 (citing Ex. 1006, 6:35–37; Ex. 1002 ¶¶ 307, 308).

9. Conclusion Regarding Claim 22

Based on the evidence of record, we determine Petitioner has shown by a preponderance of the evidence that claim 22 is unpatentable based on the combined teachings of Ting and Pani.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 19–22 are

unpatentable in view of Tang and Pani, but Petitioner has not proven the unpatentability of any of claims 1–18 or claims 23–25.⁶

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has proven by a preponderance of the evidence that claims 19–22 of the '299 patent are unpatentable;

FURTHER ORDERED that Petitioner has not proven by a preponderance of the evidence that claims 1–18 and 23–25 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

In summary:

Claims	35 U.S.C. §	References/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–18, 23–25	103	Ting		1–18, 23–25
19–22	103	Ting, Pani	19–22	
Overall Outcome			19–22	1–18, 23–25

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

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