

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIEMENS INDUSTRY SOFTWARE INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

IPR2021-01212
Patent 7,546,567 B2

Before JENNIFER MEYER CHAGNON, SCOTT C. MOORE, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Siemens Industry Software Inc. (“Petitioner”)¹ filed a Petition requesting *inter partes* review of claims 1–8, 11–20, and 23–25 (“the challenged claims”) of U.S. Patent No. 7,546,567 B2 (Ex. 1001, “the ’567 patent”). Paper 1 (“Pet.”). Synopsys, Inc. (“Patent Owner”)² filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314, which provides that an *inter partes* review may be instituted only upon a showing that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Moreover, if the Board institutes a trial, the Board will institute on all challenges raised in the petition. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355–56 (2018) (“*SAS*”) (holding that a decision to institute under 35 U.S.C. § 314 may not institute review on fewer than all claims challenged in the petition); *see also* Patent Trial and Appeal Board Consolidated Trial Practice Guide 64 (Nov. 2019), <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf> (“CTPG”) (“The Board will not institute on fewer than all claims or all challenges in a petition.”).

Applying those standards, and upon consideration of the information presented in the Petition and the Preliminary Response, as well as the

¹ Petitioner states that Siemens Industry Software Inc. is a real party-in-interest in this proceeding. Pet. ix. Petitioner also identifies Siemens AG and Siemens Corporation as real parties-in-interest “[o]ut of an abundance of caution.” *Id.*

² Patent Owner identifies itself, Synopsys, Inc., as the real party-in-interest. Paper 4, 1.

evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review of all challenged claims of the '567 patent, based on all grounds identified in the Petition.

The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely-filed response may be deemed waived, even if they were presented in the Preliminary Response.

A. Related Proceedings

The parties identify *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-004151-WHO (N.D. Cal.) (“the related district court proceeding”) as a related matter involving the '567 patent. Pet. ix; Paper 4, 1. Patent Owner also identifies IPR2021-01213 and IPR2021-01215, which challenge additional patents involved in the related district court proceeding. Paper 4, 1.

B. The '567 Patent

The '567 patent, titled “Method and Apparatus for Generating a Variation-Tolerant Clock-Tree for an Integrated Circuit Chip,” was filed on January 10, 2007, and issued on June 9, 2009. Ex. 1001, codes (22), (45), (54). The '567 patent “relates to techniques for designing clock distribution networks for integrated circuit (IC) chips.” *Id.* at 1:9–10.

The Background section of the '567 patent explains that

[t]he speed of a system on an integrated circuit (IC) chip is largely determined by system clock frequency. In a typical synchronous IC chip, a clock distribution network (referred to as a “clock-tree”) is used to distribute a clock signal from a common source to various circuit components. This clock signal is used to coordinate data transfers between circuit components. However, as increasing clock frequencies reduce the clock periods to fractions of a nanosecond, designing clock-trees is becoming increasingly more challenging. A direct result of the decreasing clock period is a shrinking “timing budget” between logically coupled clock sinks. This decreasing timing budget is requiring clock-trees to have minimal clock skew.

Id. at 1:23–35.

The '567 patent further recognizes that “variations” contribute to clock skew, and are “one of the more significant challenges in synchronous clock-tree design.” *Id.* at 1:37–39. Such “variations can include: manufacturing process variations, operational voltage variations, and ambient temperature variations.” *Id.* at 1:39–41. Variations that occur within a chip boundary are referred to as “on-chip variations” (“OCV”). *Id.* at 1:41–43. On-chip variations may result in “limit[ed] performance of the chip, and even threaten[] the functionality of the chip.” *Id.* at 1:43–46. On-chip variations also may “cause[] uncertainty in clock arrival times at circuit components,” which, in turn, “can cause clock skew.” *Id.* at 1:47–50.

One embodiment of the present invention relates to a process that generates a clock-tree on an integrated circuit (IC) chip. During operation, the process starts by receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout. The process then generates a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers. Next, the process clusters the set of registers based on the timing criticality

profile to create a clock-tree for the set of registers. By clustering the registers based on the timing criticality profile, the process facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs.

Id. at 2:12–25.

Figure 3 of the '567 patent is reproduced below.

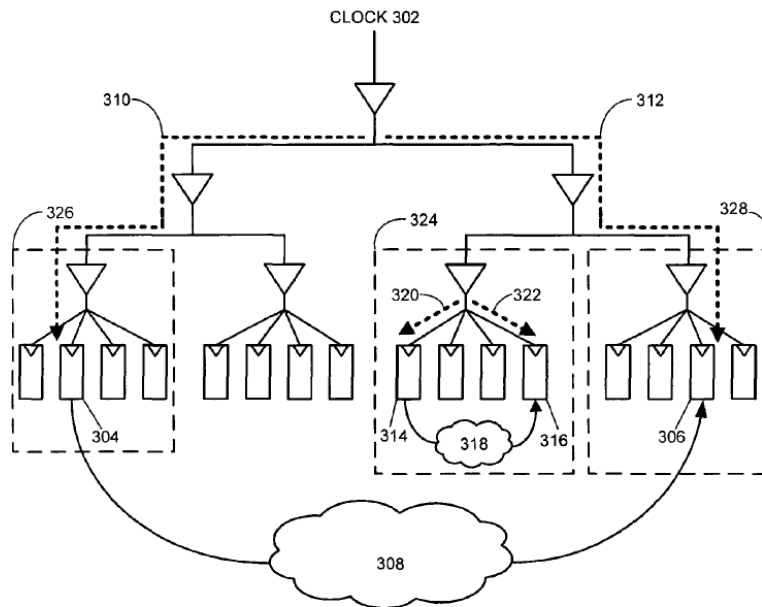


FIG. 3

Figure 3, above, is an “exemplary clock-tree structure 300 with leaf-level registers in accordance with an embodiment” of the '567 patent. Ex. 1001, 6:22–24. The '567 patent describes Figure 3 as follows:

Clock-tree structure 300 includes a main clock source 302 at the root of clock-tree 300, two middle levels of clock-buffers, and a leaf-level comprising a set of clustered registers. Registers 304 and 306 form a launcher/capturer pair which is logically coupled through a data path 308. When comparing the two clock paths from clock 302 to registers 304 and 306, note that branch 310 and branch 312 are the non-shared “private” sections of the two clock paths, respectively. These two private branches contain a total of four unshared clock buffers.

Registers 314 and 316 form another launcher/capturer pair which is logically coupled through a data path 318. Note that the clock paths for registers 314 and 316 are mostly shared, and the private sections of the two clock paths are branch 320 and branch 322, respectively. These two private branches are both local branches which contain no clock buffers. Note that register pair 314/316 achieves a significantly more clock-path sharing than the register pair 304/306.

Id. at 6:25–43. The '567 patent describes that “[i]n this embodiment, OCV causes a much more severe impact on data path 308 than on data path 318.”

Id. at 6:47–48. “[G]enerally registers within a same cluster, for example in cluster 324, are less vulnerable to OCV than register pairs in different clusters, for example, between cluster 326 and cluster 328.” *Id.* at 6:49–52.

According to the '567 patent, “[t]he present invention provides a technique for improving overall timing performance of an IC chip in the presence of clock variations.” *Id.* at 5:2–4. In particular, embodiments of the '567 patent accomplish this by “maximiz[ing] commonly-shared clock paths (including clock buffers and clock nets) to the registers in the IC design if they have tighter timing constraints between them.” *Id.* at 5:6–9. “[S]tarting from leaf-level clustering, the present invention attempts to maximize the inclusion of the timing critical register pairs into the same cluster.” *Id.* at 5:13–15.

C. Illustrative Claim

Of the challenged claims, claims 1, 13, and 25 are independent. Claims 2–8, 11, and 12 depend from claim 1; and claims 14–20, 23, and 24 depend from claim 13. Independent claim 1 of the '567 patent is reproduced below, and is illustrative of the challenged claims.

1. [1.p] A method for generating a clock-tree on an integrated circuit (IC) chip, comprising:

[1.a] receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout;

[1.b] generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers; and

[1.c] clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers, [1.d] wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other;

[1.e] wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs.

Ex. 1001, 10:55–11:7 (bracketed identifying labels added).

D. The Applied References

Petitioner relies on the following references in the asserted grounds.

Pet. 6.

Reference	Issue Date/ Publication Date	Exhibit
U.S. Patent No. 6,651,224 B1 (“Sano”)	Nov. 18, 2003 ³	Ex. 1004
U.S. Patent No. 6,367,060 B1 (“Cheng”)	Apr. 2, 2002 ⁴	Ex. 1005
Naveed A. Sherwani, <i>Algorithms for VLSI Physical Design Automation</i> , 3 rd ed. (Kluwer Academic Publishers) (1999) (“Sherwani”)	1999 ⁵	Ex. 1006

Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003) to support its positions.

³ Sano is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 20.

⁴ Cheng is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 59.

⁵ Petitioner’s expert, Dr. Robins, testifies that Sherwani was “a well-known and widely utilized textbook” that was “known and readily available to [persons of ordinary skill in the art] throughout the early 2000s, and certainly prior to 2006.” Ex. 1003 ¶¶ 200–201. Petitioner, thus, contends Sherwani is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 81. At this stage of the proceeding, Patent Owner does not challenge the status of this reference as prior art. *See generally* Prelim. Resp.

E. The Asserted Grounds

Petitioner sets forth its challenges to claims 1–8, 11–20, and 23–25 on the following grounds. Pet. 6.

Reference(s)	35 U.S.C. §	Claims Challenged
Sano	103 ⁶	1–8, 11–20, 23–25
Cheng	103	1–7, 11–19, 23–25
Cheng and Sherwani	103	4, 8, 16, 20

II. ANALYSIS

A. Discretion Under 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv* Order”), weigh in favor of denying institution. Prelim. Resp. 6. We authorized additional briefing on this issue. *See* Petitioner’s Reply to Patent Owner’s Preliminary Response, Paper 9 (“Reply”), and Patent Owner’s Sur-Reply to Petitioner’s Reply to Patent Owner’s Preliminary Response, Paper 10 (“Sur-Reply”). For the reasons discussed, we do not exercise discretion to deny institution.

⁶ Because the application leading to the ’567 patent was filed before March 16, 2013, patentability is governed by the version of 35 U.S.C. §§ 102 and 103 preceding the Leahy-Smith America Invents Act (“AIA”), Pub L. No. 112-29, 125 Stat. 284 (2011).

1. Legal Standards

Under 35 U.S.C. § 314(a), the Director has discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS*, 138 S. Ct. at 1356 (“[Section] 314(a) invests the Director with discretion on the question whether to institute review.” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”). The Director has delegated this authority under 35 U.S.C. § 314(a) to the Board. 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

In determining whether to exercise discretion to deny institution under 35 U.S.C. § 314(a), the Board considers whether the circumstances of a parallel district court proceeding are a basis for exercising such discretion. *Fintiv* Order 5–6; *see also NHK Spring Co., Ltd. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19–20 (PTAB Sept. 12, 2018) (precedential) (denying institution relying, in part, on § 314(a) because the parallel district court proceeding was scheduled to finish before the Board reached a final decision). The Board evaluates the following nonexclusive factors (“*Fintiv* factors”):

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;

5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv Order 5–6. In evaluating these factors, “the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* at 6.

2. *Analysis of the Fintiv Factors*

We consider each of the factors set forth in the *Fintiv* Order. We then weigh the factors and take a holistic view of whether efficiency and integrity of the patent system are best served by denying or instituting review.

Factor 1: whether a stay exists or is likely to be granted if a proceeding is instituted

Petitioner represents that the district court case is stayed “until at least February 2022.” Reply 1. Petitioner argues that, although not for the pending *inter partes* review, this stay should weigh against discretionary denial. *Id.* at 1–2. Petitioner further argues that further stay will be sought if *inter partes* review is instituted, and that prior actions of the district court judge in other cases indicate that such a stay is likely. *Id.* at 2–3.

Patent Owner argues that this factor favors discretionary denial because Petitioner has not asked for a stay pending *inter partes* review, and presents reasoning why the district court judge might deny such a stay. Sur-Reply 1–3.

“A district court stay of the litigation pending resolution of the PTAB trial allays concerns about inefficiency and duplication of efforts.” *Fintiv* Order 6. On the record before us, Petitioner has not produced evidence that

a stay for the results of the instant *inter partes* review has been requested. The district court stay currently in force is for a limited time, until February 2022. Thus, the stay will expire approximately one month after issuance of this decision on institution. The effect of the current stay on the pending *inter partes* review proceeding would be extremely minimal, and would not appear to meaningfully allay any concerns of inefficiency or duplication of efforts.

Furthermore, the parties' reliance on other cases in which the district court judge considered requests for stay is misplaced. As the Board has explained, "[a] judge determines whether to grant a stay based on the facts of each specific case as presented in the briefs by the parties." *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) ("*Fintiv* DI"). "We decline to infer, based on actions taken in a different case with different facts, how the District Court would rule should a stay be requested by the parties in the parallel case here." *Id.*

Accordingly, we find that this factor is neutral; i.e., it does not weigh for or against exercising our discretion to deny institution.

Factor 2: proximity of the court's trial date to the Board's projected statutory deadline

Petitioner argues that the trial date of September 26, 2022, no longer applies because earlier deadlines have not been met due to the district court's stay. Reply 3–4. Petitioner argues that the five month stay will cause the trial date to be delayed until at least March 2023, after the expected January 2023 final written decision in this *inter partes* review. *Id.* at 4.

Patent Owner argues that the district court has not issued an amended trial date. Sur-Reply 3; *see also* Prelim. Resp. 10. Patent Owner further argues that there is no certainty that the trial date will be delayed later than the existing September 2022 trial date. Sur-Reply 3–4.

Although Petitioner speculates that the dates in the original trial schedule no longer apply, Petitioner has not produced evidence of an updated scheduling order in the related district court proceeding that would affect the trial date. However, we appreciate Petitioner’s point that the fact that some dates in the district court’s existing scheduling order have not been met renders uncertain the remaining dates. For purposes of this factor, Petitioner has shown some uncertainty as to whether the trial in the related district court proceeding will go forward before the final written decision is due in this proceeding. In view of the foregoing, we determine that this factor is neutral.

Factor 3: investment in the parallel proceeding by the court and parties

Petitioner argues that this factor weighs against discretionary denial because significant district court work remains and cannot commence until at least February 2022. Reply 4. Petitioner represents that the parties “have taken no fact depositions and other significant fact discovery remains, as does other resource-intensive work, such as expert reports and depositions, and dispositive motions.” *Id.* (citing Ex. 2008, 1). Petitioner further argues that it “moved with reasonable diligence” because the petition was filed three months after final infringement contentions were served, and less than a week after mediation between the parties. *Id.* at 5. Petitioner contends that

such delay was due to a hope that the parties could resolve their differences through a mediated settlement. *Id.*

Patent Owner asserts that Petitioner waited until the final day of its one year statutory period to file its petition, and that Petitioner “offered no justification for this dilatory tactic.” Prelim. Resp. 15. Patent Owner further argues that substantial work, including for example “exchange[of] infringement, invalidity, and damages contentions” and “claim construction,” has been done by the parties and the court, which has a “deep knowledge of the facts and technology,” and that this factor thus weighs in favor or denying institution. *Id.* at 11–15.

Based on the present record, we are persuaded by Petitioner’s showing that the district court and the parties have not invested substantially in the merits of the invalidity positions. The district court addresses two terms of the ’567 patent in its claim construction order.⁷ Ex. 2001, 3–12. For both terms, Petitioner indicates that the Petition adopts Patent Owner’s proposed litigation constructions (Ex. 1010) for those terms, and that because the grounds set forth in the Petition meet those constructions, no further construction is required. Pet. 15–16. Petitioner further contends that the asserted “grounds meet the[district court’s] tentative constructions.” *Id.* at 16; *see also id.* at 34, 64; Ex. 1009, 1–2.

There is no indication in the record that the parties have completed significant discovery on the merits. Although the parties and the court have invested some effort, a significant portion of work still remains to be done in the district court proceeding—e.g., the completion of fact and expert

⁷ The claim construction order also adopts the parties’ agreed upon constructions for one other term. Ex. 2001, 9.

discovery and dispositive motions. We find instructive the similar investment in *Sand Revolution II*, which involved a *Markman* order and recognized that fact discovery, expert reports, and substantive motion practice remained. *Sand Revolution II, LLC v. Cont'l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 10–11 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”). *Sand Revolution* weighed factor 3 “marginally, if at all, in favor of denial.” *Id.* at 11.

Moreover, Petitioner’s delay is mitigated by its prompt filing after a mediation session between the parties. Although Patent Owner faults the Petitioner because Petitioner did not incur *inter partes* review costs until after the mediation session, Patent Owner does not explain why it would not be reasonable to delay seeking action until mediation was unsuccessful. Patent Owner does not explain or allege why such mediation might not reasonably have some probability of resolving the issues such that filing *inter partes* review would have been unnecessary. We find it reasonable for Petitioner to have waited until after the mediation to file its Petition.

Therefore, weighing the facts in this particular case, including the time invested by the parties and the court in the related district court proceeding, the extent to which the investment in the district court proceeding relates to issues of patent validity, and the timing of the filing of the Petition, we find that this factor weighs marginally, if at all, in favor of exercising discretion to deny institution.

Factor 4: overlap between issues raised in the petition and in the parallel proceeding

Patent Owner argues that “Siemens’ petition asserts *virtually identical* claims, arguments, and evidence as those presented to the district court.

Siemens' IPR petition challenges the same claims of the '567 patent, claims 1–8, 11–20 and 23–25, as are at issue before the district court.” Prelim.

Resp. 16. Patent Owner argues that both alleged bases for obviousness in the Petition rely on references that were asserted in the related district court proceeding. *Id.* at 16–17.

Petitioner provides a stipulation not to pursue any instituted *inter partes* review ground in district court. Reply 5 (citing Ex. 1017). The stipulation states, “Siemens stipulates that, should [*inter partes* review] be instituted in IPR2021-01212, -01213, or -01215, then Siemens will not pursue in the N.D. Cal. district court litigation any prior art invalidity defense that is the same as a ground of unpatentability in any instituted IPR.” Ex. 1017, 1. Petitioner argues that this moots overlap and weighs at least slightly against discretionary denial in factor 4, citing *Sand Revolution*. Reply 5.

In response to the stipulation, Patent Owner argues that Petitioner's stipulation fails to cure any potential overlap and that Petitioner is free to pursue arguments using the same prior art, provided that the art is combined in different ways. Sur-Reply 5. Patent Owner argues that this stipulation at best “marginally” mitigates overlap of issues, citing *Google LLC v. Ikorongo Tech. LLC*, IPR2021-00204, Paper 13 at 10–12 (PTAB June 7, 2021). Reply 5.

We are persuaded by Petitioner's arguments that the overlap in proceedings is limited as a result of the stipulation. Notably, Petitioner's stipulation is similar to the stipulation provided in *Sand Revolution*. *Sand Revolution* 12 n.5. In *Sand Revolution*, the Petitioner stipulated “only that it will not pursue, in district court, the ‘same grounds’ presented in the

Petition.” *Id.* Consistent with *Sand Revolution*, we find Petitioner’s stipulation mitigates to some degree the concerns of duplicative efforts between district court and the Board, as well as concerns of potentially conflicting decisions. *See id.* at 11–12. Thus, we find that this factor weighs somewhat against exercising discretion to deny institution.

Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

It is undisputed that Petitioner is a defendant in the related district court proceeding. Patent Owner argues that this favors denying institution. Prelim. Resp. 18.

As the Board explained in *Fintiv*, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact *against exercising discretion* to deny institution under *NHK*.” *Fintiv* Order 13–14 (emphasis added). The Board determined in *Sand Revolution* that “[a]lthough it is far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same, or where a district court is scheduled to go to trial before the Board’s final decision would be due in a related *inter partes* review, this factor weighs in favor of discretionary denial.” *Sand Revolution* 12–13. The Board has also held that “[b]ecause the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.” *Fintiv* DI 15. Here, although it is undisputed that Petitioner is a defendant in the related district court proceeding, it is unclear whether the related district court proceeding will go to trial before the final written decision is due in this proceeding. Therefore, we find that factor 5 is neutral.

Factor 6: other circumstances and considerations that impact the Board's exercise of discretion, including the merits

The final *Fintiv* factor is a catch-all that takes into account any other relevant circumstances. The decision whether to exercise discretion to deny institution is based on “a balanced assessment of all relevant circumstances in the case, including the merits.” CTPG 58. “For example, if the merits of a ground raised in the petition seem particularly strong on the preliminary record, . . . the institution of a trial may serve the interest of overall system efficiency and integrity because it allows the proceeding to continue in the event that the parallel proceeding settles or fails to resolve the patentability question presented in the PTAB proceeding.” *Fintiv* Order 14–15. A full merits analysis is not necessary as part of deciding whether to exercise discretion not to institute, but rather the parties may point out, as part of the factor-based analysis, particular “strengths or weaknesses” to aid the Board in deciding whether the merits tip the balance one way or another. *Id.* at 15–16.

Petitioner argues that the lack of any substantive merits-based argument by Patent Owner confirms the strength of the Petition, thus favoring institution. Reply 5. Patent Owner argues that the claims are at least novel, because Petitioner has not raised any anticipation grounds. Prelim. Resp. 18. Patent Owner further argues that the petition fails to address in full the district court’s claim constructions. *Id.* at 18–19. Patent Owner argues that factor six therefore favors denial. *Id.* at 19.

Patent Owner’s arguments are unavailing as to this factor. At this preliminary stage of this proceeding, Patent Owner proffers no substantive arguments to rebut Petitioner’s asserted ground of unpatentability. We have reviewed Petitioner’s unpatentability arguments and supporting evidence.

As discussed below, on this record, we determine that Petitioner has demonstrated sufficiently for purposes of this Decision that the challenged claims of the '567 patent are unpatentable. We find this factor is neutral.

Conclusion

As noted in *Fintiv*, we consider the above six factors when taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* Order 6. In weighing the totality of the evidence, under the particular circumstances of this case, we are not persuaded that the interests of efficiency and integrity of the system would be best served by invoking our authority under 35 U.S.C. § 314(a) to deny institution of a potentially meritorious Petition. We, therefore, do not exercise discretion to deny institution.

B. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc.*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined the prior art references. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

We analyze the asserted grounds of unpatentability in accordance with these principles to determine whether Petitioner has met its burden to establish a reasonable likelihood of success at trial.

C. Level of Ordinary Skill in the Art

We review the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art at the time of the invention. *Graham*, 383 U.S. at 17. For purposes of this proceeding,

⁸ At this stage of the proceeding, the parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

Petitioner and Petitioner's expert "adopt[] the [following] definition for the person of ordinary skill in the art":

a minimum of a B.S. in Electrical Engineering, Computer Engineering, or Computer Science and at least five years of work experience in the VLSI design, electronic design automation for VLSI, or ASIC (application-specific integrated circuit) design fields or an M.S. in Electrical Engineering, Computer Engineering, or Computer Science and at least two years of work experience in those fields.

Pet. 13; Ex. 1003 ¶ 66.

Petitioner notes that this assessment was presented in the related district court proceeding by Patent Owner, and that Petitioner has argued for a higher level of skill in the art in the related district court proceeding.

Pet. 13; *see* Ex. 1003 ¶ 67. Here, Patent Owner has not provided an assessment of the level of ordinary skill in the art. *See generally* Prelim. Resp. To the extent necessary, and for purposes of this Decision, we accept the assessment offered by Petitioner as it is supported by Dr. Robins's testimony and is consistent with the '567 patent and the asserted prior art.

D. Claim Construction

For this *inter partes* review proceeding claim terms

shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). Further, "[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a

proceeding before the International Trade Commission, that is timely made of record in the *inter partes* review proceeding will be considered.” *Id.*

Under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc), claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *See Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

Petitioner identifies several claim terms for which the parties have agreed upon construction in the related district court proceeding. *See* Pet. 14–15 (citing Ex. 1008; Ex. 1016). Petitioner also identifies other claim terms for which Patent Owner has proposed construction in the related district court proceeding, and/or for which the district court has provided a tentative construction. *See id.* at 15–19 (citing Ex. 1008; Ex. 1009; Ex. 1010). Patent Owner does not address claim construction, at this stage of the proceeding. *See generally* Prelim. Resp.

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). We determine that express construction of the terms identified by Petitioner is not necessary at this stage of the proceeding.

E. Asserted Obviousness in view of Sano

Petitioner asserts that claims 1–8, 11–20, and 23–25 would have been obvious in view of Sano. Pet. 20–58. At this stage of the proceeding, Patent Owner does not present arguments regarding the patentability of the

challenged claims. *See generally* Prelim. Resp. (presenting only *Fintiv*-related arguments).

1. *Overview of Sano (Ex. 1004)*

Sano is titled “Method of Optimizing Signal Lines Within Circuit, Optimizing Apparatus, Recording Medium Having Stored Therein Optimizing Program, And Method Of Designing Circuit and Recording Medium Having Stored Therein Program For Designing Circuit.” Ex. 1004, code (54). Sano “relates to a technology utilized when designing a circuit which includes a signal supplying source (e.g., clock signal supplying source) within the circuit and a plurality of elements (e.g., flip-flop cells) supplied with a signal from the signal supplying source.” *Id.* at 1:12–16. The method “optimiz[es] signal lines within the circuit” to thereby optimize “delay or skew of a signal from the signal supplying source to each of the elements.” *Id.* at 1:17–26; *see also id.* at code (57) (the method “optimiz[es] the delay of a signal transmitting through signal lines connecting a signal supplying source to each of elements, whereby skew can positively be decreased.”).

In an embodiment, Sano “calculates evaluation values for every pair of the driven elements (initially [flip-flops]) based on an improving factor of the circuit quality.” *Id.* at 20:18–20. An evaluation value may be, for example, a “hold error evaluation value,”⁹ a “setup error evaluation value,”¹⁰

⁹ Sano describes that the “hold error evaluation value becomes larger with increase of the probability at which the hold error is taken place in each pair.” Ex. 1004, 8:17–19.

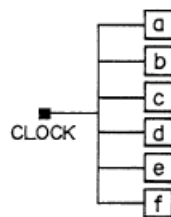
¹⁰ Sano describes that the “setup error evaluation value becomes larger with increase of the probability at which the setup error is taken place in each pair.” Ex. 1004, 8:22–24.

a “distance evaluation value,”¹¹ or combinations thereof. *See id.* at 8:12–9:2 (describing exemplary ways to calculate evaluation values); *see also id.* at Figs. 4, 7, 10, 11, 13, 14.

In Sano, pairs of flip-flops with a large evaluation value (e.g., the pair has a high hold error probability, a high setup error probability, or are placed close to each other), then “both of the elements constituting the pair tend to belong to the same group” which leads to prevention of the error and/or reduced wire length. Ex. 1004, 21:66–22:2, 23:18–25, 24:23–28, 25:11–16, 25:58–63. In other words, flip-flop pairs with a high evaluation value are grouped together. *See, e.g., id.* at 8:7–11 (“[T]he driven values [(i.e., flip-flops)] are divided into groups . . . so that . . . a pair having the largest evaluation value . . . is brought into the same group with priority.”).

Figures 3A to 3E “are diagrams illustrative of procedures for carrying out clock tree synthesizing processing according to [an] embodiment of [Sano].” *Id.* at 14:18–20. In the example of these figures, “one clock supplying element (CLOCK) supplies a clock signal to six (a to f) driven elements ([flip-flops]).” *Id.* at 19:62–64. Figure 3A is reproduced below.

FIG. 3A



¹¹ Sano describes that the “distance evaluation value becomes larger with increase in the physical distance for each pair.” Ex. 1004, 8:38–40.

Figure 3A shows “logic information or physical information about the clock supplying element and [flip-flops] which are driven elements.” *Id.* at 19:66–20:1.

Figures 3B, 3C, and 3D are reproduced below.

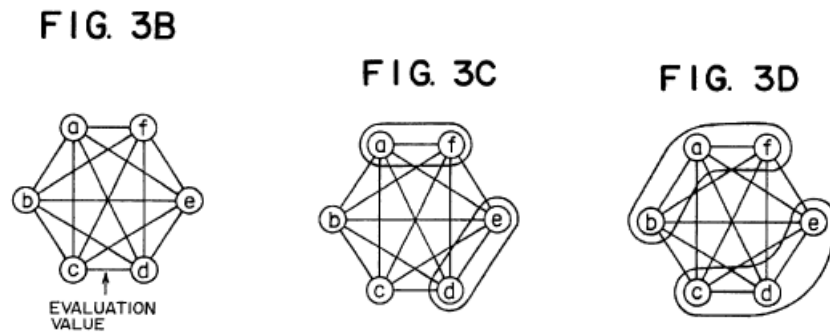


Figure 3B illustrates evaluation values that are calculated for every pair of flip-flops. *Id.* at 20:17–21. Figure 3C illustrates that “a pair having the largest evaluation value calculated at the evaluation value calculating unit 542 is made to belong (merge) to the same group with priority.” *Id.* at 20:26–28. As described in Sano, this process continues until the flip-flops are divided into a plurality of groups, as illustrated in Figure 3D. *See id.* at 20:24–47.

Figure 3E is reproduced below.

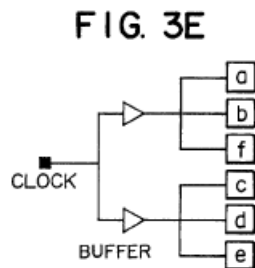


Figure 3E illustrates the resulting clock tree of the process described with respect to Figures 3B–3D. *Id.* at 20:48–52; *see also* Ex. 1003 ¶ 95.

Sano describes that this grouping strategy makes it “possible to create a clock tree in which [errors] can be positively prevented from occurrence,” “circuit quality can be remarkably increased,” “the clock skew can be positively suppressed with ease, wiring length can be shortened, and signal distribution can be more positively optimized.” *See, e.g.*, Ex. 1004, 25:64–26:3.

2. *Independent Claim 1*

We summarize Petitioner’s contentions and cited evidence as to claim 1, in the following.

[1.p] A method for generating a clock-tree on an integrated circuit (IC) chip, comprising¹²

Petitioner asserts that Sano discloses a method and system for creating a clock tree. *See* Pet. 26–27 (citing, *inter alia*, Ex. 1004, 14:18–20, 34:40–44; Ex. 1003 ¶¶ 78–79); *id.* at 27 (“Sano describes its clock tree generation method in detail in, e.g., FIGs. 2–14 and associated text.”).

Sano discloses that, in designing a circuit, “the optimizing apparatus optimizes signal distribution through clock signal lines (clock system net) connecting the clock supplying element to the number of [flip-flops] in terms of clock distribution.” Ex. 1004, 17:29–34; Pet. 26.

¹² We need not decide at this stage of the proceeding whether the preamble is limiting.

[1.a] receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout

Petitioner asserts that Sano discloses this element. *See* Pet. 27–31. Sano discloses that “an integrated circuit such as a VLSI has placed a number of driven elements (e.g., flip-flop cells . . .) which are to be driven synchronously in response to a clock signal. The driven elements are supplied with a clock signal through a clock signal line from a clock supplying source (source).” Ex. 1004, 1:34–40; Pet. 27. Dr. Robins testifies that a person of ordinary skill in the art “would have known that flip-flops were a type of register.” Ex. 1003 ¶ 81 (citing Ex. 1011, 42); Pet. 27–28.

Petitioner contends that “Sano discloses considering the placement of the flip-flops when building the clock tree, so ‘the clock tree is formed’ such that closely-located flip-flops (FFs) ‘belong to the same [clock tree] group.’” Pet. 28 (quoting Ex. 1004, 24:29–41); *see also* Ex. 1004, 24:11–17 (discussing analyzing “the physical distance between” the flip-flop elements in a given pair “based on floorplan information or placement information (layout information, physical information)”, 11:59–61 (“[W]hen the signal lines are wired, floorplan information or placement information is taken into consideration.”); Ex. 1003 ¶ 82. Sano discusses creating and using floorplan information for clock tree creation. *See, e.g.*, Ex. 1004, 6:63–65 (criticizing the prior art for not considering layout information in clock tree creation), 25:52–59 (describing how the “floorplan information file 10” includes placement information for “a plurality of modules each of which is composed of a plurality of flip-flop cells”), Fig. 21; Pet. 28–30; Ex. 1003 ¶¶ 83–84.

Relying on the testimony of Dr. Robins, Petitioner contends that a person of ordinary skill in the art “would have understood that analysis based on placement information . . . would necessarily involve first receiving [such placement information]” or that “it would have been at least obvious” “to implement the clock tree synthesis software of Sano such that it involved receiving placement information including [flip-flops] (registers) at locations fixed during a particular phase of clock tree synthesis.” Pet. 30–31; Ex. 1003 ¶¶ 86–87.

As to the claimed “*fixed* locations,” Petitioner asserts that a person of ordinary skill in the art “would have understood that the [flip-flops] (registers) were fixed during the Sano evaluation value-based clock-tree generation,” because “[t]he timing information used to create the setup evaluation value depended on the locations of the [flip-flops]” and “if the [flip-flops] were moved during this process then the evaluation values, and thus the corresponding clustering, would become unreliable.” Pet. 30; Ex. 1003 ¶ 85. Petitioner further contends that “it would have at least been obvious to keep the [flip-flops] at fixed locations so as to maintain accurate evaluat[ion] values, and thus high-quality clustering.” Pet. 30; Ex. 1003 ¶ 85.

[1.b] generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers

Petitioner asserts that Sano discloses this element. *See* Pet. 31–35. Sano discloses calculating an evaluation value for each of flip-flops in a circuit design. Ex. 1004, 8:1–9:2, 23:15–19, Figs. 2, 4, 7, 10, 11, 14. Petitioner contends that at least the disclosed “setup error” evaluation values

of Sano correspond to the claimed timing criticalities. Pet. 31; Ex. 1003 ¶ 89. Petitioner asserts that “the Sano ‘setup error’ evaluation *value* is computed for each [flip-flop] pair, and is *derived from the data path delay between [flip-flops] in a pair* and specifies a timing criticality between those [flip-flops], thus meeting the element under Synopsys’s own proposed construction.” Pet. 31 (emphasis added); *see also* Ex. 1010, 3 (Patent Owner’s proposed construction of “timing criticality between a pair of registers” in the district court is “value derived from the data path delay between a pair of registers connected by a data path”) (cited at Pet. 16–17). Supported by Dr. Robins’s testimony, Petitioner provides further details about the “well-known concept” of setup errors, and determining these values. *See* Pet. 32–33; Ex. 1003 ¶ 90.

According to Petitioner,

Each of these setup error evaluation values “specifies timing criticalities between pairs of registers” [as claimed] at least because each is “a numerical value indicating a setup error suppressing property” (*e.g.*, EX1004, 22:44-47) where “the value becomes larger with increase of the probability at which the setup error is taken place in the pair of elements” (23:12-13). *See also* EX1003, ¶91. In other words, the setup evaluation value indicates the relative likelihood that a setup error would occur between [flip-flops], based on the data path delay between those flip-flops. *Id.*

Pet. 33–34.

Relying on the testimony of Dr. Robins, Petitioner further asserts that a person of ordinary skill in the art would understand (1) “that these groups of setup evaluation values for the various pairs of [flip-flops] meet the ‘timing criticality profile for the set of registers’ because the group of values specifies timing criticalities between pairs of [flip-flops] in a set of [flip-flops]”; and (2) that “these evaluation values would necessarily be

generated by the processor [CPU 540] and stored in data structures in a part of the memory unit [530].” *Id.* at 34; Ex. 1003 ¶ 93.

[1.c] clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers

Petitioner asserts that Sano discloses this element. *See* Pet. 35–39. In particular, Petitioner asserts that

Sano discloses use of its set of setup error evaluation values to “group,” i.e., cluster, the [flip-flops] in order to create a clock tree for the [flip-flops]. *E.g.*, [Ex. 1004,] 19:9-16 (describing dividing [flip-flops] into groups based on evaluation value as part of clock tree synthesis); *id.*, 19:17-21, 19:41-46, 20:24-47; EX1003, ¶95. Sano FIGs. 3A-3E illustrate one manner in which evaluation values for [flip-flops] (items a-f in the figures) are used to group the [flip-flops] for clock tree generation.

Pet. 35. This process of Figures 3A–3E of Sano is discussed above at Section II.E.1. *See also* Pet. 35–39; Ex. 1003 ¶¶ 95–97; Ex. 1004, 22:48–23:7, Figs. 8A–8C (describing how evaluation values are used to group the flip-flops to create a clock tree, such that setup errors are eliminated).

[1.d] wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other

Petitioner asserts that Sano discloses this element. *See* Pet. 40. As also discussed above, Petitioner asserts that “Sano groups (clusters) the [flip-flops] (registers) by first grouping those [flip-flop] pairs with higher evaluation values and then grouping [flip-flops] with lower evaluation values.” *Id.* (citing, e.g., Ex. 1004, 20:23–47); Ex. 1003 ¶ 99. In Sano, a higher evaluation value indicates a higher risk of setup errors. Ex. 1004,

8:22–24. Thus, according to Petitioner, “Sano discloses first grouping a first pair of [flip-flops] with a higher timing criticality, e.g., the largest evaluation value, prior to grouping a second pair of [flip-flops] with a lower timing criticality, e.g., ‘the next largest evaluation value.’” Pet. 40; Ex. 1003 ¶ 99.

[1.e] wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs

Petitioner asserts that Sano discloses this element. *See* Pet. 41–42. According to Petitioner, relying on Dr. Robins’s testimony,

The whole purpose of Sano’s grouping is to facilitate commonly-shared clock paths to help suppress setup errors in the circuit design, i.e., provide optimal clock signal buffering to timing critical register pairs.

Pet. 41; Ex. 1003 ¶ 101. For example, Petitioner explains that Figures 8B and 8C of Sano

show how the evaluation-value-based grouping results in commonly-shared clock paths to [flip-flops] 502A and 502B, thus eliminating setup errors. . . . [I]n FIG. 8B there is a divergent clock path because the two registers in the pair are each driven by a different clock buffer (each labeled 503), whereas in FIG. 8C there is a commonly shared clock path because each register is driven by the same single clock buffer (labeled 503).

Pet. 41–42; Ex. 1003 ¶ 101.

Conclusion as to Claim 1

Petitioner’s contentions and cited evidence as to claim 1, summarized above, are persuasive on the preliminary record now before us. As noted, Patent Owner does not present any argument directed to the patentability of the challenged claims at this stage of the proceeding. Based on the current

record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 1 would have been obvious in view of Sano.

3. *Independent Claims 13 and 25*

Independent claims 13 and 25 recite a computer-readable storage medium and computer system, respectively, for generating a clock-tree on an integrated circuit, but otherwise recite limitations similar to those of claim 1. Petitioner relies on the same teachings of Sano for claims 13 and 25 as those discussed above for claim 1. *See* Pet. 57–58; Ex. 1003 ¶¶ 138, 140–141. Based on the current record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that independent claims 13 and 25 would have been obvious in view of Sano.

4. *Dependent Claims 2–8, 11, 12, 14–20, 23, and 24*

Petitioner asserts that Sano teaches each of the additional limitations of dependent claims 2–8, 11, 12, 14–20, 23, and 24. *See* Pet. 43–57. Petitioner supports these assertions with citations to the record and the testimony of Dr. Robins. *See id.*; Ex. 1003 ¶¶ 103–137, 139.

As noted above, if trial is instituted it must be instituted on all challenged claims and grounds. *See SAS*, 138 S. Ct. at 1354. In light of *SAS*, and our above-described determination that Petitioner has met its burden under 35 U.S.C. § 314(a) as to its challenge of independent claims 1, 13, and 25 as obvious in view of Sano, we also determine that it is appropriate to institute *inter partes* review based on Petitioner’s challenge against dependent claims 2–8, 11, 12, 14–20, 23, and 24. At this stage of the

proceeding, it is not necessary for us to provide a detailed assessment as to these claims.

F. Asserted Obviousness over Cheng, with or without Sherwani

Petitioner asserts that claims 1–7, 11–19, and 23–25 would have been obvious in view of Cheng. *See* Pet. 59–81. Petitioner also asserts that claims 4, 8, 16, and 20 would have been obvious in view of Cheng and Sherwani. *See id.* at 81–85. Petitioner supports these assertions with citations to the record and the testimony of Dr. Robins. *See id.* at 59–85. At this stage of the proceeding, Patent Owner does not present arguments regarding the patentability of the challenged claims. *See generally* Prelim. Resp. (presenting only *Fintiv*-related arguments). As noted above, if trial is instituted it must be instituted on all challenged claims and grounds. *See SAS*, 138 S. Ct. at 1354. In light of *SAS*, and our above-described determination that Petitioner has met its burden under 35 U.S.C. § 314(a) as to its challenge of independent claims 1, 13, and 25 as obvious in view of Sano, we also determine that it is appropriate to institute *inter partes* review based on Petitioner’s challenges based on Cheng, and based on Cheng and Sherwani. At this stage of the proceeding, it is not necessary for us to provide a detailed assessment of these grounds.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’567 patent. Thus, we institute an *inter partes* review as set forth in the Order below. Trial shall commence on the entry date of this Decision.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–8, 11–20, and 23–25 of U.S. Patent No. 7,546,567 B2 is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '567 patent is hereby instituted commencing on the entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

IPR2021-01212
Patent 7,546,567 B2

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