

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIEMENS INDUSTRY SOFTWARE INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

IPR2021-01212
Patent 7,546,567 B2

Before KEVIN F. TURNER, SCOTT C. MOORE, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Siemens Industry Software Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–8, 11–20, and 23–25 (“the challenged claims”) of U.S. Patent No. 7,546,567 B2 (Ex. 1001, “the ’567 patent”). Paper 1 (“Pet.”). Synopsys, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). On January 13, 2022, we instituted an *inter partes* review of all challenged claims of the ’567 patent, based on all grounds identified in the Petition.

During the course of trial, Patent Owner filed a Response to the Petition. Paper 19 (“Resp.”). Petitioner filed a Reply to the Response. Paper 22 (“Reply”). Patent Owner filed a Sur-reply to Petitioner’s Reply. Paper 30 (“Sur-reply”). An oral argument was held on October 19, 2022, and a transcript of the oral argument is included in the record. Paper 31 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–8, 11–20, and 23–25 of the ’567 patent. For the reasons we identify below, we determine that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable under § 103(a).

A. *Related Proceedings*

The parties identify *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-004151-WHO (N.D. Cal.) (“the related District Court proceeding”) as a related matter involving the ’567 patent. Pet. ix; Paper 4, 1. Patent Owner also identifies IPR2021-01213 and IPR2021-01215, which

challenge additional patents involved in the related District Court proceeding. Paper 4, 1.

B. Real Parties in Interest

Petitioner states that Siemens Industry Software Inc. is a real party in interest in this proceeding. Pet. ix. Petitioner also identifies Siemens AG and Siemens Corporation as real parties in interest “[o]ut of an abundance of caution.” *Id.* Patent Owner identifies itself, Synopsys, Inc., as the real party in interest. Paper 4, 1.

C. The '567 Patent

The '567 patent, titled “Method and Apparatus for Generating a Variation-Tolerant Clock-Tree for an Integrated Circuit Chip,” was filed on January 10, 2007, and issued on June 9, 2009. Ex. 1001, codes (22), (45), (54). The '567 patent “relates to techniques for designing clock distribution networks for integrated circuit (IC) chips.” *Id.* at 1:9–10.

The Background section of the '567 patent explains that

[t]he speed of a system on an integrated circuit (IC) chip is largely determined by system clock frequency. In a typical synchronous IC chip, a clock distribution network (referred to as a “clock-tree”) is used to distribute a clock signal from a common source to various circuit components. This clock signal is used to coordinate data transfers between circuit components. However, as increasing clock frequencies reduce the clock periods to fractions of a nanosecond, designing clock-trees is becoming increasingly more challenging. A direct result of the decreasing clock period is a shrinking “timing budget” between logically coupled clock sinks. This decreasing timing budget is requiring clock-trees to have minimal clock skew.

Id. at 1:23–35.

The '567 patent further recognizes that “variations” contribute to clock skew, and are “one of the more significant challenges in synchronous clock-tree design.” *Id.* at 1:37–39. Such “variations can include: manufacturing process variations, operational voltage variations, and ambient temperature variations.” *Id.* at 1:39–41. Variations that occur within a chip boundary are referred to as “on-chip variations” (“OCV”). *Id.* at 1:41–43. On-chip variations may result in “limit[ed] performance of the chip, and even threaten[] the functionality of the chip.” *Id.* at 1:43–46. On-chip variations also may “cause[] uncertainty in clock arrival times at circuit components,” which, in turn, “can cause clock skew.” *Id.* at 1:47–50.

One embodiment of the present invention relates to a process that generates a clock-tree on an integrated circuit (IC) chip. During operation, the process starts by receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout. The process then generates a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers. Next, the process clusters the set of registers based on the timing criticality profile to create a clock-tree for the set of registers. By clustering the registers based on the timing criticality profile, the process facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs. *Id.* at 2:12–25.

Figure 3 of the '567 patent is reproduced below.

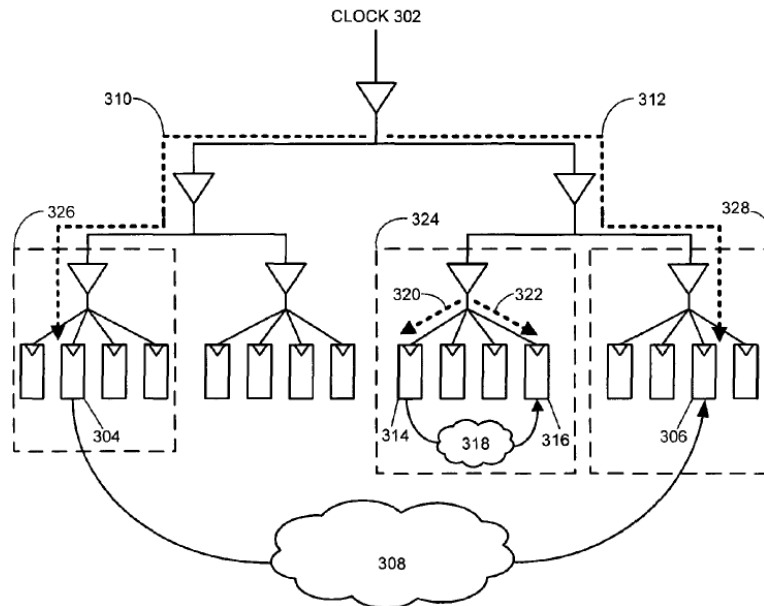


FIG. 3

Figure 3, above, is an “exemplary clock-tree structure 300 with leaf-level registers in accordance with an embodiment” of the '567 patent. Ex. 1001, 6:22–24. The '567 patent describes Figure 3 as follows:

Clock-tree structure 300 includes a main clock source 302 at the root of clock-tree 300, two middle levels of clock-buffers, and a leaf-level comprising a set of clustered registers. Registers 304 and 306 form a launcher/capturer pair which is logically coupled through a data path 308. When comparing the two clock paths from clock 302 to registers 304 and 306, note that branch 310 and branch 312 are the non-shared “private” sections of the two clock paths, respectively. These two private branches contain a total of four unshared clock buffers.

Registers 314 and 316 form another launcher/capturer pair which is logically coupled through a data path 318. Note that the clock paths for registers 314 and 316 are mostly shared, and the private sections of the two clock paths are branch 320 and branch 322, respectively. These two private branches are both local branches which contain no clock buffers. Note that register pair

314/316 achieves a significantly more clock-path sharing than the register pair 304/306.

Id. at 6:25–43 (emphasis omitted). The '567 patent describes that “[i]n this embodiment, OCV causes a much more severe impact on data path 308 than on data path 318.” *Id.* at 6:47–48. “[G]enerally registers within a same cluster, for example in cluster 324, are less vulnerable to OCV than register pairs in different clusters, for example, between cluster 326 and cluster 328.” *Id.* at 6:49–52.

According to the '567 patent, “[t]he present invention provides a technique for improving overall timing performance of an IC chip in the presence of clock variations.” *Id.* at 5:2–4. In particular, embodiments of the '567 patent accomplish this by “maximiz[ing] commonly-shared clock paths (including clock buffers and clock nets) to the registers in the IC design if they have tighter timing constraints between them.” *Id.* at 5:6–9. “[S]tarting from leaf-level clustering, the present invention attempts to maximize the inclusion of the timing critical register pairs into the same cluster.” *Id.* at 5:13–15.

D. Illustrative Claim

Of the challenged claims, claims 1, 13, and 25 are independent. Claims 2–8, 11, and 12 depend from claim 1; and claims 14–20, 23, and 24 depend from claim 13. Independent claim 1 of the '567 patent is reproduced below, and is illustrative of the challenged claims.

1. [1.p] A method for generating a clock-tree on an integrated circuit (IC) chip, comprising:

[1.a] receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout;

[1.b] generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers; and

[1.c] clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers,

[1.d] wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other;

[1.e] wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs.

Ex. 1001, 10:55–11:7 (bracketed identifying labels added).

E. The Applied References

Petitioner relies on the following references in the asserted grounds.

Pet. 6.

Reference	Issue Date/ Publication Date	Exhibit
U.S. Patent No. 6,651,224 B1 (“Sano”)	Nov. 18, 2003 ¹	Ex. 1004
U.S. Patent No. 6,367,060 B1 (“Cheng”)	Apr. 2, 2002 ²	Ex. 1005
Naveed A. Sherwani, <i>Algorithms for VLSI Physical Design Automation</i> , 3 rd ed. (Kluwer Academic Publishers) (1999) (“Sherwani”)	1999 ³	Ex. 1006

¹ Sano is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 20.

² Cheng is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 59.

³ Petitioner’s declarant, Dr. Robins, testifies that Sherwani was “a well-known and widely utilized textbook” that was “known and readily available

Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003) to support its positions.

F. The Asserted Grounds

Petitioner sets forth its challenges to claims 1–8, 11–20, and 23–25 on the following grounds. Pet. 6.

Reference(s)	35 U.S.C. §	Claims Challenged
Sano	103 ⁴	1–8, 11–20, 23–25
Cheng	103	1–7, 11–19, 23–25
Cheng and Sherwani	103	4, 8, 16, 20

II. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406

to [persons of ordinary skill in the art] throughout the early 2000s, and certainly prior to 2006.” Ex. 1003 ¶¶ 200–201. Petitioner, thus, contends Sherwani is prior art at least under 35 U.S.C. §§ 102(a), (b). *See* Pet. 81. Based on the entirety of the record, we determine that Petitioner has shown Sherwani to be prior art under § 102.

⁴ Because the application leading to the ’567 patent was filed before March 16, 2013, patentability is governed by the version of 35 U.S.C. §§ 102 and 103 preceding the Leahy-Smith America Invents Act (“AIA”), Pub L. No. 112-29, 125 Stat. 284 (2011).

(2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined the prior art references. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

We review the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art at the time of the invention. *Graham*, 383 U.S. at 17. For purposes of this proceeding, Petitioner and Patent Owner both agree that this may be characterized as a minimum of a B.S. in Electrical Engineering, Computer Engineering, or Computer Science and at least five years of work experience in the VLSI design, electronic design automation for VLSI, or ASIC (application-specific integrated circuit) design fields or an M.S. in Electrical Engineering, Computer

⁵ The parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

Engineering, or Computer Science and at least two years of work experience in those fields.

Pet. 13; Ex. 1003 ¶ 66; Resp. 11–12.

To the extent necessary, we accept the assessment offered by the parties as it is supported by Dr. Robins’s testimony and is consistent with the ’567 patent and the asserted prior art.

C. Claim Construction

For this *inter partes* review proceeding claim terms

shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). Further, “[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record in the *inter partes* review proceeding will be considered.” *Id.*

Petitioner identifies several claim terms for which the parties have agreed upon construction in the related District Court proceeding. *See* Pet. 14–15 (citing Ex. 1008; Ex. 1016). Petitioner also identifies other claim terms for which Patent Owner has proposed construction in the related District Court proceeding, and/or for which the District Court has provided a tentative construction. *See id.* at 15–19 (citing Ex. 1008; Ex. 1009; Ex. 1010).

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Nidec Motor*

Corp. v. Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017). To resolve the issues presented in the Petition, we need not construe any term except those discussed below.

Petitioner asserted that the limitation [1.a] term “registers at fixed locations” should be given Patent Owner’s proposed litigation construction of “registers [at/in] a location that is fixed during a phase of the clock tree synthesis.”⁶ Pet. 16; Ex. 2001, 9. The District Court construed this term in the following manner:

I will construe the term as follows: “registers [at/in] a location that is fixed during clock-tree generation.” As explained above, the specification supports the construction that the location of registers are fixed during clock-tree generation. See ’567 Patent at 8:29–33, 9:16–41. Although Siemens is correct that the intrinsic evidence does not support moving the registers after clock-tree generation . . . both experts testify that a POSITA would understand that the registers may change during optimization after clock-tree generation.

Ex. 2001, 11–12. During oral argument, Patent Owner agreed that the location of the registers could change during optimization subsequent to clock-tree generation. Tr. 51–53.

We agree with the District Court’s construction of “registers [at/in] fixed locations,” which is also the construction proffered by both parties in this *inter partes* review. However, the term “registers [at/in] fixed locations” is also limited by the context of the claims in which it appears. The claim as a whole was not construed by either party or the District Court;⁷ however, Patent Owner’s arguments against Ground I center on a

⁶ Petitioner asserts the same meaning should be given to the identical term in claim 13, and the term “registers in fixed locations” in claim 25.

⁷ The District Court does not use “during clock-tree generation” in reference to the “method of generating a clock-tree” language of the claim’s preamble.

construction in which “fixed location” applies to all of the limitations of claim 1. Thus, although we agree with the construction of the *term*, we must further resolve how that construction affects the reading of the *claim as a whole*. *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999) (“Proper claim construction, however, demands interpretation of the entire claim in context, not a single element in isolation”); see *Power Mosfet Techs., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1408 (Fed. Cir. 2004) (“Working with the Special Master's definitions [of two distinct claim terms], as it must after expressly agreeing with them, PMT attempts to explain how [the construction of two distinct terms] can coexist when the claims are read as a whole”); *Id.* at 1410 (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so”).

Under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc), claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. See *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

Originally, the District Court construed “registers in fixed locations” as requiring registers fixed “during the clock tree generation stage,” but altered the construction “to avoid confusion of meaning of ‘stage,’” *Id.* at 11. The District Court’s construction uses “during clock-tree generation” to contrast with clock-tree optimization, in which registers may change locations. Ex. 2001, 8–9 (explaining why “registers in fixed locations” is not indefinite). Moreover, as explained below, the District Court did not attempt to construe the scope of “clock-tree generation.” Thus, we limit the scope of the District Court’s construction to the term “registers in fixed locations” itself, consistent with their usage.

Thus, we look to the language of the claims, the description in the patent disclosure, and the prosecution history to determine to what extent the claims require the registers to be at a fixed location.

We begin with the language of the claims. Using claim 1 as an example, the only mention of “fixed locations” occurs in its first step, which recites, “receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout.” Ex. 1001, 10:57–59. The remaining limitations of claim 1 do not address the locations of the registers, instead setting forth generating a timing criticality profile (Ex. 1001, 10:60–63) and clustering the registers based on that profile (Ex. 1001, 10:64–11:7). Thus, the fixed location of the registers is limited, by the plain language of the claim, to the placement for the chip layout that is being received in the first step.

The disclosure of the ’567 patent is consistent with construing “fixed locations” as applying only to the step of receiving the placement of registers in the chip layout. The ’567 patent mentions “fixed locations” only twice, stating, “the process starts by receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout.” Ex. 1001, code [57], 2:14–16. The ’567 patent also states that the process of generating a clock-tree “starts by receiving a placement of an IC chip design (step 402). Specifically, in this IC chip design all the registers and the corresponding combinational logics between registers have been placed at respective locations within the chip boundary.” *Id.* at 6:59–64. The ’567 patent clearly describes receiving a placement of registers that are in fixed locations on an IC chip design. However, the patent (and its

originally-filed specification (Ex. 1002, 57–90)) do not explicitly detail the fate of the physical locations of the registers once received.

The prosecution history does not discuss the “fixed location” limitation in any detail. The allowance of the patent application immediately followed an amendment specifying the order in which clustering operations are performed. Ex. 1002, 30; Resp. 10. Applicant’s arguments also focused solely on that limitation. Ex. 1002 at 31–32. The Examiner’s only mention of a “fixed location” of registers was in finding the applied reference to disclose that “the placement includes a set of registers at fixed locations in the chip layout.” *Id.* at 40. Thus, the prosecution history, to the extent probative, supports that the “fixed location” applies to the received placement.

In its Response, Patent Owner similarly characterizes the “fixed location” limitation of the ’567 patent only in the context of “receiving a placement of an IC chip design” in which “[t]he placement includes a set of registers at fixed locations in the chip layout.” Resp. 5–6. The Response, in its “Overview of the ’567 Patent,” makes no further mention of a fixed location in its discussion of the other limitations, including the generating of a timing criticality profile and clustering for the set of registers. Resp. 6.

Although Patent Owner mentions that clustering may be “location-based” and involve a further step of extracting constraints from the “temporary” clock tree followed by “restor[ing] the original placement by removing all the clusters and discarding the temporary partial-clock-tree,” these limitations are reflected, if at all, in claim 8, not claim 1. Ex. 1001, 7:37–8:32; 11:45–49. And even in claim 8, these steps occur “prior to

clustering the set of registers,” and thus do not limit actions taken in the subsequent clustering step of claim 1. *Id.* at 11:43–44.

Moreover, to any extent that claim 8 requires a fixed location of registers in a step performed after receiving the register placement, claim 1’s lack of such a location-based clustering limitation merely indicates that claim 1 does not require either location-based clustering or any associated “fixed location” associated with that clustering. Under the doctrine of claim differentiation, “two claims of a patent are presumptively of different scope.” *Kraft Foods, Inc. v. Int’l Trading Co.*, 203 F.3d 1362, 1366 (Fed. Cir. 2000). As discussed, nothing in the original disclosure or prosecution history overcomes this presumption; to the contrary, claim 8’s discarding of changes made to the original placement was characterized by the District Court as “one embodiment” of the ’567 patent. Ex. 2001, 10–11. This tends to indicate that claim 1 does not require making and/or discarding changes to the original register locations, because “a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.” *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

In its Response, Patent Owner argues that the claims require the location of the registers to be fixed “during” clock tree generation. Resp. 33 (citing Ex. 2019 (“Friedman Decl.”) ¶ 58).⁸ However, the sole basis for this

⁸ Patent Owner characterizes this as “essentially a negative limitation – *i.e.*, equivalent to a requirement that registers are at locations that do not change during clock-tree generation.” Resp. 35. However, there is no heightened standard for negative claim limitations as compared to positively recited claim limitations. *Novartis Pharm. Corp. v. Accord Healthcare, Inc.*, 38 F.4th 1013, 1020 (Fed. Cir. 2022). Because it would not impact our analysis, we need not determine whether such a characterization is correct.

argument is alleged to be provided by the claimed step of “receiving a placement for a chip layout, where the placement includes a set of registers *at fixed locations* in the chip layout.” *Id.* (quoting claim 1 and citing identical or similar language in independent claims 8 and 25). During oral argument, Patent Owner further asserted that this means that the location of the registers may not move throughout the *entirety* of clock-tree generation, i.e., through each step of claim 1, but again rested that argument on the same “receiving a placement” limitation of the independent claims. Tr. 33 (stating that the method for generating a clock tree includes “receiving a placement” and “generating a time and criticality profile,” and that “there can be no movement in any of those steps”), 31 (“this fixed location limitation is recited in the independent claims, which recite receiving a placement for a chip layout where the placement includes a set of registers at fixed locations in the chip layout”). However, claim 1’s recitation of fixed locations in the placement during the step of receiving the placement relates only to the action taken in that step. No other step indicates that the locations of the registers must be maintained at the locations in which they are received.

We fully credit the evidence presented that the ’567 patent operates without moving the registers, and that its algorithm “would break if you allowed the registers to move.” *See, e.g.,* Ex. 1018, 158–172. Nevertheless, the plain meaning of the terms controls when the claim as a whole is “susceptible to only one reasonable interpretation,” even where the result or effect is “nonsensical” or “cannot perform its intended function.” *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374–1375 (Fed. Cir. 2004). The “registers [at/in] fixed locations” is clearly applied only to the placement for the chip layout received in the receiving step, and we “must

construe the claims based on the patentee’s version of the claim as he himself drafted it.” *Id.*

Patent Owner further points to the District Court’s construction to support its contention that registers must have fixed locations “*during clock-tree generation*”; i.e., throughout the entirety of claim 1. Resp. 34; Tr. 34. However, the District Court’s construction focused only on whether locations could move during post-generation optimization. Ex. 2001, 11 (“Synopsys opposes Siemens’s construction to the extent that it requires registers to not change during the entire circuit design process, including optimization. . . . I agree.”). Moreover, as discussed above, this determination involved consideration of limitations found in claim 8 but not in claim 1.

Patent Owner further asserts that having fixed locations during clock-tree generation “is the construction that both parties have been applying throughout this proceeding.” Tr. 36. However, Petitioner and Patent Owner do not agree what “during clock-tree generation” means. *See, e.g.*, Reply 2 (“Synopsys argues—with . . . no proposed construction of the term ‘clock tree generation’”); Tr. 53 (“Petitioner is saying whatever happens after clustering is irrelevant, but Petitioner never showed us why is clock-tree generation complete upon clustering”); Tr. 58–59 (“I haven’t heard Patent Owner offer an understanding of the claim that says something magical has to happen and that’s when clock-tree generation occurs”). Thus, the parties’ apparent agreement that registers are fixed during clock tree generation is undercut by their disagreement over the scope of that clock tree generation. The underlying question of when registers must be fixed and when they may move remains central to their dispute during briefing. Furthermore, any

agreement of the parties is inoperative on the ultimate legal determination of the construction of claim 1. *See Swift & Co. v. Hocking Valley Ry. Co.*, 243 U.S. 281 (1917) (“If the stipulation is to be treated as an agreement concerning the legal effect of admitted facts, it is obviously inoperative; since the court cannot be controlled by agreement of counsel on a subsidiary question of law”); *Teva Pharmaceuticals USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 326 (2015) (the “ultimate issue of the proper construction of a claim should be treated as a question of law,” although “subsidiary factfinding is sometimes necessary”).

In view of the foregoing, we construe limitation [1.a], and corresponding limitations in claims 13 and 25, as receiving a placement of registers that are in fixed locations, and that the remaining limitations are not limited by the register location.

We did not expressly construe any terms in our Institution Decision. Inst. Dec. 22. However, both parties have addressed the construction of claim 1, including the scope of “fixed locations,” during briefing, discovery, and a lengthy colloquy during oral argument. *See, e.g.*, Resp. 32–35; Tr. 5–6 (Petitioner), 30–40 (Patent Owner), 44–46 (Patent Owner); Ex. 1018, 158–172. Thus, the parties had notice of the claim construction issue, and in particular during oral argument, notice of the Board’s skepticism of Patent Owner’s construction of how the “fixed location” limitation affected the claim as a whole. *See, e.g.*, Tr. 35 (referring to Patent Owner’s explanation of support for extending “fixed location” to the entirety of claim 1 as a “circular” argument), 44–46 (questioning Patent Owner’s interpretation of the scope of “clock-tree generation” in claim 1). Further, we apply the District Court’s construction as to the term actually construed; we provide

further construction here because “the apparent agreement as to the district court’s construction concealed a fundamental disagreement between the parties as to the proper construction” of that term as it impacts the claim as a whole. *VLSI Technology LLC v. Intel Corp.*, slip. op at 9 (Fed. Cir. November 14, 2022) (sustaining the Board’s further construction where “simply adopting [a] proposed construction would not resolve the true dispute between the parties,” and finding the Board’s construction “addressed an argument not made to the district court, and it reached a conclusion not at odds with the conclusion reached by the district court”). Therefore, the parties have had notice and opportunity to be heard on the construction of claim 1 as a whole, and may request rehearing of this decision to address the particular construction taken here. See *TQ Delta, LLC v. Dish Network LLC*, 929 F.3d 1350, 1355–56 (Fed. Cir. 2019) (citing *Intellectual Ventures II LLC v. Ericsson Inc.*, 686 F. App’x 900, 906 (Fed. Cir. 2017)).

D. Asserted Obviousness in view of Sano

Petitioner asserts that claims 1–8, 11–20, and 23–25 would have been obvious in view of Sano. Pet. 20–58; Reply 1–8. Patent Owner argues against this assertion. Resp. 32–56; Sur-reply 1–7. We have considered these assertions and arguments in view of the entirety of the record of the proceeding, and determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–8, 11–20, and 23–35 would have been obvious in view of Sano.

1. *Overview of Sano (Ex. 1004)*

Sano is titled “Method of Optimizing Signal Lines Within Circuit, Optimizing Apparatus, Recording Medium Having Stored Therein Optimizing Program, And Method Of Designing Circuit and Recording Medium Having Stored Therein Program For Designing Circuit.” Ex. 1004, code (54). Sano “relates to a technology utilized when designing a circuit which includes a signal supplying source (e.g., clock signal supplying source) within the circuit and a plurality of elements (e.g., flip-flop cells) supplied with a signal from the signal supplying source.” *Id.* at 1:12–16. The method “optimiz[es] signal lines within the circuit” to thereby optimize “delay or skew of a signal from the signal supplying source to each of the elements.” *Id.* at 1:17–26; *see also id.* at code (57) (the method “optimiz[es] the delay of a signal transmitting through signal lines connecting a signal supplying source to each of elements, whereby skew can positively be decreased.”).

In an embodiment, Sano “calculates evaluation values for every pair of the driven elements (initially [flip-flops]) based on an improving factor of the circuit quality.” *Id.* at 20:18–20. An evaluation value may be, for example, a “hold error evaluation value,”⁹ a “setup error evaluation value,”¹⁰ a “distance evaluation value,”¹¹ or combinations thereof. *See id.* at 8:12–9:2

⁹ Sano describes that the “hold error evaluation value becomes larger with increase of the probability at which the hold error is taken place in each pair.” Ex. 1004, 8:17–19.

¹⁰ Sano describes that the “setup error evaluation value becomes larger with increase of the probability at which the setup error is taken place in each pair.” Ex. 1004, 8:22–24.

¹¹ Sano describes that the “distance evaluation value becomes larger with increase in the physical distance for each pair.” Ex. 1004, 8:38–40.

(describing exemplary ways to calculate evaluation values); *see also id.* at Figs. 4, 7, 10, 11, 13, 14.

In Sano, pairs of flip-flops with a large evaluation value (e.g., the pair has a high hold error probability, a high setup error probability, or the pair members are placed close to each other), then “both of the elements constituting the pair tend to belong to the same group” which leads to prevention of the error and/or a reduced wire length. Ex. 1004, 21:66–22:2, 23:18–25, 24:23–28, 25:11–16, 25:58–63. In other words, flip-flop pairs with a high evaluation value are grouped together. *See, e.g., id.* at 8:7–11 (“[T]he driven values [(i.e., flip-flops)] are divided into groups . . . so that . . . a pair having the largest evaluation value . . . is brought into the same group with priority.”).

Figures 3A to 3E “are diagrams illustrative of procedures for carrying out clock tree synthesizing processing according to [an] embodiment of [Sano].” *Id.* at 14:18–20. In the example of these figures, “one clock supplying element (CLOCK) supplies a clock signal to six (a to f) driven elements ([flip-flops]).” *Id.* at 19:62–64. Figure 3A is reproduced below.

FIG. 3A

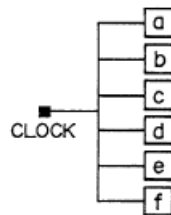


Figure 3A shows “logic information or physical information about the clock supplying element and [flip-flops] which are driven elements.” *Id.* at 19:66–20:1.

Figures 3B, 3C, and 3D are reproduced below.

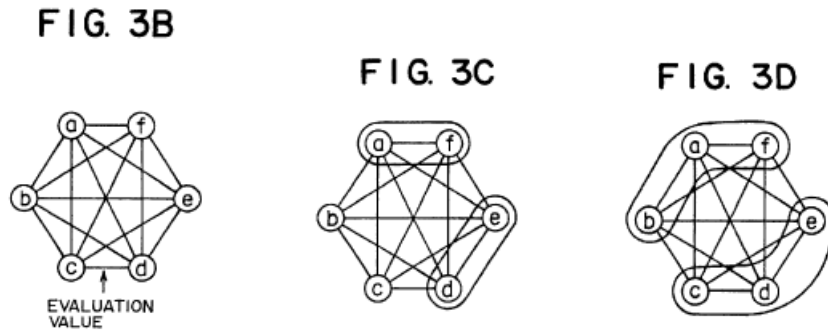


Figure 3B illustrates evaluation values that are calculated for every pair of flip-flops. *Id.* at 20:17–21. Figure 3C illustrates that “a pair having the largest evaluation value calculated at the evaluation value calculating unit 542 is made to belong (merge) to the same group with priority.” *Id.* at 20:26–28. As described in Sano, this process continues until the flip-flops are divided into a plurality of groups, as illustrated in Figure 3D. *See id.* at 20:24–47.

Figure 3E is reproduced below.

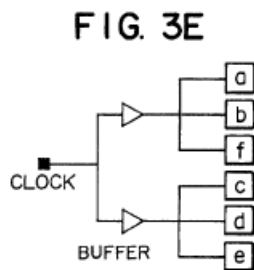


Figure 3E illustrates the resulting clock tree of the process described with respect to Figures 3B–3D. *Id.* at 20:48–52; *see also* Ex. 1003 ¶ 95.

Sano describes that this grouping strategy makes it “possible to create a clock tree in which [errors] can be positively prevented from occurrence,” “circuit quality can be remarkably increased,” “the clock skew can be positively suppressed with ease, wiring length can be shortened, and signal

distribution can be more positively optimized.” *See, e.g.*, Ex. 1004, 25:64–26:3.

2. *Independent Claim 1*

a) *Petitioner’s assertions:*

[1.p] A method for generating a clock-tree on an integrated circuit (IC) chip, comprising¹²

Petitioner asserts that Sano discloses a method and system for creating a clock tree. *See* Pet. 26–27 (citing, *inter alia*, Ex. 1004, 14:18–20, 34:40–44; Ex. 1003 ¶¶ 78–79); *id.* at 27 (“Sano describes its clock tree generation method in detail in, e.g., FIGs. 2–14 and associated text.”).

According to Petitioner, Sano discloses that, in designing a circuit, “the optimizing apparatus optimizes signal distribution through clock signal lines (clock system net) connecting the clock supplying element to the number of [flip-flops] in terms of clock distribution.” Pet. 26 (citing Ex. 1004, 17:29–34).

[1.a] receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout

Petitioner asserts that Sano’s flip-flops (“FFs”), located on an integrated circuit, teach the claimed registers. Pet. 27 (citing Ex. 1004, 1:34–40). Dr. Robins testifies that a person of ordinary skill in the art

¹² Because Patent Owner does not dispute that Sano discloses “a method for generating a clock-tree on an integrated circuit (IC) chip,” we need not decide whether the preamble is limiting.

“would have known that flip-flops were a type of register.” Ex. 1003 ¶ 81 (citing Ex. 1011, 42).

Petitioner contends that “Sano discloses considering the placement of the flip-flops when building the clock tree, so ‘the clock tree is formed’ such that closely-located flip-flops (FFs) ‘belong to the same [clock tree] group.’” Pet. 28 (quoting Ex. 1004, 24:29–41); *see also* Ex. 1004, 24:11–17 (discussing analyzing “the physical distance between” the flip-flop elements in a given pair “based on floorplan information or placement information (layout information, physical information)”), 11:59–61 (“[W]hen the signal lines are wired, floorplan information or placement information is taken into consideration.”); Ex. 1003 ¶ 82. Sano discusses creating and using floorplan information for clock tree creation. *See, e.g.*, Ex. 1004, 6:63–65 (criticizing the prior art for not considering layout information in clock tree creation), 28:52–59 (describing how the “floorplan information file 10” includes placement information for “a plurality of modules each of which is composed of a plurality of flip-flop cells”), Fig. 21; Pet. 28–30; Ex. 1003 ¶¶ 83–84.

Relying on the testimony of Dr. Robins, Petitioner contends that a person of ordinary skill in the art “would have understood that analysis based on placement information . . . would necessarily involve first receiving [such placement information]” or that “it would have been at least obvious” “to implement the clock tree synthesis software of Sano such that it involved receiving placement information including [flip-flops] (registers) at locations fixed during a particular phase of clock tree synthesis.” Pet. 30–31; Ex. 1003 ¶¶ 86–87.

As to the claimed “fixed locations,” Petitioner asserts that a person of ordinary skill in the art “would have understood that the [flip-flops] (registers) were fixed during the Sano evaluation value-based clock-tree generation,” because “[t]he timing information used to create the setup evaluation value depended on the locations of the [flip-flops]” and “if the [flip-flops] were moved during this process then the evaluation values, and thus the corresponding clustering, would become unreliable.” Pet. 30; Ex. 1003 ¶ 85. Petitioner further contends that “it would have at least been obvious to keep the [flip-flops] at fixed locations so as to maintain accurate evaluat[ion] values, and thus high-quality clustering.” Pet. 30; Ex. 1003 ¶ 85.

[1.b] generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers

Petitioner asserts that Sano discloses this element. *See* Pet. 31–35. Sano discloses calculating an evaluation value for each pair of flip-flops in a circuit design. Ex. 1004, 8:1–9:2, 23:15–19, Figs. 2, 4, 7, 10, 11, 14. Petitioner contends that at least the disclosed “setup error” evaluation values of Sano correspond to the claimed timing criticalities. Pet. 31; Ex. 1003 ¶ 89. Petitioner asserts that “the Sano ‘setup error’ evaluation *value* is computed for each [flip-flop] pair, and is *derived from the data path delay between [flip-flops] in a pair* and specifies a timing criticality between those [flip-flops], thus meeting the element under Synopsys’s own proposed construction.” Pet. 31 (emphasis added); *see also* Ex. 1010, 3 (Patent Owner’s proposed construction of “timing criticality between a pair of registers” in the District Court is “value derived from the data path delay

between a pair of registers connected by a data path”) (cited at Pet. 16–17). Supported by Dr. Robins’s testimony, Petitioner provides further details about the “well-known concept” of setup errors, and determining these values. *See* Pet. 32–33; Ex. 1003 ¶ 90.

According to Petitioner,

Each of these setup error evaluation values “specifies timing criticalities between pairs of registers” [as claimed] at least because each is “a numerical value indicating a setup error suppressing property” (*e.g.*, EX1004, 22:44-47) where “the value becomes larger with increase of the probability at which the setup error is taken place in the pair of elements” (23:12-13). *See also* EX1003, ¶91. In other words, the setup evaluation value indicates the relative likelihood that a setup error would occur between [flip-flops], based on the data path delay between those flip-flops. *Id.*

Pet. 33–34.

Relying on the testimony of Dr. Robins, Petitioner further asserts that a person of ordinary skill in the art would understand (1) “that these groups of setup evaluation values for the various pairs of [flip-flops] meet the ‘timing criticality profile for the set of registers’ because the group of values specifies timing criticalities between pairs of [flip-flops] in a set of [flip-flops]”; and (2) that “these evaluation values would necessarily be generated by the processor [CPU 540] and stored in data structures in a part of the memory unit [530].” *Id.* at 34; Ex. 1003 ¶ 93.

[1.c] clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers

Petitioner asserts that Sano discloses this element. *See* Pet. 35–39. In particular, Petitioner asserts that

Sano discloses use of its set of setup error evaluation values to “group,” i.e., cluster, the [flip-flops] in order to create a clock tree for the [flip-flops]. *E.g.*, [Ex. 1004,] 19:9-16 (describing dividing [flip-flops] into groups based on evaluation value as part of clock tree synthesis); *id.*, 19:17-21, 19:41-46, 20:24-47; EX1003, ¶95. Sano FIGs. 3A-3E illustrate one manner in which evaluation values for [flip-flops] (items a-f in the figures) are used to group the [flip-flops] for clock tree generation.

Pet. 35. This process of Figures 3A–3E of Sano is discussed above at Section II.D.1. *See also* Pet. 35–39; Ex. 1003 ¶¶ 95–97; Ex. 1004, 22:48–23:7, Figs. 8A–8C (describing how evaluation values are used to group the flip-flops to create a clock tree, such that setup errors are eliminated).

[1.d] wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other

Petitioner asserts that Sano discloses this element. *See* Pet. 40. As also discussed above, Petitioner asserts that “Sano groups (clusters) the [flip-flops] (registers) by first grouping those [flip-flop] pairs with higher evaluation values and then grouping [flip-flops] with lower evaluation values.” *Id.* (citing, e.g., Ex. 1004, 20:23–47); Ex. 1003 ¶ 99. In Sano, a higher evaluation value indicates a higher risk of setup errors. Ex. 1004, 8:22–24. Thus, according to Petitioner, “Sano discloses first grouping a first pair of [flip-flops] with a higher timing criticality, e.g., the largest evaluation value, prior to grouping a second pair of [flip-flops] with a lower timing criticality, e.g., ‘the next largest evaluation value.’” Pet. 40; Ex. 1003 ¶ 99.

[1.e] wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs

Petitioner asserts that Sano discloses this element. *See* Pet. 41–42.

According to Petitioner, relying on Dr. Robins’s testimony,

The whole purpose of Sano’s grouping is to facilitate commonly-shared clock paths to help suppress setup errors in the circuit design, i.e., provide optimal clock signal buffering to timing critical register pairs.

Pet. 41; Ex. 1003 ¶ 101. For example, Petitioner explains that Figures 8B and 8C of Sano

show how the evaluation-value-based grouping results in commonly-shared clock paths to [flip-flops] 502A and 502B, thus eliminating setup errors. . . . [I]n FIG. 8B there is a divergent clock path because the two registers in the pair are each driven by a different clock buffer (each labeled 503), whereas in FIG. 8C there is a commonly shared clock path because each register is driven by the same single clock buffer (labeled 503).

Pet. 41–42; Ex. 1003 ¶ 101.

Petitioner asserts that Sano’s first embodiment, by itself, renders obvious claims 1–7, 11–19, and 23–25. *Id.* Petitioner alternately relies on some elements from each of the first and fourth embodiments, pointing out that Sano teaches or suggests the combination by disclosing an apparatus that “*has all the function described with the first to fourth embodiments.*” Pet. 25 (citing Ex. 1004, 34:45–50).

b) Patent Owner’s arguments

Patent Owner argues that, contrary to the Petition, neither Sano’s first nor fourth embodiment, nor a combination thereof, renders obvious claim 1.

Resp. 32 (citing Pet. 25). Patent Owner argues that Sano’s clock-tree optimization in its first embodiment is not clock-tree generation as claimed, arguing that the contrary assertion of Petitioner’s declarant, Dr. Robins, is merely conclusionary. *Id.* at 34–35 (citing Ex. 1003 ¶ 79).

Petitioner responds by pointing to multiple descriptions in Sano that the process described in its first embodiment is to generate a clock-tree:

Sano describes using its first embodiment process to “create” and “form” and “synthesize” a clock tree. EX1004, 22:21-31 (“create a clock tree”), 21:11-16 (“a clock tree ... is formed” at “steps S511 to S517” of FIG. 2), FIG. 2; 22:14-17 (a “*clock tree* with a proper balance is successfully *created*”) (emphases added) (cited by Petition at 26-27), 14:18-20 (describing “synthesizing” clock trees in accordance with the first embodiment), 21:14-16 (“form[ing]” a clock tree), 24:29-41 (same).

Reply 2. Petitioner further points to a statement of Patent Owner’s declarant, Dr. Friedman, that “[t]here’s no denying that in [Sano’s] first embodiment he produces a clock tree.” *Id.* (citing Ex. 1018, 116:22–24).

Based on the testimony of Dr. Friedman, and the aforementioned descriptions in Sano, we determine that Petitioner has sufficiently shown that Sano’s first embodiment generates a clock tree.

Patent Owner also argues that Sano’s first embodiment is silent about whether the locations of flip flops change, and therefore, does not teach that its first embodiment uses registers at fixed locations during clock-tree generation, as required under Patent Owner’s claim construction. Resp. 20, 32, 35–36. Patent Owner argues that Petitioner focuses on Sano’s optimization in its first embodiment and ignores that Sano “minimizes clock skew by changing the locations of registers.” *Id.* at 33 (citing Ex. 1004, 12:64–13:20; Ex. 2019 ¶ 59). Patent Owner relies upon the declaration of its declarant, Dr. Friedman, to support its contention that Sano’s first

embodiment process does not preclude changing register locations. *Id.* at 37. Patent Owner further argues that Petitioner’s assertion that it would have been obvious to keep the registers at fixed locations “to maintain accurate evaluate values, and thus high-quality clustering” is at odds with testimony of Petitioner’s declarant, Dr. Robins, that the clock stage S12 of the fourth embodiment would be used, because stage S12 involves registers changing locations; i.e., at steps S126–S128. *Id.* at 38–42.

Petitioner responds that Sano need not describe that the registers stay fixed because no registers are described as moving throughout its entire first embodiment. Reply 3–7. Petitioner points to Sano’s Figures 5 and 8 as illustrating fixed register placement during setup and hold timing analysis (generating timing criticality profiles) on a received design placement, and clustering of registers to commonly share clock paths between registers with timing critical paths. *Id.* at 5–6. Petitioner’s expert discounts Dr. Friedman’s testimony that “registers *could* be changed for various reasons” as lacking evidence or explanation as to what “could” occur. Ex. 1019 ¶ 17; Reply 6–7. Moreover, Petitioner asserts that any movement of registers occurring after the clock tree has been generated; i.e., “after recursive application of steps S511–S517,” is not relevant to Petitioner’s characterization of how Sano teaches each recited limitation of claim 1. *Id.* at 7. Petitioner further argues that it would have been obvious to maintain registers in fixed locations through the clustering step because the evaluation values depend on the relative locations of the registers, and changing the locations of the registers would cause those evaluation values, and subsequent clustering based on those evaluation values, to be unreliable. *Id.* (citing Pet. 30; Ex. 1003 ¶ 85; Ex. 1019 ¶¶ 20–21).

Patent Owner argues that Petitioner's arguments in its Reply, to the extent that they are timely presented, fail because they assign no weight to the "fixed location" limitation. Sur-reply 2. Patent Owner further argues that Figures 5 and 8 of Sano do not describe fixed-location registers because Sano never describes those figures as depicting physical layouts. *Id.* at 3.

Upon considering all of the evidence and argument presented, we are persuaded by Petitioner's arguments and disagree with Patent Owner's. Our claim construction requires that the registers be fixed only during the step of receiving a placement for a chip layout that includes fixed registers, and Patent Owner does not contest that Sano receives a placement of registers at fixed locations in a chip layout.

Moreover, even if claim 1 was interpreted to inherently require fixed register locations throughout its recited steps, Petitioner has shown by a preponderance of the evidence that a person having ordinary skill would have found it obvious to perform each of claim 1's steps of receiving a register placement, generating a timing criticality profile, and clustering the registers based on the timing criticality profile, without physically moving the registers, based on the teachings of Sano. We credit the statement of Dr. Robins that, "[t]he timing information used to create the setup evaluation value depended on the locations of the FFs. Thus, if the FFs were moved during this process then the evaluation values would become inaccurate." Ex. 1003 ¶ 85. Dr. Robins further clarified that "if registers were allowed to move . . . during the clock synthesis phase. . . . "any timing-based information would then become inaccurate . . . because it was based on the old positions of these registers and not their purportedly new positions," and therefore, a person having ordinary skill in the art would know that "you

should keep the registers in fixed locations and not move them because otherwise you are creating moving targets with respect to timing behavior and possible timing violations.” Ex. 2022, 43–44.

This reasoning is consistent with Dr. Friedman’s explanation of how setup timing evaluation is determined. Dr. Friedman stated that it involves determining “the delay of the data signal to propagate through” the data path between two registers. Ex. 1018, 11–12. Dr. Friedman separately characterized Figure 3 of the ’567 patent as an abstraction of a clock-tree structure that is “about data paths and there’s a long path and a short path and you treat them differently.” Ex. 1018, 74. Dr. Friedman contests the obviousness of keeping the registers in fixed locations in Sano’s first embodiment because the locations could be changed for reasons such as satisfying a power dissipation or speed criterion. Ex. 2019 ¶¶ 62, 66. However, Dr. Friedman does not contest Dr. Robins’ statement that such a change in locations would create inaccuracies in Sano’s timing-based clustering process. Thus, considering the arguments of the parties and the entirety of the evidence, we determine that Petitioner has sufficiently shown that a person of ordinary skill in the art reading Sano would have found it obvious to maintain the physical locations of the registers during clustering, particularly in situations not requiring consideration other possible factors such as satisfying a power dissipation or speed criterion.

Furthermore, we agree that Petitioner’s citations to the first embodiment alone, located at Sano column 17, line 20 through column 26, line 3, provide teachings for each claim element. Thus, Patent Owner’s arguments that registers move in the fourth embodiment (Resp. 38–39) do not show that Sano’s first embodiment requires register movement.

Moreover, we agree with Petitioner's arguments that claim 1's generation of a clock tree ends with the clustering steps, and any movement of registers after that step, such as Sano's subsequent optimization method (Resp. 39–41) or Sano's moving clusters of registers into a placement restriction area (Response 41; Sur-reply 5–7), does not bear on whether Sano teaches the steps set forth in claim 1. Reply 8; Ex. 2001 (“the location of the registers [in the '567 patent] do not change during clock-tree generation but may change during post processing optimization”).

Patent Owner argues that these arguments are newly presented because Petitioner did not argue that Sano's silence discloses the “fixed location limitation,” and should not be considered. Sur-reply 1. We do not agree. The Petition advanced the assertion that the claimed “fixed registers” were met by Sano's receiving a network placement having registers in fixed locations, without setting forth any separate description in Sano to show that those registers were fixed. Thus, Petitioner's assertion of Sano's silence on this issue is not a different theory of obviousness, but a further explanation provided to address arguments presented in Patent Owner's Response.

In view of the foregoing, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 1 would have been obvious over Sano.

3. *Independent Claims 13 and 25*

Independent claims 13 and 25 recite a computer-readable storage medium and computer system, respectively, for generating a clock-tree on an integrated circuit, but otherwise recite limitations similar to those of claim 1. Petitioner relies on the same teachings of Sano for claims 13 and 25 as those discussed above for claim 1. *See* Pet. 57–58; Ex. 1003 ¶¶ 138,

140–141. For claim 13, Petitioner additionally points to Sano’s description of a “recording medium having an optimizing program stored therein.” Pet. 57 (citing Ex. 1004, 10:1–10). For claim 25, Petitioner points to Sano’s memory 530 storing information for carrying out processing on processor 540 that functions as an “evaluation value calculating unit.” *Id.* at 34 (citing Ex. 1004, 17:65–18:15; Ex. 1003 ¶ 93. Patent Owner does not specifically argue against these limitations, except through the arguments presented against claim 1. Resp. 42. For the same reasons expressed for claim 1, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 13 and 25 would have been obvious over Sano.

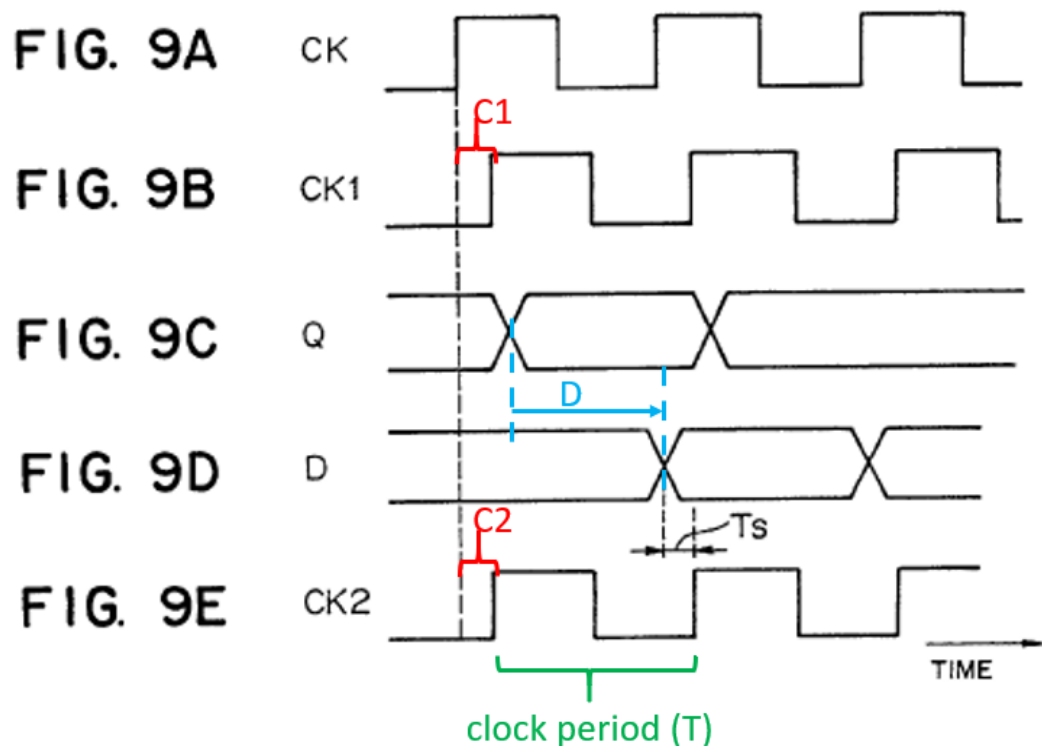
4. *Dependent Claims 2–8, 11, 12, 14–20, 23, and 24*

Petitioner asserts that Sano teaches each of the additional limitations of dependent claims 2–8, 11, 12, 14–20, 23, and 24. *See* Pet. 43–57. Petitioner supports these assertions with citations to the record and the testimony of Dr. Robins. *See id.*; Ex. 1003 ¶¶ 103–137, 139.

a) *Claims 2, 3, 14, and 15*

Claims 2 and 14 recite “wherein obtaining the timing criticality between a pair of registers in the set of registers involves computing a timing slack between the pair of registers based on the received placement.” The parties construe timing slack as “for a launcher and capturer pair, the value equal to the clock period minus the sum of the setup time of the capturer, the clock skew, and the data path delay.” Resp. 43 (citing Pet. 15–18). Claims 3 and 15 further recite that the computation of the data path and clock skew between a pair of registers is based on the received placement.

Petitioner asserts that Sano describes the following calculation of timing slack based on the received placement information:



D = data path delay

Ts = setup time

C1 = clock path delay for CK1

C2 = clock path delay for CK2

setup error evaluation value = setup error probability (Sano, 23:18-19)

inversely proportional to setup timing margin (Sano, 23:8-13)

setup timing margin = T - (C2 - C1) - D - Ts

= clock period - (clock skew) - datapath delay - setup time

Pet. 43–44 (annotating Ex. 1004, Figs. 9A–E; citing Ex. 1003 ¶ 106), 57.

Petitioner asserts that Sano considers each of the parameters in Figures 9A–E during determination of the setup evaluation value. *Id.* Petitioner asserts that one having ordinary skill in the art, conversant with the concepts of setup timing violation analysis, would have found the claimed calculation

either inherently performed by, or obvious in view of, Sano's disclosures. *Id.* at 44–45 (citing Ex. 1003 ¶ 105; Ex. 1006, 420–421).

Patent Owner argues that Sano does not suggest that its evaluation value involves computing a timing slack, or any value equal to the clock period minus the capturer setup time, data path delay, and clock skew. Resp. 43–44. Patent Owner further argues that Petitioner does not show such calculation to be a necessary part of the evaluation, especially in view of Petitioner's statement that setup violation analysis "often" involves computing slack, and Dr. Friedman's statement that "[t]here are many methods for analyzing setup requirements." *Id.* at 44; Sur-reply 8–9. Patent Owner further argues that Petitioner has not shown that it would have been obvious to discard Sano's approach to perform the claimed calculation. Resp. 44; Sur-reply 9. Petitioner responds that Patent Owner has not supplied any evidence to show that Sano's approach is different such that it would be discarded to perform the claimed calculation. Reply 9.

We agree that Petitioner has made the requisite showing. Patent Owner admits that Sano's evaluation values are based on data path delays. Sur-reply 9. Dr. Friedman states that a person of ordinary skill in the art in the computer science world would be familiar with timing slack with respect to a setup requirement. Ex. 1018, 14–16. Dr. Friedman further states that a person of ordinary skill in the art in the electrical engineering world would also "definitely understand" the concept, which is the "idea that you've got clock period minus the path delay plus any effective skew." *Id.* at 27–28. Dr. Friedman further states that such a timing slack calculation would involve not only subtraction of data path delays, but also any effect of clock skew and "all the delays from getting out of that initial register . . . to set up

into that register,” including the “setup time into the final register.” *Id.* at 17, 26, 29–30. Dr. Robins states that Sano’s Figure 9A–E illustrate that setup error depends on

the length of time it takes data to travel from the output Q of launcher FF 502A to the input D of capturer FF 502B (i.e., the data path delay), a time T_s by which the changing data must precede the rising clock edge at the capturer FF 502B (i.e., setup time or setup requirement of the FF), the relationship between the rising clock edge CK1 at the launcher FF 502A and the rising clock edge CK2 at the capturer FF 502B (i.e., the clock skew), and the time between rising edges of the clock CK (i.e., the clock period).

Ex. 1003 ¶ 104 (citing Ex. 1004, 22:48-65, 23:8-17).

Based on the cited description of Sano, which describes setup error, Dr. Robins’ statements explaining how Sano’s Figure 9 illustrates each of the claimed variables to be considered in determining setup error, and Dr. Friedman’s statements explaining how timing slack, including the claimed calculation, would have been known to the person of ordinary skill in the art, we determine that Petitioner has shown, by a preponderance of the evidence that claims 2 and 14 would have been obvious to one having ordinary skill in the art.

With respect to claim 3 and 15, Patent Owner argues that Petitioner has not shown that Sano computes a clock skew. Resp. 45-46. Patent Owner argues that Sano merely mentions clock skew and techniques for minimizing clock skew. *Id.* at 46. Petitioner argues that clock skew would have been calculated in the manner described in its assertions for claim 2. Reply 10–11. Patent Owner argues, in response, that Petitioner does not teach computing timing slack (as per claim 2), and that Sano does not necessarily teach the narrower limitation of computing a clock skew. Sur-

reply 9–10. Patent Owner points to Dr. Friedman’s testimony that “clock skew is oftentimes ignored in evaluating timing violations.” *Id.* at 10 (citing Ex. 1018, 24:8–26:9).

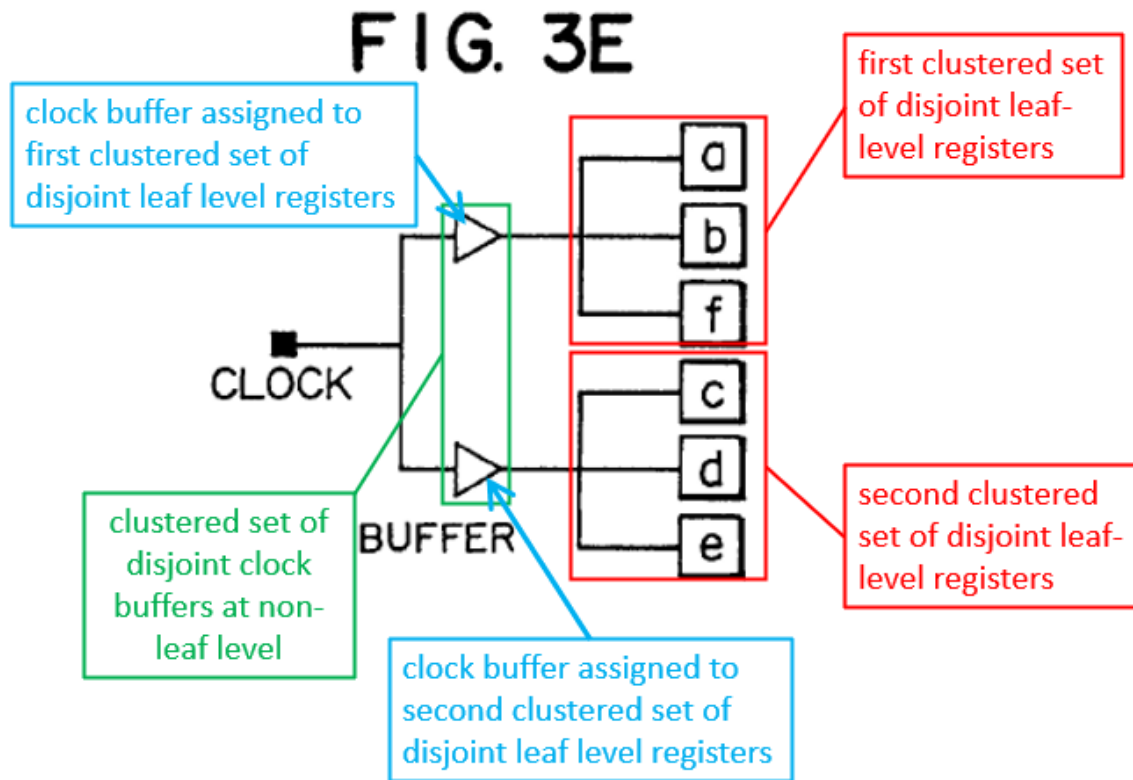
However, the fact that clock skew is “oftentimes ignored” indicates that it is at least sometimes considered. Based on the evidence discussed above with respect to claims 2 and 14, we determine that Petitioner has shown, by a preponderance of the evidence that claims 3 and 15 would have been obvious to one having ordinary skill in the art.

b) Claims 5, 6, 17, and 18

Petitioner asserts that the claimed method of clustering registers is taught by Sano. In particular, Petitioner explains:

Sano discloses “divid[ing] the driven elements [FFs] into groups” at the leaf-level (EX1004, 20:24-47), then inserting “buffer element[s]” at a non-leaf level “for each group” (*id.*, 20:48-52). This clusters a set of clock buffers to generate a disjoint set of non-leaf level clusters, with each clock buffer assigned to respective leaf level clusters of registers.

Pet. 48. Petitioner provides an annotated version of Sano’s Figure 3E to illustrate:



Id. at 49 (citing Ex. 1003 ¶ 119).

Petitioner also points to Sano as describing that,

After “calculat[ing] evaluation values for every pair of the driven elements (initially FFs)” (EX1004, 20:17-19), the FFs are grouped such that “a pair having the largest evaluation value ... is made to belong (merge) to the same group with priority” (*id.*, 20:24-33). See also, e.g., FIG. 3C. If this merging “does not results [sic] in violation of the fan out-restriction on a buffer element which will be inserted into the group at the later stage, then the pair of elements are made to belong to the same group.”

Id. at 49–50. Petitioner provides similar assertions for claims 17 and 18. *Id.* at 57.

Patent Owner does not specifically argue against Petitioner’s showing, which we find to account for each limitation of claims 5, 6, 17, and 18.

Based on the evidence and argument described above, we determine that Petitioner has shown, by a preponderance of the evidence that claims 5,

6, 17, and 18 would have been obvious to one having ordinary skill in the art.

c) Claims 7 and 19

Claims 7 and 19 further recite that “the registers within the same cluster share clock-buffers and clock-nets along associated clock paths in the clock-tree.” Petitioner argues that Sano teaches this for the same reasons set forth in its assertions for claim 5. Pet. 50, 57.

Patent Owner argues that the Petitioner, at the cited section, does not mention “clock-nets,” and that this is a “clear failure of proof.” Resp. 46–47.

Petitioner points to its reference to Figure 3E, asserting that its depicted nets are “clock-nets” because they are used to connect the clock and registers. Reply 12–13 (citing Ex. 1019 ¶ 32).

Patent Owner argues that this is new argument because it did not appear in the Petition, and that Petitioner thus failed to meet its obligation to make their case in the Petition. Sur-reply 11–12.

We determine, based on the descriptions of Sano and the cited testimony of Dr. Robins, that the Petition’s discussion of Sano’s Figure 3E describing connections (nets) between the clock and the registers would be understood to be a description of clock-nets. We do not agree that this comprises new argument because Petitioner relied upon Figure 3E in its discussion of claim 5 (to which its discussion of claim 7 refers), and the Reply merely provides further explanation of Figure 3E responsive to Patent Owner’s arguments, and does not propose a new theory of obviousness. Consequently, we determine that Petitioner has shown, by a preponderance

of the evidence that claims 7 and 19 would have been obvious to one having ordinary skill in the art.

d) Claims 8 and 20

Claim 8 further recites [with bracketed numbering added]:

[8.a] The method of claim 6, wherein prior to clustering the set of registers based on the timing criticality profile, the method further comprises: clustering the set of registers using a geometric location-based clustering process to obtain a temporary partial-clock-tree, which comprises a disjoint set of clusters;

[8.b] extracting a set of constraints from the set of clusters;
and

[8.c] discarding the temporary partial-clock-tree.

Petitioner asserts that Sano's teachings, in its first and fourth embodiments, render claim 8 obvious. Petitioner points to the "IC design process of Fig. 21, implemented to cluster flip-flop pairs based on the setup evaluation values as in Sano's first embodiment" renders obvious claim 8. Petitioner points to its earlier assertions that Sano expressly contemplates combining its first and fourth embodiments. Pet. 51 (citing Ex. 1004, 34:36–52). Petitioner provides similar assertions for claim 20. *Id.* at 57.

With respect to limitation [8.a], Petitioner asserts that Sano teaches a location-based clustering at step S113 that occurs prior to the clustering process of step S124, and later clustering at S127–130. Pet. 52. Petitioner points to Sano's driving "modules placed closed to each other" by a common clock buffer. *Id.* at 52 (citing Ex. 1004, 30:21–24). Petitioner characterizes the clustering as occurring on flip-flop modules, which would have been specified by the designer, considering at least in part the user-

specified design fan-out restriction. *Id.* (citing Ex. 1003 ¶¶ 131–132; Ex. 1004, 1:40–65, 1:66–2:29, 30:24–29, Fig. 23).

Patent Owner argues that, for the same reasons as argued against Petitioner’s assertions on claim 1, Sano’s registers have not been shown to be at or in fixed locations. *Id.* at 47.

Petitioner counters by pointing out that step S113 would not require any register movement, because Sano only teaches register movement at steps S126–S128, which is “irrelevant because it happens after Sano generates a clock-tree at S124,” and the District Court’s construction required fixed locations only through generation of the clock tree. Reply 14–15. Petitioner further highlights the initial clustering in steps S113–S124. *Id.* at 14.

Patent Owner argues that Petitioner’s position in the Reply is inconsistent with its argument in the Petition, because Petitioner either relies solely on the first embodiment, or alternately, relies on portions of the fourth embodiment that occur after step S128. Sur-reply 12–14.

We do not agree with Patent Owner’s argument that Sano fails to teach limitation [8.a] due to register movement. In our claim construction, we limit the fixedness of the registers to the received positions of the registers. *Infra* at II.C. Even were the registers required to be fixed throughout clock-tree generation, we determine that Petitioner has shown that it would have been obvious for a person having ordinary skill in the art reading Sano to do so. *Infra* at II.D.2.c. With respect to Petitioner’s reference to location-based clustering that occurs after movement of registers (in step S118), Petitioner also relies on location-based clustering at

step S113, which sufficiently teaches performing location-based clustering prior to step S118's register movement.

Patent Owner next argues that none of the cited portions suggest that Sano's modules or fan-out restrictions are user constraints, drawing from the parties' agreed construction of "geometric location-based clustering process" as meaning "clustering based primarily on physical proximity of components, while also considering user constraints." Resp. 47, 49. Patent Owner argues that Petitioner does not explain why a person of ordinary skill in the art would have considered a flip-flop module to be a constraint, and what aspects of Sano's modules are allegedly specified by the user. *Id.* (citing Ex. 2019 ¶ 80). Patent Owner further argues that Dr. Robins' supporting testimony is conclusory because it does not explain why the flip-flop modules would have been understood as having been specified by the designer. *Id.* (citing Ex. 1003 ¶ 131).

Patent Owner further argues that step S113, cited by Petitioner, does not consider a fan-out restriction. *Id.* (citing Ex. 2019 ¶ 81). To the extent that Dr. Robins does state that the fan-out restriction is a user constraint, Patent Owner argues that Dr. Robins provides no explanation; at best stating that such restrictions "must be imposed," but not that they are "*user* constraints." *Id.* at 51 (citing Ex. 1003 ¶ 132). Patent Owner points to Dr. Friedman's testimony that Sano's modules and fan-out restriction need not be user specified, and could be implemented without any user input. *Id.* at 52 (citing Ex. 2019 ¶ 82).

Petitioner argues that Sano teaches that fan-out restrictions must be considered when generating a clock-tree, because otherwise, "it will be impossible for all of the elements to be directly driven by the clock

supplying source due to a fan-out restriction.” Reply 17 (citing Ex. 1004, 1:43-45). Dr. Robins corroborates the need for a fan-out restriction, stating that a person having ordinary skill in the art would know that such a restriction is necessary to prevent some branches of the clock-tree from driving too large of a load, and to prevent buffers from driving too many elements, both preventing operation at the expected frequency. Ex. 1003 ¶ 132. Petitioner points out that the ’567 patent identifies fan-out restrictions as one of the user constraints of geometric, location-based clustering. Reply 18 (citing Ex. 1001, 7:47–48 (“conventional location-based clustering technique”), 7:58–64 (“clustering . . . also consider[s] a set of user specified ‘hard’ constraints. These user-specified constraints on a cluster can include but are not limited to . . . maximum/minimum fanout within a cluster”)). Petitioner further asserts that because fan-out restrictions are either specified or not, that limitation comprises a two-species genus for which each species would be at once envisaged by a person of ordinary skill in the art. *Id.* at 19. Petitioner thus contends that it would have been obvious to a person having ordinary skill in the art to have considered a user constraint of a fan-out restriction at S113. *Id.* at 17.

Patent Owner argues that Petitioner errs by using the ’567 patent to show obviousness. Sur-reply 16. Patent Owner further argues that Sano’s disclosure of a fan-out restriction is not a disclosure of a two-species genus, of user-specified and non-user specified fan-out restrictions. *Id.*

With respect to “user” constraints, claim 8 does not contain any “user” limitation. Patent Owner’s argument is based on an agreement between the parties that “geometric location-based clustering process” means “clustering based primarily on physical proximity of components, while also

considering user constraints.” Resp. 47–48 (citing Pet. 53). We note that neither party has discussed the scope of the term “user” in their discussion of this issue. However, we need not construe this term to resolve this issue, because we determine, based on the description in Sano and Dr. Friedman’s testimony, that Sano teaches “user” constraints.

During his deposition, Dr. Friedman discussed a person of ordinary skill in the art’s awareness of fanout, which he related to capacitive load. Ex. 1018, 185 (“Q: And so in the context of the ’567 patent, when you see the word ‘fanout,’ you understand that to mean capacitive load; is that correct? A. That there’s an effort to estimate the total capacitive load on that node.”), 180 (“The whole business is about moving charge around” which “depends on a lot of things one of which is the fanout. And so in this patent, ’567, he talks about fanout. But what he really means is capacitance.”); Reply 18. Dr. Friedman agreed that the concept of considering capacitive load of a given clock-tree buffer was “definitely known for clock-tree clock network design for sure in the general manual sense.” *Id.* at 186 (also stating that such consideration might not have been automated at the relevant time). Although Dr. Friedman testifies that such a person having ordinary skill in the art would have recognized that a restriction or constraint “need not” be user-specified, that statement indicates that it would have been known, at least as one option, for the user to specify that restriction. Ex. 2019 ¶ 82; Resp. 52. We consider those statements in the context of Sano’s description of the optimizing apparatus being used “when a designer designs a circuit.” Ex. 1004, 17:24–29. Sano describes the designer using an input unit for inputting information “necessary for synthesizing clock trees.” *Id.* at 17:51–54. Sano further describes that such

information permits “operation of optimization in terms of clock distribution [to] proceed in an interactive manner.” *Id.* at 17:54–58. Because Sano teaches that the designer inputs information necessary for synthesizing clock trees, and Dr. Friedman states that consideration of capacitive load (related to fanout) was definitely known for clock tree design in the “manual” sense, the evidence supports Petitioner’s contention that a person having ordinary skill in the art would have found it obvious for a designer (one type of user) to set the constraints on clustering parameters.¹³

With respect to limitation [8.b], Petitioner asserts that Sano describes that “a clock path is extracted from the netlist (2)” in Step S121, prior to the timing-based clustering of S124, and that Sano describes extracting “a placement restriction area . . . based on the placement of the buffer cell.” Pet. 55 (citing Ex. 1004, 29:7–8, 29:23–27). Petitioner asserts that this teaches extracting a set of constraints from the set of clusters. *Id.* (citing Ex. 1003 ¶ 134).

Patent Owner argues that Petitioner does not show Sano to extract a clock path from the claimed “set of clusters,” but instead, from the netlist. Resp. 53. Dr. Friedman testifies that a netlist is not a set of clusters. Ex. 2019 ¶ 83. Patent Owner further argues that Petitioner’s alternate argument that such extraction occurs at step S126 is flawed because such extraction is based on the placement of the buffer cell, and not from the set of clusters of registers. *Id.* at 54. Patent Owner argues that Sano describes that S126 “creates” a placement restriction area, not that is extracted. *Id.* at 55. Patent Owner addresses Dr. Robins’ statement that the placement

¹³ We do not base this determination on Petitioner’s assertions based upon statements in the ’567 patent.

restriction area is a constraint induced by Sano's set of clusters (Ex. 1003 ¶ 134), by arguing that this is not explained, and not supported by Sano. *Id.*

Petitioner asserts that a netlist "represents the connection relationship in the clock tree," and by showing all the connections in the clock-tree, "Sano's netlist necessarily represents the registers and how each register cluster is connected to its respective buffer." Reply 19 (citing Ex. 1019 ¶ 46). Petitioner further asserts that this connection relationship constrains how the clock signal propagates and is a set of "clock path constraints." *Id.* at 20. Alternately, Petitioner points to Sano's step S123 as extracting a placement area (constraint) from each of the flip-flop clusters and placing a buffer at the center of each placement area. *Id.* (citing Ex. 1004, 29:16–17; Ex. 1019 ¶ 49).

Patent Owner argues that these arguments are newly presented and should not be considered. Sur-reply 17–18. Patent Owner further argues that these arguments differ from those in the Petition, which did not mention step S123, and relied instead on Sano Fig. 23. *Id.* at 20. We do not agree. The Petition advanced the assertion that the claimed extraction from the set of clusters was met by Sano's extraction from the netlist, and the Reply does not advance a different theory of obviousness in providing further explanation to address arguments presented in Patent Owner's Response. Additionally, we agree that Sano's explicit statement that the different embodiments may be combined provides sufficient reason for one skilled in the art to combine teachings from both embodiments.

Patent Owner also argues that these arguments are wrong. *Id.* Patent Owner argues that "many clock paths in a netlist do not connect to clusters of registers." *Id.* at 18 (citing Ex. 1004, Fig. 52). Patent Owner argues that

because “the clock path connecting the clock source 285 to the buffer cell 291 is not connected to any registers,” extracting a clock path from the netlist does not necessarily involve an extraction from a “set of clusters” of registers. *Id.* at 18–19.

We determine that Petitioner has sufficiently shown that Sano teaches extracting a set of constraints from the set of clusters formed by the clustering in step [8.a]. Following Sano’s creation of a clock tree at step S113, which we determined to teach step [8.a]’s clustering, Sano creates netlist (2) and then extracts a clock path therefrom at step S121. Ex. 1004, Fig. 21. Although Patent Owner argues that the netlist contains connections not directly between clusters of registers, Patent Owner does not argue that the netlist does not include such connections. Moreover, Patent Owner’s cited figure, Figure 52 of Sano, illustrates that the great majority of connections involve clusters (282–284) of registers. Ex. 1004, Fig. 52. Thus, Patent Owner’s argument that some non-cluster connections exist in the netlist does not negate Sano’s teaching of extracting a constraint in the form of connections between clusters of registers.

With respect to limitation [8.c], Petitioner asserts that Sano’s description that “the clock path extracted at Step S121 is disregarded” teaches the claimed discarding of the temporary clock tree. *Id.* at 55 (citing Ex. 1004, 29:9–12). Petitioner further asserts that the initial temporary clock tree from step S113 is replaced by the clock tree ultimately created by the evaluation value-based clustering that would be incorporated into steps S124, S128, and S130. *Id.* (citing Ex. 1004, Figs. 35, 42–44).

Patent Owner does not specifically argue against Petitioner’s showing, which we find to account for limitation [8.c].

Based on the above showing, we determine that Petitioner has shown, by a preponderance of the evidence that claim 8, and claim 20 having similar limitations, assertions, and arguments against, would have been obvious to one having ordinary skill in the art.

e) Claims 11, 12, 23, and 24

Petitioner asserts that the further limitations of claims 11 and 12 set forth only an intended use or desired result, and are therefore entitled to no patentable weight. Pet. 56. Petitioner asserts that the limitations are met by Sano's description of improving timing performance of the chip, through its clustering, by reducing clock skew caused by on-chip process, voltage and temperature variations. Ex. 1003 ¶ 137. Petitioner asserts that the '567 patent acknowledges that such causes of clock skew were well known, and that increasing the amount of clock-path sharing between registers was known to improve OCV (On-Chip-Variation)-tolerance. *Id.* (citing Ex. 1001, 1:36–50, 1:56–58). Petitioner asserts that a person of ordinary skill would have recognized these advantages to flow from Sano. Petitioner provides similar assertions for claims 23 and 24. *Id.* at 57.

Patent Owner does not specifically argue against Petitioner's showing, which we find to account for each limitation of claims 11, 12, 23, and 24.

Based on the above evidence and argument, we determine that Petitioner has shown, by a preponderance of the evidence that claims 11, 12, 23, and 24 would have been obvious to one having ordinary skill in the art.

E. Obviousness over Cheng, with or without Sherwani

Petitioner asserts that claims 1–7, 11–19, and 23–25 would have been obvious in view of Cheng. *See* Pet. 59–81. Petitioner also asserts that

claims 4, 8, 16, and 20 would have been obvious in view of Cheng and Sherwani. *See id.* at 81–85. Petitioner supports these assertions with citations to the record and the testimony of Dr. Robins. *See id.* at 59–85.

Patent Owner argues, and we agree, that Petitioner has not shown, by a preponderance of the evidence, that Cheng, with or without Sherwani, teaches or suggests every limitation of the claims. Specifically, Patent Owner argues that Petitioner has not shown a teaching of generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers,” as recited in claim 1. Resp. 56–68. Similar limitations are required in the asserted independent claims, and thus, in each of the asserted dependent claims. Ex. 1001, 11:8–14:25.

Petitioner characterizes this limitation as requiring “a collection of timing slack information for a set of registers [without] specify[ing] what type of data structure.” Tr. 22. Petitioner admits that simply setting a flag by storing a binary value would satisfy this limitation, but it would not permit the later-claimed step of ranking based on timing criticalities. Tr. 23 (“binary choice, we don’t dispute. That would not be satisfied by that portion of the claim”). Petitioner asserts that this limitation is taught by Cheng’s step 480, “test for setup/hold time violations,” as it appears in Figure 4. Pet. 61 (citing Ex. 1005, Fig. 4; Ex. 1003 ¶¶ 144–145). Petitioner argues that Cheng performs a timing calculation for each pair of registers. Pet. 64–68. Dr. Robins states that a person having ordinary skill in the art would understand Cheng as repeating this process “until a setup timing value had been created for each register pair in the design.” Ex. 1003 ¶¶ 160–161.

As an initial matter, although Petitioner is correct that the “set of registers” in claim 1 need not be the entire set of registers in the placement (Tr. 24–25), the “set of registers” must include enough registers so as to be clustered based on the timing criticality profile, as also set forth in claim 1. Further, the claimed timing criticalities are between “pairs,” i.e., plural pairs, of registers. Having only two registers in the set would not meet the other requirements of claim 1. Thus, performing a single test for violations, even if that was obvious to include computing an individual timing criticality value for that pair, would not satisfy claim 1.

Patent Owner argues, and we agree, that Cheng teaches only a binary (true/false) determination of whether a violation exists for each pair. Resp. 59–60; Sur-reply 22–23. There is no teaching in Cheng that such values should be stored for later use for the claimed purpose of clustering a pair of registers having a higher timing criticality and clustering a second pair of registers having a lower timing criticality. Resp. 60; Ex. 1001, 10:64–11:3. As Patent Owner points out, “Cheng does not disclose clustering a pair of registers that *does not* violate a timing condition.” *Id.*, n.4.

Petitioner counters that Cheng must store such values in order to perform its step 490, clustering the registers “as needed in order *to correct any setup time and/or hold time violations.*” Reply 23–24 (citing Ex. 1005, 8:278–30; Ex. 1019 ¶ 55). Petitioner argues that Cheng performs all violation analysis at step 480, and that information from the analysis is used at step 490 to generate a clock-tree. However, Patent Owner argues, and we agree, that Cheng does not describe how the presence of a violation is used in a comparison of timing calculations. Sur-reply 23–24. Although Cheng “attempts to correct the violations by changing positions of registers in the

clock tree . . . registers can be swapped from cluster to cluster in the clock tree,” or “change the order in which a pair of dependent registers are clustered,” Petitioner does not explain how this correction relies on any comparison of timing value calculations between register pairs, either in Cheng or in the knowledge of a person having ordinary skill in the art.

Instead, Petitioner attempts to construct a chain of logical events to bridge the gap between Cheng’s description of determining whether there is a timing violation and Cheng’s later correction of violations by altering positions of registers in the clock tree:

[Cheng’s] goal is not just to flag errors and say, well, let's do a couple of things and hope that they're fixed. He's setting out to correct setup time and hold time violations. He doesn't just want to flag these violations. He wants to fix these violations. And so, having gone through this process of computing a timing slack -- because in order to know whether you're violating or not, you need to compute the timing slack; that was well-understood, and that's our obviousness argument. And so, once you've computed the timing slack, it would have made no sense to just throw that information away. You would have wanted to store it, and then, in your next step in the process, use that to actually, as Cheng says, correct any setup time or hold time violations. Unless you know the exact number, you can't know that you've corrected it.

Tr. 23–24; Pet. 69.

We have also considered that Dr. Robins states that storing these data as a data structure would have been needed in order to allow access of this information. Ex. 1003 ¶ 164. Alternately, Dr. Robins argues that storing these data would have been obvious to a person having ordinary skill in the art because it is important to store such data. *Id.* at ¶¶ 165–168 (citing as evidence Ex. 1006).

However, Petitioner’s string of logical assumptions, supported by Dr. Robins’ similar hindsight-based reading of Cheng, merely underscores the lack of any description in Cheng of the particular method by which the ’567 performs that clustering correction. Although Petitioner may be correct in arguing that one could have performed the steps of storing and comparing timing slack values in addition to Cheng’s actual descriptions, Petitioner has provided no evidence, beyond its attempt to reconstruct the process of the ’567 patent itself, that one would have performed such steps.

Consequently, Petitioner has not shown, by a preponderance of the evidence, that Cheng, with or without Sherwani, renders obvious any asserted claim of the ’567 patent.

III. CONCLUSION¹⁴

For the foregoing reasons, we determine Petitioner has established by a preponderance of the evidence the unpatentability of claims 1–8, 11–20, and 23–25 of the ’567 patent. In summary,

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–8, 11– 20, 23–25	103(a)	Sano	1–8, 11–20, 23–25	

¹⁴ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–7, 11– 19, 23–25	103(a)	Cheng		1–7, 11–19, 23–25
4, 8, 16, 20	103(a)	Cheng, Sherwani		4, 8, 16, 20
Overall Outcome			1–8, 11–20, 23–25	

IV. ORDER

Accordingly, it is

ORDERED that claims 1–8, 11–20, and 23–25 of U.S. Patent No. 7,546,567 B2 are unpatentable; and

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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