

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIEMENS INDUSTRY SOFTWARE INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

IPR2021-01213
Patent 8,234,614 B1

Before JENNIFER MEYER CHAGNON, SCOTT C. MOORE, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. BACKGROUND

A. Background and Summary

Siemens Industry Software Inc. (“Petitioner”) filed a Petition for *inter partes* review (“IPR”) of claims 1–4, 12, 13, and 16–19 of U.S. Patent No. 8,234,614 (Ex. 1001, “the ’614 patent”). Paper 1 (“Pet.”). Patent Owner, Synopsys, Inc., (“Patent Owner”), filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). An *inter partes* review may not be instituted on fewer than all claims challenged in the Petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

Having considered the Petition and the Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–4, 12, 13, and 16–19 of the ’614 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to § 314, we institute an *inter partes* review as to claims 1–4, 12, 13, and 16–19 of the ’614 patent on all grounds raised in the Petition.

B. Real Party in Interest

Petitioner identifies itself, Siemens AG, and Siemens Corporation, as real parties in interest to this IPR petition. Pet. viii. Patent Owner identifies itself as the real party in interest. Paper 7 (first unpaginated page).

C. Related Matters

The parties indicate that the '614 patent is involved in a patent infringement lawsuit brought by Patent Owner in the Northern District of California, *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-04151-WHO. *Id.* Patent Owner indicates that two additional patents (U.S. Patent No. 7,546,567 and U.S. Patent No. 8,407,655) are at issue in the above-listed proceedings, and are the subject of *inter partes* review proceedings IPR2021-01212 and IPR2021-01215. Paper 7 (first unpaginated page).

D. The '614 Patent

The '614 patent (Ex. 1001) generally relates to semiconductor chip wiring design, and more particularly, the manner of routing wires in chips. Ex. 1001, 1:5–8. Semiconductor chips may have tens of millions of individual wires, such that sophisticated routing software is typically used for routing. *Id.* at 1:10–13. To minimize the time to perform the routing calculations, multi-threading techniques may be used. *Id.* at 1:16–17. Multi-threading is the concurrent execution of threads, i.e., sequential streams of program code instructions and/or the processing resources used to process such a stream. *Id.* at 1:19–22. However, when the routing process involves subdividing the surface of the chip into a grid of tiles, such that routing may performed on a tile-by-tile basis, multi-threading is not easily applied to “global” routing of wires that extend across multiple tiles. *Id.* at 1:31–38.

The processing uses a windowing technique in which a window representing a subset of the total global net pool is selected, and the window effectively slides across the pool of global nets to route the entire pool. *Id.*

at 2:7–11. Individual nets are routed in isolation from each other, which results in a possibility that two nets will be impermissibly routed in the same region. *Id.* at 2:32–37. To address such conflicts, different types of nets are sorted by priority. *Id.* at 2:38–54. For example, power and ground nets may be identified as the highest priority, such that they are routed before other nets. *Id.* at 2:53–56.

E. Challenged Claims

Petitioner challenges claims 1–4, 12, 13, and 16–19 of the '614 patent. Claim 1, reproduced below (with bracketed identifying labels added), is an independent claim:

1. [1.1] A method of routing a semiconductor chip's global nets, comprising:

[1.2] ranking said semiconductor chip's global nets, wherein said ranking includes at least one of the following:

[1.2.a] ranking power/ground nets over clock signal nets;

[1.2.b] ranking power/ground nets over timing/slew critical nets;

[1.2.c] ranking clock signal nets over timing/slew critical nets;

[1.2.d] ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;

[1.3] identifying a subset of said global nets;

[1.4] routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;

[1.5] identifying a second subset of said global nets;

[1.6] routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second

subset's other global nets but in respect of the routes of said subset of global nets.

Ex. 1001, 8:53–9:5.

F. Prior Art Relied Upon

Petitioner relies upon the prior art references listed below. Pet. 1–2.

U.S. Patent Application Publication 2007/0028201 A1 (filed June 28, 2006; published Feb. 1, 2007) (“Mehrotra,” Ex. 1004);

U.S. Patent No. 6,397,375 B1 (filed Feb. 18, 2000; patented May 28, 2002) (“Block,” Ex. 1005);

U.S. Patent No. 6,324,674 B2 (filed Apr. 17, 1998; patented Nov. 27, 2001) (“Andreev,” Ex. 1006);

“Algorithms for VLSI Physical Design Automation,” Naveed Sherwani, Springer Science+Business Media, LLC, 2nd ed., 1995 (“Sherwani,” Ex. 1007).

Based on the current record, we determine Petitioner has made a threshold showing that these references are prior art patents or printed publications under 35 U.S.C. § 102. *See* Pet. 16, 21, 48–49; Ex. 1004, codes (22), (43); Ex. 1005, codes (22), (45); Ex. 1006, codes (22), (45); Ex. 1007, 3. Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003).

G. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–4, 12, 13, and 16–19 of the '614 patent on the following grounds (Pet. 2):

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–4, 12, 13, 16–19	103(a)	Block, Mehrotra
1–4, 12, 13, 16–19	103(a)	Andreev, Sherwani

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29,

II. DISCUSSION

A. Discretionary Denial Under 35 U.S.C. § 314(a)

Institution of an *inter partes* review is discretionary. Section 314(a) of title 35 of the United States Code provides that “[t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” The U.S. Supreme Court has explained that because § 314 includes no mandate to institute review, “the agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.” *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (explaining that under § 314(a), “the PTO is permitted, but never compelled, to institute an IPR proceeding”). The Director has delegated this authority under § 314(a) to the Board. 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

In this proceeding, Patent Owner argues that we should exercise discretion to deny institution under § 314(a) because the factors identified in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”), weigh in favor of denying institution. Prelim. Resp. 1. We authorized additional briefing on this issue. *See* Petitioner’s Reply to Patent Owner’s Preliminary Response, Paper 9 (“Reply”), and

125 Stat. 284, 287–88 (2011), revised 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application from which the ’614 patent issued was filed before this date, the pre-AIA versions of §§ 102 and 103 apply.

Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, Paper 10 ("Sur-Reply").

In *Fintiv*, the Board ordered supplemental briefing on a nonexclusive list of factors for consideration in analyzing whether the circumstances of a parallel district court action are a basis for discretionary denial of trial institution under *NHK Spring Co. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential). *Fintiv*, Paper 11 at 5–16.

Those factors include:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 5–6. Here, we consider these factors to determine whether we should exercise discretion to deny institution. In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Id.* at 6.

Factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

Petitioner represents that the district court case is stayed "until at least February 2022." Reply 1. Petitioner argues that this stay, although not for

the pending IPR, should weigh against institution. *Id.* at 1–2. Petitioner further argues that further stay will be sought if the IPR is instituted, and that prior actions of the district court judge in other cases indicate that such a stay is likely. *Id.* at 2–3.

Patent Owner argues that this factor favors discretionary denial because Petitioner has not asked for a stay pending *inter partes* review, and presents reasoning why the district court judge might deny such a stay. Sur-Reply 2–3.

In *Fintiv*, the panel stated, “[a] district court stay of the litigation pending resolution of the PTAB trial allays concerns about inefficiency and duplication of efforts.” *Fintiv*, Paper 11 at 6. On the record before us, Petitioner has not produced evidence that a stay for the results of the instant *inter partes* review has been requested. The district court stay currently in force is for a limited time, until February 2022. Thus, the stay will expire approximately one month after issuance of this decision on institution. The effect of the current stay on the pending *inter partes* review proceeding would be extremely minimal, and would not appear to meaningfully allay any concerns of inefficiency or duplication of efforts.

Furthermore, the parties’ reliance on other cases in which the district court judge considered requests for stay is misplaced. As the Board has explained, “[a] judge determines whether to grant a stay based on the facts of each specific case as presented in the briefs by the parties.” *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15, 12 (PTAB May 13, 2020) (informative) (“*Fintiv II*”). “We decline to infer, based on actions taken in a different case with different facts, how the District Court would rule should a stay be requested by the parties in the parallel case here.” *Id.*

Accordingly, we find that this factor is neutral; i.e., it does not weigh for or against exercising our discretion to deny institution.

Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Petitioner argues that the trial date of September 26, 2022, no longer applies because earlier deadlines have not been met due to the district court's stay. Reply 3–4. Petitioner argues that the five month stay will cause the trial date to be delayed until at least March 2023, after the expected January 2023 final written decision in the IPR. *Id.* at 4.

Patent Owner argues that the district court has not issued an amended trial date. Sur-Reply 3. Patent Owner further argues that there is no certainty that the trial date will be delayed later than the existing September 2022 trial date. *Id.* at 3–4.

Although Petitioner speculates that the dates in the original trial schedule no longer apply, Petitioner has not produced evidence of an updated scheduling order in the parallel litigation that would affect the trial date. However, we appreciate Petitioner's point that the fact that some dates in the district court's existing scheduling order have not been met renders uncertain the remaining dates. For purposes of this factor, Petitioner has shown some uncertainty as to whether the parallel litigation will go to trial before the final written decision is due in this proceeding. In view of the foregoing, we determine that this factor is neutral.

Factor 3: investment in the parallel proceeding by the court and the parties

Petitioner argues that this factor weighs towards institution because significant district court work remains and cannot commence until at least

February 2022. Reply 4. Petitioner represents that the parties “have taken no fact depositions and other significant fact discovery remains, as does other resource-intensive work, such as expert reports and depositions, and dispositive motions.” *Id.* (citing Ex. 2008 at 1). Petitioner further argues that it moved with reasonable diligence because the petition was filed three months after final infringement contentions were served, and less than a week after mediation between the parties. *Id.* at 5. Petitioner contends that such delay was due to a hope that the parties could resolve their differences through a mediated settlement. *Id.*

Patent Owner counters that Petitioner waited until the final day of its one year period to file its petition, and that Petitioner “offered no justification for this dilatory tactic.” Prelim. Resp. 10. Patent Owner further argues that substantial work, including for example “exchange[of] infringement, invalidity, and damages contentions” and “claim construction,” has been done by the parties and the court, which has a “deep knowledge of the facts and technology,” and that this factor thus weighs in favor or denying institution. *Id.* at 6–10.

Based on the present record, we are persuaded by Petitioner’s showing that the district court and the parties have not invested substantially in the merits of the invalidity positions. The district court addresses two terms in its claim construction order. Ex. 2001, 12–19. One of those terms, “ranking shorter length and lower fan-out nets,” is not at issue in the proceeding, because Petitioner asserts that, as an alternative limitation, it need not be taught because Petitioner has shown another alternative to be taught. Pet. 30–31. For the other construed term, addressing the prohibition of conflicts between routing of subsequent subsets, Petitioner addresses both

the construction that has been advanced by Patent Owner and the construction tentatively adopted by the district court. *Id.* at 14–15; Ex. 2001, 13–15.

There is no indication in the record that the parties have completed significant discovery on the merits. Although the parties and the court have invested some effort, a significant portion of work still remains to be done in the district court proceeding—e.g., the completion of fact and expert discovery and dispositive motions. We find instructive the similar investment in *Sand Revolution II*, which involved a *Markman* order and recognized that fact discovery, expert reports, and substantive motion practice remained. *Sand Revolution II, LLC v. Cont’l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 10–11 (PTAB June 16, 2020) (informative) (“*Sand Revolution II*”). *Sand Revolution II* weighed factor 3 “marginally, if at all, in favor of denial.” *Id.* at 11.

Moreover, Petitioner’s delay is mitigated by its prompt filing after a mediation session between the parties. Although Patent Owner faults the Petitioner because Petitioner did not incur IPR costs until after the mediation session, Patent Owner does not explain why it would not be reasonable to delay seeking action until mediation was unsuccessful. Patent Owner does not explain or allege why such mediation might not reasonably have some probability of resolving the issues such that filing *inter partes* review would have been unnecessary. We find it reasonable for Petitioner to have waited until after the mediation to file its Petition.

Therefore, weighing the facts in this particular case, including the time invested by the parties and the district court in the parallel litigation, the extent to which the investment in the district court proceeding relates to

issues of patent validity, and the timing of the filing of the Petition, we find that this factor weighs marginally, if at all, in favor of exercising discretion to deny institution.

Factor 4: overlap between issues raised in the petition and in the parallel proceeding

Patent Owner argues that “Siemens’s petition asserts *virtually identical* claims, arguments, and evidence as those presented to the district court. Siemens’s IPR petition challenges the same claims of the ’614 patent, claims 1–4, 12–13, and 16–19, as are at issue in the district court.” Prelim. Resp. 11. Patent Owner argues that both alleged bases for obviousness in the IPR petition rely on references that were asserted in the litigation. *Id.* at 12.

Petitioner provides a stipulation not to pursue any instituted IPR ground in district court. Reply 5 (citing Ex. 1017). The stipulation states, “Siemens stipulates that, should IPR be instituted in IPR2021-01212, -01213, or -01215, then Siemens will not pursue in the N.D. Cal. district court litigation any prior art invalidity defense that is the same as a ground of unpatentability in any instituted IPR.” Ex. 1017, 1. Petitioner argues that this moots overlap and weights at least slightly against discretionary denial in factor 4, citing *Sand Revolution II*, Paper 24 at 12. Reply 5.

In response to the stipulation, Patent Owner argues that Petitioner’s stipulation fails to cure any potential overlap and that Petitioner is free to pursue arguments using the same prior art, provided that the art is combined in different ways. Sur-Reply 5. Patent Owner argues that this stipulation at best “marginally” mitigates overlap of issues, citing *Google LLC v. Ikorongo Tech. LLC*, IPR2021-00204, Paper 13 at 10–12 (PTAB June 7, 2021). *Id.*

We are persuaded by Petitioner’s arguments that the overlap in proceedings is limited as a result of the stipulation. Notably, Petitioner’s stipulation is similar to the stipulation provided in *Sand Revolution*. *Sand Revolution II*, Paper 24, at 12 n.5. In *Sand Revolution*, the Petitioner stipulated “only that it will not pursue, in district court, the ‘same grounds’ presented in the Petition.” *Id.* Consistent with *Sand Revolution*, we find Petitioner’s stipulation mitigates to some degree the concerns of duplicative efforts between district court and the Board, as well as concerns of potentially conflicting decisions. *See id.* at 11–12. Thus, we find that this factor weighs somewhat against exercising discretion to deny institution.

Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

It is undisputed that Petitioner is a defendant in the parallel litigation. Patent Owner argues that this favors denying institution. Prelim. Resp. 13.

As the Board explained in *Fintiv*, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact *against exercising discretion* to deny institution under *NHK*.” *Fintiv*, Paper 11 at 13–14 (emphasis added). The Board determined in *Sand Revolution* that “[a]lthough it is far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same, or where a district court is scheduled to go to trial before the Board’s final decision would be due in a related *inter partes* review, this factor weighs in favor of discretionary denial.” *Sand Revolution II*, Paper 24 at 12–13. The Board has also held that “[b]ecause the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.” *Fintiv II*, Paper 15 at 15. Here,

although it is undisputed that Petitioner is a defendant in the parallel litigation, it is unclear whether the parallel litigation will go to trial before the final written decision is due in this proceeding. Therefore, we find that factor 5 is neutral.

Factor 6: other circumstances that impact the Board's exercise of discretion, including the merits.

The final *Fintiv* factor is a catch-all that takes into account any other relevant circumstances. The decision whether to exercise discretion to deny institution is based on “a balanced assessment of all relevant circumstances in the case, including the merits.” Consolidated Trial Practice Guide 58, *available at* <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

“For example, if the merits of a ground raised in the petition seem particularly strong on the preliminary record, . . . the institution of a trial may serve the interest of overall system efficiency and integrity because it allows the proceeding to continue in the event that the parallel proceeding settles or fails to resolve the patentability question presented in the PTAB proceeding.” *Fintiv*, Paper 11 at 14–15. A full merits analysis is not necessary as part of deciding whether to exercise discretion not to institute, but rather the parties may point out, as part of the factor-based analysis, particular “strengths or weaknesses” to aid the Board in deciding whether the merits tip the balance one way or another. *Id.* at 15–16.

Petitioner argues that the lack of any substantive merits-based argument by Patent Owner confirms the strength of the Petition, thus favoring institution. Reply 5. Patent Owner argues that the claims are at least novel, because Petitioner has not raised any anticipation grounds. Prelim. Resp. 14. Patent Owner further argues that the petition fails to

address in full the district court's claim constructions. *Id.* Patent Owner argues that factor six therefore favors denial.

Patent Owner's arguments are unavailing as to this factor. At this preliminary stage of this proceeding, Patent Owner proffers no substantive arguments to rebut Petitioner's asserted ground of unpatentability. We have reviewed Petitioner's unpatentability arguments and supporting evidence. As discussed below, on this record, we determine that Petitioner has demonstrated sufficiently for purposes of this Decision that the challenged claims of the '614 patent are unpatentable. We find this factor is neutral.

Conclusion on Discretionary Denial Under § 314(a)

As noted in *Fintiv*, we consider the above six factors when taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. In weighing the totality of the evidence, we decide not to exercise discretion under § 314(a) to deny institution.

Accordingly, under the particular circumstances of this case, we are not persuaded that the interests of efficiency and integrity of the system would be best served by invoking our authority under § 314(a) to deny institution of a potentially meritorious Petition.

B. Legal Standards

1. *§ 103(a)*

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze the asserted grounds based on obviousness with these principles in mind.

C. Level of Skill in the Art

Petitioner offers an assessment as to the level of skill in the art as of the time the ’614 patent was filed. Pet. 4. For purposes of this proceeding, Petitioner and Petitioner’s expert “adopt the [following] definition for the person of ordinary skill in the art”: a person with “a bachelor’s degree in electrical engineering, computer engineering or electrical and computer engineering or equivalent and two or more years of experience with CMOS VLSI (very large-scale integration) circuit design, electronic design automation for VLSI, or ASIC (application-specific integrated circuit) design fields.” *Id.* at 11; Ex. 1003 ¶ 70 (Robins Declaration). Petitioner notes that this assessment was presented to the district court by Patent Owner, but that Petitioner has also argued for a higher level of skill in the art. Pet. 11. Here, Patent Owner has not provided an assessment of the level of ordinary skill in the art. *See generally* Prelim. Resp. To the extent necessary, and for purposes of this Decision, we accept the assessment

² Patent Owner does not identify any secondary considerations to be considered. Accordingly, we do not consider this aspect of the obviousness analysis at this stage of the proceeding.

offered by Petitioner as it is supported by the Robins Declaration and is consistent with the '614 patent and the asserted prior art.

D. Claim Construction

Petitioner asserts that in litigation, the parties have agreed that the term “global nets” should be construed as “nets not contained wholly within any single tile on the chip.” Pet. 4 (citing Ex. 1009, 2). Petitioner further adopts Patent Owner’s construction for the terms and phrases listed below.

The phrase “each of said global nets within said second subset routed by one of said threads in isolation of said second subset’s other global nets but in respect of the routes of said subset of global nets” is proposed to be construed as “each global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset and where the routing is in respect of the routes of said [first] subset of global nets.” *Id.* at 14–15 (alteration in original, emphasis omitted). Petitioner notes that the district court has tentatively construed the phrase as “Each global net of the second subset is independently routed by a respective thread, where the threads routing nets of the second subset do not communicate routing information with one another, and the resulting routing does not conflict with routings of the first subset of global nets.” *Id.* (citing Ex. 1011, 2) (emphasis omitted).

The phrase “timing/slew critical nets” is proposed to be construed as nets that are not clock nets and whose signals should be fast. *Id.* at 16.

In its Preliminary Response, Patent Owner does not propose any explicit claim constructions. *See* Prelim. Resp.

We apply the same standard that is used to construe a patent claim in a civil action under 35 U.S.C. § 282(b), and construe each claim in accordance

with the ordinary and customary meaning of such claim, as understood by one of ordinary skill in the art in the context of the patent, and the prosecution history pertaining to the patent, as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019)). “[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). For the purposes of institution, we do not expressly construe any claim terms beyond the extent necessary in our discussion of the parties’ arguments below.

E. Asserted Obviousness of Claims over Block and Mehrotra

Petitioner contends that claims 1–4, 12, 13, and 16–19 of the ’614 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the combined teachings of Block and Mehrotra. Pet. 16.

Petitioner also relies upon the Robins Declaration to support its positions. Ex. 1003. At this stage of the proceeding, we are persuaded by Petitioner’s explanations and supporting evidence. We begin our analysis with a brief overview of Block and Mehrotra.

1. Overview of Block

Block relates to interconnect routing in integrated circuit design, and more particularly, to managing the metal resources used in over-the-block routing in integrated circuits. Ex. 1005, 1:7–9. Figure 3 is reproduced below.

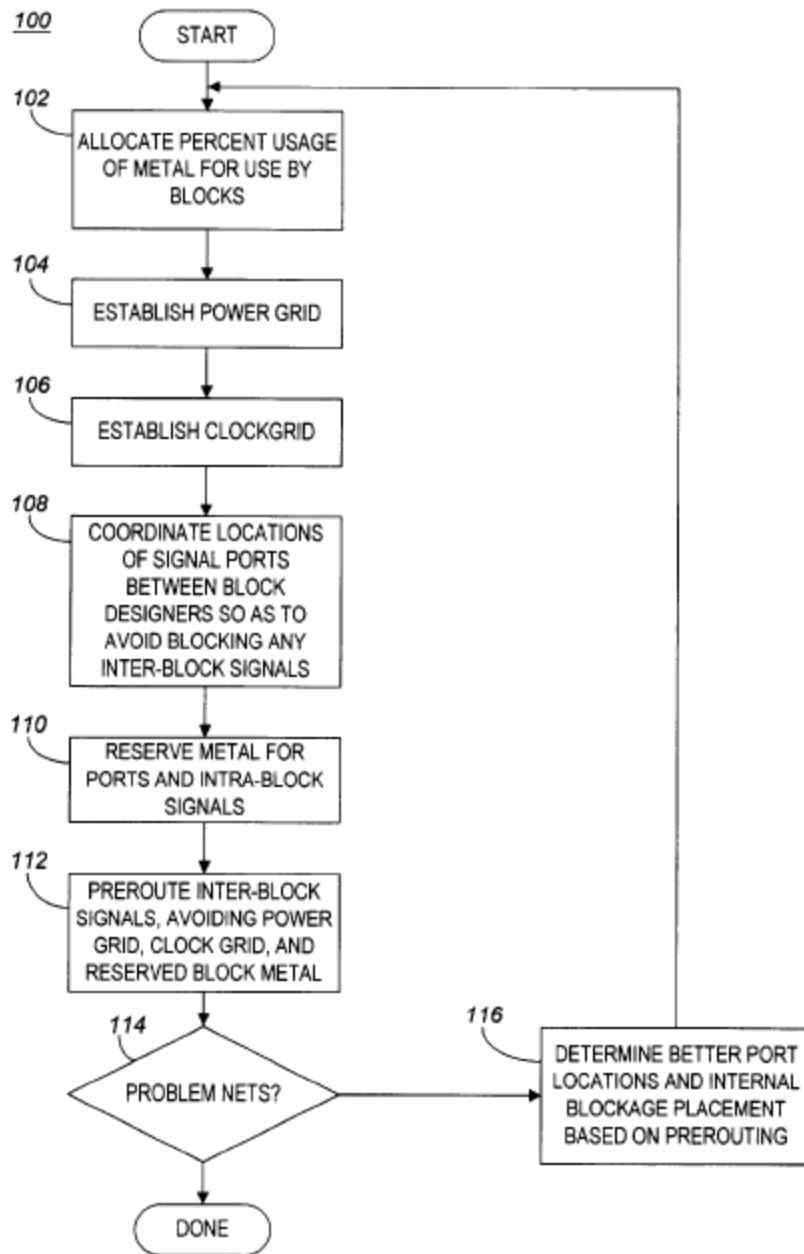


FIG. 3

Figure 3 portrays a flowchart for the physical design process of an integrated circuit to efficiently reserve metal wiring. *Id.* at 3:53–57; Fig. 3. Starting with allocating percent usage of metal for use by blocks, the process then establishes a power grid layout, then establishes a clock grid layout. Ex. 1005, 4:1–41. The process then coordinates inter-block routing,

reserving metal for ports and intra-block signals, and pre-routing global routing. *Id.* at 4:41–5:13. During the pre-routing process, if any nets are encountered that have problematic timing or routing, the signal port locations and placement of sub-blocks within the blocks are altered, and better port locations and internal blockage placement are determined based on pre-routing. *Id.* at 5:13–36.

2. Overview of Mehrotra

Mehrotra relates to strategies for optimizing and evaluating possible routes for netlist connections. Ex. 1004 ¶ 13. Figure 9, as annotated and altered by Petitioner,³ is reproduced below.

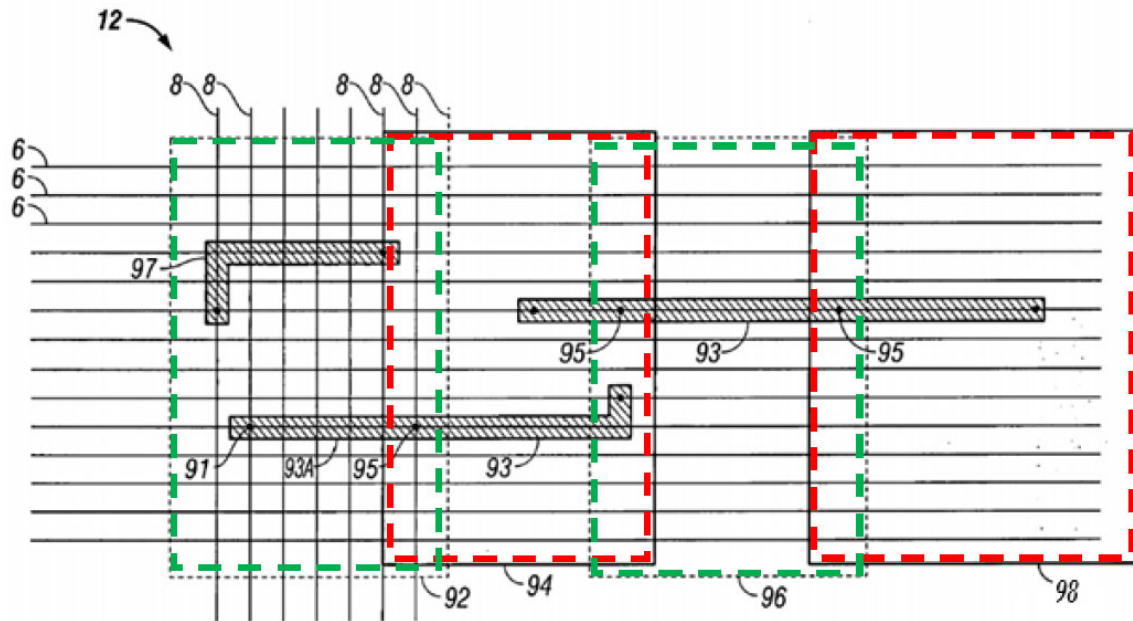


Figure 9 portrays a routing grid 12 having gridlines 6, traces 93 and 97, and virtual pins 95, wherein the grid is divided into areas 92, 94, 96, and 98, for which non-overlapping and non-adjacent areas may be routed in

³ Petitioner has altered the number of the rightmost area from 97 to 98, based on an apparent misnumbering in Mehrotra. Pet. 23–24.

parallel. *Id.* ¶¶ 96–100. In an example processing routine, areas 92 and 96 are chosen for parallel processing. *Id.* ¶ 96. Multi-area traces 93 are subdivided into subtraces, such as subtrace 93A. *Id.* ¶¶ 99–100. Route searches are then performed for traces in areas 92 and 96 simultaneously. *Id.* ¶ 100. Subsequently, route searches are performed simultaneously for traces and subtraces in areas 94 and 98. *Id.* ¶ 102. Petitioner annotates Figure 9 to highlight simultaneously routed areas: areas 92 and 96 are highlighted with a green dashed line and dotted-line border; areas 94 and 98 are highlighted with a red dashed line and solid-line border. Pet. 23.

3. *Analysis*

Petitioner provides a detailed analysis supported by testimony about how the references teach the limitations in the claims. Pet. 27–47. We begin with claim 1.

a) *Claim 1*

[1.1] A method of routing a semiconductor chip's global nets

Petitioner points to Block's description of an integrated circuit having functional blocks and using metal layers to route nets across the circuit. *Id.* at 29 (citing Ex. 1005, 3:26–43). Petitioner further points to Block's power, clock, and inter-block signals being routed in as global nets in steps 104, 106, and 112. *Id.*

Petitioner further points to Mehrotra's parallel processing routing scheme that routes global nets, i.e., “nets not contained wholly within any single tile on the chip.” *Id.* (citing Ex. 1004 ¶¶ 92–93). Petitioner points to description of routing traces 93, “which a POSITA would have recognized as corresponding to nets that span multiple tiles because they ‘span many tiles created by the routing grid; not only do these traces span multiple tiles

but they also span multiple areas of the design.” *Id.* at 29–30 (citing Ex. 1004, Fig. 9, ¶¶ 96, 99; Ex. 1003 ¶ 106). Petitioner additionally points to Mehrotra’s “global routing function employed in combination with [its] parallel processing function.” *Id.* at 30 (quoting Ex. 1004, ¶ 106).

Regardless of whether the preamble is limiting, which we do not reach here, Petitioner shows sufficiently for purposes of institution that the recitation in the preamble is satisfied by the prior art.

[1.2] ranking said semiconductor chip’s global nets, wherein said ranking includes at least one of the following:
[1.2.a] ranking power/ground nets over clock signal nets;
[1.2.b] ranking power/ground nets over timing/slew critical nets;
[1.2.c] ranking clock signal nets over timing/slew critical nets;
[1.2.d] ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;

Petitioner argues that the claim’s recitation, “includes at least one of the following,” requires only one of the recited rankings to be shown. *Id.* at 31 n.10. Petitioner points to Block’s order of routing, with power/ground being routed first, then clock nets, and then other signals including global inter-block signals. *Id.* at 31–32 (citing Ex. 1005, Fig. 3). Petitioner relies upon declarant Robins’ testimony that a POSITA would have understood “that the Block method ranked power/ground over all other nets, including clock signal nets and timing/slew critical nets, and that Block ranked clock signal nets second, over all other non-power/ground nets.” *Id.* at 31 (citing Robins ¶¶ 109–110).

[1.3] identifying a subset of said global nets;

Petitioner points to the combined teachings of Block and Mehrotra; specifically, modifying Block to use Mehrotra's parallel processing routing scheme. *Id.* at 33. Petitioner points to Mehrotra's identification of areas 92 and 96 to be processed during a first parallel processing period and areas 94 and 98 to be processed during a second parallel processing period. *Id.* (citing Ex. 1004 ¶¶ 96–97). Petitioner points to step 1004 of Mehrotra as identifying a subset of global nets for the first parallel processing period and to step 1005 of Mehrotra as identifying a subset of global nets for the second parallel processing period. *Id.* at 33–34 (citing Ex. 1004 ¶¶ 100–102; Ex. 1003 ¶ 118). Petitioner further points to Mehrotra's description of “dividing the design into ‘parallel processing areas’ and then routing the respective global nets in each area.” *Id.* at 34 (citing Ex. 1004 ¶¶ 112–114, Figs. 11–13). Petitioner relies on declarant Robins' testimony that “[r]outing the nets during the different parallel processing periods necessarily would have required identifying the subsets of nets for each period.” *Id.* (citing Ex. 1003 ¶ 118).

[1.4] routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;

Petitioner points to Mehrotra's description of using parallel processors to simultaneously route the subset of global nets for areas 92 and 96. *Id.* (citing Ex. 1004 ¶ 101). Relying on its declarant, Petitioner characterizes Mehrotra's parallel processors as multiple threads, and Mehrotra's traces and subtraces as global nets. *Id.* at 34–35 (citing Ex. 1003 ¶¶ 121–122). With regard to routing in isolation, Petitioner points to Mehrotra's

description of its parallel processing scheme as “not requir[ing] communication between processors as they work on their assigned parallel tasks,” and that the distance between areas “helps avoid any need to communicate between processors.” *Id.* at 35 (quoting Ex. 1004 ¶¶ 95–96).

[1.5] identifying a second subset of said global nets;

Petitioner points to a second subset of global nets in the form of traces and subtraces within areas 94 and 98, with the first subset being within areas 92 and 96. *Id.* at 37 (citing Ex. 1004 ¶ 97). Petitioner further points to Mehrotra’s dividing multi-area traces into subtraces, in step 1003, and performing route searches for traces and subtraces in areas 94 and 98 simultaneously. *Id.* (citing Ex. 1004 ¶¶ 99, 102).

[1.6] routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subset’s other global nets but in respect of the routes of said subset of global nets.

Petitioner points to the route searches in areas 94 and 98 being performed simultaneously, and alleges that the description of a separate processor running in parallel for the search in areas 92 and 96 would also apply to areas 94 and 98. *Id.* at 38–39 (citing Ex. 1004 ¶ 101; Ex. 1003 ¶ 135). Petitioner relies on the reasoning presented for element 1.4, *supra*, in characterizing Mehrotra’s parallel processors as multiple threads, and Mehrotra’s traces and subtraces as global nets, and the routing of one thread being performed in isolation of the second subset’s other global nets. *Id.* at 39–41. Petitioner relies on Mehrotra’s description that the later-routed areas 94 and 98 are coupled to a memory that stores completed traces. *Id.* at 41 (citing Ex. 1004 ¶¶ 100–102). Petitioner points to Mehrotra’s description of

processing multiple regions on multiple processors simultaneously “***without creating conflicts***, that could arise, for example, when two processors try to route a trace on the same gridpoint.” *Id.* at 42 (citing Ex. 1004 ¶ 15).

Petitioner relies on declarant Robins’ testimony that “the later-occurring processing for areas 94 and 98 would take into account the previously completed traces for areas 92 and 96, for example, by accessing those completed traces stored in common memory.” *Id.* at 41–42 (citing Ex. 1003 ¶¶ 139–141).

- b) *Claim 2. The method of claim 1 further comprising geographically dispersing said subset of global nets prior to said routing of said subset of global nets.*

Petitioner points to Mehrotra’s description of creating geographically dispersed areas, e.g., areas 92 and 96 that “are separated by a separation distance.” *Id.* at 43 (citing Ex. 1004 ¶ 96). Petitioner relies on its declarant Robins, stating a person having ordinary skill in the art “would understand [] the traces within areas 92 and 96 to be geographically dispersed prior to routing by being non-adjacent and non-overlapping with traces found within the other area.” *Id.* at 43–44 (citing Ex. 1003 ¶ 146).

- c) *Claim 3. The method of claim 2 further comprising geographically dispersing said second subset of global nets prior to said routing of said second subset of global nets.*

Petitioner points to Mehrotra’s description of creating geographically dispersed second areas, e.g., areas 94 and 98, that are “non-overlapping and non-adjacent.” *Id.* at 44 (citing Ex. 1004 ¶ 97). Petitioner relies on its declarant, as for claim 2, to support that a person having ordinary skill in the art would understand Mehrotra’s areas to be geographically dispersed prior to routing the second subset of global nets. *Id.* (citing Ex. 1003 ¶ 149).

- d) *Claim 4. The method of claim 1 wherein said routing said subset of global nets further comprises issuing each of said global nets to one of said threads because said one thread is available.*

Petitioner points to Mehrotra’s description of “any number of areas [that] may be routed in parallel in a given processing period,” and relies on its declarant to support its position that a person having ordinary skill in the art would have found it obvious to utilize additional processors (threads) as they are available for the global nets within those areas. *Id.* at 45–46 (citing Ex. 1004 ¶ 98; Ex. 1003 ¶ 154).

- e) *Claim 12. A non transitory machine readable storage medium having program code stored thereon that when executed by a machine causes a method to be performed . . .*

Petitioner characterizes claim 12 as “nearly identical to claim 1 but written in CRM form.” *Id.* at 46. Petitioner points to the reasoning presented for claim 1, and to the descriptions in Mehrotra and Block of performing their disclosed routing methods using a computer. *Id.* Petitioner relies upon its declarant, and Mehrotra’s statement, “[c]omputer-driven routing systems are often used to build layouts to articulate designs to be expressed in an integrated circuit,” to argue that a person having ordinary skill in the art would have found it obvious to implement the combination as a non-transitory machine-readable storage medium having program code stored thereon, causing the method of claim 1 to be performed when that code is executed. *Id.* (citing Ex. 1004 ¶¶ 3, 143; Ex. 1003 ¶ 155).

- f) *Claim 13. The machine readable medium of claim of claim 12 wherein said method further comprises geographically dispersing said subset of global nets prior to said routing of said subset of global nets.*

Petitioner characterizes claim 13 as reciting limitations nearly identical to claim 2. *Id.* at 47. Petitioner asserts that claim 13 is thus obvious over the combination of Mehrotra and Block for the same reasons as presented for claims 2 and 12. *Id.* (citing Ex. 1003 ¶ 157).

- g) *Claims 16–19*

Petitioner characterizes claim 16 as reciting a computing system configured to carry out steps nearly identical to those in claims 1 and 12. *Id.* Petitioner further characterizes claims 17–19 as reciting language nearly identical to claims 2–4. *Id.* For the same reasons advanced for those claims, Petitioner asserts that claims 16–19 are obvious over the combination of Mehrotra and Block. *Id.* (citing Ex. 1003 ¶ 159).

- h) *Determination*

Patent Owner makes no arguments specific to claims 1–4, 12, 13, and 16–19. *See generally* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

At this stage of the proceeding, for purposes of institution, Petitioner has provided sufficient explanations and supporting evidence concerning these claims. These explanations identify how each limitation of these claims is taught or suggested by the applied combination of prior art.

Petitioner has further provided a rationale for each proposed combination, as well as an explanation how each combination would be accomplished with a reasonable expectation of success. Pet. 27–29.

Petitioner alleges that it would have been obvious to a person having ordinary skill in the art to implement Block's circuit design method, ranking routing of power/ground signals over clock signals, and clock signals over other global nets, to use a parallel processor routing for other global nets as taught by Mehrotra. *Id.* at 27. Petitioner points to Mehrotra's stated advantage of greatly improving the speed at which routing may take place, as providing motivation for a person having ordinary skill in the art to include Mehrotra's parallel processor routing when implementing the Block circuit design method. *Id.* (citing Ex. 1004 ¶ 94).

Petitioner argues that the combination would have a reasonable expectation of success because the techniques are compatible and complementary, stating,

Block discloses a method of routing high-priority global routes (i.e., power/ground nets, then clock signal nets) prior to remaining global nets. E.g., EX1005, EX1005, Fig. 3, 5:12-30. But Block does not specify any particular method for routing remaining lower priority global nets. A POSITA would have naturally looked to other references for teachings on how best to carry out this routing and, in doing so, would have recognized the benefits and compatibility of Mehrotra's method of parallel routing of global nets.

Id. at 28.

In view of the foregoing, we are persuaded on the current record that Petitioner is reasonably likely to prevail on its assertions that claims 1–4, 12, 13, and 16–19 would have been obvious in view of the applied combination of Block and Mehrotra.

F. Asserted Obviousness over Andreev and Sherwani

Petitioner contends that claims 1–4, 12, 13, and 16–19 of the '614 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the

combined teachings of Andreev and Sherwani. Pet. 48.

Petitioner also relies upon the Robins Declaration to support its positions. Ex. 1003. At this stage of the proceeding, we are persuaded by Petitioner's explanations and supporting evidence. We begin our analysis with a brief overview of Andreev and Sherwani.

1. *Overview of Andreev*

Andreev relates to microelectronic integrated circuits; in particular, the art of processing high fanout nets for routing integrated circuit chips. Ex. 1006, 1:7–11. Andreev addresses the problem of creating a circuit layout from a circuit diagram through a five stage process: partitioning, floor planning, placement, routing, and compaction. *Id.* at 2:45–50. Partitioning, performed to reduce the computational difficulty, results in a set of blocks and the interconnections required between blocks. *Id.* at 2:51–60. Floor planning and placement are concerned with selecting good layout alternatives for each block and inter-block and edges, relying on an initial placement and iterative improvements. *Id.* at 3:1–16. The routing phase completes the interconnections between the blocks, with the goal of using the shortest possible wire length and the space not occupied by the blocks (divided into channels). *Id.* at 3:24–30. In routing, large nets are divided into smaller nets, and routed in parallel. *Id.* at 6:43–52. The final compaction phase compresses the layout in all directions to reduce the overall chip size. *Id.* at 6:46–48.

2. *Overview of Sherwani*

Sherwani provides an overview of the VLSI (Very Large Scale Integration) physical design automation field. Ex. 1007, xviii. Sherwani addresses such topics as partitioning, placement, floorplanning, global

routing, detailed routing algorithms, reducing routing areas, and addressing problems of routing clock and power/ground nets. *Id.* at xviii–xix.

3. *Analysis*

Petitioner provides a detailed analysis supported by testimony about how Andreev and Sherwani teach the limitations in the claims. Pet. 48–74. We begin with claim 1.

a) *Claim 1* [1.1]

Petitioner points to Andreev’s description of global routing of a netlist in a method for routing nets in a semiconductor chip integrated circuit design. Pet. 54 (citing Ex. 1006, Abstr., 1:13–15, 22:45–57). Petitioner alleges that Andreev’s global routing would be understood as including routing global nets from Andreev’s description of “Steiner trees . . . constructed for connecting sets of tiles on the routing graph,” because each Steiner tree corresponds to a net. *Id.* (citing Ex. 1006, 22:44, 24:65–67; Ex. 1003 ¶ 177) (alteration in original). Petitioner further points to Sherwani’s chapter 6, dedicated to global routing, and describing global routing as finding paths for each net in a routing graph. *Id.* at 55 (citing Ex. 1007, 223, 229, 231; Ex. 1003 ¶¶ 178–179). Regardless of whether the preamble is limiting, which we do not reach here, Petitioner shows sufficiently for purposes of institution that the recitation in the preamble is satisfied by the prior art.

[1.2]

Petitioner points to Sherwani’s description of giving power and ground nets first priority over other types of nets in a semiconductor chip. *Id.* at 56 (citing Ex. 1007, 417; Ex. 1003 ¶ 182). Relying on its declarant,

Petitioner asserts that a person having ordinary skill in the art would “find it obvious to apply the teachings of Sherwani to prioritize power and ground nets for routing over clock nets and other global nets and would therefore be motivated to route power and ground nets before all other global nets, including timing/slew critical nets.” *Id.* at 56–57 (citing Ex. 1003 ¶ 183). Petitioner asserts that Sherwani’s description would be understood to teach elements 1.2.a and 1.2.b, and by teaching at least one of the alternate limitations, teaches limitation 1.2. *Id.* at 57.

[1.3]

Petitioner points to Andreev’s description of dividing a semiconductor chip “into four parts, [and giving] different processors different parts and instruct them to route only the nets that are completely contained in the corresponding parts.” *Id.* at 57 (quoting Ex. 1006, 26:15–19). Petitioner further points to Andreev’s Fig 23A as showing four quadrants, corresponding to the claimed first subset of global nets. *Id.* at 57–58. Relying on its declarant, Petitioner asserts that such nets would necessarily be identified before being routed. *Id.* at 58 (citing Ex. 1003 ¶ 186).

[1.4]

Petitioner points to Andreev’s description of routing nets, such as those shown in Figure 23A, in parallel. *Id.* at 59 (citing Ex. 1006, Fig. 18, 24:64). Relying on its declarant, Petitioner asserts that such each routed subset would be by a different processor acting in parallel with other processors acting on other subsets. *Id.* at 59–60 (citing Ex. 1003 ¶ 190). Petitioner further points to Andreev’s explanation that “nets worked on simultaneously are not in the same area,” relying on its declarant to further show that one having ordinary skill in the art would understand that the

parallel processors are operating independently, not sharing routing information with each other, and thus routing the nets of the subset in isolation of one another. *Id.* at 61 (citing Ex. 1003 ¶ 191). Petitioner further asserts, relying on its declarant, that it would be a simple design choice to have nets routed in isolation of each other, for example, to increase processing speeds. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 191–193).

[1.5]

Petitioner points to Andreev’s description of shifting the quadrants to the right to begin a new routing operation on a second set of quadrants after routing is completed for a first set of quadrants. *Id.* at 62 (citing Ex. 1006, 26:19–25). Petitioner, relying on its declarant, asserts that a person of ordinary skill in the art would find it obvious that the nets wholly within the shifted parts constitute a second subset of global nets, and that such nets must be identified in order to route the nets. *Id.* at 62–63 (citing Ex. 1003 ¶¶ 196–198).

[1.6]

Petitioner points to Andreev’s shifted quadrants as containing a second subset of global nets, and that these are routed using a different processor in parallel. *Id.* at 65–66 (citing Ex. 1006, Fig. 23A, 24:64, 26:8–11, 26:15–19, 26:19–25; Ex. 1003 ¶ 202). Petitioner further points to Andreev’s explanation that “nets worked on simultaneously are not in the same area,” relying on its declarant to further show that one having ordinary skill in the art would understand that the parallel processors are operating independently, not sharing routing information with each other, and thus routing the nets of the subset in isolation of one another. *Id.* at 67 (quoting Ex. 1006, 26:1–7; citing Ex. 1003 ¶ 203). Petitioner further asserts, relying

on its declarant, that it would be a simple design choice to have nets routed in isolation of each other, for example, to increase processing speeds. *Id.* (citing Ex. 1003 ¶¶ 204–205). Petitioner further points to Andreev’s replacement of projected occupancies with actual occupancies due to the routing of the nets, and Andreev’s description of taking into account such occupancy to avoid wire congestion. *Id.* at 68 (citing Ex. 1006, 6:28–30, 22:47–50, 24:23–63). Relying on its declarant, Petitioner further asserts that one having ordinary skill in the art would have found it obvious to consider previously-routed nets in subsequent processing periods to avoid conflicts. *Id.* at 69 (citing Ex. 1003 ¶¶ 206–207).

b) *Claims 12 and 16*

Petitioner points to description in Andreev of semiconductor design, including routing, being performed using computer applications. *Id.* at 72–73 (citing Ex. 1006, 2:1–8; 39:26–40). Petitioner, relying on its declarant, asserts that a person having ordinary skill would have found it obvious to implement the combination of Andreev and Sherwani as a non-transitory machine readable storage medium having program code thereon that when executed by a machine, performs the recited steps. *Id.* at 74 (citing Ex. 1003 ¶¶ 218, 220).

c) *Claims 2, 3, 17, and 18*

Petitioner points to Andreev’s description of splitting the chip into four parts, instructing the processors to route only the nets completely contained in those parts, and that the nets being worked on simultaneously are not in the same area. *Id.* at 69–71, 74. Petitioner further points to Andreev’s following the same operation after the quadrants are shifted to the right. *Id.* at 70, 74.

d) *Claims 4, 13, and 19*

Petitioner points to Andreev's description of processing nets in parallel in each quadrant, with a different processor processing each part. *Id.* at 72, 74. Petitioner further points to Andreev's statement that there may be thousands, or hundreds of thousands, of nets in a semiconductor chip. *Id.* (quoting Ex. 1006, 1:25–31). Relying on its declarant, Petitioner asserts that a person having ordinary skill in the art would understand that “each processor is capable of routing a single assigned net at a time and would route each net within the processor's quadrant in turn as the processor becomes available.” *Id.* at 71, 74; Ex. 1003 ¶ 214.

e) *Determination*

Patent Owner makes no arguments specific to claims 1–4, 12, 13, and 16–19. *See generally* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

At this stage of the proceeding, for purposes of institution, Petitioner sufficiently provides an explanation of how each limitation of these claims is taught or suggested by the applied combination of prior art.

Petitioner has further provided a rationale for each combination, as well as an explanation how each combination would be accomplished with a reasonable expectation of success. Pet. 50–53. Petitioner alleges that it would have been obvious to a person having ordinary skill in the art to implement Andreev's circuit design method by prioritizing routing of power/ground signals over clock signals, and clock signals over other global nets, as taught by Sherwani. *Id.* at 50. Petitioner points to Sherwani's stated advantage of best utilizing low resistivity metal layers, as providing

motivation for a person having ordinary skill in the art to implement Sherwani's routing prioritization in the parallel processing method of Andreev. *Id.* at 51 (citing Ex. 1007, 393–394, 414, 417; Ex. 1003 ¶ 172).

Petitioner argues that the combination would have a reasonable expectation of success because the techniques are compatible and complementary, stating,

Modifying Andreev with Sherwani merely arranges Andreev's routing so that power and ground are routed before clock nets and clock nets are routed before remaining global nets, and the combination has essentially no impact on Andreev's subsequent routing of smaller nets in parallel. Sherwani confirms this compatibility, stating that routing of signal nets is performed after routing power and ground nets (“[r]outing of power and ground nets is often given first priority, because the power and ground wires are usually laid out entirely on a metal layer(s) due to its low resistivity, as described above. Signal nets may share the metal layer(s) with power and ground, but they change layers whenever a power or ground wire is encountered.” EX1007, 417) and explains the complementarity (“Power and ground signals do not complicate global routing because these signals are distributed on separate layers” EX1007, 479).

Id. at 52. Petitioner further points to Sherwani's use as a treatise in the field of VLSI design automation at the relevant time. *Id.* at 52–53.

In view of the foregoing, we are persuaded that Petitioner is reasonably likely to prevail on its assertion that claims 1–4, 12, 13, and 16–19 would have been obvious in view of the applied combination of Andreev and Sherwani.

III. CONCLUSION

Taking into account the Preliminary Response, we conclude that the information presented in the Petition demonstrates that there is a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–4, 12, 13, and 16–19 of the ’614 patent as unpatentable. Given this determination, we institute trial on all challenged claims and all grounds raised in the Petition. *See SAS Inst.*, 138 S. Ct. at 1359–60; Patent Trial and Appeal Board Consolidated Trial Practice Guide 64 (Nov. 2019), *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf> (“The Board will not institute on fewer than all claims or all challenges in a petition.”). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any challenged claim.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted based on all claims and all grounds raised in the Petition, which follow:

Claims 1–4, 12, 13, and 16–19 under 35 U.S.C. § 103(a) over Block and Mehrotra;
Claims 1–4, 12, 13, and 16–19 under 35 U.S.C. § 103(a) over Andreev and Sherwani; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

IPR2021-01213
Patent 8,234,614 B1

For PETITIONER:

Andrew Mason
Todd Siegel
Cameron Clawson
Samuel Thacker
KLARQUIST SPARKMAN, LLP
andrew.mason@klarquist.com
todd.siegel@klarquist.com
cameron.clawson@klarquist.com
samuel.thacker@klarquist.com

For PATENT OWNER:

Celine Jimenez Crowson
Scott Hughes
HOGAN LOVELLS US LLP
celine.crowson@hoganlovells.com
scott.hughes@hoganlovells.com

Krista Schwartz
JONES DAY
ksschwartz@jonesday.com