

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

SIEMENS INDUSTRY SOFTWARE INC.,  
Petitioner,

v.

SYNOPSYS, INC.,  
Patent Owner.

---

IPR2021-01213  
Patent 8,234,614 B1

---

Before KEVIN F. TURNER, SCOTT C. MOORE, and  
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining No Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

## I. BACKGROUND

### *A. Background and Summary*

Siemens Industry Software Inc. (“Petitioner”) filed a Petition for *inter partes* review (“IPR”) of claims 1–4, 12, 13, and 16–19 of U.S. Patent No. 8,234,614 B1 (Ex. 1001, “the ’614 patent”). Paper 1 (“Pet.”). Patent Owner, Synopsys, Inc., (“Patent Owner”), filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). On January 13, 2022, pursuant to § 314, we instituted an *inter partes* review as to claims 1–4, 12, 13, and 16–19 of the ’614 patent on all grounds raised in the Petition. Paper 11 (“Inst. Dec.”) On May 6, 2022, Patent Owner filed a Response. Paper 22 (“Resp.”). On July 29, 2022, Petitioner filed a Reply (Paper 24, “Reply”), and on September 23, 2022, Patent Owner filed a Sur-reply (Paper 32, “Sur-reply”). Oral argument transpired on October 18, 2022, and a transcript was entered into the file of the proceeding. Paper 34 (“Tr.”). We determine Petitioner has not established by a preponderance of the evidence that claims 1–4, 12, 13, and 16–19 are unpatentable.

### *B. Real Party in Interest*

Petitioner identifies itself, Siemens AG, and Siemens Corporation, as real parties in interest to this IPR petition. Pet. viii. Patent Owner identifies itself as the real party in interest. Paper 7 (first unpaginated page).

### *C. Related Matters*

The parties indicate that the ’614 patent is involved in a patent infringement lawsuit brought by Patent Owner in the Northern District of California, *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-04151-WHO. *Id.* Patent Owner indicates that two additional patents (U.S. Patent No. 7,546,567 and U.S. Patent No. 8,407,655) are at issue in the

above-listed proceedings, and are the subject of *inter partes* review proceedings IPR2021-01212 and IPR2021-01215. Paper 7 (first unpaginated page).

*D. The '614 Patent*

The '614 patent (Ex. 1001) generally relates to semiconductor chip wiring design, and more particularly, the manner of routing wires in chips. Ex. 1001, 1:5–8. Semiconductor chips may have tens of millions of individual wires, such that sophisticated routing software is typically used for routing. *Id.* at 1:10–13. To minimize the time to perform the routing calculations, multi-threading techniques may be used. *Id.* at 1:16–17. Multi-threading is the concurrent execution of threads, i.e., sequential streams of program code instructions and/or the processing resources used to process such a stream. *Id.* at 1:19–22. However, when the routing process involves subdividing the surface of the chip into a grid of tiles, such that routing may performed on a tile-by-tile basis, multi-threading is not easily applied to “global” routing of wires that extend across multiple tiles. *Id.* at 1:31–38.

The processing uses a windowing technique in which a window representing a subset of the total global net pool is selected, and the window effectively slides across the pool of global nets to route the entire pool. *Id.* at 2:7–11. Individual nets are routed in isolation from each other, which results in a possibility that two nets will be impermissibly routed in the same region. *Id.* at 2:32–37. To address such conflicts, different types of nets are sorted by priority. *Id.* at 2:38–54. For example, power and ground nets may be identified as the highest priority, such that they are routed before other nets. *Id.* at 2:53–56.

*E. Challenged Claims*

Petitioner challenges claims 1–4, 12, 13, and 16–19 of the '614 patent. Claim 1, reproduced below (with bracketed identifying labels added), is an independent claim:

1. [1.1] A method of routing a semiconductor chip's global nets, comprising:

[1.2] ranking said semiconductor chip's global nets, wherein said ranking includes at least one of the following:

[1.2.a] ranking power/ground nets over clock signal nets;

[1.2.b] ranking power/ground nets over timing/slew critical nets;

[1.2.c] ranking clock signal nets over timing/slew critical nets;

[1.2.d] ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;

[1.3] identifying a subset of said global nets;

[1.4] routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;

[1.5] identifying a second subset of said global nets;

[1.6] routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subset's other global nets but in respect of the routes of said subset of global nets.

Ex. 1001, 8:53–9:5.

*F. Prior Art Relied Upon*

Petitioner relies upon the prior art references listed below. Pet. 1–2.

US Patent Application Publication 2007/0028201 A1 (filed June 28, 2006; published Feb. 1, 2007) (“Mehrotra,” Ex. 1004);

US Patent No. 6,397,375 B1 (filed Feb. 18, 2000; patented May 28, 2002) (“Block,” Ex. 1005);

US Patent No. 6,324,674 B2 (filed Apr. 17, 1998; patented Nov. 27, 2001) (“Andreev,” Ex. 1006);

“Algorithms for VLSI Physical Design Automation,” Naveed Sherwani, Springer Science+Business Media, LLC, 2<sup>nd</sup> ed., 1995 (“Sherwani,” Ex. 1007).

Based on the record, we determine Petitioner has shown that these references are prior art patents or printed publications under 35 U.S.C.

§ 102. *See* Pet. 16, 21, 48–49; Ex. 1004, codes (22), (43); Ex. 1005, codes (22), (45); Ex. 1006, codes (22), (45); Ex. 1007, 3. Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003).

*G. Asserted Grounds of Unpatentability*

Petitioner challenges the patentability of claims 1–4, 12, 13, and 16–19 of the ’614 patent on the following grounds (Pet. 2):

| Claim(s) Challenged | 35 U.S.C. § <sup>1</sup> | Reference(s)/Basis |
|---------------------|--------------------------|--------------------|
| 1–4, 12, 13, 16–19  | 103(a)                   | Block, Mehrotra    |
| 1–4, 12, 13, 16–19  | 103(a)                   | Andreev, Sherwani  |

---

<sup>1</sup> The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), revised 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application from which the ’614 patent issued was filed before this date, the pre-AIA versions of §§ 102 and 103 apply.

## II. DISCUSSION

### *A. Legal Standards*

#### 1. § 103(a)

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).<sup>2</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze the asserted grounds based on obviousness with these principles in mind.

### *B. Level of Skill in the Art*

Petitioner offers an assessment as to the level of skill in the art as of the time the ’614 patent was filed. Pet. 11. For purposes of this proceeding, Petitioner and Petitioner’s expert “adopt the [following] definition for the person of ordinary skill in the art”: a person with “a bachelor’s degree in electrical engineering, computer engineering or electrical and computer engineering or equivalent and two or more years of experience with CMOS VLSI (very large-scale integration) circuit design, electronic design

---

<sup>2</sup> Patent Owner does not identify any secondary considerations to be considered. Accordingly, we do not consider this aspect of the obviousness analysis at this stage of the proceeding.

automation for VLSI, or ASIC (application-specific integrated circuit) design fields.” *Id.* at 11; Ex. 1003 ¶ 70 (Robins Declaration). Petitioner notes that this assessment was presented to the district court by Patent Owner, but that Petitioner has also argued for a higher level of skill in the art. *Id.* Patent Owner and its declarant, Dr. Friedman, adopt this assessment. Resp. 8 (citing Ex. 2020 ¶¶ 25–26). We accept the assessment offered by the parties as it is supported by both declarants and is consistent with the ’614 patent and the asserted prior art.

### *C. Claim Construction*

The parties apply the District Court’s construction of certain terms. The term “global nets” is construed as “nets not contained wholly within any single tile on the chip.” Pet. 4 (citing Ex. 1009, 2); Resp. 8; Ex. 2015, 3. The phrase “[e]ach of said global nets within said second subset routed by one of said threads in isolation of said second subset’s other global nets but in respect of the routes of said subset of global nets” is construed as “[e]ach global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset, and the resulting routing does not conflict with routings of the first subset of global nets.” Resp. 7; Ex. 2001, 13; Ex. 2020 ¶ 26; Reply 3–4.

We apply the same standard that is used to construe a patent claim in a civil action under 35 U.S.C. § 282(b), and construe each claim in accordance with the ordinary and customary meaning of such claim, as understood by one of ordinary skill in the art in the context of the patent, and the prosecution history pertaining to the patent, as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019)). “[W]e need only construe terms ‘that are in controversy, and only

to the extent necessary to resolve the controversy.’’ *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). We do not expressly construe any claim terms beyond the extent necessary in our discussion of the parties’ arguments below.

*D. Asserted Obviousness of Claims over Block and Mehrotra*

Petitioner asserts that claims 1–4, 12, 13, and 16–19 of the ’614 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the combined teachings of Block and Mehrotra. Pet. 16.

Petitioner also relies upon the Robins Declaration to support its positions. Ex. 1003. Patent Owner argues that neither Block nor Mehrotra discloses routing a subset of global nets in which *each* of the global nets are routed in isolation of each other. Resp. 16. Patent Owner also argues that Mehrotra does not identify a subnet of global nets. *Id.* at 24. Patent Owner further argues that a person of ordinary skill in the art would not combine Block and Mehrotra as proposed by Petitioner. *Id.* at 29. Based on the entirety of the record, we are not persuaded by Petitioner’s explanations and supporting evidence that the combination of Block and Mehrotra teaches routing a subset of global nets in which *each* of the global nets are routed in isolation of each other. We begin our analysis with a brief overview of Block and Mehrotra.

*1. Overview of Block*

Block relates to interconnect routing in integrated circuit design, and more particularly, to managing the metal resources used in over-the-block routing in integrated circuits. Ex. 1005, 1:7–9. Figure 3 is reproduced below.

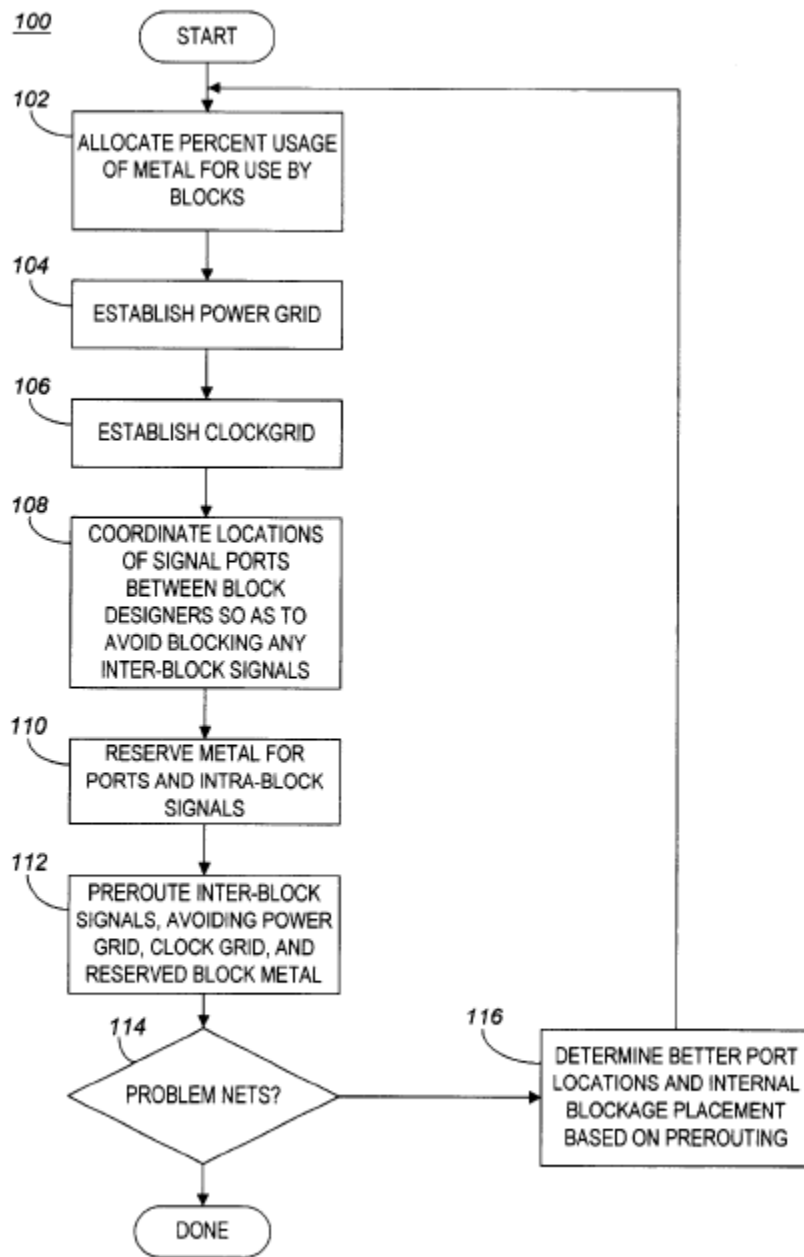


**FIG. 3**

Figure 3 portrays a flowchart for the physical design process of an integrated circuit to efficiently reserve metal wiring. *Id.* at 3:53–57; Fig. 3. Starting with allocating percent usage of metal for use by blocks, the process then establishes a power grid layout, then establishes a clock grid layout.



98, for which non-overlapping and non-adjacent areas may be routed in parallel. *Id.* ¶¶ 96–100. In an example processing routine, areas 92 and 96 are chosen for parallel processing. *Id.* ¶ 96. Multi-area traces 93 are subdivided into subtraces, such as subtrace 93A. *Id.* ¶¶ 99–100. Route searches are then performed for traces in areas 92 and 96 simultaneously. *Id.* ¶ 100. Subsequently, route searches are performed simultaneously for traces and subtraces in areas 94 and 98. *Id.* ¶ 102. Petitioner annotates Figure 9 to highlight simultaneously routed areas: areas 92 and 96 are highlighted with a green dashed line and dotted-line border; areas 94 and 98 are highlighted with a red dashed line and solid-line border. Pet. 23.

### 3. *Analysis*

We find that Petitioner’s obviousness contention fails to be persuasive as to limitations [1.4] and [1.6]. We start by addressing, for context, Petitioner’s assertions for the entirety of claim 1.

#### a) *Petitioner’s assertions*

*[1.1] A method of routing a semiconductor chip’s global nets*

Petitioner points to Block’s description of an integrated circuit having functional blocks and using metal layers to route nets across the circuit. Pet. 29 (citing Ex. 1005, 3:26–43). Petitioner further points to Block’s power, clock, and inter-block signals being routed in as global nets in steps 104, 106, and 112. *Id.*

Petitioner further points to Mehrotra’s parallel processing routing scheme that routes global nets, i.e., “nets not contained wholly within any single tile on the chip.” *Id.* (citing Ex. 1004 ¶¶ 92–93). Petitioner points to description of routing traces 93, “which a POSITA would have recognized as corresponding to nets that span multiple tiles because they ‘span many

tiles created by the routing grid; not only do these traces span multiple tiles but they also span multiple areas of the design.” *Id.* at 29–30 (citing Ex. 1004, Fig. 9, ¶¶ 96, 99; Ex. 1003 ¶ 106). Petitioner additionally points to Mehrotra’s “global routing function employed in combination with [its] parallel processing function.” *Id.* at 30 (quoting Ex. 1004, ¶ 106).

Regardless of whether the preamble is limiting, which we do not reach here, Petitioner shows sufficiently for purposes of institution that the recitation in the preamble is satisfied by the prior art.

*[1.2] ranking said semiconductor chip’s global nets, wherein said ranking includes at least one of the following:*

*[1.2.a] ranking power/ground nets over clock signal nets;*

*[1.2.b] ranking power/ground nets over timing/slew critical nets;*

*[1.2.c] ranking clock signal nets over timing/slew critical nets;*

*[1.2.d] ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;*

Petitioner argues that the claim’s recitation, “includes at least one of the following,” requires only one of the recited rankings to be shown. *Id.* at 31 n.10. Petitioner points to Block’s order of routing, with power/ground being routed first, then clock nets, and then other signals including global inter-block signals. *Id.* at 31–32 (citing Ex. 1005, Fig. 3). Petitioner relies upon declarant Robins’ testimony that a POSITA would have understood “that the Block method ranked power/ground over all other nets, including clock signal nets and timing/slew critical nets, and that Block ranked clock signal nets second, over all other non-power/ground nets.” *Id.* at 31 (citing Robins ¶¶ 109–110).

*[1.3] identifying a subset of said global nets;*

Petitioner points to the combined teachings of Block and Mehrotra; specifically, modifying Block to use Mehrotra's parallel processing routing scheme. *Id.* at 33. Petitioner points to Mehrotra's identification of areas 92 and 96 to be processed during a first parallel processing period and areas 94 and 98 to be processed during a second parallel processing period. *Id.* (citing Ex. 1004 ¶¶ 96–97). Petitioner points to step 1004 of Mehrotra as identifying a subset of global nets for the first parallel processing period and to step 1005 of Mehrotra as identifying a subset of global nets for the second parallel processing period. *Id.* at 33–34 (citing Ex. 1004 ¶¶ 100–102; Ex. 1003 ¶ 118). Petitioner further points to Mehrotra's description of “dividing the design into ‘parallel processing areas’ and then routing the respective global nets in each area.” *Id.* at 34 (citing Ex. 1004 ¶¶ 112–114, Figs. 11–13). Petitioner relies on declarant Robins' testimony that “[r]outing the nets during the different parallel processing periods necessarily would have required identifying the subsets of nets for each period.” *Id.* (citing Ex. 1003 ¶ 118).

*[1.4] routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;*

Petitioner points to Mehrotra's description of using parallel processors to simultaneously route the subset of global nets for areas 92 and 96. *Id.* (citing Ex. 1004 ¶ 101). Relying on its declarant, Petitioner characterizes Mehrotra's parallel processors as multiple threads, and Mehrotra's traces and subtraces as global nets. *Id.* at 34–35 (citing Ex. 1003 ¶¶ 121–122). With regard to routing in isolation, Petitioner points to Mehrotra's

description of its parallel processing scheme as “not requir[ing] communication between processors as they work on their assigned parallel tasks,” and that the distance between areas “helps avoid any need to communicate between processors.” *Id.* at 35 (quoting Ex. 1004 ¶¶ 95–96). Petitioner further asserts that a person having ordinary skill in the art “would have understood that separate parallel processors routing each of areas 92 and 96 to be a form of multi-threading, and thus constitutes routing the global nets within the subset (e.g., those traces and subtraces contained in 92 and 96) using multiple threads with each global net routed by a thread (i.e., a processor).” *Id.* at 35–36. Petitioner further argues that Mehrotra’s routing of nets is performed without reference to any other net because “the traces do not become ‘fixed in their location’ until ‘after searches are performed in the various areas.’” *Id.* at 36 (citing Ex. 1003 ¶¶ 125–127).

*[1.5] identifying a second subset of said global nets;*

Petitioner points to a second subset of global nets in the form of traces and subtraces within areas 94 and 98, with the first subset being within areas 92 and 96. *Id.* at 37 (citing Ex. 1004 ¶ 97). Petitioner further points to Mehrotra’s dividing multi-area traces into subtraces, in step 1003, and performing route searches for traces and subtraces in areas 94 and 98 simultaneously. *Id.* (citing Ex. 1004 ¶¶ 99, 102).

*[1.6] routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subset’s other global nets but in respect of the routes of said subset of global nets.*

Petitioner points to the route searches in areas 94 and 98 being performed simultaneously, and alleges that the description of a separate

processor running in parallel for the search in areas 92 and 96 would also apply to areas 94 and 98. *Id.* at 38–39 (citing Ex. 1004 ¶ 101; Ex. 1003 ¶ 135). Petitioner relies on the reasoning presented for element 1.4, *supra*, in characterizing Mehrotra’s parallel processors as multiple threads, and Mehrotra’s traces and subtraces as global nets, and the routing of one thread being performed in isolation of the second subset’s other global nets. *Id.* at 39–41. Petitioner relies on Mehrotra’s description that the later-routed areas 94 and 98 are coupled to a memory that stores completed traces. *Id.* at 41 (citing Ex. 1004 ¶¶ 100–102). Petitioner points to Mehrotra’s description of processing multiple regions on multiple processors simultaneously “***without creating conflicts***, that could arise, for example, when two processors try to route a trace on the same gridpoint.” *Id.* at 42 (citing Ex. 1004 ¶ 15). Petitioner relies on declarant Robins’ testimony that “the later-occurring processing for areas 94 and 98 would take into account the previously completed traces for areas 92 and 96, for example, by accessing those completed traces stored in common memory.” *Id.* at 41–42 (citing Ex. 1003 ¶¶ 139–141).

#### *Reason to Combine*

Petitioner alleges that it would have been obvious to a person having ordinary skill in the art to implement Block’s circuit design method, ranking routing of power/ground signals over clock signals, and clock signals over other global nets, to use a parallel processor routing for other global nets as taught by Mehrotra. *Id.* at 27–28. Petitioner points to Mehrotra’s stated advantage of greatly improving the speed at which routing may take place, as providing motivation for a person having ordinary skill in the art to

include Mehrotra's parallel processor routing when implementing the Block circuit design method. *Id.* (citing Ex. 1004 ¶ 94).

Petitioner argues that the combination would have a reasonable expectation of success because the techniques are compatible and complementary, stating,

Block discloses a method of routing high-priority global routes (i.e., power/ground nets, then clock signal nets) prior to remaining global nets. E.g., EX1005, EX1005, Fig. 3, 5:12-30. But Block does not specify any particular method for routing remaining lower priority global nets. A POSITA would have naturally looked to other references for teachings on how best to carry out this routing and, in doing so, would have recognized the benefits and compatibility of Mehrotra's method of parallel routing of global nets.

*Id.* at 28.

b) *Determination*

We determine that Petitioner has not met its burden to show that the combination of Block and Mehrotra teaches or suggests limitations [1.4] and [1.6]; particularly, Petitioner has not shown Mehrotra to teach or suggest “*each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets,*” as recited in limitation [1.4], and similarly recited in limitation [1.6]. Ex. 1001, 8:64–66 (emphases added). Petitioner agrees that the District Court's construction requires each net of a subset to be routed “without reference to the routing of any other net within [that] subset.” Reply 2–4 (citing Ex. 2001, 13) (stating that this construction is applicable to routing within the first and second subsets of both limitations [1.4] and [1.6]). Although Petitioner shows that Mehrotra's different areas (e.g., areas 92 and 96) are handled by parallel processors acting in isolation from each other, Petitioner has not shown that the nets within the same area

(e.g. area 92) are routed in isolation from each other.

*(1) Isolation due to parallel processing*

The Petition asserts that separate areas 92 and 96 are handled by separate parallel processors that route the global nets within the subset defined as “those traces and subtraces contained in 92 and 96.” Pet. 35–36. Petitioner asserts that Mehrotra’s statement that its parallel processing does not require communication between processors, and its silence elsewhere, demonstrates that routing of nets within an area (e.g., area 92) is performed without reference to the routing of any other nets during that same processing period. Reply 7.

Patent Owner agrees with that characterization, but argues that the claim requires *each* of the global nets to be routed in isolation of all of the other global nets within the same subset. Resp. 16–17, 20–21. Patent Owner argues that even if the two traces within area 92 are routed in isolation of the two traces within area 96, the two traces within area 92 are not routed in isolation of each other. *Id.* at 21 (citing Ex. 2020 ¶ 56).

Patent Owner provides an annotated version of Mehrotra’s Figure 9 that highlights two nets being routed within the same area, reproduced below:

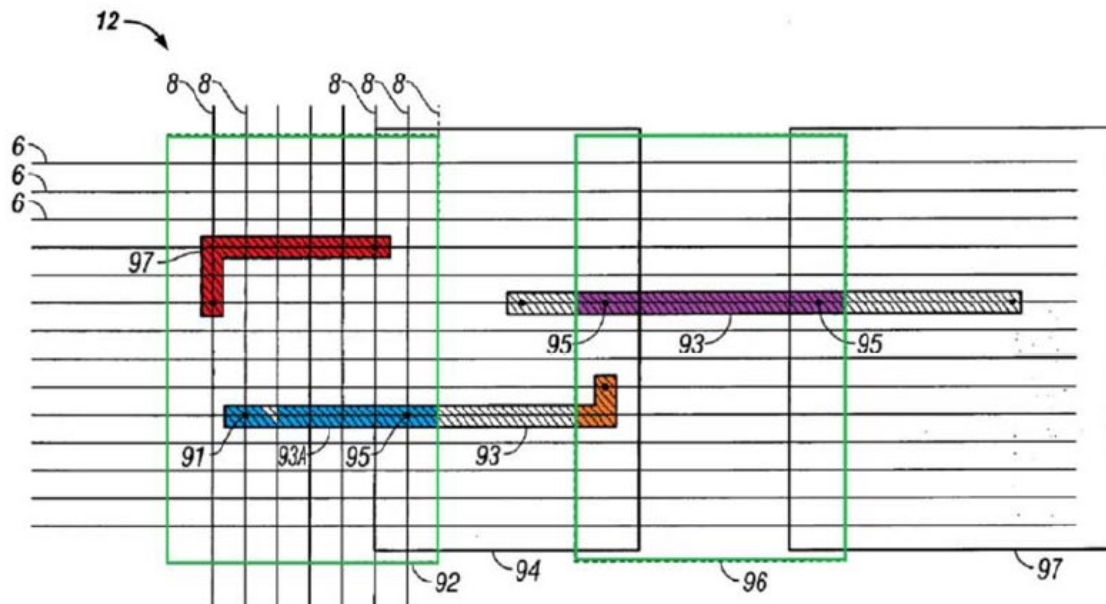


**FIG. 9**

Resp. 22. Annotated Figure 9 depicts an area of horizontal lines 6 and vertical lines 8, with green-dotted rectangles 92 and 96 therein including all or part of shaded boxes 91, 93, 95, and 97, with various highlighting annotating the parts included in those rectangles. *Id.* Patent Owner argues that rectangle 92, representing a single net-routing area, contains two traces or subtraces, i.e., trace 97 (shaded in red) and contiguous subtraces 91, 93, and 95 (shaded in blue). *Id.* at 21. Dr. Friedman states that even if traces within 92 are routed in isolation of traces within 96, the traces within area 92 are not routed in isolation of each other. Ex. 2020 ¶ 56.

We agree with Patent Owner that Petitioner's citations to Mehrotra illustrate that the nets in a first area are processed in isolation from a second area that is processed in parallel with the first area, but do not teach that each net within a given area is processed in isolation of others within that same area. Petitioner's reasoning is based on the parallel processing of distinct

areas. Petitioner attributes the lack of any need for communication between processors as resulting from the “separation distance” between “areas 92 and 96.” Thus, the benefits flowing from Mehrotra’s parallel processing; i.e., improving the speed of routing, are limited to processing areas in parallel, and are not taught to apply to nets within a single processing area.

Furthermore, Dr. Robins’ testimony illustrates that the nets within a given area are processed sequentially, not in parallel. Dr. Robins states that the global nets are assigned to the processor for that area when that processor is available, i.e., sequential processing of global nets within an area. Ex. 1003 ¶ 154 (“Mehrotra therefore discloses issuing each global net of a subset to [a] thread (i.e., a processor) because the thread is available”); Ex. 1019 ¶ 26 (“Area 92 contains two traces [that are] assigned to a single processor[, which] would perform routing for a first one of the nets and would then become available to route the second trace”). Dr. Robins clearly states that the second trace is processed “after routing the preceding trace.” *Id.* Thus, Dr. Robins’ testimony concerning how traces (nets) within a subset are processed in Mehrotra (sequentially) contradicts Petitioner’s reasoning why Mehrotra’s traces would be routed in isolation (to gain the advantages of parallel processing).

We further note that Petitioner characterizes Mehrotra’s subset as “those traces and subtraces contained in 92 and 96.” Pet. 35–36. Each of areas 92 and 96 are shown to have multiple traces or subtraces therein. Ex. 1004, Fig. 9. Thus, Petitioner’s subset requires plural traces (nets) within each area, and it is not sufficient that those traces in 92 are routed in isolation from those in 96 if the traces within each area are not routed in isolation from those in the same area (nor does Petitioner argue otherwise).

In view of the foregoing, Petitioner's argument based on Mehrotra's parallel, independent processing of distinct areas does not persuasively show that *each* of the nets within an area is processed in isolation from the other nets in the area.

(2) *Traces not "fixed in their location"*

Petitioner further argues that Mehrotra's routing of nets is performed without references to any other net because "the traces do not become 'fixed in their location' until 'after searches are performed in the various areas.'" Pet. 36–37 (citing Ex. 1003 ¶¶ 125–127). Dr. Robins states that, to a person having ordinary skill in the art, Mehrotra's description that its traces are not "fixed in their location" until after "searches are performed in the various areas" indicates that the nets would not reference the routing of other nets in the subset. Ex. 1003 ¶ 124 (citing Ex. 1004 ¶ 102)).

However, this argument is premised on parallel processing within a single area, which have found not to be taught or suggested by Mehrotra. *Infra* at II(D)(3)(b)(1). Dr. Robins' "fixed in their location" statement is based on the desirability of minimizing communications between processes being performed in parallel. Ex. 1003 ¶¶ 124–126, 153 ("A POSITA would understand that, under the principles disclosed in Mehrotra, for each area routed in parallel during a given processing period, a separate processor would be used"); Ex. 1019 ¶¶ 25–26. Likewise, Petitioner's argument is based upon "a subset of nets being processed in parallel." Pet. 37.

As discussed above, Mehrotra does not teach or suggest that traces within a single area (such as area 92) are processed in parallel. *Infra* at II(D)(3)(b)(1). Petitioner's declarant instead describes Mehrotra's traces within a single area as being processed by a single processor in turn. *Id.*

Because Petitioner’s “fixed in their location” argument is based on parallel processing within a single area, which we find unsupported, we are not persuaded.

Moreover, Patent Owner argues that Petitioner’s assertion that traces that are not fixed until after the routing process is complete would instead tend to demonstrate that the traces are routed in consideration of other traces, and not in isolation of each other. Resp. 23–24 (citing Ex. 2020 ¶ 58). We agree that Petitioner insufficiently explains, beyond its reliance on parallel processing, how delaying routing of a single trace until all traces are routed demonstrates that each trace in an area is routed in isolation of other traces in that area.

(3) *Isolation due to Mehrotra’s silence*

In its Reply, Petitioner argues that Mehrotra may meet this construction merely through silence on how routing is performed, characterizing the claim limitation as a negative limitation. Reply 4–5 (citing *Teradata Corp. v. SAP SE*, IPR2020-00943, Paper 12 at 48 (PTAB Nov. 25, 2020); *CLIO USA, Inc. v. The Procter and Gamble Co.*, IPR2013-00448, Paper 15 at 3 (PTAB Feb. 4, 2014); *Palo Alto Networks, Inc. v. Juniper Networks Inc.*, IPR2013-00466, Paper 17 at 18 (PTAB Jan. 28, 2014)). Petitioner acknowledges that Mehrotra describes a “cost matrix” taking other nets into consideration when routing a net, but asserts that this is limited to a single embodiment, and therefore, Mehrotra teaches a routing method that does not use the cost matrix. *Id.* at 5–7. During oral argument, Petitioner pointed to Mehrotra’s embodiment of Figures 9 and 10, which it characterized as a “complete process . . . that does not contain – that routes nets without reference to other nets in a subset.” Tr. 8:23–9:1. Petitioner

further stated that the absence of the cost matrix description within that process illustrates that no other nets are referenced in the routing of that embodiment. Tr. 9:9–15.

Patent Owner argues that Mehrotra is not silent on whether routing of traces within a subset is performed in isolation of other traces within that subset. Patent Owner argues that the traces within the same area (e.g., area 92) are not routed in isolation with each other because Mehrotra uses a “cost matrix” that takes neighboring traces into consideration, such as through a requirement that a 100 nm wide trace be 100 nm from any neighboring trace. *Id.* at 22–23 (citing Ex. 1004 ¶¶ 42–46). Patent Owner argues that this cost matrix scheme would be understood to apply to all embodiments in Mehrotra because it is described “immediately after its description of the prior art, and before describing any of the particular examples or embodiments.” Sur-reply 7. Patent Owner recognizes Mehrotra’s description of the cost matrix scheme in the context of “one embodiment,” “a preferred embodiment,” or “preferred embodiments” as inconsistent, but argues that a person having ordinary skill in the art would understand it to apply to all embodiments because of its placement in the reference. *Id.* at 8. Patent Owner further argues that, even if the cost matrix is not applied, Mehrotra describes a prior art method of searching for an unblocked route, which would be applied as an alternative to Mehrotra’s routing. *Id.* Patent Owner argues that these descriptions would imply, to a person having ordinary skill in the art, that nets are typically routed using algorithms that consider route blockages from other nets. Sur-reply 5, 8.

In an *inter partes* review, the Petitioner has the burden to show, by a preponderance of the evidence, that the claims are unpatentable. 35 U.S.C. §

316(e). Applied here, the Petitioner has the burden to show that Mehrotra and Block make obvious the claimed routing of each net in isolation of the other nets within that same subset. However, even assuming Petitioner's assertion that Mehrotra's Figure 9 embodiment does not include the inter-routing considerations of Mehrotra's "cost matrix" method or Mehrotra's disclosed prior art method, Petitioner does not explain why Mehrotra's silence should be considered to teach routing nets in isolation of other nets of the same area.

The Federal Circuit has explained that a "reference need not state a features' absence in order to disclose a negative limitation." *Almirall, LLC v. Amneal Pharmaceuticals LLC*, 28 F. 4<sup>th</sup> 265, 273 (Fed. Cir. 2022) (quoting *AC Techs, S.A. v. Amazon.com, Inc*, 912 F.3d 1358, 1367 (Fed. Cir. 2019)). However, Petitioner's argument that "the claim requires the *absence of reference to* the routing of any other net within a routed subset," attempts to go further in eliminating any analysis of how a person of ordinary skill would view the teachings of the reference. Reply 4 (emphasis added). Like any other limitation, determining whether a reference teaches or discloses a negative limitation requires an analysis of the reference from the viewpoint of a person of ordinary skill in the art. *See Almirall*, 28 F.4<sup>th</sup> at 273–274; *Novartis Pharmaceuticals Corp. v. Accord Healthcare, Inc.*, 38 F. 4<sup>th</sup> 1013, 1020 (Fed. Cir. 2022)(finding that, for written description, "[j]ust as disclosure is the hallmark of written description for positive limitations . . . so too for negative limitations," and "[w]hile silence will not generally suffice to support a negative claim limitation, there may be circumstances in which it can be established that a skilled artisan would understand a negative

limitation to necessarily be present in a disclosure.”).<sup>4</sup> The PTAB cases cited by Petitioner, which as non-final, non-precedential decisions are not binding on this proceeding, are not to the contrary. Thus, we do not agree with Petitioner that the absence of an explicit statement in Mehrotra of considering other nets within a subset of nets during routing would be necessarily dispositive.

Moreover, Mehrotra is not merely silent on whether other nets in the same subset are considered during routing. Rather, as pointed out by Patent Owner, and supported by testimony of Dr. Friedman, Mehrotra describes techniques in the prior art, and in embodiments of Mehrotra’s invention, in which nets are routed in dependence on other nets within the same subset. Resp. 22–23; Sur-reply 5–8. At oral argument, Petitioner argued that Mehrotra’s Figure 9 presents a complete process having no need for, or reference to, the routing of other global nets. Tr. 5. However, even assuming Mehrotra’s Figure 9 does not explicitly use its cost matrix approach, or the approach it describes for use in the prior art, Petitioner has not explained why a skilled artisan would recognize Mehrotra’s Figure 9 embodiment as providing a complete description of the routing within areas such that it excludes the possibility of routing nets in consideration of other

---

<sup>4</sup> Note that the dissent in *Novartis* agrees that “written description support is a fact-based inquiry based on the understandings of a person of ordinary skill in the art, and while ultimately recognizing that the standard for negative limitations is the same as for any other limitation.” *Id.* at 1020–1021 (Linn, dissenting).

nets within the same area. *See Almirall*, 28 F.4<sup>th</sup> at 273 (“a skilled artisan would recognize that the reference discloses a complete formulation – excluding the possibility of an additional [excluded] ingredient”).

Here, the only mention of a routing each of a subset of nets using threads in isolation of the subset’s other nets appears in the ’614 patent. Petitioner has not provided any assurances that Mehrotra’s silence as to the claimed routing method is due to common knowledge in the art rather than the inventiveness of that method. Consequently, we find unpersuasive Petitioner’s assertion that Mehrotra teaches or suggests, by its silence, “routing [a] subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset’s other global nets.”

Because we find Petitioner’s assertions that Mehrotra’s silence illustrates that its routing occurs absent reference to the routing of any other nets within the same subset unpersuasive, we need not address Patent Owner’s argument that this was impermissibly presented as a new argument in the Reply. Sur-reply 1–2.

#### (4) *Conclusion*

In view of the foregoing, we are not persuaded that Petitioner has shown, by a preponderance of the evidence, that claim 1 would have been obvious in view of the applied combination of Block and Mehrotra. Because the remaining asserted claims also require those limitations, we further determine that Petitioner has not shown, by a preponderance of the evidence, that claims 2–4, 12, 13, and 16–19 would have been obvious in view of the applied combination of Block and Mehrotra.

*E. Asserted Obviousness over Andreev and Sherwani*

Petitioner contends that claims 1–4, 12, 13, and 16–19 of the '614 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the combined teachings of Andreev and Sherwani. Pet. 48. Petitioner also relies upon the Robins Declaration to support its positions. Ex. 1003. We begin our analysis with a brief overview of Andreev and Sherwani.

*1. Overview of Andreev*

Andreev relates to microelectronic integrated circuits; in particular, the art of processing high fanout nets for routing integrated circuit chips. Ex. 1006, 1:7–11. Andreev addresses the problem of creating a circuit layout from a circuit diagram through a five-stage process: partitioning, floor planning, placement, routing, and compaction. *Id.* at 2:45–50. Partitioning, performed to reduce the computational difficulty, results in a set of blocks and the interconnections required between blocks. *Id.* at 2:51–60. Floor planning and placement are concerned with selecting good layout alternatives for each block and inter-block and edges, relying on an initial placement and iterative improvements. *Id.* at 3:1–16. The routing phase completes the interconnections between the blocks, with the goal of using the shortest possible wire length and the space not occupied by the blocks (divided into channels). *Id.* at 3:24–30. In routing, large nets are divided into smaller nets, and routed in parallel. *Id.* at 6:43–52. The final compaction phase compresses the layout in all directions to reduce the overall chip size. *Id.* at 3:46–48.

*2. Overview of Sherwani*

Sherwani provides an overview of the VLSI (Very Large Scale Integration) physical design automation field. Ex. 1007, xviii. Sherwani

addresses such topics as partitioning, placement, floorplanning, global routing, detailed routing algorithms, reducing routing areas, and addressing problems of routing clock and power/ground nets. *Id.* at xviii–xix.

### 3. *Analysis*

#### a) *Petitioner’s Assertions*

##### *[1.1] A method of routing a semiconductor chip’s global nets*

Petitioner points to Andreev’s description of global routing of a netlist in a method for routing nets in a semiconductor chip integrated circuit design. Pet. 54 (citing Ex. 1006, Abstr., 1:13–15, 22:45–57). Petitioner alleges that Andreev’s global routing would be understood as including routing global nets from Andreev’s description of “Steiner trees . . . constructed for connecting sets of tiles on the routing graph,” because each Steiner tree corresponds to a net. *Id.* (citing Ex. 1006, 22:44, 24:65–67; Ex. 1003 ¶ 177) (alteration in original). Petitioner further points to Sherwani’s chapter 6, dedicated to global routing, and describing global routing as finding paths for each net in a routing graph. *Id.* at 55 (citing Ex. 1007, 223, 229, 231; Ex. 1003 ¶¶ 178–179).

*[1.2] ranking said semiconductor chip’s global nets, wherein said ranking includes at least one of the following:*

*[1.2.a] ranking power/ground nets over clock signal nets;*

*[1.2.b] ranking power/ground nets over timing/slew critical nets;*

*[1.2.c] ranking clock signal nets over timing/slew critical nets;*

*[1.2.d] ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;*

Petitioner points to Sherwani’s description of giving power and

ground nets first priority over other types of nets in a semiconductor chip. *Id.* at 56 (citing Ex. 1007, 417; Ex. 1003 ¶ 182). Relying on its declarant, Petitioner asserts that a person having ordinary skill in the art would “find it obvious to apply the teachings of Sherwani to prioritize power and ground nets for routing over clock nets and other global nets and would therefore be motivated to route power and ground nets before. . . . all other global nets, including timing/slew critical nets.” *Id.* at 56–57 (citing Ex. 1003 ¶ 183). Petitioner asserts that Sherwani’s description would be understood to teach elements 1.2.a and 1.2.b, and by teaching at least one of the alternate limitations, teaches limitation 1.2. *Id.* at 57.

*[1.3] identifying a subset of said global nets;*

Petitioner points to Andreev’s description of dividing a semiconductor chip “into four parts, [and giving] different processors different parts and instruct them to route only the nets that are completely contained in the corresponding parts.” *Id.* at 57 (quoting Ex. 1006, 26:15–19). Petitioner further points to Andreev’s Fig 23A as showing four quadrants, corresponding to the claimed first subset of global nets. *Id.* at 57–58. Relying on its declarant, Petitioner asserts that such nets would necessarily be identified before being routed. *Id.* at 58 (citing Ex. 1003 ¶ 186).

*[1.4] routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;*

Petitioner points to Andreev’s description of routing nets, such as those shown in Figure 23A, in parallel. *Id.* at 59 (citing Ex. 1006, Fig. 18, 24:64). Relying on its declarant, Petitioner asserts that such each routed subset would be by a different processor acting in parallel with other

processors acting on other subsets. *Id.* at 59–60 (citing Ex. 1003 ¶ 190). Petitioner further points to Andreev’s explanation that “nets worked on simultaneously are not in the same area,” relying on its declarant to further show that one having ordinary skill in the art would understand that the parallel processors are operating independently, not sharing routing information with each other, and thus routing the nets of the subset in isolation of one another. *Id.* at 61 (citing Ex. 1003 ¶ 191). Petitioner further asserts, relying on its declarant, that it would be a simple design choice to have nets routed in isolation of each other, for example, to increase processing speeds. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 191–193).

*[1.5] identifying a second subset of said global nets;*

Petitioner points to Andreev’s description of shifting the quadrants to the right to begin a new routing operation on a second set of quadrants after routing is completed for a first set of quadrants. *Id.* at 62 (citing Ex. 1006, 26:19–25). Petitioner, relying on its declarant, asserts that a person of ordinary skill in the art would find it obvious that the nets wholly within the shifted parts constitute a second subset of global nets, and that such nets must be identified in order to route the nets. *Id.* at 62–63 (citing Ex. 1003 ¶¶ 196–198).

*[1.6] routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subset’s other global nets but in respect of the routes of said subset of global nets.*

Petitioner points to Andreev’s shifted quadrants as containing a second subset of global nets, and that these are routed using a different processor in parallel. *Id.* at 65–66 (citing Ex. 1006, Fig. 23A, 24:64, 26:8–

11, 26:15–19, 26:19–25; Ex. 1003 ¶ 202). Petitioner further points to Andreev’s explanation that “nets worked on simultaneously are not in the same area,” relying on its declarant to further show that one having ordinary skill in the art would understand that the parallel processors are operating independently, not sharing routing information with each other, and thus routing the nets of the subset in isolation of one another. *Id.* at 67 (quoting Ex. 1006, 26:1–7; citing Ex. 1003 ¶ 203). Petitioner further asserts, relying on its declarant, that it would be a simple design choice to have nets routed in isolation of each other, for example, to increase processing speeds. *Id.* (citing Ex. 1003 ¶¶ 204–205). Petitioner further points to Andreev’s replacement of projected occupancies with actual occupancies due to the routing of the nets, and Andreev’s description of taking into account such occupancy to avoid wire congestion. *Id.* at 68 (citing Ex. 1006, 6:28–30, 22:47–50, 24:23–63). Relying on its declarant, Petitioner further asserts that one having ordinary skill in the art would have found it obvious to consider previously-routed nets in subsequent processing periods to avoid conflicts. *Id.* at 69 (citing Ex. 1003 ¶¶ 206–207).

*Reason to Combine*

Petitioner has further provided a rationale for each combination, as well as an explanation how each combination would be accomplished with a reasonable expectation of success. Pet. 50–53. Petitioner alleges that it would have been obvious to a person having ordinary skill in the art to implement Andreev’s circuit design method by prioritizing routing of power/ground signals over clock signals, and clock signals over other global nets, as taught by Sherwani. *Id.* at 50. Petitioner points to Sherwani’s stated advantage of best utilizing low resistivity metal layers, as providing

motivation for a person having ordinary skill in the art to implement Sherwani's routing prioritization in the parallel processing method of Andreev. *Id.* at 51 (citing Ex. 1007, 393–394, 414, 417; Ex. 1003 ¶ 172).

Petitioner argues that the combination would have a reasonable expectation of success because the techniques are compatible and complementary, stating,

Modifying Andreev with Sherwani merely arranges Andreev's routing so that power and ground are routed before clock nets and clock nets are routed before remaining global nets, and the combination has essentially no impact on Andreev's subsequent routing of smaller nets in parallel. Sherwani confirms this compatibility, stating that routing of signal nets is performed after routing power and ground nets (“[r]outing of power and ground nets is often given first priority, because the power and ground wires are usually laid out entirely on a metal layer(s) due to its low resistivity, as described above. Signal nets may share the metal layer(s) with power and ground, but they change layers whenever a power or ground wire is encountered.” EX1007, 417) and explains the complementarity (“Power and ground signals do not complicate global routing because these signals are distributed on separate layers” EX1007, 479).

*Id.* at 51–52. Petitioner further points to Sherwani's use as a treatise in the field of VLSI design automation at the relevant time. *Id.* at 52–53.

b) *Determination*

We determine that Petitioner has not met its burden to show that the combination of Andreev and Sherwani teaches or suggests limitations [1.4] and [1.6]; particularly, that Petitioner has not shown Andreev to teach or suggest “*each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets,*” as recited in limitation [1.4], and similarly recited in limitation [1.6]. Ex. 1001, 8:64–66 (Emphasis

added). Petitioner agrees that the District Court’s construction requires each net of a subset, to be routed “without reference to the routing of any other net within [that] subset.” Reply 2–4 (citing Ex. 2001, 13) (stating that this construction is applicable to routing within the first and second subsets of both limitations [1.4] and [1.6]). Although Petitioner shows that Andreev’s different areas (e.g., its four separate areas in Figure 23A) are handled by parallel processors acting in isolation from each other (Pet. 60–61; Reply 20), Petitioner has not shown that the nets within the same area are routed in parallel from each other. Resp. 33–38. To the contrary, Dr. Robins explains that in Andreev, “the nets worked on simultaneously are not in the same area.” Ex. 1003 ¶ 191. Thus, the nets within an area are not, themselves, processed simultaneously, i.e., in parallel. Petitioner confirms this, stating, “where multiple nets are routed within a single quadrant, those nets would be routed by the processor assigned to that processor in turn. . . . As the processor completes routing of a net, each subsequent net would be issued to the processor because the processor has become available for routing.” Reply 27. Consequently, any effect flowing from parallel processing, such as routing nets in isolation from each other, does not accrue to the nets in the same processed area.

For this reason also, Petitioner has not persuasively shown that it “would have been a simple design choice” to have nets “belonging to a subset and processed in parallel to be routed without reference to the routing of other nets within the same subset.” Pet. 61–62; Reply 21–22. Because the nets in a single subset are not processed in parallel from the other nets in the same subset, Petitioner’s reasoning based on parallel processing is not persuasive.

Moreover, Patent Owner points out that Andreev describes a “Course Global Routing Process” in which the multiple nets within a single area are “routed to avoid conflicts by utilizing a routing process that considers projected and actual occupancies by other nets along a routing path.” Resp. 37–38 (citing Ex. 2020 ¶ 80). Although Petitioner argues that “it is unclear” whether such consideration occurs after each net is routed or after all of the nets within an area are routed (Reply 21), we agree with Patent Owner that Andreev states that consideration occurs as nets are routed, and therefore does not teach “routing each net . . . in isolation.” Sur-reply 17–18 (quoting Ex. 1006, 24:38–41 (“As nets are routed, we replace the projected occupancies with the actual ones, i.e., if the net passes through this edge, we add 1 to its occupancy and subtract the projected occupancy relative to the particular net”). We further agree with Patent Owner that this explicit teaching of Andreev contradicts Petitioner’s “design choice” reasoning in that a person having ordinary skill in the art would have reason to share routing information among nets when routing nets in a subset, and would not regard the sharing/non-sharing choices as being equally desirable. *Id.* at 18–19.

In view of the foregoing, we determine that Petitioner has not shown the combination of Andreev and Sherwani to teach or suggest limitations [1.4] and [1.5] of claim 1. Because the remaining claims include the same or similar limitations, for which Petitioner relies upon the same teachings, Petitioner has not shown the combination of Andreev and Sherwani to teach or suggest each limitation of those claims.

Therefore, we are persuaded that Petitioner has not shown, by a preponderance of the evidence, that claims 1–4, 12, 13, and 16–19 would

have been obvious in view of the applied combination of Andreev and Sherwani.

### III. CONCLUSION

For the foregoing reasons, we determine Petitioner has not established by a preponderance of the evidence that claims 1–4, 12, 13, and 16–19 are unpatentable. In summary,

| <b>Claim(s)</b>            | <b>35<br/>U.S.C. §</b> | <b>Reference(s)/Basis</b> | <b>Claim(s)<br/>Shown<br/>Unpatentable</b> | <b>Claim(s) Not<br/>Shown<br/>Unpatentable</b> |
|----------------------------|------------------------|---------------------------|--------------------------------------------|------------------------------------------------|
| 1–4, 12,<br>13, 16–19      | 103(a)                 | Block, Mehrotra           |                                            | 1–4, 12, 13,<br>16–19                          |
| 1–4, 12,<br>13, 16–19      | 103(a)                 | Andreev, Sherwani         |                                            | 1–4, 12, 13,<br>16–19                          |
| <b>Overall<br/>Outcome</b> |                        |                           |                                            | 1–4, 12, 13,<br>16–19                          |

### ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner *has not shown* based on a preponderance of evidence that claims 1–4, 12, 13, and 16–19 are unpatentable over the combined teachings of Block and Mehrotra;

ORDERED that Petitioner *has not shown* based on a preponderance of evidence that claims 1–4, 12, 13, and 16–19 are unpatentable over the combined teachings of Andreev and Sherwani;

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2021-01213  
Patent 8,234,614 B1

For PETITIONER:

Andrew Mason  
Todd Siegel  
Cameron Clawson  
Samuel Thacker  
KLARQUIST SPARKMAN, LLP  
andrew.mason@klarquist.com  
todd.siegel@klarquist.com  
cameron.clawson@klarquist.com  
samuel.thacker@klarquist.com

For PATENT OWNER:

David Cochran  
Joshua Nightingale  
Matthew Johnson  
Joseph Sauer  
Marlee Hartenstein  
Robert Breetz  
JONES DAY  
dcochran@jonesday.com  
jrmightingale@jonesday.com  
mwjohnson@jonesday.com  
jmsauer@jonesday.com  
mhartenstein@jonesday.com  
rbreetz@jonesday.com