

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIEMENS INDUSTRY SOFTWARE INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

IPR2021-01215
Patent 8,407,655 B2

Before JENNIFER MEYER CHAGNON, SCOTT C. MOORE, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. BACKGROUND

A. Background and Summary

Siemens Industry Software Inc. (“Petitioner”) filed a Petition for *inter partes* review (“IPR”) of claims 1–24 of U.S. Patent No. 8,407,655 B2 (Ex. 1001, “the ’655 patent”). Paper 2 (“Pet.”). Patent Owner, Synopsys, Inc., (“Patent Owner”), filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). An *inter partes* review may not be instituted on fewer than all claims challenged in the Petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

Having considered the Petition and the Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–24 of the ’655 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to § 314, we institute an *inter partes* review as to claims 1–24 of the ’655 patent on all grounds raised in the Petition.

B. Real Party in Interest

Petitioner identifies itself, Siemens AG, and Siemens Corporation, as real parties in interest to this IPR petition. Pet. viii. Patent Owner identifies itself as the real party in interest. Paper 8 (first unpaginated page).

C. Related Matters

The parties indicate that the ’655 patent is involved in a patent infringement lawsuit brought by Patent Owner in the Northern District of

California, *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-04151-WHO. Pet. viii; Paper 8 (first unpaginated page). Patent Owner indicates that two additional patents (U.S. Patent Number 7,546,567 and U.S. Patent Number 8,234,614) are at issue in the above-listed proceedings, and are the subject of *inter partes* review proceedings IPR2021-01212 and IPR2021-01213. Paper 8 (first unpaginated page).

D. The '655 Patent

The '655 patent (Ex. 1001) generally relates to integrated circuit design; in particular, determining changes to the design responsive to indications that the current circuit design does not comply with the design requirements. Ex. 1001, 1:19–21. Design requirement violations may include violations of setup timing, hold timing, electrical design rules, and power budgets. *Id.* at 2:16–20. The changes to the design, referred to as engineering change orders (“ECO”s), may in turn result in new violations of the design requirements. *Id.* at 1:27–28. Furthermore, violations may occur under certain combinations of operating conditions, referred to as a “scenario.” *Id.* at 1:51–54. Once a design is violation-free, then the circuit design can be readied for manufacturing. *Id.* at 1:28–30.

Determining an ECO to fix one or more violations can involve estimating parameter values for one or more components. *Id.* at 2:6–10.

The parameter values can include

- (1) timing slack values at one or more pins in the circuit design,
- (2) capacitive load values at one or more pins in the circuit design,
- (3) transition time values at one or more pins in the circuit design, and
- (4) leakage power values for gates in the circuit design.

Id. at 2:16–20.

E. Challenged Claims

Petitioner challenges claims 1–24 of the ’655 patent. Claim 1, reproduced below (with bracketed identifying labels added), is an independent claim:

1. [1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Ex. 1001, 9:54–67.

F. Prior Art Relied Upon

Petitioner relies upon the prior art references listed below. Pet. 1–2.

U.S. Patent No. 7,464,355 B2 (filed October 2, 2006; issued December 9, 2008) (“Yoshimura,” Ex. 1007);

“EDA for IC Implementation, Circuit Design, and Process Technology,” Louis Scheffer et al., CRC Press, Taylor & Francis Group (2006) (“Scheffer,” Ex. 1008);

U.S. Patent No. 7,092,838 B1 (filed June 4, 2004; patented August 15, 2006) (“Srinivas,” Ex. 1010);

Based on the current record, we determine Petitioner has made a threshold showing that these references are prior art patents or printed publications under 35 U.S.C. § 102. *See* Pet. 14, 39, 48; Ex. 1007, codes

(22), (45); Ex. 1010, codes (22), (45); Ex. 1008, 5. Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003).

G. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–24 of the ’655 patent on the following grounds (Pet. 3):

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–24	102	Yoshimura
1–24	103	Yoshimura
4–7, 9, 10, 14–17, 19, 20, 23, 24	103(a)	Yoshimura, Scheffer
1–24	103(a)	Srinivas
6, 9, 10, 16, 19, 20, 23, 24	103(a)	Srinivas, Scheffer

II. DISCUSSION

A. Discretionary Denial Under 35 U.S.C. § 314(a)

Institution of an *inter partes* review is discretionary. Section 314(a) of title 35 of the United States Code provides that “[t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” The U.S. Supreme Court has explained that because § 314 includes no mandate to institute review, “the agency’s decision to deny a

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), revised 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application from which the ’655 patent issued was filed before this date, the pre-AIA versions of §§ 102 and 103 apply.

petition is a matter committed to the Patent Office’s discretion.” *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (explaining that under § 314(a), “the PTO is permitted, but never compelled, to institute an IPR proceeding”). The Director has delegated this authority under § 314(a) to the Board. 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

In this proceeding, Patent Owner argues that we should exercise discretion to deny institution under § 314(a) because the factors identified in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”), weigh in favor of denying institution. Prelim. Resp. 1–2. We authorized additional briefing on this issue. *See* Petitioner’s Reply to Patent Owner’s Preliminary Response, Paper 10 (“Reply”), and Patent Owner’s Sur-Reply to Petitioner’s Reply to Patent Owner’s Preliminary Response, Paper 11 (“Sur-Reply”).

In *Fintiv*, the Board ordered supplemental briefing on a nonexclusive list of factors for consideration in analyzing whether the circumstances of a parallel district court action are a basis for discretionary denial of trial institution under *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential). *Fintiv*, Paper 11 at 5–16. Those factors include:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;

4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 5–6. Here, we consider these factors to determine whether we should exercise discretion to deny institution. In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Id.* at 6.

Factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

Petitioner represents that the district court case is stayed “until at least February 2022.” Reply 1. Petitioner argues that this stay, although not for the pending IPR, should weigh against institution. *Id.* at 1–2. Petitioner further argues that further stay will be sought if the IPR is instituted, and that prior actions of the district court judge in other cases indicate that such a stay is likely. *Id.* at 2–3.

Patent Owner argues that this factor favors discretionary denial because Petitioner has not asked for a stay pending *inter partes* review, and presents reasoning why the district court judge might deny such a stay. Sur-Reply 2–3.

In *Fintiv*, the panel stated, “[a] district court stay of the litigation pending resolution of the PTAB trial allays concerns about inefficiency and duplication of efforts.” *Fintiv*, Paper 11 at 6. On the record before us, Petitioner has not produced evidence that a stay for the results of the instant *inter partes* review has been requested. The district court stay currently in

force is for a limited time, until February 2022. Thus, the stay will expire approximately one month after issuance of this decision on institution. The effect of the current stay on the pending *inter partes* review proceeding would be extremely minimal, and would not appear to meaningfully allay any concerns of inefficiency or duplication of efforts.

Furthermore, the parties' reliance on other cases in which the district court judge considered requests for stay is misplaced. As the Board has explained, "[a] judge determines whether to grant a stay based on the facts of each specific case as presented in the briefs by the parties." *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15, 12 (PTAB May 13, 2020) (informative) ("*Fintiv I*"). "We decline to infer, based on actions taken in a different case with different facts, how the District Court would rule should a stay be requested by the parties in the parallel case here." *Id.*

Accordingly, we find that this factor is neutral; i.e., it does not weigh for or against exercising our discretion to deny institution.

Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Petitioner argues that the trial date of September 26, 2022, no longer applies because earlier deadlines have not been met due to the district court's stay. Reply 3–4. Petitioner argues that the five month stay will cause the trial date to be delayed until at least March 2023, after the expected January 2023 final written decision in the IPR. *Id.* at 4.

Patent Owner argues that the district court has not issued an amended trial date. Sur-Reply 3. Patent Owner further argues that there is no certainty that the trial date will be delayed later than the existing September 2022 trial date. *Id.* at 3–4.

Although Petitioner speculates that the dates in the original trial schedule no longer apply, Petitioner has not produced evidence of an updated scheduling order in the parallel litigation that would affect the trial date. However, the fact that some dates in the district court's existing scheduling order have not been met renders uncertain the remaining dates.

For purposes of this factor, Petitioner has shown some uncertainty as to whether the parallel litigation will go to trial before the final written decision is due in this proceeding. In view of the foregoing, we determine that this factor is neutral.

Factor 3: investment in the parallel proceeding by the court and the parties

Petitioner argues that this factor weighs towards institution because significant district court work remains and cannot commence until at least February 2022. Reply 4. Petitioner represents that the parties “have taken no fact depositions and other significant fact discovery remains, as does other resource-intensive work, such as expert reports and depositions, and dispositive motions.” *Id.* (citing Ex. 2008 at 1). Petitioner further argues that it moved with reasonable diligence because the petition was filed three months after final infringement contentions were served, and less than a week after mediation between the parties. *Id.* at 5. Petitioner contends that such delay was due to a hope that the parties could resolve their differences through a mediated settlement. *Id.*

Patent Owner counters that Petitioner waited until the final day of its one year period to file its petition, and that Petitioner “offered no justification for this dilatory tactic[.]” Prelim. Resp. 11. Patent Owner further argues that substantial work, including for example “exchange[of]

infringement, invalidity, and damages contentions” and “claim construction,” has been done by the parties and the court, which has a “deep knowledge of the facts and technology,” and that this factor thus weighs in favor or denying institution. *Id.* at 6–10.

Based on the present record, we are persuaded by Petitioner’s showing that the district court and the parties have not invested substantially in the merits of the invalidity positions. The district court addresses three terms in its claim construction order. Ex. 2001, 19–26. Petitioner indicates that the Petition adopts Patent Owner’s proposed litigation constructions (Ex. 1006) for those terms, and that because the grounds set forth in the Petition meet those constructions, no further construction is required. Pet. 11–12. Petitioner further addresses tentative constructions considered by the district court in the Petition. *See, e.g., id.* at 21–22.

There is no indication in the record that the parties have completed significant discovery on the merits. Although the parties and the court have invested some effort, a significant portion of work still remains to be done in the district court proceeding—e.g., the completion of fact and expert discovery and dispositive motions. We find instructive the similar investment in *Sand Revolution II*, which involved a *Markman* order and recognized that fact discovery, expert reports, and substantive motion practice remained. *Sand Revolution II, LLC v. Cont’l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 10–11 (PTAB June 16, 2020) (informative) (“*Sand Revolution II*”). *Sand Revolution II* weighed factor 3 “marginally, if at all, in favor of denial.” *Id.* at 11.

Moreover, Petitioner’s delay is mitigated by its prompt filing after a mediation session between the parties. Although Patent Owner faults the

Petitioner because Petitioner did not incur IPR costs until after the mediation session, Patent Owner does not explain why it would not be reasonable to delay seeking action until mediation was unsuccessful. Patent Owner does not explain or allege why such mediation might not reasonably have some probability of resolving the issues such that filing *inter partes* review would have been unnecessary. We find it reasonable for Petitioner to have waited until after the mediation to file its Petition.

Therefore, weighing the facts in this particular case, including the time invested by the parties and the district court in the parallel litigation, the extent to which the investment in the district court proceeding relates to issues of patent validity, and the timing of the filing of the Petition, we find that this factor weighs marginally, if at all, in favor of exercising discretion to deny institution.

Factor 4: overlap between issues raised in the petition and in the parallel proceeding

Patent Owner argues that “Siemens’s petition asserts *virtually identical* claims, arguments, and evidence as those presented to the district court. . . . Siemens’ [IPR] petition challenges the same claims of the ’655 patent, claims 1–24, as are at issue in the district court.” Prelim. Resp. 12. Patent Owner argues that both alleged bases for obviousness in the IPR petition rely on references that were asserted in the litigation. *Id.* at 12.

Petitioner provides a stipulation not to pursue any instituted IPR ground in district court. Reply 5 (citing Ex. 1017). The stipulation states, “Siemens stipulates that, should IPR be instituted in IPR2021-01212, -01213, or -01215, then Siemens will not pursue in the N.D. Cal. district court litigation any prior art invalidity defense that is the same as a ground

of unpatentability in any instituted IPR.” Ex. 1017, 1. Petitioner argues that this moots overlap and weights at least slightly against discretionary denial in factor 4, citing *Sand Revolution II*, Paper 24 at 12. Reply 5.

In response to the stipulation, Patent Owner argues that Petitioner’s stipulation fails to cure any potential overlap and that Petitioner is free to pursue arguments using the same prior art, provided that the art is combined in different ways. Sur-Reply 5. Patent Owner argues that this stipulation at best “marginally” mitigates overlap of issues, citing *Google LLC v. Ikorongo Tech. LLC*, IPR2021-00204, Paper 13 at 10–12 (PTAB June 7, 2021). *Id.*

We are persuaded by Petitioner’s arguments that the overlap in proceedings is limited as a result of the stipulation. Notably, Petitioner’s stipulation is similar to the stipulation provided in *Sand Revolution*. *Sand Revolution II*, Paper 24, at 12 n.5. In *Sand Revolution*, the Petitioner stipulated “only that it will not pursue, in district court, the ‘same grounds’ presented in the Petition.” *Id.* Consistent with *Sand Revolution*, we find Petitioner’s stipulation mitigates to some degree the concerns of duplicative efforts between district court and the Board, as well as concerns of potentially conflicting decisions. *See id.* at 11–12. Thus, we find that this factor weighs somewhat against exercising discretion to deny institution.

Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

It is undisputed that Petitioner is a defendant in the parallel litigation. Patent Owner argues that this favors denying institution. Prelim. Resp. 13.

As the Board explained in *Fintiv*, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact *against exercising discretion* to deny institution under *NHK*.” *Fintiv*,

Paper 11 at 13–14 (emphasis added). The Board determined in *Sand Revolution* that “[a]lthough it is far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same, or where a district court is scheduled to go to trial before the Board’s final decision would be due in a related *inter partes* review, this factor weighs in favor of discretionary denial.” *Sand Revolution*, Paper 24 at 12–13. The Board has also held that “[b]ecause the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.” *Fintiv II*, Paper 15 at 15. Here, although it is undisputed that Petitioner is a defendant in the parallel litigation, it is unclear whether the parallel litigation will go to trial before the final written decision is due in this proceeding. Therefore, we find that factor 5 is neutral.

Factor 6: other circumstances that impact the Board’s exercise of discretion, including the merits.

The final *Fintiv* factor is a catch-all that takes into account any other relevant circumstances. The decision whether to exercise discretion to deny institution is based on “a balanced assessment of all relevant circumstances in the case, including the merits.” Patent Trial and Appeal Board Consolidated Trial Practice Guide (“CTPG”) 58 (Nov. 19), *available at* <https://www.uspto.gov/TrialPracticeGuideConsolidated>. “For example, if the merits of a ground raised in the petition seem particularly strong on the preliminary record, . . . the institution of a trial may serve the interest of overall system efficiency and integrity because it allows the proceeding to continue in the event that the parallel proceeding settles or fails to resolve the patentability question presented in the PTAB proceeding.” *Fintiv*, Paper

11 at 14–15. A full merits analysis is not necessary as part of deciding whether to exercise discretion not to institute, but rather the parties may point out, as part of the factor-based analysis, particular “strengths or weaknesses” to aid the Board in deciding whether the merits tip the balance one way or another. *Id.* at 15–16.

Petitioner argues that the lack of any substantive merits-based argument by Patent Owner confirms the strength of the Petition, thus favoring institution. Reply 5. Patent Owner further argues that the petition fails to address in full the district court’s claim constructions. Prelim. Resp. 15. Patent Owner argues that factor six therefore favors denial.

Patent Owner’s arguments are unavailing as to this factor. At this preliminary stage of this proceeding Patent Owner proffers no substantive arguments to rebut Petitioner’s asserted ground of unpatentability. We have reviewed Petitioner’s unpatentability arguments and supporting evidence. As discussed below, on this record, we determine that Petitioner has demonstrated sufficiently for purposes of this Decision that the challenged claims of the ’655 patent are unpatentable. We find this factor is neutral.

Conclusion on Discretionary Denial Under § 314(a)

As noted in *Fintiv*, we consider the above six factors when taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. In weighing the totality of the evidence, we decide not to exercise discretion under § 314(a) to deny institution.

B. Legal Standards

1. § 102

A claim is unpatentable under 35 U.S.C. § 102 “if each and every [claim] limitation is found either expressly or inherently in a single prior art reference.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1273 (Fed. Cir. 2017) (citation omitted). “A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present.” *Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003) (citing *Rosco, Inc. v. Mirror Lite, Co.*, 304 F.3d 1373, 1380 (Fed. Cir. 2002)). We analyze the asserted ground based on anticipation with these principles in mind.

2. § 103(a)

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).² *Graham v. John Deere Co.*, 383 U.S. 1,

² Patent Owner does not identify any secondary considerations to be considered. Accordingly, we do not consider this aspect of the obviousness analysis at this stage of the proceeding.

17–18 (1966). We analyze the asserted grounds based on obviousness with these principles in mind.

C. Level of Skill in the Art

Petitioner offers an assessment as to the level of skill in the art as of the time the '655 patent was filed. Pet. 9. For purposes of this proceeding, Petitioner and Petitioner's declarant "adopt the [following] definition for the a person of ordinary skill in the art": "a Bachelor of Science degree in Electrical Engineering or Computer Engineering, and has either received academic credits for an ASIC design course or completed at least one year of work experience in the VLSI design, electronic design automation for VLSI, or ASIC design fields." *Id.* at 9–10; Ex. 1003 ¶ 78 (Robins Declaration). Petitioner notes that this assessment was presented to the district court by Patent Owner, but that Petitioner has also argued for a higher level of skill in the art. *Id.* at 10. Patent Owner has not provided an assessment of the level of ordinary skill in the art. *See generally* Prelim. Resp. To the extent necessary, and for purposes of this Decision, we accept the assessment offered by Petitioner as it is supported by the Robins Declaration and is consistent with the '655 patent and the asserted prior art.

D. Claim Construction

Petitioner asserts that in litigation, the parties have agreed on the construction of two terms. Pet. 10. First, that the term "circuit objects" should be construed as particular object[s] in the circuit design such as gate[s], net[s], or pin[s]." *Id.* at 11 (citing Ex. 1004, 2). Second, that the term "timing slack values" should be construed as "the differences between the required time and the arriv[al] time of data signals at timing endpoints." *Id.*

Petitioner further adopts Patent Owner’s litigation constructions for the terms and phrases listed below.

The term “scenario image” is proposed to be construed as “information required to detect and/or fix design requirement violations in a circuit design in a particular scenario.” *Id.* at 12. Petitioner notes that the district court has tentatively construed the term in the same manner. *Id.*

The phrase “a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios” is proposed to be construed as a database containing circuit information for multiple scenarios. *Id.* (citing Ex. 1005, 14–15). Petitioner notes that the district court has tentatively construed the phrase as “a database **separate from the scenario image**, containing circuit information for multiple scenarios.” *Id.* (citing Ex. 1006, 3).

Petitioner proposes that all remaining terms and phrases be given their plain and ordinary meaning. *Id.* at 10, 13.

In its Preliminary Response, Patent Owner does not propose any explicit claim constructions. *See generally* Prelim. Resp.

We apply the same standard that is used to construe a patent claim in a civil action under 35 U.S.C. § 282(b), and construe each claim in accordance with the ordinary and customary meaning of such claim, as understood by one of ordinary skill in the art in the context of the patent, and the prosecution history pertaining to the patent, as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). “[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” *Nidec Motor Corp. v.*

Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). For the purposes of institution, we do not expressly construe any claim terms beyond the extent necessary in our discussion of the parties' arguments below, and we consider multiple constructions where presented by Petitioner.

E. Asserted Anticipation of Claims by Yoshimura

Petitioner contends that claims 1–3, 8, 11–13, 18, and 21–22 of the '655 patent are unpatentable as anticipated by Yoshimura. Pet. 14. Petitioner relies upon the Robins Declaration to support its positions. Ex. 1003. At this stage of the proceeding, we are persuaded by Petitioner's explanations and supporting evidence. We begin our analysis with a brief overview of Yoshimura.

1. Overview of Yoshimura

Yoshimura relates to timing analysis for a semiconductor integrated circuit. Ex. 1007, 1:14–15. The layout of the circuit is corrected based on the timing analysis, which takes into account gate delay and net delay. *Id.* at 1:16–19. Gate delay and net delay vary with the ambient temperature, and the gate delay also varies with the power supply voltage. *Id.* at 1:21–24. Specific combinations of temperature and voltage conditions are referred to as corner conditions. *Id.* at 1:35–38. Yoshimura is concerned with reducing timing analysis time through completing timing error elimination and layout correction within a short period of time. *Id.* at 4:29–32.

2. *Analysis*

Petitioner provides a detailed analysis, supported by testimony, to show that Yoshimura discloses the limitations in the claims. Pet. 27–47. We begin with claim 1.

a) *Claim 1*

[1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

To the extent that the preamble is limiting, Petitioner points to Yoshimura’s description of fixing timing errors, which Petitioner describes as a type of design requirement violation. Pet. 18. Petitioner points to Yoshimura’s description of an error correction device 16 that searches for a layout that does not cause a timing error under various corner conditions, and that performs layout correction to satisfy the hold margin and slack time under those conditions. *Id.* (citing Ex. 1007, 7:18–20, 8:24–26). Petitioner characterizes Yoshimura’s corner conditions as the claimed scenarios, noting that both the conditions and the scenarios represent conditions of temperature, voltage, and process. *Id.* at 20–21 (citing Ex. 1007, Figs. 4–5, 5:67–6:9; Ex. 1001, 1:35–37, 1:48–50). Petitioner further points to Yoshimura’s description of the error correction device including the addition of a buffer circuit and/or the replacement of buffer circuits with inverter circuits. *Id.* at 19 (citing Ex. 1007, Figs. 7A, 7B, 8B).

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;

Petitioner points to Yoshimura’s receipt, by the error correction device 16, of datasets in the form of a timing list 12 and a slack file 13. *Id.* (citing Yoshimura Figs. 4, 5, 5:67–6:9). Petitioner alleges that Yoshimura’s timing list and slack file constitute the claimed “scenario image” because

they include the same type parameter values as in the '655 patent. *Id.* at 19–20. Petitioner notes that Yoshimura's parameter values include delay characteristics and slack time, just as the '655 patent stores slack and delay values. *Id.* at 20 (citing Ex. 1001, Fig. 5, 2:16–17, 7:20–24, 5:62–66, 6:35–45; Ex. 1003; Ex. 1007, 5:20–23).

Petitioner alleges that Yoshimura's timing list and slack file also meet the agreed-upon construction of “information required to detect and/or fix design requirement violations in a circuit design in a particular scenario.” *Id.* at 15, 21–22. Petitioner points to the timing list and slack file as being required in steps S4–S8 to detect and fix timing errors; i.e., design requirement violations. *Id.* at 22 (citing Ex. 1007, Fig. 5, 6:61–7:67, 6:58–60, 7:18–21). Petitioner highlights Yoshimura's statement, “[t]he automatic EC device 16 performs steps S4 to S8 based on the timing list 12, the slack file 13, and” *Id.* at 22 (citing Ex. 1007, 6:58–60).

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and

Petitioner alleges that Yoshimura discloses this element under the district court's construction, “a database separate from the scenario image, containing circuit information for multiple scenarios.” *Id.* at 23. Petitioner notes that the Patent Owner's construction, which Petitioner adopts for purposes of this proceeding, is broader. *Id.* at 24 n.5. Petitioner points to Yoshimura's libraries 11a,b as databases storing delay information (net delay and gate delay) for two corners. *Id.* at 24 (citing Ex. 1007, Fig. 4, 5:67–6:9, 3:5–8; Ex. 1003 ¶¶ 112–113). Petitioner alleges that Yoshimura's delay information is circuit information because it provides signal delay

information for specific parts (gates and nets) of the circuit. *Id.* Petitioner further alleges that the libraries 11a,b are databases because both a library and a database are just a large collection of data. *Id.* (citing a definition of “database”). Petitioner further alleges that Yoshimura discloses a subset of parameter values as claimed, because Yoshimura’s libraries contain delay information but not slack values. *Id.* at 25 (citing Ex. 1007, Fig. 4, 5:67–6:9, 3:5–8, 5:20–21). Petitioner further alleges that Yoshimura discloses receiving the multi-scenario ECO database because Yoshimura’s EC device 16 receives the libraries 11 a,b. *Id.* at 26 (citing Ex. 1007, 6:10–16, Fig. 4; Ex. 1003 ¶ 119).

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

Petitioner refers to the explanation for claim element 1.1. *Id.* Petitioner further points to Yoshimura’s examples of possible ECOs in which a buffer circuit is either added or replaced with a different circuit. *Id.* (citing Ex. 1007, Figs. 7A, 7B, 8B, 7:42–67, 8:8–12). Relying on its declarant, Petitioner argues that Yoshimura’s description of its “automatic engineering change device,” its “store,” and the fact that the name of its field being “Electronic Design **Automation**,” shows that Yoshimura inherently uses one or more processors as claimed. *Id.* at 27–28 (citing Ex. 1007, 5:27–32, 6:17–30, 6:58–60, 7:18–27; Ex. 1003 ¶¶ 125–127).

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Petitioner points to Yoshimura’s description of estimating parameter values in the form of hold margins in a scenario based on parameter values

of gate delay and net delay stored in its libraries; i.e., its multi-scenario ECO database. *Id.* at 28–29 (citing Ex. 1007, 7:4–8:23, Fig. 6, step S5).

Petitioner points to Yoshimura’s description for estimating parameter values based on parameter values stored in the scenario image, in the form of slack times and delay characteristics in the timing list and slack file. *Id.* at 29. Petitioner highlights step S5, in which the hold margin parameter values are estimated, as illustrating that the estimating is based on the scenario image because “these parameter values from the scenario image are needed to figure out which circuit paths to analyze in step S5.” *Id.* at 29–30 (citing Ex. 1003 ¶ 137).

- b) *Claim 2. The method of claim 1, wherein each scenario in the multiple scenarios is associated with one or more of: a process corner, an operating condition, or an operating mode.*

Petitioner alleges Yoshimura discloses at least one of the alternative options, in the form of a corner that includes a process corner, in the form of a fast or slow process, and multiple operating conditions, in the form of temperature and voltage. *Id.* at 30 (citing Ex. 1007 Figs. 4–5, 5:67–6:9).

- c) *Claim 3. The method of claim 1, wherein the parameter values include timing slack values at one or more pins in the circuit design.*

Petitioner points to Yoshimura’s slack file 13 as including slack values in the form of slack times for the cells of the circuit. *Id.* at 31 (citing Ex. 1007, 5:20–23). Relying on its expert, Petitioner argues that the slack values for the cells of the circuit are the same as the slack values at one or more pins of the cell, because “slack values for the cells of the circuit are really just the slack values at one or more pins in the cells since the slack value of a cell is the difference between the arrival time of the data input

signal on one of the input pins of the cell and the arrival time of the clock signal at the other input pin of the cell.” *Id.* (citing Ex. 1003 ¶ 146).

a) *Claim 8. The method of claim 1, wherein the one or more design requirement violations include a hold timing violation.*

As discussed with respect to claim 1, Petitioner points to Yoshimura’s timing errors, corresponding to the claimed design requirement violations, as including a negative hold margin, corresponding to the claimed hold timing violation. *Id.* at 35. Petitioner further notes that Yoshimura describes implementing an ECO to correct the timing requirement violation, in the form of adding a buffer circuit into the data path when the hold margin is insufficient. *Id.* (citing Ex. 1007, 6:17–8:27, 7:56–67, Fig. 7B).

b) *Claims 11–13, 18 and 21–22.*

Petitioner asserts that claims 11 and 21 are nearly identical to claim 1, and are disclosed by Yoshimura for the same reasons as asserted for claim 1. Petitioner further asserts that claims 12, 13, 18, and 22 recite language nearly identical to claims 2, 3, 8, and 2, respectively. *Id.* at 37–38.

c) *Determination*

Patent Owner makes no arguments specific to claims 1–3, 8, 11–13, 18, 21, and 22. *See generally* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

At this stage of the proceeding, for purposes of institution, Petitioner has provided sufficient explanation, supported by evidence, of how each limitation of these claims is disclosed by Yoshimura. In view of the foregoing, we are persuaded that Petitioner is reasonably likely to prevail on

its assertion that claims 1–3, 8, 11–13, 18, 21, and 22 would have been anticipated by Yoshimura.

Petitioner additionally argues that to the extent Patent Owner argues that claims 1–3, 8, 11–13, 18, 21, and 22 are not anticipated by Yoshimura, they are obvious over Yoshimura. Pet. 14. However, Patent Owner has not made such an argument at this point of the proceedings. Furthermore, we have found Petitioner’s anticipation arguments persuasive. Accordingly, at this stage of the proceeding, we do not discuss Petitioner’s alternative obviousness ground over Yoshimura for those claims.

F. Asserted Obviousness over Yoshimura

Petitioner contends that claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24 of the ’655 patent are unpatentable as obvious under 35 U.S.C. § 103(a) over Yoshimura. Petitioner claims that the limitations recited in these claims would have been obvious to one having ordinary skill in the art, relying upon the Robins Declaration to support its positions. Pet. 31–38, Ex. 1003.

Petitioner relies, at least in part, on teachings of prior art not applied in this ground of unpatentability, including on teachings of Scheffer. *See* Pet. 37 (relying on Scheffer to corroborate the need to ensure compliance with electrical design rules). Because a separate ground addressing these claims explicitly relies on Scheffer and Yoshimura (*infra* at II(G)), and we determine that ground to be persuasive as to the obviousness of these claims for purposes of institution, we need not discuss this ground based on Yoshimura and Petitioner’s declarant’s assertions as to what was well known in the art.

G. Asserted Obviousness over Yoshimura and Scheffer

Petitioner contends that claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24

of the '655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over Yoshimura and Scheffer. Petitioner relies upon the Robins Declaration to support its positions. Ex. 1003. At this stage of the proceeding, we are persuaded by Petitioner's explanations and supporting evidence. We begin our analysis with a brief overview of Scheffer.

1. *Overview of Scheffer*

Scheffer is a handbook on Electronic Design Automation ("EDA"). Ex. 1008, 8. Chapters were contributed by experts from across the disciplines involved in EDA. *Id.* at 9. Scheffer explains that the chapters in the handbook "represent a snapshot of the state of the art, written in 2004–2005." *Id.* Scheffer's chapters include chapters on noise considerations in digital integrated circuits and layout analysis. *Id.* at 20.

2. *Analysis*

Petitioner provides a detailed analysis supported by testimony about how the references teach the limitations in the claims.

a) *Claims 4–6, 14–16, and 23*

Claims 4–6 further limit the parameter values recited in claim 1. Claim 4 limits the parameter values to including capacitive load values at one or more pins. Claim 5 limits the parameter values to including transition time values at one or more pins. Claim 6 limits the parameter values to include leakage power values for gates. Petitioner asserts that none of these specific types of parameter values are disclosed by Yoshimura, but that each were taught by Scheffer for assessing integrated circuit operating behavior. Pet. 40–43.

With respect to claim 4, Petitioner points to Scheffer's description of capacitive load values at one or more gates in the circuit design, including at

the pins of the gates. *Id.* at 40 (citing Ex. 1008, 126; Ex. 1003 ¶ 179). Petitioner additionally points to Scheffer's characterization of capacitive load as critical for assessing gate delay and power budget violations. *Id.* (citing Ex. 1008, 126, 196). Petitioner further points to Scheffer's various means for estimating capacitive load values. *Id.* (citing Ex. 1008, 485–488, 493).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use capacitive load values as a parameter value in Yoshimura, because the capacitive load values at the pins affect the rate at which the pins' voltage can change, and would be needed to determine whether a timing or power requirement has been violated. *Id.* (citing Ex. 1003 ¶¶ 180–181). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including capacitive load values in Yoshimura's scenario image and/or multi-scenario ECO database, because Yoshimura's database already includes similar types of parameter values. *Id.* at 40–41 (citing Ex. 1003 ¶ 181).

With respect to claim 5, Petitioner points to Scheffer's description of transition time values at one or more pins in the circuit design. *Id.* at 41 (citing Ex. 1008, 48, 126–129; Ex. 1003 ¶ 184). Petitioner additionally points to Scheffer's characterization of transition times as important for assessing noise, timing, and gate delay. *Id.* (citing Ex. 1008, 126–129, 455–473; Ex. 1003, ¶ 185).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use transition time values as a parameter value in Yoshimura, because the transition times

at the pins affect the timing of the circuit, and would be needed to determine whether a timing requirement has been violated. *Id.* at 41–42 (citing Ex. 1003 ¶ 185). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including transition time values in Yoshimura’s scenario image and/or multi-scenario ECO database, because Yoshimura’s database already includes similar types of parameter values. *Id.* at 42 (citing Ex. 1003 ¶ 186).

With respect to claim 6, Petitioner points to Scheffer’s description of leakage power values as a parameter value for gates in circuit design. *Id.* (citing Ex. 1008, 35, 42, 196, 204). Petitioner additionally points to Scheffer’s characterization of leakage power values as being estimated based on logic count technology parameters, and voltage. *Id.* (citing Ex. 1008, 204).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use leakage power values as a parameter value in Yoshimura, because the leakage power values affect the total power budget of the circuit, and would be needed to determine whether a power budget requirement has been violated. *Id.* at 43 (citing Ex. 1003 ¶ 190). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including leakage power values in Yoshimura’s scenario image and/or multi-scenario ECO database, because Yoshimura’s database already includes similar types of parameter values. *Id.* (citing Ex. 1003 ¶ 191).

Petitioner asserts that claims 14–16 recite language nearly identical to claims 4–6, and that claim 23 collectively recites one or more of the types of

parameter values recited in claims 3–6. *Id.* at 47. Petitioner argues that claims 14–16 and 23 are obvious over Yoshimura in view of Scheffer for the same reasons advanced for claims 4–6. *Id.*

b) *Claims 7, 9, 10, 17, 19, 20, and 24*

Claims 7, 9, and 10 further recite specific types of design requirement violations that Petitioner admits are not explicitly disclosed by Yoshimura, but allegedly are taught by Scheffer. *Id.* at 43–47.

Claim 7 further recites, “wherein the one or more design requirement violations include a setup timing violation.” Petitioner relies upon Scheffer for teaching performing a timing analysis to ensure that setup timing requirements are not violated. *Id.* at 44 (citing Ex. 1008, 6–8; Ex. 1003 ¶ 194). Petitioner further points to Scheffer’s description of timing requirement violations as being fixed by resizing gates, buffering, or widening wires. *Id.* (citing Ex. 1008, 175, 214–216).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix setup timing violations, because such violations prevent a circuit from operating at the desired clock rate. *Id.* (citing Ex. 1003 ¶ 195). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing timing violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* (citing Ex. 1007, 6:17–8:27).

Claim 9 further recites, “wherein the one or more design requirement violations include an electrical design rule violation.” Petitioner relies upon

Scheffer for teaching performing a design rule analysis, in the form of noise analysis to ensure that noise requirements are not violated. *Id.* at 45 (citing Ex. 1008, 192, 196–197, 454–464). Petitioner further points to Scheffer’s description of setting a maximum allowable limit on the glitch peak. *Id.* (citing Ex. 1008, 211; Ex. 1003 ¶ 299). Petitioner additionally relies on Scheffer for teaching that it was well known in the art to fix electrical design rule violations by resizing gates, buffering large fan-out nets, and inserting repeaters. *Id.* (citing Ex. 1008, 211).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix electrical design rule violations, because such violations prevent a circuit from operating properly when deployed, and that excessive noise can compromise performance. *Id.* at 45–46 (citing Ex. 1003 ¶ 200). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing design rule violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* at 46 (citing Ex. 1007, 6:17–8:27).

Claim 10 further recites, “wherein the one or more design requirement violations include a power budget violation.” Petitioner relies upon Scheffer for teaching performing a power analysis to ensure that power budget requirements are not violated. *Id.* (citing Ex. 1008, 65, 191–196). Petitioner further relies on Scheffer for teaching that it was well known in the art to fix power budget violations by resizing gates. *Id.* (citing Ex. 1008, 211).

Petitioner alleges that a person having ordinary skill in the art at the

time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix power budget violations, because such violations prevent a circuit from operating properly when deployed, and that a circuit will not operate properly if it cannot support and/or meet certain power constraints. *Id.* at 47 (citing Ex. 1003 ¶ 205). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing power budget violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* (citing Ex. 1007, 6:17–8:27).

Petitioner asserts that claims 17 and 19–20 recite language nearly identical to claims 7 and 9–10, respectively, and that claim 24 collectively recites one or more of the types of design requirement violations recited in claims 7–10. *Id.* at 48. Petitioner argues that claims 17 and 19–20 are obvious over Yoshimura in view of Scheffer for the same reasons advanced for claims 7 and 9–10. *Id.*

c) *Determination*

Patent Owner makes no arguments specific to claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24. *See generally* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378.

At this stage of the proceeding, for purposes of institution, Petitioner has provided sufficient explanation, supported by evidence, of how each limitation of these claims is taught by the combination of Yoshimura and Scheffer. In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 4–7,

9, 10, 14–17, 19, 20, 23, and 24 would have been obvious over the combination of Yoshimura and Scheffer.

H. Asserted Obviousness over Srinivas

Petitioner contends that claims 1–24 of the '655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over Srinivas. Petitioner relies upon the Robins Declaration to support its positions. Ex. 1003. We begin our analysis with a brief overview of Srinivas.

1. Overview of Srinivas

Srinivas relates to computer-aided design of integrated circuits. Ex. 1010, 1:8–10. As the dimensions of circuits shrink, “many electrical properties that were previously second and third order effects have come to play a major role in determining circuit performance and power consumption.” *Id.* at 1:23–27. Such effects may be environmental (such as temperature), artifacts of manufacturing (such as material thickness), reliability (such as degradation), or operational (such as design constraints for different operating modes. *Id.* at 1:36–3:31. Srinivas seeks to “accommodate design variability in an efficient way so that performance can be analyzed and optimized over a large number of corners with a reasonable computational overhead.” *Id.* at 4:24–28. Srinivas describes an embodiment that incrementally updates timing graphs over all combinations of corner and mode, such that only the information that needs to be updated is re-computed. *Id.* at 9:35–40. Illustrating that embodiment is Figure 4, which, as annotated by Petitioner, is reproduced below.

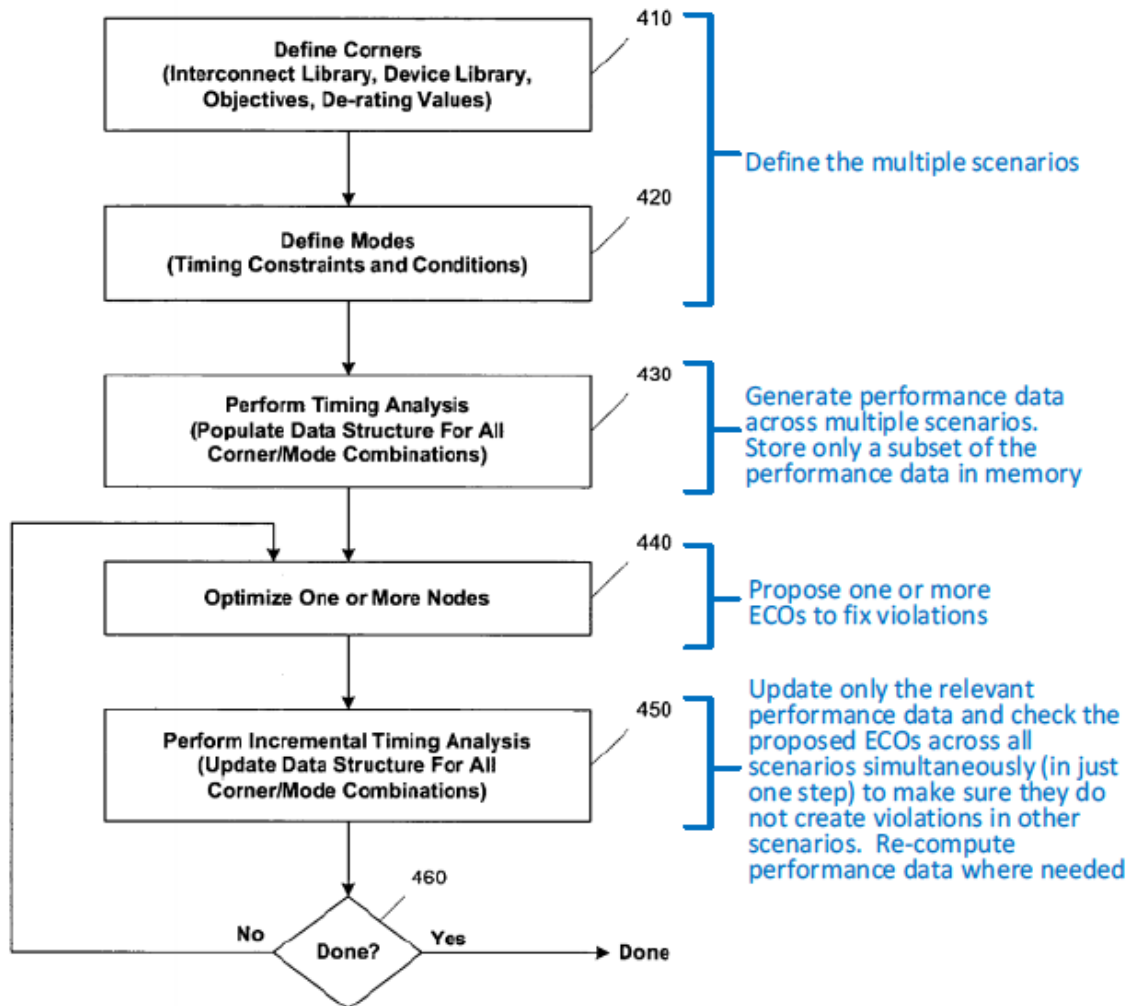


FIG. 4

Pet. 50. Figure 4 describes a process of defining corners (step 410), defining modes (step 420), performing timing analysis (step 430), optimizing one or more nodes (step 440), performing incremental timing analysis (step 450), and determining whether the process is done, or if the process should move to step 440. Petitioner annotates steps 410 through 450, characterizing steps 410 and 420 as "Define the multiple scenarios," step 430 as "Generate performance data across multiple scenarios. Store only a subset of the performance data in memory," step 440 as "Propose one or more ECOs to

fix violations,” and step 450 as “Update only the relevant performance data and check the proposed ECOs across all scenarios simultaneously (in just one step) to make sure they do not create violations in other scenarios. Re-compute performance data where needed.” *Id.*

2. *Analysis*

Petitioner provides a detailed analysis supported by its declarant’s testimony to show how Srinivas discloses the claimed limitations.

a) *Claim 1*

[1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

Petitioner points to Srinivas’ corners and modes as disclosing the claimed multiple scenarios. *Id.* at 51. Srinivas’ corners include “any combination of process, voltage and temperature (PVT), as well as other environmental, manufacturing or reliability factors.” *Id.* (citing Ex. 1010, 3:34–37). Petitioner asserts that Srinivas’ described modes and corners disclose the claimed multiple scenarios, which are described in the ‘655 patent as “the combination of ‘a particular process corner, a particular operating condition [(e.g., temperature, voltage)], and/or a particular operating mode.’” *Id.* (citing Ex. 1001, 1:35–37, 1:48–50).

With respect to fixing design requirements in a circuit, Petitioner points to Srinivas’ disclosure that “[o]nce a change is made to the circuit, the optimizer typically decides to accept the change based on improvement in the worst slack over all combinations of corner and mode.” *Id.* at 52 (citing Ex. 1010, 10:4–7).

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario

With respect to parameter values, Petitioner points to Srinivas' description of performance data that can include timing data, slew, and capacitance. *Id.* (citing Ex. 1010, 7:53–55, 8:4–6, 8:40–43). Petitioner asserts that these are the same type of data described as parameter values in the '655 patent; i.e., capacitance and slew. *Id.* at 52–53 (citing Ex. 1001, 5:61–64).

With respect to a scenario image, Petitioner points to Srinivas' circuit graph, which includes the aforementioned performance data, and can be stored in data structures such as matrices for each node of the circuit graph. *Id.* at 53 (citing Ex. 1010, Fig. 3, 8:4–53). Petitioner also points to Srinivas' Table 1 as an example matrix at a single node, containing three modes (“sleep,” “standby,” and “active”) and three corners (“setup/hold,” “noise,” and “setup”). *Id.* at 53–54 (citing Ex. 1010, Fig. 3, 8:15–30).

Petitioner alleges that these descriptions in Srinivas disclose claim limitation 1.2 under the agreed-to construction. *Id.* Petitioner also alleges that these descriptions would meet the tentative district court construction, also requiring the scenario image to contain information needed to detect and/or fix design requirement violations in a particular scenario, because the matrices store the kind and quantity of data needed to fix and identify design requirement violations. *Id.* at 54–56 (pointing to similar data used in the '655 patent to identify and fix violations).

With respect to the scenario image being “received” as claimed, Petitioner asserts that a person having ordinary skill in the art would have understood Srinivas to inherently disclose some form of memory that would

receive the circuit graph, based on the nature of Srinivas' data structures and timing analysis. *Id.* at 56.

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios

Petitioner points to Srinivas' circuit graph as including both the scenario image and the multi-scenario ECO database. *Id.* at 57. Petitioner alleges that Srinivas' circuit graph includes "at least enough information to identify and/or fix violations in one scenario (the scenario image) and also include circuit information for other scenarios (the multi-scenario ECO database)." *Id.* (citing Ex. 1010, 9:1–9).

Petitioner also addresses the district court's tentative construction that the "multi-scenario ECO database" should be interpreted to mean "a database separate from the scenario image, containing circuit information for multiple scenarios. *Id.* (citing Ex. 1006, 3). Relying on its declarant, Petitioner argues that, because the circuit graph contains sufficient information for both, one having ordinary skill in the art would have considered splitting data from the circuit graph into separate databases as a mere choice of design, well within the skill of the ordinary artisan. *Id.* (citing Ex. 1003 ¶ 239).

With respect to the "subset" of circuit objects, Petitioner asserts that Srinivas describes that the data structures may contain less than all parameter values, because some parameter values may be re-computed when performing timing analysis. *Id.* at 58 (citing Ex. 1010, 8:45–53).

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

With respect to an ECO, i.e., a “change order,” Petitioner points to Srinivas’ step 440 as making a change to the circuit, which may be accepted “based on improvement in the worst slack over all combinations of corner and mode.” *Id.* at 59 (citing Ex. 1010, 10:4–7). Petitioner characterizes the “worst slack” as a design requirement violation, fixed by the change to the circuit. *Id.*

With respect to a processor, Petitioner points to the process of Figure 4 as being executed by processor 510. *Id.* (citing Ex. 1010, 10:32–34).

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Petitioner points to Srinivas’ re-computing performance data for nodes in at least some of the combinations stored in the circuit graph. *Id.* at 60. As discussed for earlier limitations in claim 1, Petitioner characterizes Srinivas’ performance data as the claimed “parameter values,” nodes as the claimed “circuit objects,” and the circuit graph as making obvious the separately claimed “scenario image” and “multi-scenario ECO database.” Petitioner asserts that the re-computing is based on at least some data in the stored parameter values because some of the parameter values for at least some of the nodes can be omitted. *Id.* (citing Ex. 1010, 8:44–9:9, 9:56–10:3).

b) *Determination for Claim 1*

At this stage of the proceeding, for purposes of institution, Petitioner

has provided an explanation, supported by evidence, of how each limitation of claim 1 is taught or suggested by Srinivas. In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claim 1 would have been obvious in view of Srinivas.

c) *Claims 11 and 21*

Petitioner asserts that claims 12 and 21 are nearly identical in substance to method claim 1, but claim a device and system, respectively. Pet. 68. Petitioner asserts that these claims are obvious over Srinivas for the same reasons as explained for claim 1. In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 11 and 21 would have been obvious in view of Srinivas.

d) *Claims 2, 12, and 22 (“wherein each scenario in the multiple scenarios is associated with one or more of: a process corner, an operating condition, or an operating mode”)*

Petitioner points to its explanation, for elements 1.1 and 1.2, that Srinivas teaches a scenario in the form of a corner and a mode, including an operating condition such as temperature or voltage, a process corner in the form of a process, and an operating mode. *Id.* at 61. Petitioner asserts that Srinivas describes each of the “one or more” limitations set forth in claims 2, 12, and 22. *Id.* at 61, 68.

In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 2, 12, and 22 would have been obvious in view of Srinivas.

e) *Claims 3–6, 13–16, and 23*

Claims 3–6 further limit the parameter values recited in claim 1.

Claims 3 and 13 limit the parameter values to include timing slack values at one or more pins in the circuit design. Claims 4 and 14 limit the parameter values to include capacitive load values at one or more pins. Claims 5 and 15 limit the parameter values to including transition time values at one or more pins. Claims 6 and 16 limit the parameter values to include leakage power values for gates. Claim 23 recites “one or more” of the parameter values set forth in claims 3–6. Ex. 1001, 12:4–12.

(1) Claims 3, 13, 23

With respect to timing slack values, Petitioner asserts that Srinivas must teach calculating timing slack values and including those values in a scenario image or multi-scenario ECO database because Srinivas determines a change order based on the worst negative slack. *Id.* at 61–62 (citing Ex. 1010, 9:26–27). In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 3, 13, and 23 would have been obvious in view of Srinivas.

(2) Claims 4, 14, 23

With respect to capacitive load values, Petitioner asserts that Srinivas teaches the use of capacitance in its circuit graph. *Id.* at 62. Petitioner points to Srinivas’ description of the effective input pin capacitance being determined based on capacitance and the slew. *Id.* at 62–63 (citing Ex. 1010, 2:1–16; Ex. 1003 ¶ 260). Petitioner asserts that these descriptions illustrate that Srinivas’ capacitance is inherently the capacitive load value at one or more pins. *Id.* at 63 (citing Ex. 1003 ¶ 260). In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 4, 14, and 23 would have been obvious in view of Srinivas. Thus, we do not discuss Petitioner’s

alternate argument based on other background references (*id.*).

(3) *Claims 5, 15*

With respect to “transition time values,” Petitioner asserts that Srinivas’ disclosure of slew as a parameter value indicates that transition time can be directly inferred from the slew, because slew measures the rate of change of voltage at a particular pin. *Id.* (citing Ex. 1010, 8:40–42; Ex. 1003, ¶ 264). Robins explains, “‘slew’ measures the rate of change in voltage over time, and transition time is the amount of time it takes for the voltage to change by a predetermined amount.” Ex. 1003 ¶ 264.

However, claims 5 and 15 explicitly require “transition time values,” not values from which transition time may be inferred. Although declarant Robins’ testimony is accepted to show that transition time may be inferred from slew value, Petitioner has not explained why one having ordinary skill in the art would use transition time rather than slew as the claimed parameter value. Consequently, Petitioner has not shown, on the record before us, that Srinivas makes obvious the use of transition time values as recited in claims 5 and 15.

Petitioner also argues that it would have been obvious to use transition time values based on additional references, such as Scheffer, illustrating that it was well known in the art to use transition time as a parameter value.

Pet. 64. Petitioner does not, however, base its argument on a combination of Srinivas and Scheffer, but instead on Srinivas alone.³ However, Petitioner’s

³ In a separate ground, Petitioner argues that other claims are obvious over the combined teachings of Srinivas and Scheffer, but not claims 5 or 15. *Id.* at 69.

obviousness argument appears to rely on the explicit teachings of Scheffer, particularly for its rationale to modify Srinivas, rather than explaining how Scheffer provides a showing of knowledge generally available in the art that would, with the teachings of Srinivas, make obvious the claimed limitations. *Id.* (citing Ex. 1008 48, 126–129). Accordingly, at this point in the proceedings, Petitioner has not sufficiently explained this ground such that there is a reasonable likelihood of prevailing on its assertions that claims 5 and 15 would have been obvious in view of Srinivas, even considering the evidence of Scheffer and the Robins declaration as to the pertinent knowledge in the art.

(4) *Claims 6, 16*

Petitioner relies, at least in part, on teachings of prior art not applied in this ground of unpatentability, including on teachings of Scheffer. *See* Pet. 65 (relying on Scheffer to provide motivation for using leakage power values as one of the parameter values). Because a separate ground explicitly relies on Scheffer and Srinivas (*infra* at II(I)), and we determine that ground to be persuasive as to the obviousness of these claims for purposes of institution, we do not here discuss this ground based on Srinivas in view of the evidence as to what was well known in the art provided by Scheffer and declarant Robins.

f) *Claims 7, 8, 17, 18, and 24*

Claims 7 and 17 further recite, “wherein the one or more design requirement violations include a setup timing violation.” Claims 8 and 18 further recite, “wherein the one or more design requirement violations include a hold timing violation.” Claim 24 recites, “wherein the one or more design requirement violations include one or more of: a setup timing

violation, a hold timing violation,” and other violations as recited in claims 9 and 10.

Petitioner asserts that Srinivas inherently discloses hold timing and setup timing violations. Pet. 66. Petitioner points to Srinivas’ teaching of performing setup and hold analyses, and disclosing setup and hold objectives. *Id.* at 66, 68–69 (citing Ex. 1010, 3:35–42, 4:31–33, 8:15–30). Relying on its declarant, Petitioner argues that sole purpose of including those objectives, and performing those analyses, is to detect and/or fix setup and hold timing violations. *Id.* (citing Ex. 1003 ¶ 274). In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 7, 8, 17, 18, and 24 would have been obvious in view of Srinivas.

g) *Claims 9, 10, 19, and 20*

Claims 9 and 19 further recite, “wherein the one or more design requirement violations include an electrical design rule violation.” Claims 10 and 20 further recite, “wherein the one or more design requirement violations include a power budget violation.”

Petitioner relies, at least in part, on teachings of prior art not applied in this ground of unpatentability, including on teachings of Scheffer. *See* Pet. 67 (relying on Scheffer to teach that it was well known to assess the viability of a circuit design using those criteria). Because a separate ground explicitly relies on Scheffer and Srinivas, and we determine that ground to be persuasive as to the obviousness of these claims for purposes of institution (*infra* at II(I)), we do not here discuss this ground based on Srinivas in view of the evidence as to what was well known in the art provided by Scheffer and declarant Robins.

h) *Summary*

Patent Owner makes no arguments specific to claims 1–24. *See generally* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. In view of the foregoing, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertions that claims 1–4, 7, 8, 11–14, 17, 18, and 21–24 would have been obvious in view of Srinivas, are not so persuaded for claims 5 and 15, and do not discuss Petitioner’s assertions concerning claims 6, 9, 10, 16, 19, and 20.

I. Asserted Obviousness over Srinivas and Scheffer

Petitioner contends that claims 6, 9, 10, 16, 19, 20, 23, and 24 of the ’655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the combination of Srinivas and Scheffer. Petitioner also relies upon the Robins Declaration to support its positions. Ex. 1003. At this stage of the proceeding, we are persuaded by Petitioner’s explanations and supporting evidence.

1. Analysis

Petitioner provides a detailed analysis, supported by testimony, to explain how the references teach the limitations in the claims. We have addressed the teachings of Scheffer for claims 6, 9, 10, 16, 19, 20, 23, and 24 in section II(G)(2), *supra*, and found Scheffer to provide teachings of the limitations of those claims.

Petitioner relies on the reasons provided in section II(G)(2) for its rationale for combining the teachings of Scheffer with those of Srinivas and how such would be achieved with a reasonable expectation of success. Pet. 69–70. Based on such reasons as applied to the teachings of Srinivas, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on

its assertions that claims 6, 9, 10, 16, 19, 20, 23, and 24 would have been obvious in view of Srinivas and Scheffer.

III. CONCLUSION

Taking into account the Preliminary Response, we conclude that the information presented in the Petition demonstrates that there is a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–24 of the '655 patent as unpatentable. Given this determination, we institute trial on all challenged claims and all grounds raised in the Petition. *See SAS Inst.*, 138 S. Ct. at 1359–60; CTPG 64 (“The Board will not institute on fewer than all claims or all challenges in a petition.”). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any challenged claim.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted based on all claims and all grounds raised in the Petition, which follow:

Claims 1–24 under 35 U.S.C. §§ 102, 103(a) over Yoshimura;

Claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24 under 35 U.S.C. § 103(a) over Yoshimura and Scheffer;

Claims 1–24 under 35 U.S.C. § 103(a) over Srinivas;

Claims 6, 9, 10, 16, 19, 20, 23, and 24 under 35 U.S.C. § 103(a) over Srinivas and Scheffer; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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