

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIEMENS INDUSTRY SOFTWARE INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

IPR2021-01215
Patent 8,407,655 B2

Before KEVIN F. TURNER, SCOTT C. MOORE, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. BACKGROUND

A. Background and Summary

Siemens Industry Software Inc. (“Petitioner”) filed a Petition for *inter partes* review (“IPR”) of claims 1–24 of U.S. Patent No. 8,407,655 B2 (Ex. 1001, “the ’655 patent”). Paper 2 (“Pet.”). Patent Owner, Synopsys, Inc., (“Patent Owner”), filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). Pursuant to § 314, we instituted an *inter partes* review as to claims 1–24 of the ’655 patent on all grounds raised in the Petition. Paper 12 (“Inst. Dec.”).

During the course of trial, Patent Owner filed a Response to the Petition. Paper 19 (“Resp.”). Petitioner filed a Reply to the Response. Paper 22 (“Reply”). Patent Owner filed a Sur-reply to Petitioner’s Reply. Paper 30 (“Sur-reply”). An oral argument was held on October 18, 2022, and a transcript of the oral argument is included in the record. Paper 33 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–24 of the ’655 patent. For the reasons we identify below, we determine that Petitioner *has shown* based on a preponderance of evidence that claims 1–5, 7, 8, 11–15, 17, 18, and 21–24 are unpatentable; and Petitioner *has not shown* based on a preponderance of evidence that claims 6, 9, 10, 16, 19, and 20 are unpatentable.

B. Real Party in Interest

Petitioner identifies itself, Siemens AG, and Siemens Corporation, as real parties in interest to this IPR petition. Pet. viii. Patent Owner identifies itself as the real party in interest. Paper 8 (first unpaginated page).

C. Related Matters

The parties indicate that the '655 patent is involved in a patent infringement lawsuit brought by Patent Owner in the Northern District of California, *Synopsys, Inc. v. Siemens Industry Software Inc.*, Case No. 3:20-cv-04151-WHO. Pet. viii; Paper 8 (first unpaginated page). Patent Owner indicates that two additional patents (U.S. Patent Number 7,546,567 and U.S. Patent Number 8,234,614) are at issue in the above-listed proceedings, and are the subject of *inter partes* review proceedings IPR2021-01212 and IPR2021-01213. Paper 8 (first unpaginated page).

D. The '655 Patent

The '655 patent (Ex. 1001) generally relates to integrated circuit design; in particular, determining changes to the design responsive to indications that the current circuit design does not comply with the design requirements. Ex. 1001, 1:19–21. Design requirement violations may include violations of setup timing, hold timing, electrical design rules, and power budgets. *Id.* at 2:16–20. The changes to the design, referred to as engineering change orders (“ECO”s), may in turn result in new violations of the design requirements. *Id.* at 1:27–28. Furthermore, violations may occur under certain combinations of operating conditions, referred to as a “scenario.” *Id.* at 1:51–54. Once a design is violation-free, then the circuit design can be readied for manufacturing. *Id.* at 1:28–30.

Determining an ECO to fix one or more violations can involve estimating parameter values for one or more components. *Id.* at 2:6–10.

The parameter values can include:

- (1) timing slack values at one or more pins in the circuit design,
- (2) capacitive load values at one or more pins in the circuit design,
- (3) transition time values at one or more pins in the

circuit design, and (4) leakage power values for gates in the circuit design.

Id. at 2:16–20.

E. Challenged Claims

Petitioner challenges claims 1–24 of the ’655 patent. Claim 1, reproduced below (with bracketed identifying labels added), is an independent claim:

1. [1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Ex. 1001, 9:54–67.

F. Prior Art Relied Upon

Petitioner relies upon the prior art references listed below. Pet. 1–2.

U.S. Patent No. 7,464,355 B2 (filed October 2, 2006; issued December 9, 2008) (“Yoshimura,” Ex. 1007);

“EDA for IC Implementation, Circuit Design, and Process Technology,” Louis Scheffer et al., CRC Press, Taylor & Francis Group (2006) (“Scheffer,” Ex. 1008);

U.S. Patent No. 7,092,838 B1 (filed June 4, 2004; patented August 15, 2006) (“Srinivas,” Ex. 1010);

Based on the current record, we determine Petitioner has shown that these references are prior art patents or printed publications under 35 U.S.C. § 102. *See* Pet. 14, 39, 48; Ex. 1007, codes (22), (45); Ex. 1010, codes (22), (45); Ex. 1008, 5. Petitioner also relies on the Declaration of Gabriel Robins, Ph.D. (Ex. 1003).

G. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–24 of the ’655 patent on the following grounds (Pet. 3, 14):

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–3, 8, 11–13, 18, 21, 22 ²	102	Yoshimura
1–24	103(a)	Yoshimura
4–7, 9, 10, 14–17, 19, 20, 23, 24	103(a)	Yoshimura, Scheffer
1–24	103(a)	Srinivas
6, 9, 10, 16, 19, 20, 23, 24	103(a)	Srinivas, Scheffer

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), revised 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the application from which the ’655 patent issued was filed before this date, the pre-AIA versions of §§ 102 and 103 apply.

² Although Petitioner states, on page 3, that claims 1–24 are asserted as being anticipated by Yoshimura, the detailed discussion asserts only the subset of claims listed here, with the remainder stated to be asserted as obvious rather than as anticipated. Pet. 14, 31–38.

II. DISCUSSION

A. Legal Standards

1. § 102

A claim is unpatentable under 35 U.S.C. § 102 “if each and every [claim] limitation is found either expressly or inherently in a single prior art reference.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1273 (Fed. Cir. 2017) (citation omitted). “A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present.” *Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003) (citing *Rosco, Inc. v. Mirror Lite, Co.*, 304 F.3d 1373, 1380 (Fed. Cir. 2002)). We analyze the asserted ground based on anticipation with these principles in mind.

2. § 103(a)

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).³ *Graham v. John Deere Co.*, 383 U.S. 1,

³ Patent Owner does not identify any secondary considerations to be considered. Accordingly, we do not consider this aspect of the obviousness analysis at this stage of the proceeding.

17–18 (1966). We analyze the asserted grounds based on obviousness with these principles in mind.

B. Level of Skill in the Art

Petitioner offers an assessment as to the level of skill in the art as of the time the '655 patent was filed. Pet. 9. For purposes of this proceeding, Petitioner and Petitioner's declarant "adopt the [following] definition for the person of ordinary skill in the art": "a Bachelor of Science degree in Electrical Engineering or Computer Engineering, and has either received academic credits for an ASIC design course or completed at least one year of work experience in the VLSI design, electronic design automation for VLSI, or ASIC design fields." *Id.* at 9–10; Ex. 1003 ¶ 78 (Robins Declaration). Patent Owner applies the same definition. Resp. 5. To the extent necessary, we accept this definition because it is supported by the Robins Declaration and consistent with the '655 patent and the asserted prior art.

C. Claim Construction

We apply the same standard that is used to construe a patent claim in a civil action under 35 U.S.C. § 282(b), and construe each claim in accordance with the ordinary and customary meaning of such claim, as understood by one of ordinary skill in the art in the context of the patent, and the prosecution history pertaining to the patent, as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). "[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

In litigation, the parties have agreed on the certain constructions. Pet. 10; Resp. 6. First, that the term “circuit objects” should be construed as particular object[s] in the circuit design such as gate[s], net[s], or pin[s].” Pet. 11 (citing Ex. 1004, 2). Second, that the term “timing slack values” should be construed as “the differences between the required time and the arriv[al] time of data signals at timing endpoints.” *Id.* Additionally, the term “scenario image” is agreed to be construed as “information required to detect and/or fix design requirement violations in a circuit design in a particular scenario.” Pet. 12; Resp. 6. Because they are consistent with the language of the claims and the disclosure of the ’655 patent, we accept and apply these definitions. We next address two claim terms that are the subject of some dispute in the proceeding.

1. *Multi-scenario engineering change order (ECO) database*

The phrase “a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios” has been the subject of construction in the parallel litigation. Ex. 2001, 20–21 (“Claim Construction Order”). The District Court, based on the parties’ proposed constructions, adopted the construction, “[a] database separate from the scenario image that stores a subset of parameter values for a subset of circuit objects in the multiple scenarios.” *Id.* During litigation, Petitioner argued that the subset need be “only a small fraction of the information stored in the scenario image;” Patent Owner argued that the subset could be “the entire set,” and the Court adopted Patent Owner’s position. *Id.* Both parties agreed that the database must be “separate from” the scenario image. *Id.*

However, in this proceeding, the parties dispute the meaning of “separate from” within that construction. Patent Owner argues that this term was “a variation of Petitioner’s ‘distinct from’ language,” referring to Petitioner’s statement in its initial claim construction brief that

The patent’s multi-scenario ECO database is supposedly a new data structure, whose data was copied from pre-existing scenario images, and which is loaded into memory while all but one of the scenario images remain on disk. It therefore is distinct from each scenario image. (’655 Fig. 4[])

Resp. 7–8. Petitioner argues that this construction requires that each be separately accessible, i.e., “separately recovered and queried and maintained implemented, information.” Tr. 71.

Although the phrase “separate from,” is not found in the claims, we look to the language of the claims, the description in the patent disclosure, and the prosecution history to determine what type of separateness is required by the claims. We start with the relied-upon Figure 4 of the ’655 patent, which illustrates a box labeled “Multi-Scenario ECO Database 426” that is near, but not overlapping with or surrounding, boxes labeled “Image 424” through “Image 422” and “Image 420.” Ex. 1001, Fig. 4. The ’655 patent also describes a storage device 408 as “storing scenario images 420–424 that correspond to different scenarios,” and “can additionally store multi-scenario ECO database 426,” which “can include circuit information for multiple scenarios that can be used to estimate the impact of ECOs in multiple scenarios.” Ex. 1001, 5:9–11, 5:18–21.

Turning to the claims, each independent claim requires that the “scenario image stores parameter values for circuit objects” and the “database stores a subset of parameter values for a subset of circuit objects.”

Ex. 1001, 9:56–61, 10:30–36; 11:6–11. Independent claims 1 and 11 recite separate steps of receiving the image and the database, but do not specify the source from which they are received; claim 21 specifies that both are stored in a memory. *Id.* The reasons for allowance in the prosecution history, while highlighting certain limitations of the originally presented claims, do not provide further clarification. Ex. 1002, 55.

With respect to its interpretation of “separate” as meaning “separately accessible,” Petitioner bases this on Dr. Friedman’s characterization of the Srinivas reference, not the ’655 patent, and only to the extent that Srinivas’s virtual timing graph is an “accessible data structure.” Reply 17 (citing Ex. 1029, 132:5). The characteristics of Srinivas are not probative of the construction of claim 1 of the ’655 patent. Furthermore, if the scenario image is merely a conceptual grouping of data within an entire set of data termed the multi-scenario ECO database, Petitioner does not clearly explain how one could access the scenario image without simultaneously accessing the multi-scenario ECO database. *See, e.g.,* Tr. 69–70.

The District Court’s construction of “separate from” is therefore adopted with respect to the above described statements of the parties and the disclosure of the ’655 patent. Notably, the scenario image must be received separately from the database, and each must contain a set of parameter values for circuit objects, but may not be merely a conceptual grouping of a single set of data.

2. *Determining an ECO to fix one or more design requirement violations, said determining includes estimating parameter values for circuit objects in at least some of the multiple*

scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database

Petitioner asserts that this term should be given its plain and ordinary meaning, which was the District Court’s tentative construction of the term.

Pet. 13. Patent Owner argues for application of the District Court’s final construction, which is,

determin[e/ing . . .] an ECO to fix one or more design requirement violations, wherein said determining includes identifying an ECO to fix a design requirement violation in the scenario and checking that ECO against at least some of the multiple scenarios by estimating parameter values based on parameter values stored in the scenario image and the multi-scenario ECO database.

Resp. 10 (citing Ex. 2001, 21-24).

In reviewing the term, the District Court explained that the multi-scenario ECO database “stores parameters and allows for a quick estimation of an ECO’s impact across multiple scenarios.” Ex. 2001, 19. The District Court further summarized the ’655 patent as describing that a scenario image is “[f]irst” loaded, and if there is a design requirement violation, an ECO is determined for that scenario, and then subsequent scenarios are loaded to check whether the ECO from the first scenario will create new, or exacerbate existing, design violations. *Id.* (citing Ex. 1001, 4:21–33). However, as recognized by the Court, the process at the cited section is described in the ’655 patent as an “approach [that] may take an impracticably long time to fix design requirement violations in multiple scenarios” due to the long time that is required to load a scenario image. *Id.* at 24; Ex. 1001, 4:43–47. The Court reasoned that in order to determine an ECO to fix a violation, “determine” must involve “identifying” a possible fix and “checking”

whether that fix is suitable. *Id.* at 23. Thus, the District Court’s construction requires both identifying and checking as part of the claimed determining step. *Id.* at 23–24. We agree with the District Court’s reasoning, and apply their construction in this proceeding.

The parties dispute whether this construction additionally requires a certain order of operations within the claimed steps. Patent Owner, in its arguments against Yoshimura, argues, “limitations 1.4 and 1.5 set forth an ordering requirement that is “integral to the ’655 Patent’s invention,” requiring the ECO be first identified, and then checked against multiple scenarios by estimating parameter values.” Resp. 16. Patent Owner further argues that estimating parameter values must be performed after an ECO is determined. *Id.* at 17. Patent Owner provides an example of an ECO that replaces one gate (602) with another gate (604), which would be an example of identifying an ECO as a possible fix. *Id.* Such a change would need to be checked for suitability; if a parameter (P1) relevant to gate 604 is not in the multi-scenario ECO database, that parameter must be estimated. *Id.* The estimation is based on information in the original scenario (e.g., the value of gate 604) and information from the multi-scenario database. *Id.* Patent Owner argues that this estimation could not occur before the ECO (that suggests replacing gate 602 with 604) is identified, because “the system would not yet know the identity of the suggested replacement gate.” *Id.*

The District Court stated,

Synopsys’s expert opines that “a POSITA would understand with reasonable certainty that in the context of the ’655 Patent the determining term requires both identifying a possible fix (based on the scenario image) and checking whether the possible fix is suitable (based on parameter values stored in the scenario

image and the multi-scenario ECO database” in at least some scenarios) Because the claim language indicates that estimation is a part of “determining,” “determining” can also encompass “checking” because parameter estimation is a way to check the ECO.

Ex. 2001, 23. The District Court treats “determining” as “encompass[ing]” each of identifying, checking, and estimating. Patent Owner’s argument that an ECO must be identified before it is checked is consistent with the District Court’s analysis.

However, the District Court does not state that the estimated parameters, which the determination of the change in the ECO relies upon, must be calculated only after the ECO is identified, rather than having a pre-calculated set of estimated values that may be retrieved when required. Patent Owner points to two statements from its expert, Dr. Edwards, in support of this requirement. Sur-reply 4–5. First, that Dr. Edwards, states that “the purpose of estimating those parameter values [in claim 1] was to use those values as part of the determination of what ECO’s to consider, what ECO’s to implement, that kind of thing.” Sur-reply 4 (citing Ex. 1034, 17). Second, to Dr. Edwards’ further characterization of claim 1 as being understood “to require both identifying a possible fix” based on the scenario image) and checking whether fix is suitable (based on estimating parameter values).” Sur-reply 5 (citing Ex. 1028, 17). Dr. Edward’s requirement is that determination is “based on” the estimated values, not that the step of estimating parameter values occurs at any particular time so long as the estimated values are “part of” the determination of what changes (ECOs) to implement. Thus, we do not agree with Patent Owner that the District Court’s construction requires estimating parameter values must be

performed after an ECO is determined. Under the Court's construction, which we apply here, parameter estimation must be performed such that it is a way to check an identified ECO.

D. Asserted Anticipation of Claims by Yoshimura

Petitioner contends that claims 1–3, 8, 11–13, 18, and 21–22 of the '655 patent are unpatentable as anticipated by Yoshimura. Pet. 14.

Petitioner relies upon the Robins Declaration to support its positions.

Ex. 1003. We begin our analysis with a brief overview of Yoshimura.

1. Overview of Yoshimura

Yoshimura relates to timing analysis for a semiconductor integrated circuit. Ex. 1007, 1:14–15. The layout of the circuit is corrected based on the timing analysis, which considers gate delay and net delay. *Id.* at 1:16–19. Gate delay and net delay vary with the ambient temperature, and the gate delay also varies with the power supply voltage. *Id.* at 1:21–24. Specific combinations of temperature and voltage conditions are referred to as corner conditions. *Id.* at 1:35–38. Yoshimura is concerned with reducing timing analysis time through completing timing error elimination and layout correction within a short period of time. *Id.* at 4:29–32.

2. Claim 1.

a) Petitioner's assertions

[1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

To the extent that the preamble is limiting, Petitioner points to Yoshimura's description of fixing timing errors, which Petitioner describes as a type of design requirement violation. Pet. 18. Petitioner points to Yoshimura's description of an error correction device 16 that searches for a

layout that does not cause a timing error under various corner conditions, and that performs layout correction to satisfy the hold margin and slack time under those conditions. *Id.* (citing Ex. 1007, 7:18–20, 8:24–26). Petitioner characterizes Yoshimura’s corner conditions as the claimed scenarios, noting that both the conditions and the scenarios represent conditions of temperature, voltage, and process. *Id.* at 20–21 (citing Ex. 1007, Figs. 4–5, 5:67–6:9; Ex. 1001, 1:35–37, 1:48–50). Petitioner further points to Yoshimura’s description of the error correction device including the addition of a buffer circuit and/or the replacement of buffer circuits with inverter circuits. *Id.* at 19 (citing Ex. 1007, Figs. 7A, 7B, 8B).

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;

Petitioner points to Yoshimura’s receipt, by the error correction device 16, of datasets in the form of a timing list 12 and a slack file 13. *Id.* (citing Yoshimura Figs. 4, 5, 5:67–6:9). Petitioner alleges that Yoshimura’s timing list and slack file constitute the claimed “scenario image” because they include the same type parameter values as in the ’655 patent. *Id.* at 19–20. Petitioner notes that Yoshimura’s parameter values include delay characteristics and slack time, just as the ’655 patent stores slack and delay values. *Id.* at 20 (citing Ex. 1001, Fig. 5, 2:16–17, 7:20–24, 5:62–66, 6:35–45; Ex. 1003; Ex. 1007, 5:20–23).

Petitioner alleges that Yoshimura’s timing list and slack file also meet the agreed-upon construction of “information required to detect and/or fix design requirement violations in a circuit design in a particular scenario.” *Id.* at 15, 21–22. Petitioner points to the timing list and slack file as being required in steps S4–S8 to detect and fix timing errors; i.e., design

requirement violations. *Id.* at 22 (citing Ex. 1007, Fig. 5, 6:61–7:67, 6:58–60, 7:18–21). Petitioner highlights Yoshimura’s statement, “[t]he automatic EC device 16 performs steps S4 to S8 based on the timing list 12, the slack file 13, and . . .” *Id.* at 22 (citing Ex. 1007, 6:58–60).

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and

Petitioner alleges that Yoshimura discloses this element under the district court’s construction, “a database separate from the scenario image, containing circuit information for multiple scenarios.” *Id.* at 23. Petitioner notes that the Patent Owner’s construction, which Petitioner adopts for purposes of this proceeding, is broader. *Id.* at 24 n.5. Petitioner points to Yoshimura’s libraries 11a,b as databases storing delay information (net delay and gate delay) for two corners. *Id.* at 24 (citing Ex. 1007, Fig. 4, 5:67–6:9, 3:5–8; Ex. 1003 ¶¶ 112–113). Petitioner alleges that Yoshimura’s delay information is circuit information because it provides signal delay information for specific parts (gates and nets) of the circuit. *Id.* Petitioner further alleges that the libraries 11a,b are databases because both a library and a database are just a large collection of data. *Id.* (citing a definition of “database”). Petitioner further alleges that Yoshimura discloses a subset of parameter values as claimed, because Yoshimura’s libraries contain delay information but not slack values. *Id.* at 25 (citing Ex. 1007, Fig. 4, 5:67–6:9, 3:5–8, 5:20–21). Petitioner further alleges that Yoshimura discloses receiving the multi-scenario ECO database because Yoshimura’s EC device 16 receives the libraries 11 a,b. *Id.* at 26 (citing Ex. 1007, 6:10–16, Fig. 4; Ex. 1003 ¶ 119).

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

Petitioner refers to the explanation for claim element 1.1. *Id.*

Petitioner further points to Yoshimura's examples of possible ECOs in which a buffer circuit is either added or replaced with a different circuit. *Id.* (citing Ex. 1007, Figs. 7A, 7B, 8B, 7:42–67, 8:8–12). Relying on its declarant, Petitioner argues that Yoshimura's description of its “automatic engineering change device,” its “store,” and the fact that the name of its field being “Electronic Design **Automation**,” shows that Yoshimura inherently uses one or more processors as claimed. *Id.* at 27–28 (citing Ex. 1007, 5:27–32, 6:17–30, 6:58–60, 7:18–27; Ex. 1003 ¶¶ 125–127).

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Petitioner points to Yoshimura's description of estimating parameter values in the form of hold margins in a scenario based on parameter values of gate delay and net delay stored in its libraries; i.e., its multi-scenario ECO database. *Id.* at 28–29 (citing Ex. 1007, 7:4–8:23, Fig. 6, step S5).

Petitioner points to Yoshimura's description for estimating parameter values based on parameter values stored in the scenario image, in the form of slack times and delay characteristics in the timing list and slack file. *Id.* at 29. Petitioner highlights step S5, in which the hold margin parameter values are estimated, as illustrating that the estimating is based on the scenario image because “these parameter values from the scenario image are needed to figure out which circuit paths to analyze in step S5.” *Id.* at 29–30 (citing Ex. 1003 ¶ 137).

b) *Analysis of Patent Owner's Arguments*

(1) *identifying an ECO . . . and checking that ECO
. . . include[ing] estimating parameter values*

Patent Owner first argues that Yoshimura does not anticipate the claimed invention because it does not perform “identifying an ECO . . . and checking that ECO,” which “includes estimating parameter values,” as required by the “determining” step of claim 1 (limitations 1.4 and 1.5), and similar steps of claims 11 and 25. Resp. 14–15.

Patent Owner argues that Yoshimura does not estimate parameter values after an ECO is determined. Resp. 19. Patent Owner argues that Yoshimura “performs its alleged estimating at step S5, which is completed before the alleged determining step—steps S6, S7, and S8.” Resp. 17–18 (citing Ex. 1007, 7:18–21). Patent Owner highlights Petitioner’s annotated Figure 5, with Petitioner’s annotations indicating that S5 “(Recalculation of Path Delays and Slack with Coefficient”) is an “Estimating Parameter Values Step” and that S6 (“Search for Optimal EC Location Satisfying Slack and Eliminating Timing Errors Under Both Normal Conditions and Temperature-Reversed Conditions”) is a “Determining ECO Step”, reproduced here:

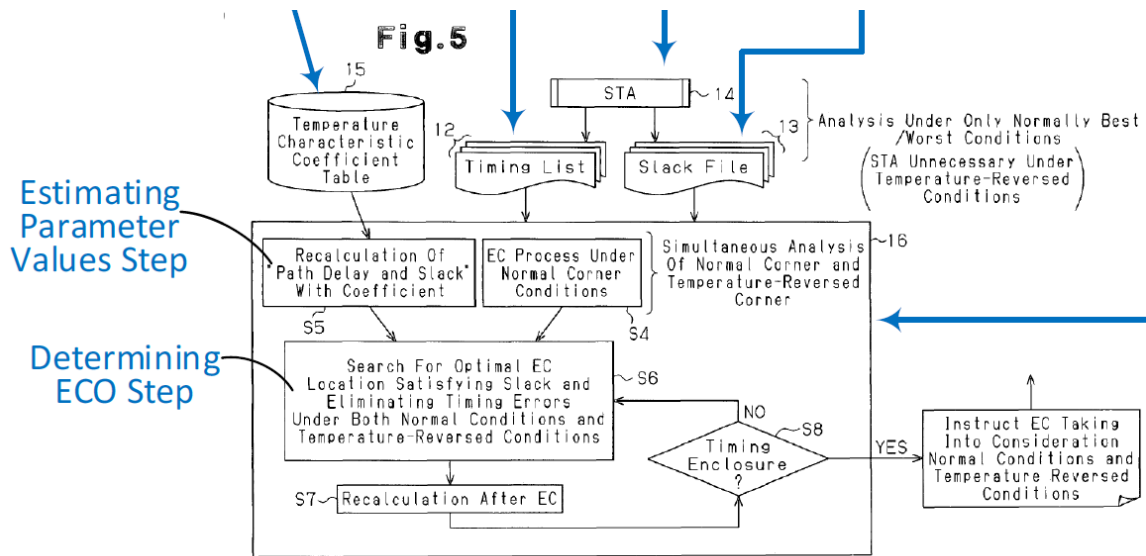


Figure 5 illustrates a process in which Step S5 receives a “Temperature Characteristic Coefficient Table” and, in combination with Step S4 (“EC Process Under Normal Corner Conditions”), leads to Step S6. Ex. 1007, Fig. 4; Resp. 18. Step S6 leads to step S7 (“Recalculation After EC”), after which it is determined whether the timing enclosure is satisfied at step S8. Ex. 1007, Fig. 4; Resp. 18–19. If the timing enclosure is not satisfied, the process proceeds back to step S6, looping through step S7 until the timing enclosure is satisfied at step S8. Ex. 1007, Fig. 4; Resp. 19.

Thus, because the estimation step S5 occurs before a particular EC is identified in step S6, Patent Owner argues that Yoshimura does not teach “identifying an ECO . . . and checking that ECO,” which “includes estimating parameter values.” Resp. 19.

Petitioner responds by arguing that Patent Owner’s construction requiring estimating to occur after ECO identification is wrong. Reply 9. As discussed *infra* at Section II(C)(2), we agree with Petitioner that claim 1 does not require estimating to occur after the ECO identification so long as the parameter estimation is performed so as to check an identified ECO.

Petitioner assertion that Yoshimura's estimation in step S5 is performed to check an identified ECO is supported by the record. In determining the change to be made (the ECO), Yoshimura uses estimated parameters for the third and fourth corner conditions, calculated in step S5 through the "Hold Margin" equation. Ex. 1007, 6:63–67. Those third and fourth corner conditions are then used to check potential layouts identified in step S6. *Id.* at 7:18–20 ("In step S6, the automatic EC device 16 searches for a layout that does not cause a timing error under any one of the first to fourth corner conditions from the analysis results of step S4 and step S5."). In this manner, step S5 sets an initial third corner condition having estimated parameter values that is included, as the initial step, in checking an identified ECO at steps S6–S8. Thus, Yoshimura's determination of a change to satisfy the corner conditions is, to use Dr. Edward's phrase, "based on" its third and fourth corner conditions having parameters estimated in step S5. For this reason, we determine that Petitioner has sufficiently shown that Yoshimura discloses the claimed limitation.

Furthermore, Petitioner shows that the parameters in step S5 become "part of" the analysis in steps S6–S8. As asserted by Petitioner, Yoshimura's step S7 modifies the S5 calculation by adding a buffer timing, i.e., by adding a value to the prior calculation. *Id.* at 7:55–67. For example, a failed layout may be changed to add a buffer, which then causes the "Hold Margin" equation to be modified by the additional buffer's time delay. *Id.* at 7:55–67. Patent Owner argues that "no estimating occurs in step S7," noting that no temperature coefficient (Petitioner's asserted manner of estimation) is input to step S7. Sur-reply 15. However, Yoshimura uses the third corner condition in its examples of determining ECO changes, and that third corner

condition is estimated by applying a temperature characteristic coefficient. Thus, Patent Owner's argument that no estimation coefficient is added at S7 would simply reinforce S5 as the locus of the estimation that is part of, and indeed integral to, the third and fourth corner ECO determinations. *See* Ex. 1007, 7:5–17, 7:28–67 (estimating the third corner condition by applying temperature coefficients to the data path delay (the total sum of the known gate and net delays of the second corner condition), 3:17–3:43; 7:33–54 (the gate delays (70ps total) and net delays of the second corner condition (16ps total), become temperature adjusted in the third corner condition to a 77 ps total gate delay and a 25.6 ps total net delay, resulting in an increase of total delay from 86 ps to 102.6 ps), 7:55–63 (identifying an ECO in the form of replacing an 11ps buffer with a 5 ps buffer, reducing the buffer by 7 ps, and determining that the total delay is now increased by 7ps from the third corner value to 109.6, causing the ECO to be successful)).

Consequently, we determine that Petitioner has shown Yoshimura to disclose “determining, by using one or more processors, an ECO to fix one or more design requirement violations, wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.”⁴

(2) *estimating parameter values for circuit objects*

Patent Owner also argues that Yoshimura does not teach “estimating parameter values for *circuit objects*.” Resp. 19. Patent Owner argues that

⁴ Consequently, we need not address whether step S7 alone provides the claimed “estimating” or whether Petitioner’s discussion of such in the Reply constitutes impermissible new argument.

Yoshimura's step S5 applies equation 6 to estimate parameter values, but that Step S5 calculates a single value (the hold margin) rather than parameter values for multiple circuit objects. *Id.* at 20. Equation 6 is as follows:

$$\text{Hold Margin} = \{kg \times \sum DG_i + kl \times \sum DL_i\} - \{kg \times \sum CG_j + kl \times \sum CL_j\} - T_{\text{hold}} \times kt \quad (\text{equation 6})$$

Patent Owner argues that the '655 Patent requires an estimated parameter for a specific circuit object, such as parameter P1 of gate 604, because that value is missing and needs to be estimated. *Id.* at 21 (citing Ex. 1001, 6:5–25, 6:49–65).

Petitioner argues that equation 6 represents individual gate and net delays using a summation notation; e.g., " $\sum DG_i$ " is the sum of all of the individual gate delay values DG_i in the non-temperature reversed corner. Reply 14 (citing Ex. 1007, 7:4–5; Ex. 1031 ¶¶ 31–32). Petitioner asserts that it is the application of the temperature characteristic coefficient (kg or kl in equation 6) that provides the estimation, because each of the other DG and DL values are from known values stored in the libraries (for corners 1 and 2). Pet. 27–28 (citing Ex. 1007, 7:4–8:23).

We determine that Petitioner has sufficiently shown that Yoshimura estimates parameter values for circuit objects. Equation 6 relies on gate delay values, and Patent Owner characterizes gates as circuit objects. Although equation 6 calculates a single value in the form of the hold margin, the individual values, such as the individual gate delay values, are summed in equation 6. Equation 6 multiplies its temperature characteristic coefficient by the sum of the individual values, which is mathematically equivalent (by the distributive property) to multiplying its temperature

characteristic coefficient by each individual value and summing the resulting products. We further agree with Petitioner's assertion, set forth in its Reply, that the hold margin itself is a parameter value for (plural) circuit objects, and that plural hold margins are determined in Yoshimura's S6–S8 loop. Reply 5–7. For the foregoing reasons, we do not agree that equation 6 does not demonstrate estimating parameters of specific circuit objects.

(3) determining includes estimating parameter values . . . based on parameter values stored in the scenario image and the multi-scenario ECO database.

Patent Owner argues that Yoshimura does not disclose estimating parameter values that are based on parameter values stored in the scenario image, and based on parameter values stored in the multi-scenario ECO database. Resp. 23. Patent Owner argues that Petitioner characterizes Yoshimura's "Analysis Results and Slack Information" as the claimed scenario image and Yoshimura's libraries 11a,b as the claimed multi-scenario ECO database. *Id.* Patent Owner argues that Petitioner does not show how step S5 estimates parameter values based on parameter values stored in the libraries 11a,b. *Id.* Patent Owner argues as unsupported Petitioner's asserted link between libraries 11a,b in Figure 4 with the Timing list in Figure 5. *Id.* at 24.

In its Sur-reply, Patent Owner instead argues that only libraries 11a,b and the temperature characteristic coefficient table 15 are used in estimating, because equation 6 contains only individual net and gate delays from the libraries 11 and temperature coefficients from table 15. Sur-reply 19–20. Because Petitioner attributes the libraries 11 to the multi-scenario ECO database, and the scenario image to the timing list 12 and slack file 13,

Patent Owner argues that the estimating is not based on any scenario image in Yoshimura. *Id.* at 16–21. Patent Owner argues that Yoshimura discloses only that “the timing list 12 and slack file 13 are used *somewhere* in steps S4 to S8,” and that does not show that the estimating in equation 6 is based on values stored in the timing list 12 and slack file 13. *Id.* at 21.

Petitioner supports its assertion that the estimating step S5 is based upon scenario image components timing list and slack file 12 with the following quotation from Yoshimura: “[t]he automatic EC device 16 performs steps S4 to S8 based on the timing list 12, the slack file 13, and the temperature characteristic coefficient table 15.” Pet. 29 (quoting Ex. 1007, 6:58–60). Petitioner reasons, “[s]ince step S5 (which is the step in which the parameter values (‘hold margins’) are estimated) is included in steps S4-S8, a POSITA would have understood that the estimating is based on the Yoshimura scenario image.” *Id.* (citing Ex. 1003 ¶ 137).

We find Petitioner’s assertions supported by the evidence. In particular, Yoshimura describes, “[u]nder each corner condition . . . timing analysis [is] performed. Based on the analysis results and the slack information, an EC process is performed (step S3).” Ex. 1007, 6:10–13. Yoshimura further describes, “[i]n step S3, an automatic EC device calculates a hold margin using a temperature characteristic coefficient corresponding to each corner condition.” *Id.* at 6: 17–19. The same hold margin calculation is performed in estimating step S5, which is labeled “Recalculation of ‘Path Delay and Slack’ With Coefficient.” Thus, step S5 explicitly states that it recalculates slack as well as path delay. Although Petitioner asserts that path delay may come from either the scenario image via timing list 12 or from the multi-scenario ECO database via libraries 11

holding net delay and gate delay, Petitioner asserts that slack is only located in slack file 13, which is only in the scenario image. Pet. 25 (citing Ex. 1007, 5:20–21).

For the above described reasons, Petitioner has sufficiently shown Yoshimura to disclose that its determining includes estimating parameter values . . . based on parameter values stored in the scenario image and the multi-scenario ECO database.

3. *Remaining asserted claims*

- a) *Claim 2. The method of claim 1, wherein each scenario in the multiple scenarios is associated with one or more of: a process corner, an operating condition, or an operating mode.*

Petitioner alleges Yoshimura discloses at least one of the alternative options, in the form of a corner that includes a process corner, in the form of a fast or slow process, and multiple operating conditions, in the form of temperature and voltage. *Id.* at 30 (citing Ex. 1007 Figs. 4–5, 5:67–6:9).

- b) *Claim 3. The method of claim 1, wherein the parameter values include timing slack values at one or more pins in the circuit design.*

Petitioner points to Yoshimura’s slack file 13 as including slack values in the form of slack times for the cells of the circuit. *Id.* at 31 (citing Ex. 1007, 5:20–23). Relying on its expert, Petitioner argues that the slack values for the cells of the circuit are the same as the slack values at one or more pins of the cell, because “slack values for the cells of the circuit are really just the slack values at one or more pins in the cells since the slack value of a cell is the difference between the arrival time of the data input signal on one of the input pins of the cell and the arrival time of the clock signal at the other input pin of the cell.” *Id.* (citing Ex. 1003 ¶ 146).

c) *Claim 8. The method of claim 1, wherein the one or more design requirement violations include a hold timing violation.*

As discussed with respect to claim 1, Petitioner points to Yoshimura's timing errors, corresponding to the claimed design requirement violations, as including a negative hold margin, corresponding to the claimed hold timing violation. *Id.* at 35. Petitioner further notes that Yoshimura describes implementing an ECO to correct the timing requirement violation, in the form of adding a buffer circuit into the data path when the hold margin is insufficient. *Id.* (citing Ex. 1007, 6:17–8:27, 7:56–67, Fig. 7B).

d) *Claims 11–13, 18 and 21–22.*

Petitioner asserts that claims 11 and 21 are nearly identical to claim 1, and are disclosed by Yoshimura for the same reasons as asserted for claim 1. Petitioner further asserts that claims 12, 13, 18, and 22 recite language nearly identical to claims 2, 3, 8, and 2, respectively. *Id.* at 37–38.

4. *Determination*

Patent Owner does not provide argument specific to these claims. For the reasons set forth above, we find Petitioner has made the requisite showing for each of these claims. In view of the foregoing, Petitioner has shown, by a preponderance of the evidence, that claims 1–3, 8, 11–13, 18, and 21–22 are anticipated by Yoshimura.

E. Asserted Obviousness over Yoshimura

Petitioner contends that claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24 of the '655 patent are unpatentable as obvious under 35 U.S.C. § 103(a) over Yoshimura. Petitioner claims that the limitations recited in these claims would have been obvious to one having ordinary skill in the art, relying upon the Robins Declaration to support its positions. Pet. 31–38, Ex. 1003.

Petitioner relies, at least in part, on teachings of prior art not applied in this ground of unpatentability, including on teachings of Scheffer. *See* Pet. 37 (relying on Scheffer to corroborate the need to ensure compliance with electrical design rules). Because a separate ground addressing these claims explicitly relies on Scheffer and Yoshimura (*infra* at II(G)), we address Yoshimura and Petitioner’s declarant’s assertions as to what was well known in the art in that ground.

F. Asserted Obviousness over Yoshimura and Scheffer

Petitioner contends that claims 4–7, 9, 10, 14–17, 19, 20, 23, and 24 of the ’655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over Yoshimura and Scheffer. Petitioner relies upon the Robins Declaration to support its positions. Ex. 1003. We begin our analysis with a brief overview of Scheffer.

1. Overview of Scheffer

Scheffer is a handbook on Electronic Design Automation (“EDA”). Ex. 1008, 8. Chapters were contributed by experts from across the disciplines involved in EDA. *Id.* at 9. Scheffer explains that the chapters in the handbook “represent a snapshot of the state of the art, written in 2004–2005.” *Id.* Scheffer’s chapters include chapters on noise considerations in digital integrated circuits and layout analysis. *Id.* at 20.

2. Analysis

Petitioner provides a detailed analysis, supported by testimony, to show how the references teach the limitations in the claims.

a) Claims 4–6, 14–16, and 23

Claims 4–6 further limit the parameter values recited in claim 1. Claim 4 limits the parameter values to including capacitive load values at

one or more pins. Claim 5 limits the parameter values to including transition time values at one or more pins. Claim 6 limits the parameter values to include leakage power values for gates. Petitioner asserts that none of these specific types of parameter values are disclosed by Yoshimura, but that each were taught by Scheffer for assessing integrated circuit operating behavior. Pet. 40–43.

With respect to claim 4, Petitioner points to Scheffer’s description of capacitive load values at one or more gates in the circuit design, including at the pins of the gates. *Id.* at 40 (citing Ex. 1008, 126; Ex. 1003 ¶ 179). Petitioner additionally points to Scheffer’s characterization of capacitive load as critical for assessing gate delay and power budget violations. *Id.* (citing Ex. 1008, 126, 196). Petitioner further points to Scheffer’s various means for estimating capacitive load values. *Id.* (citing Ex. 1008, 485–488, 493).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use capacitive load values as a parameter value in Yoshimura, because the capacitive load values at the pins affect the rate at which the pins’ voltage can change, and would be needed to determine whether a timing or power requirement has been violated. *Id.* (citing Ex. 1003 ¶¶ 180–181). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including capacitive load values in Yoshimura’s scenario image and/or multi-scenario ECO database, because Yoshimura’s database already includes similar types of parameter values. *Id.* at 40–41 (citing Ex. 1003 ¶ 181).

With respect to claim 5, Petitioner points to Scheffer’s description of

transition time values at one or more pins in the circuit design. *Id.* at 41 (citing Ex. 1008, 48, 126–129; Ex. 1003 ¶ 184). Petitioner additionally points to Scheffer’s characterization of transition times as important for assessing noise, timing, and gate delay. *Id.* (citing Ex. 1008, 126–129, 455–473; Ex. 1003, ¶ 185).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use transition time values as a parameter value in Yoshimura, because the transition times at the pins affect the timing of the circuit, and would be needed to determine whether a timing requirement has been violated. *Id.* at 41–42 (citing Ex. 1003 ¶ 185). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including transition time values in Yoshimura’s scenario image and/or multi-scenario ECO database, because Yoshimura’s database already includes similar types of parameter values. *Id.* at 42 (citing Ex. 1003 ¶ 186).

With respect to claim 6, Petitioner points to Scheffer’s description of leakage power values as a parameter value for gates in circuit design. *Id.* (citing Ex. 1008, 35, 42, 196, 204). Petitioner additionally points to Scheffer’s characterization of leakage power values as being estimated based on logic count, technology parameters, and voltage. *Id.* (citing Ex. 1008, 204).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to use leakage power values as a parameter value in Yoshimura, because the leakage power values affect the total power budget of the circuit, and would be needed to determine whether a power budget requirement has been violated. *Id.* at 43

(citing Ex. 1003 ¶ 190). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in including leakage power values in Yoshimura's scenario image and/or multi-scenario ECO database, because Yoshimura's database already includes similar types of parameter values. *Id.* (citing Ex. 1003 ¶ 191). Petitioner also points to Figures 3 and 4 of the '655 patent, arguing that similarities in prior art Figure 3 and inventive Figure 4 indicate, in the absence of description to the contrary, that the scenario images in both rely on the same type of information, including leakage power values. *Id.* at 33; Reply 21–22.

Petitioner asserts that claims 14–16 recite language nearly identical to claims 4–6, and that claim 23 collectively recites one or more of the types of parameter values recited in claims 3–6. *Id.* at 47. Petitioner argues that claims 14–16 and 23 are obvious over Yoshimura in view of Scheffer for the same reasons advanced for claims 4–6. *Id.*

Patent Owner argues only claims 6 and 16. Resp. 38. Patent Owner argues that using leakage power values in Yoshimura would render its timing analysis systems inoperable for their intended purpose. *Id.* Patent Owner argues that although Scheffer shows that non-timing parameters existed, it is Patent Owner's "innovation in this EDA design space" that "modif[ied] timing systems to determine and estimate non-timing parameters." Sur-reply 35. Patent Owner argues that Petitioner has not shown how Yoshimura's timing system could determine a leakage power value, or how such modification of the timing system to leakage power values would be performed. *Id.* at 34.

We agree. Dr. Friedman had testified that Yoshimura is incompatible

with determining a leakage power. Ex. 2020 ¶¶ 65–66. Scheffer does not describe how leakage power would be used in a timing system. At best, Scheffer indicates that leakage power may also be estimated at a fast process and high temperature corner condition; however, Scheffer indicates that hold-time violations (as in Yoshimura) are estimated at a different corner, the low temperature corner. Ex. 1008, 34–35. Consequently, Petitioner has not shown that it would have been obvious to a person of ordinary skill in the art at the relevant time to modify Yoshimura’s process for leakage power.

We also agree with Patent Owner’s argument that Figure 3 is not explicitly described as prior art, and that nothing in the ’655 patent implies that leakage power values in an ECO was known in the prior art. Resp. 39 (addressing Petitioner’s argument that the use of leakage power would be obvious over Yoshimura alone). We decline to interpret the ’655 patent’s silence on this matter as an implicit description of such.

In view of the foregoing, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 6 and 16 would have been obvious over Yoshimura, either by itself or in combination with Scheffer. However, we are persuaded that the parameter values of claims 4, 5, 14, and 15 have been shown to be sufficiently related to timing such that it would have been obvious to use them in the system of Yoshimura. Claim 23 requires “one or more of” values that include timing slack, capacitive load, and transition time, each of which we have found to be taught by Yoshimura (claims 3, 13) or Yoshimura and Scheffer (claims 4, 5, 14, 15). Thus, Petitioner has shown, by a preponderance of the evidence, that claims 4, 5, 14, 15, and 23 would have been obvious over the combination of Yoshimura and Scheffer.

b) *Claims 7, 9, 10, 17, 19, 20, and 24*

Claims 7, 9, and 10 further recite specific types of design requirement violations that Petitioner admits are not explicitly disclosed by Yoshimura, but allegedly are taught by Scheffer. *Id.* at 43–47.

Claim 7 further recites, “wherein the one or more design requirement violations include a setup timing violation.” Petitioner relies upon Scheffer for teaching performing a timing analysis to ensure that setup timing requirements are not violated. *Id.* at 44 (citing Ex. 1008, 6–8; Ex. 1003 ¶ 194). Petitioner further points to Scheffer’s description of timing requirement violations as being fixed by resizing gates, buffering, or widening wires. *Id.* (citing Ex. 1008, 175, 214–216).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix setup timing violations, because such violations prevent a circuit from operating at the desired clock rate. *Id.* (citing Ex. 1003 ¶ 195). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing timing violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* (citing Ex. 1007, 6:17–8:27).

Claim 9 further recites, “wherein the one or more design requirement violations include an electrical design rule violation.” Petitioner relies upon Scheffer for teaching performing a design rule analysis, in the form of noise analysis to ensure that noise requirements are not violated. *Id.* at 45 (citing Ex. 1008, 192, 196–197, 454–464). Petitioner further points to Scheffer’s

description of setting a maximum allowable limit on the glitch peak. *Id.* (citing Ex. 1008, 211; Ex. 1003 ¶ 299). Petitioner additionally relies on Scheffer for teaching that it was well known in the art to fix electrical design rule violations by resizing gates, buffering large fan-out nets, and inserting repeaters. *Id.* (citing Ex. 1008, 211).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix electrical design rule violations, because such violations prevent a circuit from operating properly when deployed, and that excessive noise can compromise performance. *Id.* at 45–46 (citing Ex. 1003 ¶ 200). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing design rule violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* at 46 (citing Ex. 1007, 6:17–8:27).

Claim 10 further recites, “wherein the one or more design requirement violations include a power budget violation.” Petitioner relies upon Scheffer for teaching performing a power analysis to ensure that power budget requirements are not violated. *Id.* (citing Ex. 1008, 65, 191–196). Petitioner further relies on Scheffer for teaching that it was well known in the art to fix power budget violations by resizing gates. *Id.* (citing Ex. 1008, 211).

Petitioner alleges that a person having ordinary skill in the art at the time the invention was made would have been motivated to modify Yoshimura to also identify and/or fix power budget violations, because such violations prevent a circuit from operating properly when deployed, and that

a circuit will not operate properly if it cannot support and/or meet certain power constraints. *Id.* at 47 (citing Ex. 1003 ¶ 205). Petitioner further alleges that a person having ordinary skill in the art would have had a reasonable expectation of succeeding in also determining and fixing power budget violations, because this would require no more than adding another design requirement to the similar requirements already present in Yoshimura. *Id.* (citing Ex. 1007, 6:17–8:27).

Petitioner asserts that claims 17 and 19–20 recite language nearly identical to claims 7 and 9–10, respectively, and that claim 24 collectively recites one or more of the types of design requirement violations recited in claims 7–10. *Id.* at 48. Petitioner argues that claims 17 and 19–20 are obvious over Yoshimura in view of Scheffer for the same reasons advanced for claims 7 and 9–10. *Id.*

With respect to both electrical design rule violations and power budget violations, Petitioner argues that a person having ordinary skill in the art would have known how to fix the former and identify the latter. Reply 23 (also stating that it was well known to use software tools to consider and address both), 24 (citing Ex. 1001, 1:23–30). Petitioner further points to statements by Patent Owner of its capability to handle both of these as well as timing violations. *Id.* at 23–24. Petitioner further asserts that the lack of any special instruction on how to address non-timing violations in the '655 patent indicates that a person having ordinary skill would have considered such to be known in the art. *Id.* at 24–28 (citing *In re Fox*, 471 F.2d 1405, 1407 (CCPA 1973)).

Patent Owner argues that the electrical design rule violations and power budget violations of claims 9, 10, 19, and 20 require “fundamentally

different analyses.” Sur-reply 37. Although Patent Owner’s declarant admitted that a person of ordinary skill in the art would know how to fix design rule violations, Patent Owner argues that such a statement does not indicate that such a person would have known how to do so by modifying timing software. *Id.* at 37–38. Patent Owner points to statements by its declarant and Scheffer that separate software would be used for timing analyses, power analyses, and electrical design rule analyses. *Id.* at 38 (citing Ex. 2020 ¶ 80; Ex. 1008, 192). Patent Owner further characterizes *In re Fox* as permitting that “an examiner may take official notice that a[n] unremarkable limitation was known in the art,” but not mandating that every feature not described in detail is admitted as prior art. *Id.* at 39.

We agree. As discussed for claim 6, Petitioner has not shown that it would have been obvious to a person of ordinary skill in the art at the relevant time to modify Yoshimura’s timing process for non-timing variables, in the absence of specific reasons to do so and a reasonable expectation of success. Petitioner provides neither. At best, Petitioner shows that a person of ordinary skill in the art would know how to fix electrical design rule violations and power budget violations. However, Petitioner has not shown that such a person would have had a reason to do so by modifying Yoshimura’s timing process, or that such a person would have had a reasonable expectation of success in doing so.

Petitioner’s argument that such a modification must have been known because the ’655 patent is silent is erroneous. Petitioner’s citation to *In re Fox*, referring to an examiner’s ability to find an element well known in the art, may support an argument that a person having ordinary skill in the art, reading the ’655 patent, would understand what electrical design rule

violations and power budget violations are. In *Fox*, notice was taken “in part in express statements in appellant’s specification and in part is deducible from the fact that . . . [anyone] would know of the equipment and techniques to be used.” However, nothing in the ’655 patent implies that identifying and fixing electrical design rule violations and power budget violations *in the claimed manner* was known in the prior art. Nor does Scheffer or any statement of either declarant. Thus, we decline to interpret the ’655 patent’s silence on this matter as an implicit recognition of such.

In view of the foregoing, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 9, 10, 19, and 20 would have been obvious over Yoshimura, either by itself or in combination with Scheffer. However, we are persuaded that the setup timing parameter of claims 7 and 17 has been shown to be sufficiently related to Yoshimura’s timing parameters such that it would have been obvious to use it in the system of Yoshimura. Claim 24 requires “one or more of” values that include setup timing and hold timing, both of which we have found to be taught by Yoshimura (claims 8, 18) or Yoshimura and Scheffer (claims 7, 17). Thus, Petitioner has shown, by a preponderance of the evidence, that claims 7, 17, and 24 would have been obvious over the combination of Yoshimura and Scheffer.

G. Asserted Obviousness over Srinivas

Petitioner contends that claims 1–24 of the ’655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over Srinivas. Petitioner relies upon the Robins Declaration to support its positions. Ex. 1003. We begin our analysis with a brief overview of Srinivas.

1. *Overview of Srinivas*

Srinivas relates to computer-aided design of integrated circuits.

Ex. 1010, 1:8–10. As the dimensions of circuits shrink, “many electrical properties that were previously second and third order effects have come to play a major role in determining circuit performance and power consumption.” *Id.* at 1:23–27. Such effects may be environmental (such as temperature), artifacts of manufacturing (such as material thickness), reliability (such as degradation), or operational (such as design constraints for different operating modes. *Id.* at 1:36–3:31. Srinivas seeks to “accommodate design variability in an efficient way so that performance can be analyzed and optimized over a large number of corners with a reasonable computational overhead.” *Id.* at 4:24–28. Srinivas describes an embodiment that incrementally updates timing graphs over all combinations of corner and mode, such that only the information that needs to be updated is re-computed. *Id.* at 9:35–40. Illustrating that embodiment is Figure 4, which, as annotated by Petitioner, is reproduced below.

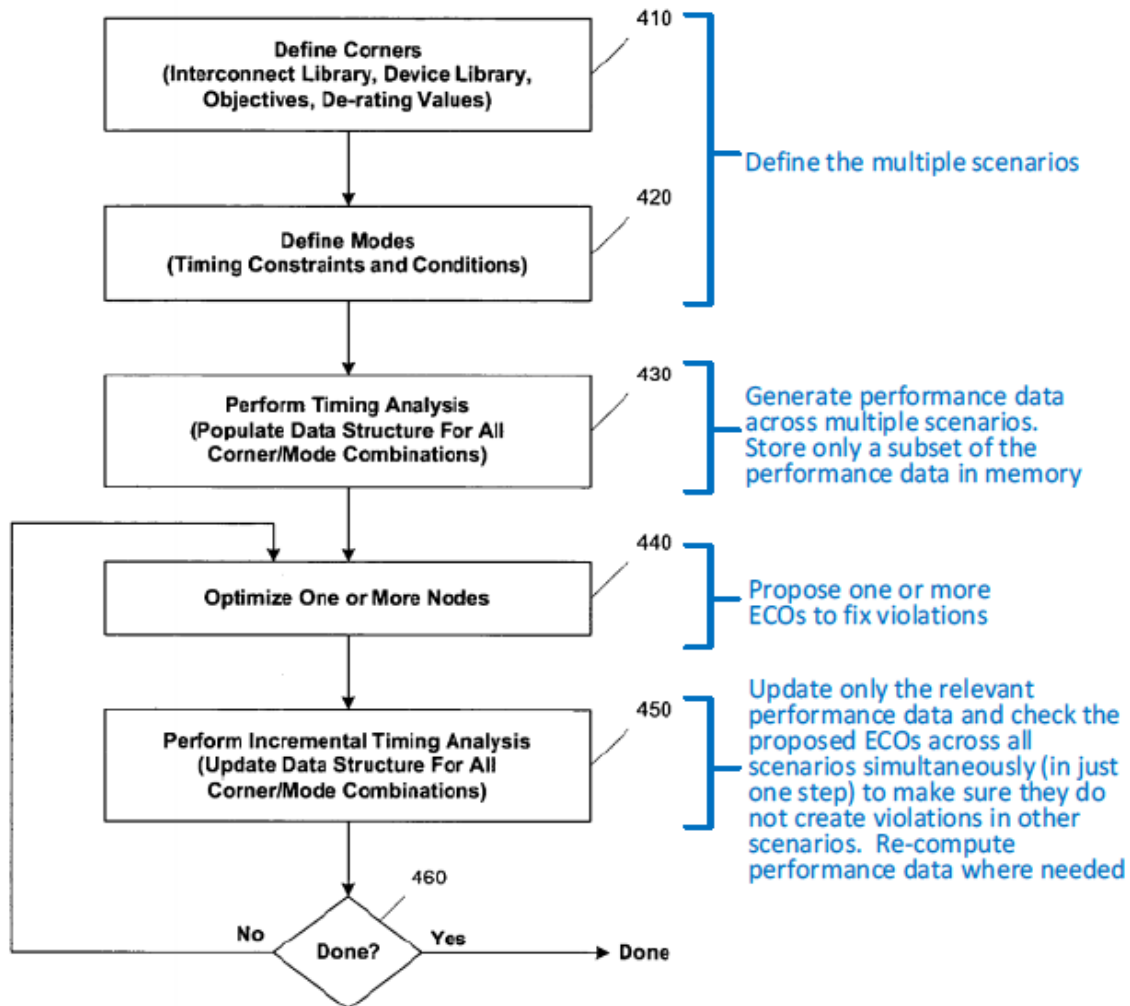


FIG. 4

Pet. 50. Figure 4 describes a process of defining corners (step 410), defining modes (step 420), performing timing analysis (step 430), optimizing one or more nodes (step 440), performing incremental timing analysis (step 450), and determining whether the process is done, or if the process should move to step 440. Petitioner annotates steps 410 through 450, characterizing steps 410 and 420 as “Define the multiple scenarios,” step 430 as “Generate performance data across multiple scenarios. Store only a subset of the performance data in memory,” step 440 as “Propose one or more ECOs to

fix violations,” and step 450 as “Update only the relevant performance data and check the proposed ECOs across all scenarios simultaneously (in just one step) to make sure they do not create violations in other scenarios. Re-compute performance data where needed.” *Id.*

2. Claim 1

a) *Petitioner’s assertions*

[1.1] A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:

Petitioner points to Srinivas’ corners and modes as disclosing the claimed multiple scenarios. *Id.* at 51. Srinivas’ corners include “any combination of process, voltage and temperature (PVT), as well as other environmental, manufacturing or reliability factors.” *Id.* (citing Ex. 1010, 3:34–37). Petitioner asserts that Srinivas’ described modes and corners disclose the claimed multiple scenarios, which are described in the ‘655 patent as “the combination of ‘a particular process corner, a particular operating condition [(e.g., temperature, voltage)], and/or a particular operating mode.’” *Id.* (citing Ex. 1001, 1:35–37, 1:48–50).

With respect to fixing design requirements in a circuit, Petitioner points to Srinivas’ disclosure that “[o]nce a change is made to the circuit, the optimizer typically decides to accept the change based on improvement in the worst slack over all combinations of corner and mode.” *Id.* at 52 (citing Ex. 1010, 10:4–7).

[1.2] receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario

With respect to parameter values, Petitioner points to Srinivas’ description of performance data that can include timing data, slew, and

capacitance. *Id.* (citing Ex. 1010, 7:53–55, 8:4–6, 8:40–43). Petitioner asserts that these are the same type of data described as parameter values in the '655 patent; i.e., capacitance and slew. *Id.* at 52–53 (citing Ex. 1001, 5:61–64).

With respect to a scenario image, Petitioner points to Srinivas' circuit graph, which includes the aforementioned performance data, and can be stored in data structures such as matrices for each node of the circuit graph. *Id.* at 53 (citing Ex. 1010, Fig. 3, 8:4–53). Petitioner also points to Srinivas' Table 1 as an example matrix at a single node, containing three modes ("sleep," "standby," and "active") and three corners ("setup/hold," "noise," and "setup"). *Id.* at 53–54 (citing Ex. 1010, Fig. 3, 8:15–30).

Petitioner alleges that these descriptions in Srinivas disclose claim limitation 1.2 under the agreed-to construction. *Id.* Petitioner also alleges that these descriptions would meet the tentative district court construction, also requiring the scenario image to contain information needed to detect and/or fix design requirement violations in a particular scenario, because the matrices store the kind and quantity of data needed to fix and identify design requirement violations. *Id.* at 54–56 (pointing to similar data used in the '655 patent to identify and fix violations).

With respect to the scenario image being "received" as claimed, Petitioner asserts that a person having ordinary skill in the art would have understood Srinivas to inherently disclose some form of memory that would receive the circuit graph, based on the nature of Srinivas' data structures and timing analysis. *Id.* at 56.

[1.3] receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios

Petitioner points to Srinivas' circuit graph as including both the scenario image and the multi-scenario ECO database. *Id.* at 57. Petitioner alleges that Srinivas' circuit graph includes "at least enough information to identify and/or fix violations in one scenario (the scenario image) and also include circuit information for other scenarios (the multi-scenario ECO database)." *Id.* (citing Ex. 1010, 9:1–9).

Petitioner also addresses the district court's tentative construction that the "multi-scenario ECO database" should be interpreted to mean "a database separate from the scenario image, containing circuit information for multiple scenarios. *Id.* (citing Ex. 1006, 3). Relying on its declarant, Petitioner argues that, because the circuit graph contains sufficient information for both, one having ordinary skill in the art would have considered splitting data from the circuit graph into separate databases as a mere choice of design, well within the skill of the ordinary artisan. *Id.* (citing Ex. 1003 ¶ 239).

With respect to the "subset" of circuit objects, Petitioner asserts that Srinivas describes that the data structures may contain less than all parameter values, because some parameter values may be re-computed when performing timing analysis. *Id.* at 58 (citing Ex. 1010, 8:45–53).

[1.4] determining, by using one or more processors, an ECO to fix one or more design requirement violations,

With respect to an ECO, i.e., a "change order," Petitioner points to Srinivas' step 440 as making a change to the circuit, which may be accepted

“based on improvement in the worst slack over all combinations of corner and mode.” *Id.* at 59 (citing Ex. 1010, 10:4–7). Petitioner characterizes the “worst slack” as a design requirement violation, fixed by the change to the circuit. *Id.*

With respect to a processor, Petitioner points to the process of Figure 4 as being executed by processor 510. *Id.* (citing Ex. 1010, 10:32–34).

[1.5] wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database.

Petitioner points to Srinivas’ re-computing performance data for nodes in at least some of the combinations stored in the circuit graph. *Id.* at 60. As discussed for earlier limitations in claim 1, Petitioner characterizes Srinivas’ performance data as the claimed “parameter values,” nodes as the claimed “circuit objects,” and the circuit graph as making obvious the separately claimed “scenario image” and “multi-scenario ECO database.” Petitioner asserts that the re-computing is based on at least some data in the stored parameter values because some of the parameter values for at least some of the nodes can be omitted. *Id.* (citing Ex. 1010, 8:44–9:9, 9:56–10:3).

b) *Patent Owner’s Arguments*

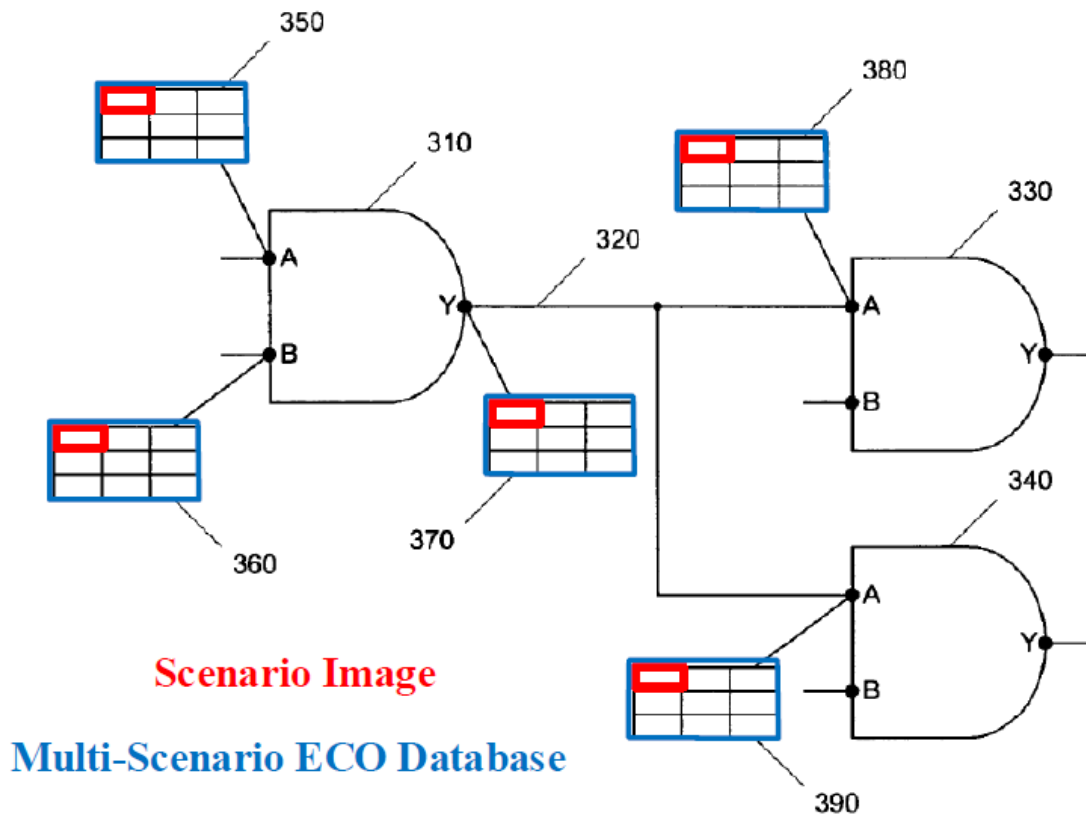
Patent Owner argues that Srinivas does not teach estimating parameter values based on both the scenario image and the multi-scenario ECO database. Resp. 25. Patent Owner highlights Petitioner’s reliance on Srinivas’ Circuit Graph as being both the scenario image and the multi-scenario ECO database. *Id.* (citing Pet. 53, 57). Patent Owner argues that,

based on case law and the agreed-to claim construction, these must be separate objects, and cannot both be the same Circuit Graph. *Id.* (citing *Becton, Dickinson and Co. v. Tyco Healthcare Group, LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010); Ex. 2024, 21:3–10). Patent Owner highlights that in the parallel litigation, both parties asserted, and the District Court ruled, that the database is “separate from the scenario image.” *Id.* at 27 (citing Ex. 2001, 20. Patent Owner argues that the separate nature of these objects is “central to the ’655 Patent’s invention” because utilizing the scenario image with a complementary ECO database “enables the system to quickly estimate the impact that an ECO is expected to have in each scenario.” *Id.* at 26–28 (quoting Ex. 1001, 4:64–5:2).

Patent Owner argues that Petitioner has insufficiently explained how a person of ordinary skill would split the singular Circuit Graph into separate databases so as to meet the claimed scenario image and multi-scenario ECO database. *Id.* at 29–32 (citing Pet. 54). Patent Owner further argues that Dr. Robins did not present a clear explanation of the demarcation between these two objects in the singular Circuit Graph. *Id.* at 32–33 (citing Ex. 2024, 42:4–14 (“Q. And so, conceptually, Srinivas’s circuit graph contains the scenario image and the multi-scenario ECO database? A. Not necessarily, even on a conceptual level.”)). Patent Owner also points to Dr. Friedman’s testimony that he is “unable to discern any way that a [person having ordinary skill in the art] could divide Srinivas’s Circuit Graph into a separate scenario image and ECO database while meeting all of the limitations of the claims.” *Id.* at 33 (citing Ex. 2020 ¶¶ 57–60). Further, Patent Owner argues that Srinivas explicitly states that its Circuit Graph should remain intact, thus undercutting Petitioner’s “design choice” reasoning for splitting the Graph.

Id. at 33–34 (citing Ex. 2020 ¶ 60, Ex. 1010, 8:54–57, 9:41–10:3). Patent Owner highlights Srinivas’ reliance on “*using a single actual timing graph*” to maintain and optimize all modes simultaneously. *Id.* at 34 (citing Ex. 2020 ¶ 60; Ex. 1010 6:7–14, 5:62–65, 8:54–57, 9:56–10:3).

Petitioner replies to these arguments by asserting that the District Court’s Claim Construction Order requires the scenario image and multi-scenario ECO database to be separate, but does not preclude the two from overlapping. Reply 16. Petitioner further asserts that the ’655 patent shows overlap of parameters between the scenario image and the multi-scenario ECO database. *Id.* at 19. Petitioner argues that Srinivas’ Circuit Graph contains parameter values sufficient to meet the required parameter values of both scenario image and ECO database, as claimed. *Id.* at 16. Petitioner argues that the entirety of Srinivas’ Circuit Graph teaches the multi-scenario ECO database, and that, for example, “a collection of information stored in the top left field of the tables is just one of Srinivas’ scenario images.” *Id.* at 16–17. Petitioner provides an annotated version of Srinivas’s Figure 3:



Petitioner’s annotated Figure 3 characterizes tables 350, 360, 370, 380, and 390 of a circuit graph as the “Multi-Scenario ECO Database” with blue highlighting, with each table having nine boxes, and the top left-hand box in each table highlighted in red and labeled as “Scenario Image.” *Id.* at 17.

Petitioner asserts that Srinivas recognizes these scenario images as separate entities by referring to them as a “virtual timing graph.” *Id.* Petitioner provides three reasons why Srinivas’ related boxes within separate tables should be considered a virtual timing graph that is separate from the circuit graph:

First, individual virtual timing graphs can be and are processed separately from the entire circuit graph. For example, “it is possible to recover a virtual timing graph for any corner and any mode.” EX1010, 7:58-60.

Second, a user can query an individual virtual timing graph for performance data for a particular scenario: “[a] query could be for a specific corner/mode combination.” EX1010, 4:42-43. “In this way, the resulting data structure implements a virtual timing graph for each combination of corner and mode.” *Id.* 4:45-47.

Third, Srinivas emphasizes that the performance data for different scenarios is maintained separately. “Performance data is kept separately for each analysis corner and can be globally queried, allowing for simultaneous optimization.” *Id.* 6:32-35. The data is not “mixed” between scenarios: “A preferred embodiment accepts mode specific timing constraints and performs analysis without mixing the data across different modes. Each mode represents different timing conditions and results in a different timing graph.” EX1010, 5:55-59.

Id. at 18.

Petitioner further argues that the Court’s construction of “scenario image” as “information,” rather than a “database,” permits the scenario image to be part of the ECO database. *Id.* at 19 (citing Ex. 2001, 24).

Petitioner further points to Dr. Friedman’s testimony that the virtual timing graphs are “accessible data structure[s].” *Id.* (citing Ex. 1029, 132:5).

Petitioner further argues that to the extent that Dr. Friedman focuses on Srinivas’ term “a data structure” to indicate a single data structure, this focus errs because “a” can mean “one or more.” *Id.* at 20. (citing Ex. 2020 ¶ 37; *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008)).

In its Sur-reply, Patent Owner argues that Petitioner’s reliance on different portions of the circuit graph (e.g., the top left-hand box in each table) in its Reply is a new argument that deviates from its assertion in the Petition that both the scenario image and ECO database are met by “the

circuit graph.” Sur-reply 23–26. Patent Owner argues that this new reasoning should not be considered. *Id.* at 26.

Patent Owner further argues that even under this new reasoning, the top left-hand box of each table is not distinct from the entirety of the tables that make up the circuit graph; rather, the boxes are “wholly subsumed within the 54 total fields” of the tables that make up the alleged ECO database. *Id.* Patent Owner dismisses the three arguments presented in the Reply because they show only that one virtual timing graph is separate from other timing graphs – not that any virtual timing graph is separate from the database within which it resides. *Id.* at 27–28. Patent Owner points out that in the ’655 patent, the scenario image overlaps incompletely with the ECO database, and is not wholly subsumed therein. *Id.* at 28–29.

Patent Owner further argues that Srinivas does not describe estimating parameter values “based on parameter values stored in the scenario image and the [separate] multi-scenario database.” Sur-reply 30. Patent Owner argues that Srinivas’s recomputing of omitted data, which Petitioner assigns to the “estimating,” is performed using only data from a single virtual timing graph, i.e., a single scenario image. *Id.* at 31 (citing Ex. 1010, 8:57–65; Ex. 2025, 77:4–78:7).

We determine that Petitioner has insufficiently shown Srinivas to teach or suggest the invention of claim 1. For essentially the entirety of the limitations of the claim, Petitioner relies upon Srinivas’ timing graph of Figure 3, Srinivas’ statement that some values may be “eliminated” and then “re-computed,” and the selection of the cell of the timing graph data having the worst violation as an ECO. From this, Petitioner infers (1) that the timing graph may be separated into distinct data sets as a design choice, (2)

that these data sets are “receiv[ed]” “just by the fact that the circuit graph and its data structures . . . exist,” (3) that “re-computing” data from the circuit graph that existed and was eliminated is “estimating” such data from both of the separate (scenario image and ECO database) datasets. Pet. 56–57, 60. However, none of these three inferences are sufficiently supported by the arguments and evidence of record.

With respect to separating the timing graph into two data sets, i.e., a scenario image and a multi-scenario ECO database, Petitioner argues that it would have been obvious as a design choice. Pet. 57. Petitioner’s support for this contention is a statement by Robins that it “would have been well within the skill” of a person having ordinary skill to alter Srinivas to do so “depending on how the [person] wished to organize the data.” *Id.* (citing Ex. 1003 ¶ 239). Robins’ reason for doing such is because the organization of data “is not essential or consequential to the functionality.” Ex. 1003 ¶ 239. This statement is not borne out by the evidence. In fact, Dr. Robins admitted that Srinivas’s circuit graph does not necessarily, even on a conceptual level, contain the scenario image and the multi-scenario ECO database. Ex. 2024, 42:4–14. Furthermore, Srinivas emphasizes that “an efficient data structure is used that minimizes the memory and CPU overhead of performing analysis over an arbitrary number of corners,” and that “a single traversal of the circuit graph is all that is needed to populate the data structure.” Ex. 1010, 7:55–56, 7:64–66. Srinivas is focused on “allow[ing] the memory footprint of the analysis engines to be small.” Patent Owner highlights other sections supporting Srinivas’ reliance on “*using a single actual timing graph*” to maintain and optimize all modes simultaneously. Resp. 34 (citing Ex. 2020 ¶ 60; Ex. 1010 6:7–14, 5:62–65, 8:54–57, 9:56–10:3). These

statements are inconsistent with a timing graph that may be split to perform some ill-explained wish to organize the data. The above evidence indicates that the form of the data structure is of particular importance to Srinivas for efficiency, memory allocation, and CPU overhead. Consequently, Petitioner's argument that it would have been obvious, as a mere design choice inconsequential to its functionality, to split Srinivas's circuit graph into separate data sets is not sufficiently supported by the record.

With respect to Srinivas teaching "receiving" a separate scenario image and multi-scenario ECO database, we also find Petitioner's case to lack sufficient evidentiary support. Dr. Robins states that the data being relied upon for the timing analysis described in Figure 4 of Srinivas was stored in memory 520, and necessarily would have been received. Ex. 1003 ¶ 231. However, the fact that the entirety of the data exists in Srinivas' memory 520 does not sufficiently teach or suggest that it would have been received via the two distinct receiving steps in claim 1, "receiving a scenario image" and "receiving a multi-scenario engineering change order (ECO) database." Ex. 1001, 9:58–61. Even were Petitioner persuasive in showing that the data could have been (at some unspecified time) organized into those datasets, the agreed-to construction requires those to be separate sets, and thus, that they be received as separate sets. The mere fact that their underlying data components exist in memory, and that they could have been separately arranged once in memory 520, does not sufficiently teach or suggest that they were received as separate, distinct datasets.

Finally, with respect to Srinivas's alleged teaching that the estimating is based on parameter values stored in the scenario image and the multi-scenario database, Petitioner has not provided explanation or evidence that

shows the estimating to be based on parameter values from both sources. Patent Owner points to testimony of Dr. Robins as confirming that Srinivas's "re-computing of missing data," the alleged "estimating," uses data from other nodes in that scenario image. Reply 31 (citing Ex. 2025, 77:4–78:7). Although Dr. Robins states that "other information" must be used, neither Dr. Robins nor Patent Owner explain how Srinivas's re-computing teaches using data from a scenario image and data from the multi-scenario database. Ex. 2025, 65:11–78:15. Nor does Petitioner specify why the data which it is based upon, "data at other nodes," would involve data outside that scenario image. Pet. 60, Reply 21. To the contrary, Petitioner argues that "data is not 'mixed' between scenarios." Reply 18. Further, although Petitioner asserts that the re-computing is of "omitted/eliminated" data, Dr. Robins instead points to re-computing as being performed after an ECO fix is implemented to "make sure the ECO improved" sufficiently through that fix. Ex. 1031 ¶¶ 51–53; Ex. 2025, 65. Although Dr. Robins also points to Srinivas re-computing data to replace eliminated or omitted data, Dr. Robins does not specify that the re-computing for replacement of data is part of the estimating, or that it would involve data from both the scenario image and from the multi-scenario database. (Ex. 2024, 57–58). Consequently, we do not find Petitioner's assertion to be persuasive.

3. Determination

In view of the foregoing, Petitioner has not met its burden to show, by a preponderance of the evidence, that claim 1 would have been obvious over Srinivas. Because Petitioner's assertions for the other claims in the ground

contain the same flaws as determined for claim 1, Petitioner has not met its burden to show that those claims would have been obvious over Srinivas.

H. Asserted Obviousness over Srinivas and Scheffer

Petitioner contends that claims 6, 9, 10, 16, 19, 20, 23, and 24 of the '655 patent are unpatentable as obvious under 35 U.S.C. § 103(a), over the combination of Srinivas and Scheffer. For the same reasons as discussed at section II(G)(2), regarding claim 1, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 6, 9, 10, 16, 19, 20, 23, and 24 would have been obvious over Srinivas and Scheffer.

Furthermore, because Srinivas, like Yoshimura, describes timing-based ECO determination, we determine that Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 6, 9, 10, 16, 19, and 20 are obvious over Srinivas and Scheffer, for the same reasons discussed at section II(F)(2).

III. CONCLUSION⁵

For the foregoing reasons, we determine Petitioner has established by a preponderance of the evidence that claims 1–5, 7, 8, 11–15, 17, 18, and

⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

21–24 are unpatentable, but has not established by a preponderance of evidence that claims 6, 9, 10, 16, 19, and 20 are unpatentable. In summary,

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–3, 8, 11–13, 18, 21, 22	102	Yoshimura	1–3, 8, 11–13, 18, 21, 22	
1–3, 8, 11–13, 18, 21, 22	103(a)	Yoshimura ⁶		
4–7, 9, 10, 14– 17, 19, 20, 23, 24	103(a)	Yoshimura, Scheffer	4, 5, 7, 14, 15, 17, 23, 24	6, 9, 10, 16, 19, 20
1–24	103(a)	Srinivas		1–24
6, 9, 10, 16, 19, 20, 23, 24	103(a)	Srinivas, Scheffer		6, 9, 10, 16, 19, 20, 23, 24
Overall Outcome			1–5, 7, 8, 11– 15, 17, 18, 21–24	6, 9, 10, 16, 19, 20

ORDER

For the foregoing reasons, it is:

ORDERED that Petitioner *has shown* based on a preponderance of

⁶ As explained *supra* at § II.E, we do not reach this rejection because it relies on Scheffer to evidence what is well known in the art; we instead address these contentions for the asserted ground based on Yoshimura and Scheffer.

evidence that claims 1–5, 7, 8, 11–15, 17, 18, and 21–24 are unpatentable; and Petitioner *has not shown* based on a preponderance of evidence that claims 6, 9, 10, 16, 19, and 20 are unpatentable;

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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