

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY, INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-01265
Patent 7,870,404 B2

Before FRANCES L. IPPOLITO, NATHAN A. ENGELS, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Microchip Technology Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–21 of U.S. Patent No. 7,870,404 B2 (Ex. 1001, “the ’404 patent”). HD Silicon Solutions LLC (“Patent Owner”) filed a Preliminary Response to the Petition (Paper 6, “Prelim. Resp.”).

To institute an *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons set forth below, upon considering the Petition, Preliminary Response, and evidence of record, we determine the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we do not institute *inter partes* review.

A. Related Proceedings

The parties indicate that the ’404 patent has been asserted in *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092 (W.D. Tex), filed November 30, 2020 (“Texas case”). Pet. 1; Paper 4, 2. The parties also indicate that, on October 25, 2021, the Texas case was transferred to the Northern District of California as *HD Silicon Solutions, LLC v. Microchip Technology Inc.*, No. 3:21-cv-08295-SK (N.D. Cal.) (“District Court Litigation”). Paper 7, 2; Prelim. Resp. 45. Petitioner also indicates that it has filed several IPRs against various patents related to the ’404 patent, including: IPR2021-00752, IPR2021-00872, IPR2021-01042, IPR2021-01089, IPR2021-01420, and IPR2021-01567. Paper 7, 2–4.

B. The '404 Patent

The '404 patent, titled “Transitioning to and from a Sleep State of a Processor,” is directed to reducing power use by a computer system during intervals in which processing is stopped. Ex. 1001, code (54), 1:18–20. The '404 patent describes a method that includes the steps of (1) “determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled,” and (2) “reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.” *Id.* at 2:12–18. The '404 patent explains that, even in the mode in which its clocks are disabled, “the processor must maintain state sufficient to immediately return to an operating condition” so that “it can respond rapidly to interrupts provided by the circuitry that controls application of the system clocks.” *Id.* at 3:1–9. As a result, “a significant amount of unnecessary power may be expended.” *Id.* at 3:21–23. To address this problem, the '404 patent describes a technique that “reduces the voltage applied to the processor significantly below the lowest voltage normally furnished as a core voltage for the processor during the mode in which system clocks are disabled thereby reducing the power utilized by the processor in the deep sleep state.” *Id.* at 3:27–31.

C. Illustrative Claims

Petitioner challenges claims 1–21 (“challenged claims”), which are all of the claims of the '404 patent. Pet. 1. Claims 1, 7, 11, 15, and 18 are independent claims. Claim 1 is reproduced below.

1. A computer system comprising:
a processing unit;
circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit:

a sleep voltage;
a first operating voltage; and
a second operating voltage that is less than the first operating voltage;
wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;
wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;
wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and
wherein said first transition time is greater than said allowed time.

Ex. 1001, 7:26–44.

D. The Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–21 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–21	103	NEC-Databook ¹ , Stratakos ² , and the knowledge of a person of ordinary skill in the art

Pet. 4. Petitioner further relies on the testimony of Donald Alpert, PhD. Ex. 1002. *Id.* at 5.

¹ Single-Chip Microcomputer Databook, NEC Electronics Inc. (May 1990). Ex. 1004 (“NEC-Databook”).

² Anthony J. Stratakos, High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications (1998). Ex. 1005 (“Stratakos”).

II. ANALYSIS

A. *Principles of Law*

In *Graham v. John Deere Co.*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) “secondary considerations” of non-obviousness such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the Federal Circuit has “repeatedly emphasized that an obviousness inquiry requires examination of all four *Graham* factors and that an obviousness determination can be made only after consideration of each factor.” *WPIP v. Kohler*, 829 F.3d 1317, 1328 (Fed. Cir. 2016) (“A determination of whether a patent claim is invalid as obvious under § 103 requires consideration of all four *Graham* factors, and it is error to reach a conclusion of obviousness until all those factors are considered.”).

We note that, with respect to the fourth *Graham* factor, the current record in this proceeding does not include any argument or evidence directed to secondary considerations of nonobviousness.

B. *Level of Ordinary Skill in the Art*

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus. Inc.*, 807 F.2d 955, 962 (Fed. Cir.

1986); *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends that a person of ordinary skill in the art at the time of the invention of the '404 patent “would have possessed a bachelor’s degree in electrical engineering, computer engineering, or computer science, with two years of experience in computer system development, including experience in developing power/voltage regulation systems for portable devices.” Pet. 5. Petitioner also states:

A person could also have qualified as a person of ordinary skill in the art with some combination of (1) more formal education (such as a master’s of science degree) and less technical experience or (2) less formal education and more technical or professional experience in the fields listed above.

Id. Patent Owner does not dispute this level of skill. *See generally* Prelim. Resp. For purposes of this Decision, we adopt Petitioner’s proposal as reasonable.

C. Claim Construction

For petitions filed on or after November 13, 2018, the “broadest reasonable interpretation” standard has been replaced with the federal court claim construction standard that is used to construe a claim in a civil action under 35 U.S.C. § 282(b). This is the same claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny.

Petitioner asserts that “[f]or the purposes of this Petition, claim terms should be given their plain and ordinary meaning.” Pet. 12.

Patent Owner indicates that it “takes no position in this response on whether it agrees or disagrees with Petitioner’s proposal that the claim terms should be given their plain and ordinary meaning.” Prelim. Resp. 27–28.

On this record, we determine that no claim term requires an express construction for the purpose of determining whether to institute *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over NEC-Databook, Stratakos, and the Knowledge of a Person of Ordinary Skill in the Art – Claims 1–21

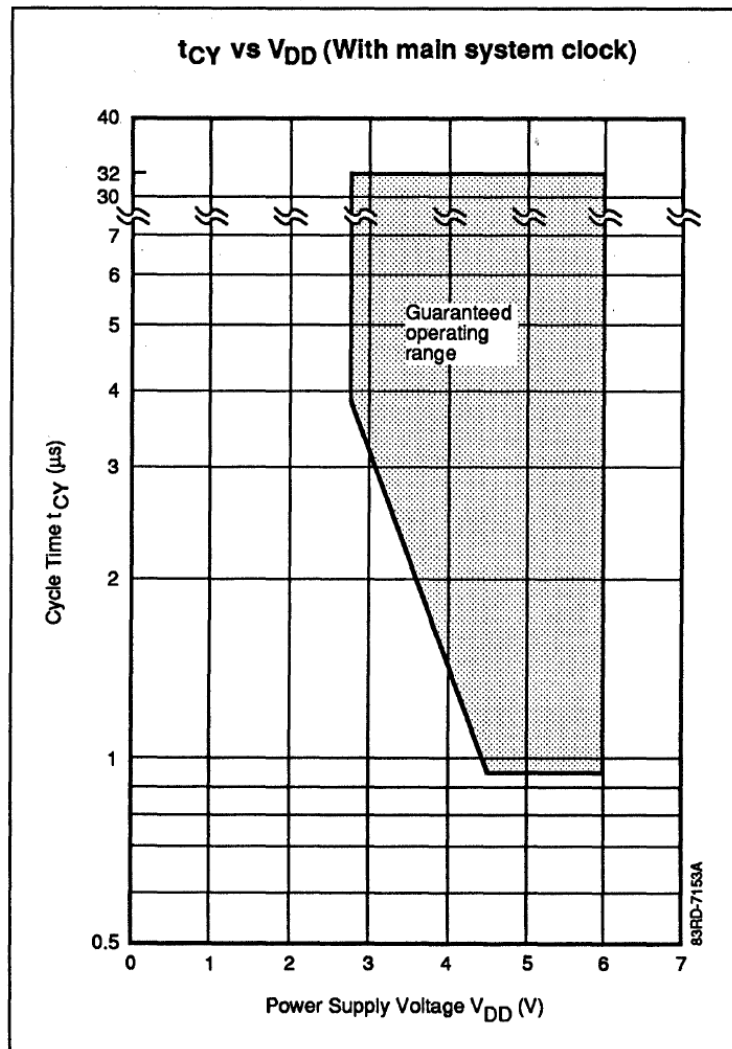
Petitioner asserts claims 1–21 would have been obvious over the combination of NEC-Databook, Stratakos, and POSITA’s knowledge. Pet. 18–109. For the reasons that follow, we determine that Petitioner has not established a reasonable likelihood of prevailing with respect to this ground.

1. Overview of NEC-Databook (Ex. 1004)

NEC-Databook is a product data book for NEC single-ship microcontrollers published in May 1990. Ex. 1004, 1;³ Ex. 1038, 20–21. NEC-Databook describes the μ PD751xx/P1xx “family of high-performance single-chip CMOS microcomputers containing CPU, ROM, RAM, I/O ports, comparator, interval timer, two timer/counters, vectored interrupts, and a serial interface.” Ex. 1004, 024. Figure 17 of NEC-Databook, reproduced below, depicts the operating range of the μ PD751xx.

³ We refer to Petitioner’s added page numbers in Ex. 1004.

**Figure 17. Guaranteed Operating Range
(μ PD751xx)**



NEC-Databook's Figure 17 depicts the guaranteed operating range of the μ PD751xx.

Id. at 062. In Figure 17, the vertical axis depicts Cycle Time t_{CY} (μs) and the horizontal axis depicts Power Supply Voltage V_{DD} (V). Cycle time is a “minimum Instruction execution time” and “is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC).” *Id.*

NEC-Databook further teaches a standby mode that consists of three submodes, HALT, STOP, and Data Retention. Ex. 1004, 47. In the HALT

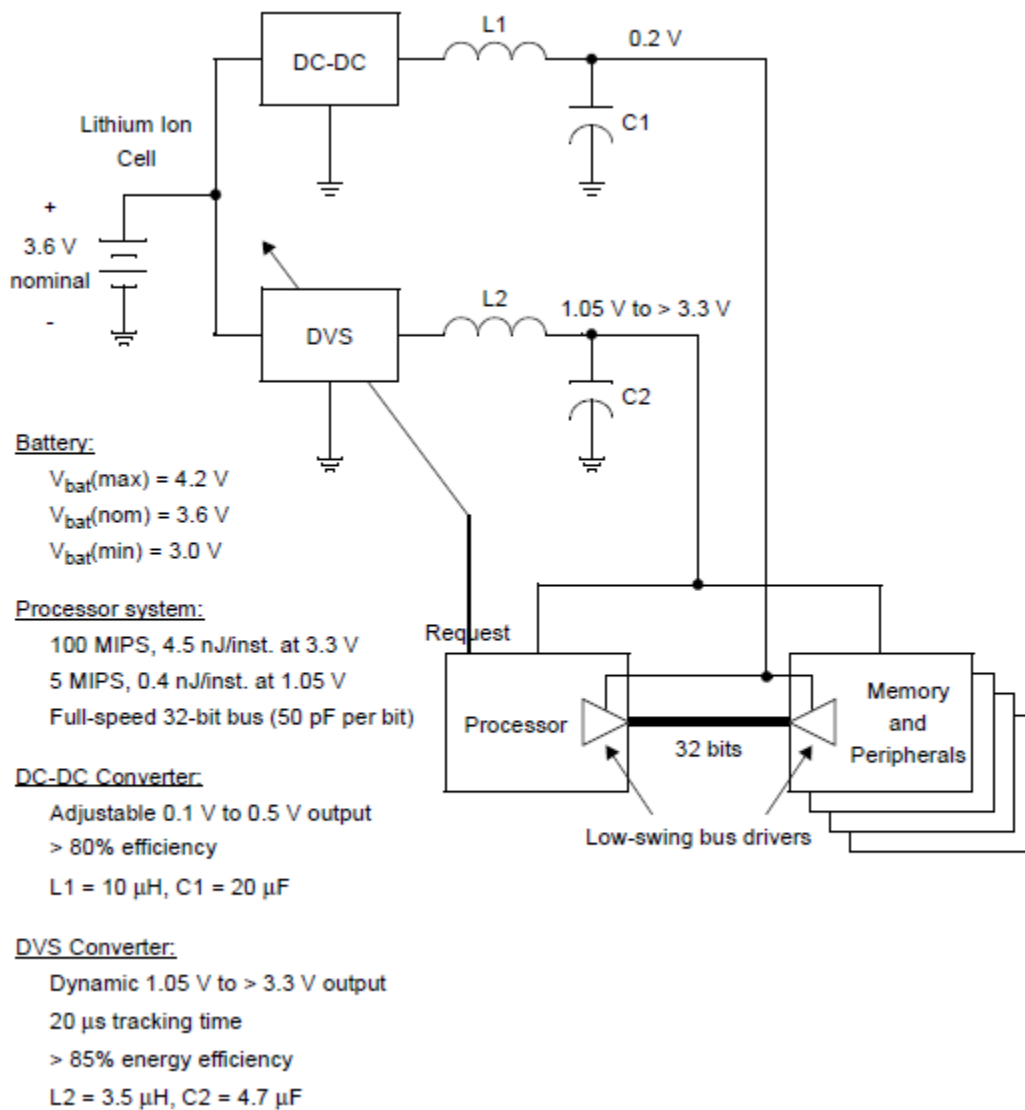
and STOP modes, the clock is shut off. *Id.* “The HALT and STOP modes are released by a RESET or by any interrupt request.” *Id.* Additionally, the “[Data Retention mode] may be entered after entering the STOP mode.” *Id.* The V_{DD} may be lowered to 2 volts to further reduce power consumption. *Id.* “The contents of the RAM and registers are retained. This mode is released by first raising V_{DD} to the proper operating range, then releasing the STOP mode.” *Id.* Additionally, NEC-Databook teaches a minimum t_{SREL} release signal set time of 0, but does not teach a minimum t_{WAIT} time. Ex. 1004, 64.

2. *Overview of Stratakos (Ex. 1005)*⁴

Stratakos is a doctoral dissertation entitled “High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications” published in 1998. Ex. 1005, 1; Ex. 1038, 24. By way of introduction, Stratakos explains that “[p]ortable electronic equipment demands ultra-low-power hardware to maximize battery run-time.” Ex. 1005, 10. Stratakos discloses that “[p]erhaps the most effective low-power technique is to operate each digital CMOS subsystem at its optimum voltage, realizing a quadratic reduction in power dissipation with decreasing supply voltage.” *Id.* In Chapter 2, Stratakos “describes a number of low-power digital CMOS design techniques which are enabled by DC-DC converters, and the potential battery run-time enhancements effected by DC-DC converters in portable electronic systems.” *Id.* at 10–11. In Chapter 6, Stratakos teaches “[a] complete power delivery system for an energy-efficient microprocessor is shown to demonstrate design at both the system and circuit levels.” *Id.* at

⁴ We note that Petitioner cites pagination on the upper right-hand corner of the exhibit. For consistency, we do the same.

147. Figure 6.1 of Stratakos depicts power delivery for an energy-efficient microprocessor subsystem (*id.*) and is reproduced below.



Stratakos’s Figure 6.1 depicts power delivery for an energy-efficient microprocessor subsystem.

In the system of Figure 6.1, “critical digital hardware is operated from the dynamically scaled voltage supply” (“DVS converter”) which “scales the energy per operation of the converters’ digital control circuits together with those of the microprocessor and peripherals, helping to maintain conversion efficiencies.” *Id.* at 148–149. “In addition, the 0.2 V supply is utilized by

the dynamic voltage converter to enable low-swing communication from the processor to the dynamic DC-DC converter IC.” *Id.* at 149.

Table 6.7: Tracking performance summary.

Transition	Tracking Time	Tracking Energy ^a
$f_{VCO} = 5 \text{ MHz to } 100 \text{ MHz}$ $V_{dd} = 1.08 \text{ V to } 3.78 \text{ V}$	23.5 μs	4.6 μJ
$f_{VCO} = 100 \text{ MHz to } 5 \text{ MHz}$ $V_{dd} = 3.78 \text{ V to } 1.08 \text{ V}$	44.0 μs	
$f_{VCO} = 20 \text{ MHz to } 40 \text{ MHz}$ $V_{dd} = 1.39 \text{ V to } 1.82 \text{ V}$	7.3 μs	0.2 μJ
$f_{VCO} = 40 \text{ MHz to } 20 \text{ MHz}$ $V_{dd} = 1.82 \text{ V to } 1.39 \text{ V}$	9.9 μs	
$f_{VCO} = 40 \text{ MHz to } 80 \text{ MHz}$ $V_{dd} = 1.82 \text{ V to } 2.95 \text{ V}$	16.2 μs	1.2 μJ
$f_{VCO} = 80 \text{ MHz to } 40 \text{ MHz}$ $V_{dd} = 2.95 \text{ V to } 1.82 \text{ V}$	19.3 μs	

a. Estimated for the full low-to-high-to-low tracking cycle.

Table 6.7 summarizes tracking performance for a variety of high-to-low and low-to-high frequency transitions at $\frac{1}{4}$ full-load and $V_{bat} = 6.0 \text{ V}$. Ex. 1005, 211.

In Table 6.7, Stratakos teaches that the DVS converter can supply voltages in the range of 1.08 to 3.78 V. *Id.*

3. Analysis of Independent Claim 1

a) Petitioner’s Contentions

(1) “sleep voltage,” “first operating voltage,” “second operating voltage”

Independent claim 1 is directed to a computer system that includes a “processing unit” and “circuitry coupled to the processing unit.” Ex. 1001, 7:26–29. Additionally, claim 1 requires that the circuitry is configured to provide to the processing unit:

- a sleep voltage;
- a first operating voltage; and

a second operating voltage that is less than the first operating voltage.

Ex. 1001, 7:26–31.

Petitioner asserts that NEC-Databook teaches “a processing unit” in the form of “ μ PD751xx/P1xx [that] is a family of high-performance single-chip CMOS microcomputers containing CPU, ROM, RAM,” which operate in the voltage range of 2.7–6.0 V. Pet. 18–19 (citing Ex. 1004, 24), 29.

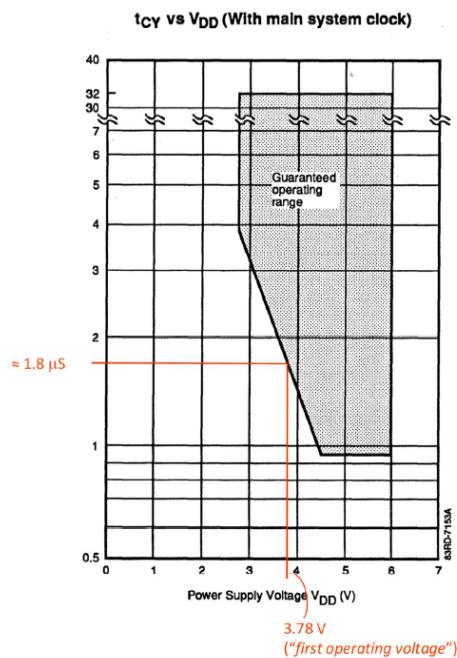
Petitioner further contends that Stratakos discloses a DVS converter that supplies varying voltages in the range of 1.08–3.78V to a processor (i.e., “circuitry” recited in independent claim 1). Pet. 19 (citing Ex. 1002 ¶ 182; Ex. 1005, 149, Fig. 6.1, 2, 22–22), 21 (citing Ex. 1002 ¶¶ 188–192; Ex. 1005, 23 (Fig. 2.11), 126, (Fig. 5.2), 177, 188 (Fig. 6.38), 211 (Table 6.7)).

Petitioner further asserts that “NEC-Databook’s μ PD751xx-CPU (processing unit) has a V_{DD} pin to receive a voltage from a power supply.” Pet. 22 (citing Ex. 1004, 26 (Figure “Pin Configurations”), 28 (Figure “Block Diagram”); Ex. 1002 ¶¶ 193–194).

For “sleep voltage,” Petitioner argues that POSITA would have understood that when NEC-Databook’s μ PD751xx-CPU is in the STOP mode, it is in a sleep state. Pet. 25 (citing Ex. 1004, 44; Ex. 1002 ¶ 199). Petitioner argues that the μ PD751xx-CPU may enter Data Retention mode after entering the STOP mode. *Id.* According to Petitioner, “[s]ince the μ PD751xx-CPU enters Data Retention mode from STOP mode where the CPU clock is stopped, Data Retention mode is also a sleep state and, hence, the data retention voltage of **2.0 V is a sleep voltage.**” *Id.* at 26 (citing Ex. 1002 ¶¶ 201–202) (emphasis added). Referring to the Table: “Product Comparison” on page 31 of NEC-Databook, Petitioner asserts that the μ PD751xx-CPU operates between 2.7 to 6.0 V and “a POSITA would have

understood that in Data Retention mode, any voltage in the range of 2.0 to 2.69 V is a sleep voltage.” Pet. 27–28.

For “first operating voltage” and “a second operating voltage that is less than the first operating voltage,” Petitioner asserts that NEC-Databook’s μ PD751xx-CPU operates between 2.7 to 6.0 V. Pet. 29, 32. Within this range, Petitioner picks 3.78 V as “a first operating voltage” based on the voltage range supplied by Stratakos’s DVS converter, 1.08–3.78 V. *Id.* at 30. Petitioner further relies on an annotated version of NEC-Databook’s Figure 17 that is provided in Dr. Alpert’s declaration. The annotated Figure 17 is reproduced below:



Annotated Figure 17 from NEC-Databook is provided in paragraph 225 of Dr. Alpert’s declaration. Ex. 1002 ¶ 225. Petitioner asserts that the cycle time for V_{DD} at 3.78 V is approximately 1.8 μ s. Pet. 31.

Petitioner picks 3.3 V as a second operating voltage for μ PD751xx-CPU that is less than the 3.78 V (the “*first operating voltage*”). Pet. 32 (citing Ex. 1002 ¶ 230; Ex. 1004, 62 (Figure 17)). Referring to Stratakos’s

Figure 17, Petitioner contends that NEC-Databook teaches that when $V_{DD} = 3.3\text{ V}$ the cycle time is approximately $2.4\text{ }\mu\text{s}$. Pet. 32.

(2) “first transition time” and “second transition time”

Additionally, Independent claim 1 further requires “a first transition time” and “a second transition time”:

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage.

Ex. 1001, 7:34–39.

Relying on its annotated Figure 6.54 of Stratakos (reproduced below), Petitioner contends that Stratakos teaches a tracking transition where the x-axis shows a time unit of approximately $1\text{ }\mu\text{s}$ and the y-axis shows a voltage unit of 0.4 V . Pet. 34.

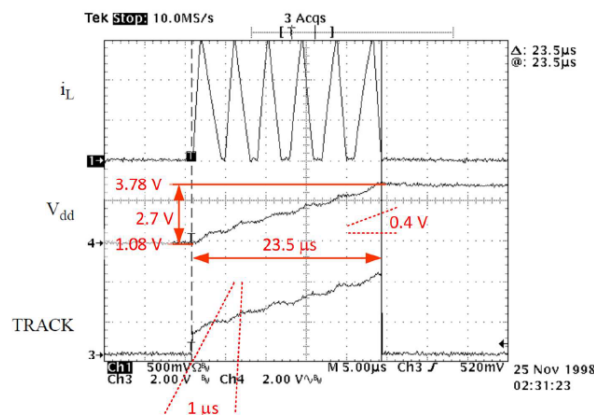
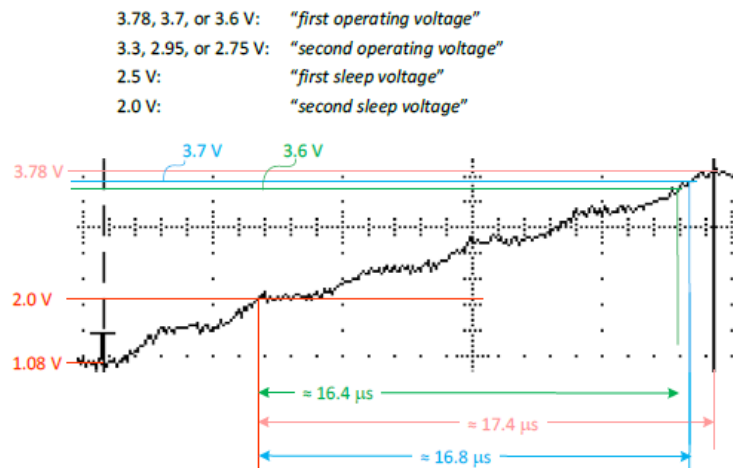


Fig. 6.54: A 5 MHz to 100 MHz tracking transition.

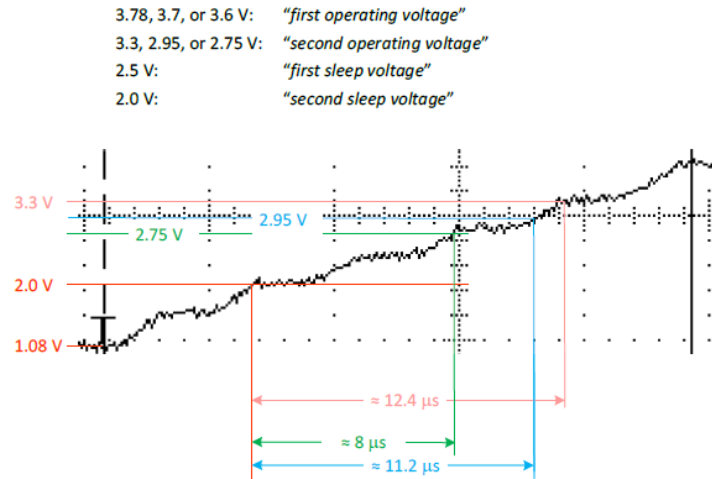
Annotated Figure 6.54 from page 34 of the Petition showing time versus voltage. *Id.* According to Petitioner, the annotated figure shows that the transition period from 1.08 V to 3.78 V (voltage operation range for Stratakos’s DVS converter) is $23.5\text{ }\mu\text{s}$. *Id.*

On page 35 of the Petition, Petitioner provides another annotated version of a portion of Figure 6.54 (reproduced below) that purports to show the transition time from a sleep voltage 2.0 V to a first operating voltage 3.78 V. Pet. 35.



Petitioner's annotated Figure 6.54 on page 35 of the Petition. *Id.* Petitioner asserts that the first transition time is 16.8 or 16.4 μs . *Id.* (citing Ex. 1002 ¶¶ 238–239).

And, in yet another annotated version of Figure 6.54 (reproduced below), Petitioner asserts that the time for voltage transition from 2.0 V (sleep voltage) to 3.3 V (second operating voltage) is approximately 12.4 μs , which is the "second transition time." *Id.* at 36. Alternatively, Petitioner asserts that if 2.95 or 2.75 V is selected as the "second operating voltage," the corresponding "second transition time" is 11.2 or 8 μs . *Id.* at 37 (citing Ex. 1002 ¶¶ 242–243).



Petitioner's annotated Figure 6.54 on page 37 of the Petition. Pet. 37.

Based on the voltages that Petitioner has picked, Petitioner asserts that the first transition time is 16.8 or 16.4 μs and the second transition time is 8, 11.2, or 12.4 μs . See Pet. 35, 37.

(3) "allowed time"

Independent claim 1 further defines an "allowed time" and the "first transition time" and "second transition time" relative to the "allowed time":

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

Ex. 1001, 7:34–44.

Petitioner contends that the limitation "allowed time for transitioning from a sleep state to an operating state" recited in claim 1 is "undefined and indeterminate." Pet. 41.

Alternatively, Petitioner asserts that "allowed time" is akin to latency. In particular, Petitioner argues that

a POSITA would have known that it would take a processor a certain amount of time to transition from a sleep state to an

operating state, described as the “*exit latency*” in the Advanced Configuration and Power Interface Specification standard (the “ACPI”). A POSITA would have known further that a *maximum exit latency* can be based on one or more system parameters such as, *e.g.*, a worst case interrupt latency, a maximum memory write latency, *etc.*, so that the system operation is not unreasonably delayed waiting for the processor to wake up from a sleep state.

Pet. 42 (citing Ex. 1002 ¶¶ 263–264; Ex. 1006, 69 (Fig. 4-13 (depicting a processor transitioning from a C3 (sleep) state to C0 (operating) state in response to an interrupt)) (emphasis added)).

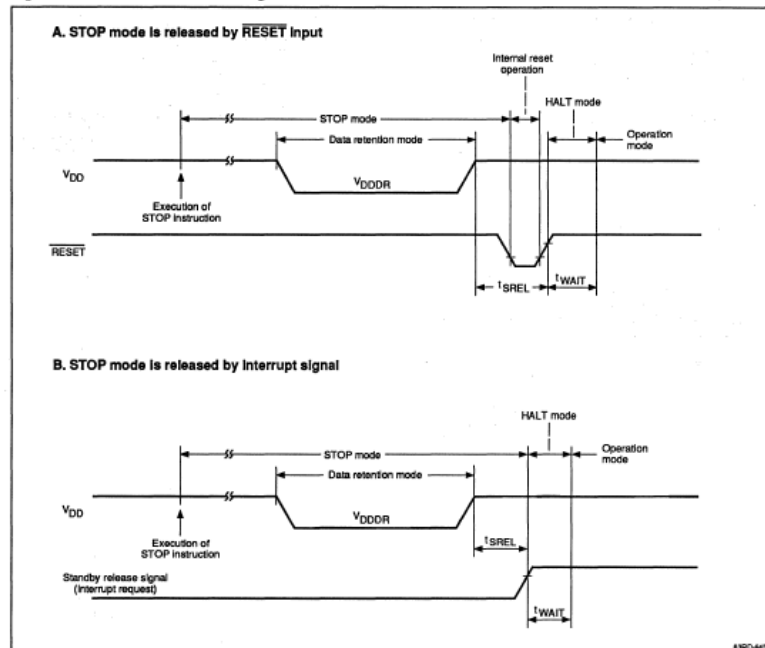
Based on NEC-Databook’s example systems (*e.g.*, μ PD751xx and μ PD7821x family computers), Petitioner contends that “a POSITA would have considered **15 μ s** as one example of maximum exit latency for sleep to operating state transition, *i.e.*, an ‘allowed time,’ *e.g.*, for a μ PD751xx family microcomputer used for real-time processing or as a PCI-connected component.” Pet. 44 (citing Ex. 1002 ¶¶ 272, 275).

Petitioner further contends that Stratakos discloses a “second transition time” of approximately 12.4 μ s from 2.0 to 3.3 V, which is less than 15 μ s and, thus “within [the] allowed time for transitioning from a sleep state to an operating state.” *Id.* (citing Ex. 1002 ¶ 280). Petitioner asserts that NEC-Databook teaches the data retention mode can be released by raising V_{DD} to the operating range and then releasing the STOP mode by any interrupt signal. Pet. 37 (citing Ex. 1004, 47 (Fig. 10), 65 (Fig. 19B); Ex. 1002 ¶¶ 244, 246). Petitioner refers to NEC-Databook’s Figure 19B, reproduced below.

μPD751xx/75P1xx

NEC

Figure 19. Data Retention Timing



NEC-Databook's Figures 19A–B show a data retention mode, a STOP mode released by a RESET or an interrupt signal, t_{SREL} (release signal time), and t_{WAIT} in HALT mode. Ex. 1004, 65.

According to Petitioner, NEC-Databook teaches that t_{SREL} can be 0 μ s. Pet. 38 (citing Ex. 1004, 326). For t_{WAIT} , Petitioner argues that a POSITA would have modified NEC-Databook's μPD751xx-CPU to utilize an external clock according to other microcomputers that NEC-Databook discloses. *Id.* Specifically, Petitioner contends that μPD7527A and μPD7821x microcomputers transition to/from the STOP and data retention modes while using an external clock. *Id.* (citing Ex. 1002 ¶¶ 247–249). Petitioner argues that when an external clock is used, no time is required for the system oscillator to stabilize and “a transition to the operating mode from Data Retention/STOP mode can occur as soon as the voltage transition from V_{DDDR} to V_{DD} is completed.” Pet. 38. Petitioner argues that because

μ PD7527A and μ PD7821x microcomputers use an external clock, the transition period is the time from Data Retention mode to the operating mode as soon as the voltage transition V_{DDDR} to V_{DD} is completed. *See* Pet. 39–40.

Petitioner acknowledges that NEC-Databook’s μ PD751xx-CPU cannot enter STOP mode (and hence, Data Retention mode) while using an external clock. Pet. 40–41 (citing Ex. 1004, 55 (Fig. 15B (stating “[w]hen the input is an external clock, the stop mode cannot be set”))). Yet, Petitioner argues there’s no restriction on the μ PD7527A and μ PD7821x microcomputers’ use of an external clock. Pet. 41. That being the case, Petitioner contends that, despite NEC-Databook’s teaching otherwise:

a POSITA would have understood that a *μ PD751xx-CPU configured according to a μ PD7821x microcomputer may enter the STOP and Data retention modes while using an external clock*, as μ PD7527A can, and that such a μ PD751xx-CPU, may immediately transition to the operating mode, without delay, when the CPU voltage is raised from V_{DD} to V_{DDDR} .

Pet. 41 (citing Ex. 1002 ¶¶ 257–260) (emphasis added).

Next, Petitioner contends that its selected “first transition time” of approximately 17.4 μ s is greater than greater than Petitioner’s selected “allowed time” of 15 μ s. Pet. 45 (citing Ex. 1002 ¶ 283; Ex. 1005, 210 (Fig. 6.54)).

b) Patent Owner’s Contentions

Patent Owner makes several arguments. Among these, Patent Owner points out that Petitioner’s setting of t_{WAIT} to 0 directly contradicts NEC-Databook’s teachings. Specifically, Patent Owner asserts that “For the μ PD751xx microcomputer, NEC-Databook does state a minimum t_{SREL} of 0 s, but it does not state a minimum t_{WAIT} . (Ex. 1004 at 64). However, it

describes typical t_{WAIT} as varying from a low of *1.95 ms to a high of 250 ms*. (Ex. 1004 at 64).” Prelim. Resp. 37 (emphasis added). Patent Owner further notes that while Petitioner asserts the μ PD751xx microcomputer could be modified with an external clock to render $t_{WAIT} = 0$, the reference expressly contradicts this modification. Specifically, Patent Owner argues that

[d]irectly contradicting Petitioner’s assertion, however, is NEC-Databook’s explicit statement that when an external clock is used with the μ PD751xx, it cannot be transitioned into STOP or Data Retention modes. (Ex. 1004 at 55). Recognizing the flaw in its position, Petitioner points to different microcomputers (namely, the μ PD7527A and μ PD7821x models), which Petitioner contends may enter the STOP and Data retention modes while using an external clock. (Paper No. 1 at 38-39).

Id. at 37. Patent Owner adds that neither “Ppetitioner nor its expert even attempt to explain how a POSITA could have modified the μ PD751xx microcomputer to overcome the external clock limitation expressly imposed by its manufacturer.” *Id.* at 38.

Furthermore, Patent Owner argues that “Ppetitioner fails to show that connecting the μ PD751xx microcomputer of NEC-Databook to Stratakos would result in Petitioner’s arbitrary “example” allowed time of 15 μ s.” *Id.* at 29. Patent Owner adds that Petitioner’s “arbitrary selection of 15 μ s does not come close to establishing this as an allowed time of any NEC-Databook processor.” *Id.* at 34. According to Patent Owner, none of the references cited for specific exit latency times mention a NEC-Databook processor or an exit latency time for any such processor. *Id.*

c) *Discussion*

- (1) “*wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state*”

As Petitioner notes, independent claim 1 requires “said second transition time is within an allowed time for transitioning from a sleep state to an operating state.” Ex. 1001, 7:40–42. In this regard, we observe that Petitioner selects 12.4 μ s as part of the “second transition time” based on the voltage tracking figure shown in Stratakos’s Figure 6.54. *See* Pet. 44. Petitioner further acknowledges that Stratakos’s Figure 6.54 does not take into account the delays times experienced by NEC-Databook’s μ PD751xx microcomputer when it exits STOP mode. *See* Pet. 38. When releasing the STOP mode, Dr. Alpert testifies “[NEC-Databook’s] Figure 19B depicts that after the CPU voltage is raised from V_{DDDR} to V_{DD} , two delays, indicated by t_{SREL} and t_{WAIT} may be incurred before the μ PD751xx-CPU transitions to the operating mode.” Ex. 1002 ¶ 248 (citing Ex. 1004, 65, Fig. 19B).

With respect to these two delays, NEC-Databook teaches a minimum t_{SREL} release signal set time of 0, but does not teach a minimum t_{WAIT} time. Ex. 1004, 64. Dr. Alpert notes that “the delay t_{WAIT} must be *at least 1.95 ms*, presupposing the use of the 4.19 MHz crystal for clock generation.” Ex. 1002 ¶ 248 (citing Ex. 1004, 64) (emphasis added). Dr. Alpert explains that in the STOP mode, the main system clock oscillator is stopped and must be started and stabilized before resuming CPU operation. *Id.* According to Petitioner’s and Dr. Alpert’s theory, the “second transition time” recited in claim 1 would include both the 12.4 μ s and any delay time, including t_{WAIT} , which by Dr. Alpert’s admission is at least 1.95 ms. *See* Ex. 1002 ¶ 248.

Therein lies the problem, NEC-Databook teaches t_{WAIT} delays in milliseconds, which are orders of magnitude greater than the **15 μ s** that Petitioner relies upon for the “allowed time.” *See* Pet. 44. Thus, a “second transition time” in milliseconds would not be “within an allowed time for

transitioning from a sleep state to an operating state” per Petitioner’s own selection of voltages and transition times.

To sidestep this problem, Petitioner attempts to remove the t_{WAIT} delay by modifying NEC-Databook’s $\mu\text{PD751xx}$ microcomputer with an external clock. According to Petitioner, NEC-Databook’s other microcomputers $\mu\text{PD7527A}$ and $\mu\text{PD7821x}$ use external clocks where “no time is needed for the system oscillator to stabilize and, as such, a transition to the operating mode from Data Retention/STOP mode can occur as soon as the voltage transition from V_{DDDR} to V_{DD} is completed.” Pet. 38 (citing Ex. 1002 ¶¶ 247–249).

Petitioner is correct that $\mu\text{PD7527A}$ and $\mu\text{PD7821x}$ use external clocks with STOP mode. Moreover, Petitioner is correct that NEC-Databook contemplates the possibility of using an external clock with the $\mu\text{PD751xx}$ microcomputer. *See* Ex. 1004, 55. However, NEC-Databook also explicitly states that “[w]hen the input is an external clock, *the stop mode cannot be set because the X1 pin is connected to System ground (V_{ss})*.” *Id.* In other words, when using an external clock, the $\mu\text{PD751xx}$ microcomputer cannot enter STOP mode, which is also the mode in which the $\mu\text{PD751xx}$ microcomputer enters Data Retention Mode. Dr. Alpert’s testimony agrees with our understanding of NEC-Databook. He testifies that “since the data retention mode is entered by lowering V_{DD} after entering the STOP mode, (*see id.* at 47), the $\mu\text{PD751xx/P1xx}$ microcomputers are not specified to support data retention mode when an external clock is used.” Ex. 1002 ¶ 250.

Dr. Alpert contends that a POSITA would look to the other computers, $\mu\text{PD7527A}$ and $\mu\text{PD7821x}$, that use external clocks with STOP mode in NEC-Databook to modify $\mu\text{PD751xx}$ to avoid t_{WAIT} delays. *See* Ex.

1002 ¶¶ 253–260. But even here, Petitioner runs into trouble. Despite relying on the features of μ PD7527A, Dr. Alpert concedes that the external clock configuration for μ PD7527A microcomputers is not the same as the external clock configuration of the μ PD751xx microcomputers. Ex. 1002 ¶ 254 (citing Ex. 1004, 21, 55). Indeed, this is not a surprise because NEC-Databook teaches that one microcomputer is designed to work with an external clock with STOP mode while the other isn't. *See* Ex. 1004, 55.

To fix this, Dr. Alpert then relies on the external clock configuration of μ PD7821x and asserts that μ PD7821x and μ PD751xx share a similar configuration. Ex. 1002 ¶ 254. However, Dr. Alpert also observes that the μ PD7821x has a Data Retention Mode voltage of 2.5 V that is different from the 2.0 V of μ PD751xx, and that μ PD7821x has a *minimum V_{DD} rise time of 200 μ s*. *Id.* ¶ 255.

As such, when Petitioner and Dr. Alpert attempt to modify μ PD751xx with two other microcomputers, they acknowledge but do not adequately explain how to address these differences. In particular, μ PD751xx/P1xx expressly teaches t_{WAIT} in milliseconds and that use of an external clock prevents the use of STOP and Data Retention modes. Ex. 1004, 64. The μ PD7527A microcomputer employs an external clock, STOP and Data Retention modes, and a minimum delay of 0 μ s. *Id.* at 21. However, the μ PD7527A's external clock configuration is different from the μ PD751xx/P1xx, which Dr. Alpert acknowledges requires modification by looking to a third microcomputer. Ex. 1002 ¶ 254. The μ PD7821x microcomputer has an external clock, STOP and Data Retention modes, a data retention voltage of 2.5 V, and a minimum V_{DD} rise time of 200 μ s. Ex. 1004, 105.

With regard to these differences, Dr. Alpert concludes that a POSITA would have understood that

a μ PD751xx-CPU configured according to a μ PD7821x microcomputer may enter the STOP and Data retention modes, with a different data retention voltage from that of a μ PD7821x microcomputer, i.e., a minimum V_{DDDR} of 2.0 V (see Ex.1004 at 32, col. 1, 47, col. 2), while using an external clock, as μ PD7527A can. In light of the timing characteristics of the μ PD7527A microcomputer discussed above, which do not include a minimum V_{DD} rise time, a POSITA would have also understood that for a μ PD751xx-CPU, no delay would be required to activate the standby release signal after the transition from V_{DDDR} to V_{DD} is complete. A POSITA would have further understood that, accordingly, the transition from the data retention mode to the operating mode need not be delayed by the time period for clock stabilization t_{WAIT} , and can occur immediately upon the activation of the standby release signal in response to an interrupt request.

Ex. 1002 ¶ 257. Essentially, Dr. Alpert concludes that a POSITA would have understood how to combine and modify the disparate features of three microsystems to reach the claimed limitations. However, given the differences disclosed by each of the microsystems, we observe that Dr. Alpert's testimony is conclusory and largely dismisses or discounts NEC-Databook's express teaching that the μ PD751xx-CPU cannot enter Data Retention Mode when using an external clock, and moreover, enters that mode at different voltages from μ PD7821x. Likewise, Dr. Alpert does not explain why or how the minimum V_{DD} rise time of 200 μ s from the μ PD7821x microcomputer can be avoided based on the configuration of the μ PD7527A microcomputer, which Dr. Alpert acknowledges is different from the μ PD751xx-CPU. *Id.* ¶ 254 ("Even though the external clock configuration of the μ PD7527A microcomputer is not the same as that of the μ PD751xx-CPU . . . NEC-Databook discloses a μ PD7821x microcomputer .

. . that employs an external clock in a similar manner as the μ PD751xx-CPU does.”).

In short, Dr. Alpert asserts, but does not explain sufficiently why or how, the μ PD751xx/P1xx configured according to a μ PD7821x and μ PD7527A microcomputers “may enter the STOP and Data retention modes, with a *different data retention voltage from that of a μ PD7821x microcomputer*, i.e., a minimum V_{DDDR} of 2.0 V. . . while using an external clock, as μ PD7527A can.” Ex. 1002 ¶ 257 (citing Ex. 1004, 32, 47). In the same way, Petitioner’s reliance on Dr. Alpert’s testimony suffers from a failure to explain with particularity how or why a POSITA would modify μ PD751xx-CPU to use an external clock to eliminate t_{WAIT} for Petitioner’s selected “second transition time” of 12.4 μ s. See Pet. 37–41. For this reason alone, the Petition is deficient.⁵

Generally, bare conclusory statements in the Petition are deficient—lacking sufficient analysis and evidence, and fail to comply with 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a)(2). Under 35 U.S.C. § 312(a)(3), a petition must “identif[y], in writing and *with particularity*, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim” (emphasis added). Similarly, 37 C.F.R. § 42.22(a)(2) requires each petition to include “[a] *full statement of the reasons* for the relief requested, including a *detailed explanation* of the significance of the evidence

⁵ Dr. Alpert asserts that a POSITA would understand there to be power and time savings from the proposed modification. Ex. 1002 ¶¶ 258–260. Nonetheless, Petitioner has not explained why a POSITA would have had reason to modify the μ PD751xx-CPU microcomputer specifically when the μ PD7527A and μ PD7821x presumably already employed these features—external clock and no delay time.

including material facts, and the governing law, rules, and precedent” (emphases added).

(2) “*wherein said first transition time is greater than said allowed time.*”

Additionally, we are not persuaded Petitioner has adequately explained how its asserted combination teaches or suggests the limitation “wherein said first transition time is greater than said allowed time” recited in independent claim 1.

Petitioner acknowledges in the Petition that there are several choices for “first operating voltage,” “second operating voltage,” and “sleep voltage.” *See* Pet. 28 (“POSITA would have understood that in Data Retention mode, any voltage in the range of 2.0 to 2.69 V is a sleep voltage.”), 30 (“Stratakos discloses a DVS converter that can supply regulated voltages in the range 1.08-3.78 V.”), 31 (“Other voltages, such as 3.7 V, 3.6 V, can also be selected as the ‘first operating voltage.’)), 32 (“Other voltages, such as 2.95 V, 2.75 V, can also be selected as the ‘second operating voltage.’”). Moreover, according to Petitioner, selection of specific voltages determines the “first transition time” and “second transition time.” *See* Pet. 37 (Petitioner’s annotated Fig. 6.54 from Stratakos).

Similarly, Petitioner asserts that a POSITA could select an “allowed time.” Petitioner states “a POSITA would have considered 15 μ s as one example maximum exit latency for sleep to operating state transition, i.e., an ‘allowed time,’ e.g., for a μ PD751xx family microcomputer used for real-time processing or as a PCI-connected component.” Pet. 44 (citing Ex.1002 ¶¶ 272, 275).

Because of the number of choices (as Petitioner has acknowledged), the question then is why a POSITA would choose a “first transition time” that is “greater than said allowed time.” In choosing an “allowed time” of

15 μ s, Dr. Alpert testifies on the importance of operating within exit latency.

He states:

Regardless, before 2000, a POSITA would have known that it would take a processor a certain amount of time to transition from a sleep state to an operating state, described as the “exit latency” in the Advanced Configuration and Power Interface Specification (the “ACPI”), an industry standard that was widely adopted before 2000. (*See* Ex.1006 at 69.) *A POSITA would have further understood a maximum exit latency as a system design parameter.* The reason is, while a POSITA would have understood that to achieve the benefit of power and/or energy saving some delay incurred as the processor transitions between sleep and operating states may be tolerated, *the delay should not be excessive because, otherwise, the completion of the computing tasks designated to the processor would be unreasonably delayed.*

Ex. 1002 ¶ 263 (emphasis added). Dr. Alpert further cautions that “a POSITA would have known that the time taken for state transitions between sleep and operating states of a processor *should not exceed a specified maximum exit latency*, i.e., the transition should occur ‘within an allowed time.’” *Id.* (emphasis added). In paragraph 344 of his declaration,

Dr. Alpert reiterates that

to facilitate saving of power/energy, *the transition should occur within a maximum exit latency determined by parameter(s) of the overall system* (such as interrupt latency, memory write time, etc.) and/or the intended system use, i.e., within an allowed time, so as not to delay excessively the processing of events such as interrupt handling, attending to memory write requests, etc.

Id. ¶ 344 (emphasis added).

Though Dr. Alpert testifies as to the purported importance of operating within the maximum exit latency, e.g., “allowed time,” neither Petitioner nor Dr. Alpert explains why a POSITA would have selected a “first transition time” that is “greater than said allowed time.” Instead, for

this limitation, Petitioner asserts that “[t]he DVS converter (circuitry) that Stratakos describes transitions from 2.0 V (the sleep voltage) to 3.78 V (the first operating voltage)” that is approximately 17.4 μ s (i.e., “first transition time”) which “‘is greater than said allowed time’ of 15 μ s.” Pet. 44 (citing Ex.1002 ¶ 283; Ex. 1005, 210 (Fig. 6.54)).

On pages 106 through 108 of the Petition, Petitioner articulates several reasons why a POSITA would modify NEC-Databook’s μ PD751xx microcomputer to include Stratakos’s DVS converter. For example, Petitioner asserts that “a POSITA would have recognized that since NEC-Databook does not explicitly describe a voltage regulator, Stratakos’s DVS converter can be readily used to supply different sleep and operating voltages to the μ PD751xx-CPU, to facilitate energy/power saving contemplated by both.” Pet. 107 (citing Ex. 1002 ¶¶ 171–174). Petitioner adds that “this combination would have been nothing more than combining prior art elements according to known methods (coupling a power supply or a voltage regulator to a processor), or simple substitution of one known element for another.” *Id.* (citing Ex. 1002 ¶ 175). Further, Petitioner contends that

[a] POSITA would have also understood this combination to be the use of a known technique (dynamic adjustment of processor voltages and frequencies) to improve a system employing a similar technique (the μ PD751xx family microcomputer) in the same way as Stratakos describes, or applying a known technique (described above) to a known system (NEC-Databook’s) that is ready for improvement, *e.g.*, by using a dynamically adjustable voltage regulator, to yield predictable results described above. (Ex.1002, ¶176.)

Additionally, a POSITA would have understood that these predictable, beneficial results can be obtained without requiring substantial changes or modifications to either the μ PD751xx

family microcomputer or Stratakos's DVS controller, and without adversely affecting the operation of these systems or components. (*Id.*, ¶177.) A POSITA would have also been able to apply known, conventional circuitry configuration techniques to perform the necessary modifications. Accordingly, a POSITA would have expected the combination of NEC-Databook and Stratakos to succeed.

Pet. 108.

If we were to agree with Petitioner that a POSITA would have reason to combine Stratakos's DVS converter with NEC-Databook's microcomputers, we still lack Petitioner's explanation for why a POSITA would select specific voltages to result in a "first transition time" that is greater than the "allowed time." Even if prior art references disclose all of the limitations in a claim when combined, there must be evidence to explain why a person of ordinary skill in the art would have combined the references to arrive at the claimed invention. *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (citing *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (holding that post-KSR "some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]")). A precise teaching directed to the specific subject matter of a challenged claim is not necessary to establish obviousness. *KSR*, 550 U.S. at 418. Rather, "any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.* at 420. Accordingly, Petitioner must show that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a

reasonable expectation of success in doing so.” *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (internal quotations and citations omitted).

Here, Dr. Alpert testifies as to the importance of remaining within a maximum exit latency, which he and Petitioner analogize to “allowed time,” but Dr. Alpert does not explain why a POSITA would disregard that general understanding of maximum exit latency to select a voltage that would give a transition time greater than the “allowed time.”

Accordingly, for the reasons discussed above, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing on the challenge to claim 1 as having been obvious over NEC-Databook, Stratakos, and POSITA’s knowledge.

4. *Analysis of Dependent Claims 2–6*

Claims 2–6 depend from claim 1 and require:

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

See Ex. 1001, 7:34–44.

For these shared limitations, Petitioner applies the same arguments and evidence discussed above with respect to claim 1. *See* Pet. 47 (“the maximum exit latency for the μ PD751xx-CPU would be based on the worst-case interrupt latency for a μ PD7821x family microcomputer configured as a non-networked real-time system, or on the maximum memory write completion time for a μ PD7821x family microcomputer configured as a PCI-based component.”), 48 (“[A]s discussed for Element 1[d.1] and claim 2, the example maximum exit latency (allowed time) of 15 μ s is based on a

worst case interrupt latency of a μ PD751xx family microcomputer configured as a non-networked realtime system, and/or the maximum completion time for memory write operations (MCT) of a μ PD751xx family microcomputer used in a PCI-based system.”), 49–53.

For the same reasons discussed with respect to claim 1, Petitioner has not demonstrated a reasonable likelihood of prevailing on the challenge to claims 2–6 based on the proposed combination of NEC-Databook, Stratakos, and POSITA’s knowledge.

5. *Analysis of Independent Claim 7*

Independent claim 7 is directed to a method of operating a computer system that includes the step:

transitioning from said providing said first operating voltage to said computer processor to providing a second operating voltage to said computer processor, wherein *a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.*

Ex. 1001, 7:66–8:5 (emphasis added).

For these limitations, Petitioner relies on the arguments presented for claim 1. *See* Pet. 67 (“As discussed for Elements 1[c.1] and 1[d.2], the time required to transition from providing 2.0 V (sleep voltage) to providing 3.78 V (second operating voltage) is approximately 17.4 μ s, which is greater than the maximum exit latency based on system parameters of 15 μ s (the allowed time for transitioning from said sleep state to said operating state.)”).

Accordingly, for the reasons discussed with respect to claim 1, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 7 is unpatentable under 35 U.S.C. § 103

as obvious over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

6. *Analysis of Dependent Claims 8–10*

Claims 8–10 depend from independent claim 7. Accordingly, for the reasons discussed with respect to claims 1 and 7, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 8–10 are unpatentable under 35 U.S.C. § 103 over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

7. *Analysis of Independent Claim 11*

Independent claim 11 is directed to a computer system that includes an adjustable voltage supply, “wherein said adjustable voltage supply is configured to generate a *voltage transition from said second sleep voltage to said first operating voltage in a time period greater than a time period allowed for transition from a sleep state to an operating state of said computer system.*” Ex. 1001, 8:30–36 (emphasis added).

For these limitations, Petitioner relies on the same arguments discussed above with respect to claim 1. Pet. 81 (“As discussed for Elements 1[c.1], 1[d.2], and 7[d], the DVS converter that Stratakos discloses transitions from supplying 2.0 V to supplying 3.78 V in approximately 17.4 μ s.”), 81–82 (“[A]s discussed for Element 1[d.1], a POSITA would have known that for the processors and computer systems that were available and in use around and before 2000, 15 μ s was an maximum latency for a processor to transition from a sleep state to an operating state. (Ex.1002, ¶406.) “Since the time required for a transition from 2.0 V (second sleep voltage) to 3.78 V (first operating voltage) of 17.4 μ s is greater than 15 μ s, Stratakos in view of the knowledge of a POSITA teaches this Element.”).

Accordingly, for the reasons discussed with respect to claim 1, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 11 is unpatentable under 35 U.S.C. § 103 as obvious over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

8. *Analysis of Dependent Claims 12–14*

Claims 12–14 depend from independent claim 11. Accordingly, for the reasons discussed with respect to claim 11, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 12–14 are unpatentable under 35 U.S.C. § 103 over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

9. *Analysis of Independent Claim 15*

Independent claim 15 is directed to a computer system that recites: “a voltage transition from said second sleep voltage to said first operating voltage is greater than a time allowed for transition from a sleep state to an operating state of said computer system.” Ex. 1001, 8:61–64.

For these limitations, Petitioner relies on arguments presented for claim 11, which also rely on arguments presented for independent claim 1 discussed above. *See* Pet. 91.

Accordingly, for the reasons discussed with respect to claims 1 and 11, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 15 is unpatentable under 35 U.S.C. § 103 as obvious over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

10. Analysis of Dependent Claims 16 and 17

Claims 16 and 17 depend from independent claim 15. Accordingly, for the reasons discussed with respect to claim 15, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 16 and 17 are unpatentable under 35 U.S.C. § 103 over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

11. Analysis of Independent Claim 18

Independent claim 18 is directed to a computer system in which a “means for supplying a voltage comprises means to generate a voltage transition from said second sleep voltage to said first operating voltage *in a time period greater than a time period allowed for transition from a sleep state to an operating state of said computer system.*” Ex. 1001, 9:19–10:3. (emphasis added).

For these limitations, Petitioner argues that

[a]s discussed for Element 11[c], Stratakos's DVS converter can provide a “second sleep voltage” of 2.0 V and a “first operating voltage” of 3.78 V, so that a “transition from said second sleep voltage to said first operating voltage” would occur in approximately 17.4 μ s, i.e., “in a time period greater than” 15 μ s, e.g., “a time period allowed for transition.”

Pet. 103–104.

Accordingly, for the reasons discussed with respect to claims 1 and 11, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 18 is unpatentable under 35 U.S.C. § 103 as obvious over the proposed combination of NEC-Databook, Stratakos, and POSITA's knowledge.

12. Analysis of Dependent Claims 19–21

Claims 19–21 depend from independent claim 18. Accordingly, for the reasons discussed with respect to claim 18 we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 19–21 are unpatentable under 35 U.S.C. § 103 over the proposed combination of NEC-Databook, Stratakos, and POSITA’s knowledge.

III. CONCLUSION

For the above reasons, we determine Petitioner has not established a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim of the ’404 patent. Therefore, we deny institution of review on the merits. *See* 35 U.S.C. § 314(a). We do not reach Patent Owner’s arguments that we should exercise discretion under 35 U.S.C. § 314(a) to deny the Petition.

IV. ORDER

Upon consideration of the record before us, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), the institution of an *inter partes* review of claims 1–21 of U.S. Patent No. 7,870,404 B2 is denied.

IPR2021-01265
Patent 7,870,404 B2

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