

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

FUTURE LINK SYSTEMS, LLC,
Patent Owner.

IPR2021-01301
Patent 6,622,108 B2

Before KARL D. EASTHOM, KEVIN C. TROCK, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–4, 6–8 and 10–13 of 6,622,108 (Ex. 1001, the “’108 Patent”). Future Link Systems, LLC (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Thereafter, pursuant to Board authorization (Ex. 1017), the parties filed supplemental briefing, a Preliminary Reply by Petitioner (Paper 7, “Pet. Prelim. Reply”), and a Preliminary Sur-reply by Patent Owner (Paper 8, “PO Prelim. Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. See 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2020). To institute an *inter partes* review, we must determine that the information presented in the Petition shows “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons set forth below, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim. Accordingly, we institute an *inter partes* review of the ’108 patent.

II. BACKGROUND

A. *Real Parties in Interest*

The parties identify themselves as real parties in interest. Pet. 1; Paper 4, 1. Petitioner also identifies ATI Technologies ULC as a real party in interest. Pet. 1.

B. *Related Matters*

The parties identify the following proceedings as related matters involving the ’108 patent: *Future Link Systems, LLC v. Advanced Micro Devices, Inc.*, No. 6:20-01176-ADA (W.D. Tex.) (the “Waco District

Court”); *Future Link Systems, LLC v. Apple Inc.*, No. 6:21-cv-00263-ADA (W.D. Tex.); and *Intel Corp. v. Future Link Systems, LLC*, No. 14-377-LPS (D. Del.) (the “Delaware District Court”). Pet. 1; Paper 4, 1.

The Texas Waco District Court recently transferred the case to its sister court in Austin. See Ex. 1019, 1; *Future Link Systems, LLC v. Advanced Micro Devices, Inc.*, No. 6:20-01176-RP (W.D. Tex.) (the “Austin District Court”).

C. The '108 Patent

The '108 patent discloses systems and methods for testing interconnects of electronic circuits. Ex. 1001, code (57). The '108 patent describes using a test unit operated as a low complexity memory as part of a first electronic circuit for testing the interconnects between that first circuit and a second electronic circuit. *Id.* at 5:4–8, 6:15–19. “Low complexity memories are those memories that do not have to be put through a complex initiali[z]ation process before they can be accessed, and that have simple access protocols without dynamic restrictions.” *Id.* at 2:35–38.

Examples of “[l]ow complexity memory types” include “Static Random Access Memories (SRAMs)” and “Programmable” Read Only Memories (“ROMs”). Ex. 1001, 4:61–62. These memory types “can readily be tested for their connectivity using neighbo[]ring circuits equipped with boundary-scan or neighbor[]ring microprocessors and/or ASICs.” *Id.* at 4:63–65. An example of high complexity memory is an SDRAM (synchronous dynamic random access memory). *Id.* at 3:61–4:2.

The '108 patent describes another embodiment for “the test unit being operable as a low complexity memory” as a “combinatorial circuit.” Ex. 1001, 3:37–43. In this embodiment, “it is not required that the test unit is implemented as a real ROM table. Especially if only a small number of

test patterns is used, the test unit could be implemented as a combinatorial circuit, leading to more efficient area usage.” *Id.* Examples of combinatorial circuits include circuits with XOR (exclusive or) or XNOR (exclusive nor) gates. *Id.* at 10:42–49, 13:12–19, Fig. 5 (2 XNOR gates), Fig. 6 (2 XOR gates).

Figure 4 of the '108 patent follows:

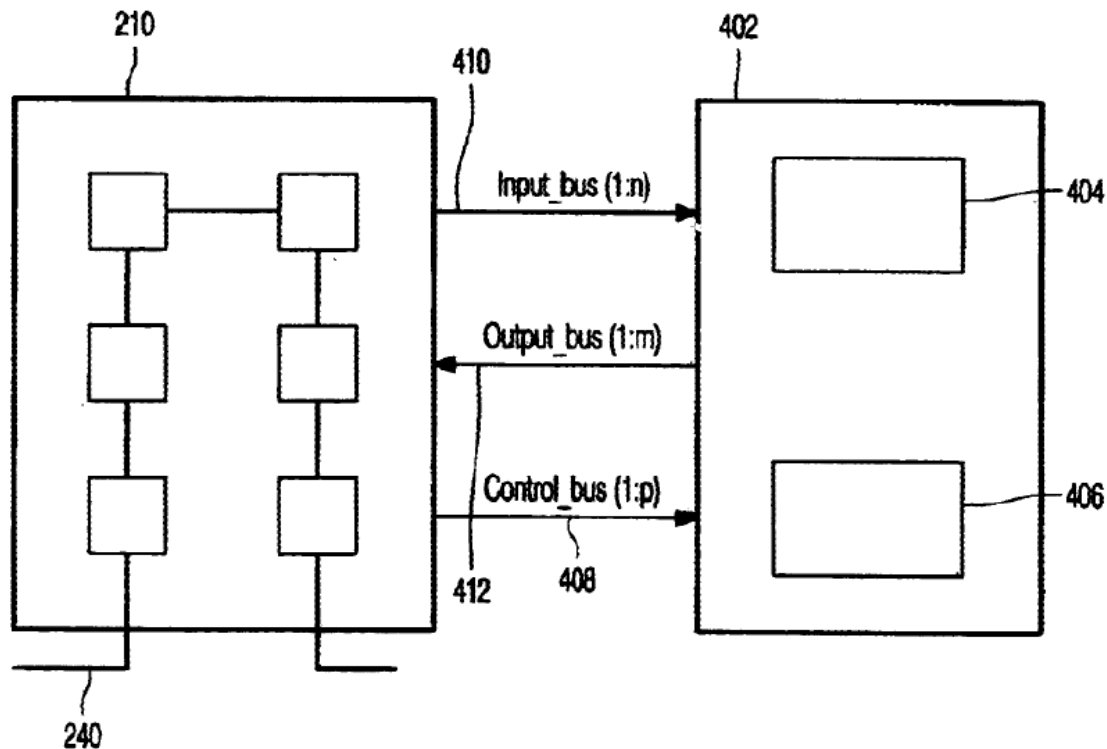


FIG. 4

Figure 4 above illustrates an embodiment for testing circuit 402's interconnects using boundary scan chain 240 of neighboring processor 210. Ex. 1001, 9:30–36. Circuit 402 includes main unit 404 and test unit 406. *Id.* at 9:30–31. Test unit 406 is a “combinatorial circuit” between input bus 410 and output bus 412 and “implements the functionality of a ROM table.” *Id.* at 10:8–9. “The main unit 404 is active in the normal operational mode of

the circuit and the test unit is active in the test mode of the circuit.” *Id.* at 9:33–35.

D. Illustrative Claim

Independent claim 1 follows:

1. An electronic circuit comprising:
a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,
a main unit for implementing a normal mode function of the electronic circuit, and
a test unit for testing the interconnects,
the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit,
such that in the test mode the test unit is operable as a low complexity memory via the I/O nodes.

E. Asserted Grounds of Unpatentability

Petitioner contends that claims 1–4, 6–8 and 10–13 are unpatentable as follows:¹

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. Because the ’108 patent’s effective filing date precedes the March 16, 2013, effective date of the applicable AIA amendments, the pre-AIA versions of §§ 102, 103 apply.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 8, 11–13	103(a)	Cuppens, ² Bhavsar ³
1, 3, 6–8, 10–11	102(b)	Hong ⁴
4	103(a)	Hong, Wakerly ⁵

Pet. 2–3. Petitioner supports its challenge with the Declaration of Dr. Donald Alpert (Ex. 1002).

III. ANALYSIS

A. *Legal Standards*

A “prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

² U.S. Pat. No. 4,862,418, issued Aug. 29, 1989 (Ex. 1005).

³ D.K. Bhavsar, *Testing interconnections to static RAMs*, IEEE (June 1991) (Ex. 1006).

⁴ U.S. Pat. No. 4,241,307, issued Dec. 23, 1980 (Ex. 1009).

⁵ John. F. Wakerly, *DIGITAL DESIGN, PRINCIPLES & PRACTICES* (2d. Ed. 1994) (Ex. 1011).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103; *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). “[W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.” *KSR*, 550 U.S. at 416 (citing *United States v. Adams*, 383 U.S. 39, 50–51 (1966)). The question of obviousness involves resolving underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Determining whether an invention would have been obvious under 35 U.S.C. § 103 requires resolving the level of ordinary skill in the pertinent art at the time of the effective filing date of the claimed invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The person of ordinary skill in the art is a hypothetical person who knows the relevant art. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors in determining the level of ordinary skill in the art include the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *Id.* One or more factors may predominate. *Id.*

Petitioner contends that a person having ordinary skill in the art (“POSITA”) “would have had a bachelor’s degree in electrical or computer engineering or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 7 (citing Ex. 1002 ¶ 21). Patent Owner does not dispute Petitioner’s proposed level of ordinary skill in the art in its Preliminary Response, nor does it propose a different level of skill.

Based on our review of the record, Petitioner’s stated level of ordinary skill in the art is reasonable because it is consistent with the evidence of record, including the asserted prior art. Accordingly, for the purposes of this Institution Decision, we adopt Petitioner’s definition.

C. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the district-court-type standard, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b). Under that standard, claim terms have their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. See *Phillips*, 415 F.3d at 1313–14. Any extrinsic evidence should be considered in the context of the intrinsic evidence. See *id.* at 1317–19.

Petitioner “interprets the ’108 [p]atent’s claims according to *Phillips*,” 415 F.3d at 1303, and notes that “certain terms of the ’108 [p]atent were previously construed in” the Delaware District Court. Pet. 8; see Ex. 1007 (Delaware District Court claim construction order). Petitioner asserts “it is not necessary to construe any claim terms to resolve the grounds presented

in this Petition,” because “the prior art discloses the claim limitations in a manner that closely tracks the ’108 [p]atent’s embodiments.” Pet. 9 (citing *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that only claim terms “that are in controversy” must be construed and “only to the extent necessary to resolve the controversy”)).

Claim 1 recites that “in the test mode the test unit is operable as a low complexity memory.” After the Petition was filed, the Waco District Court construed “low complexity memor[y]” under its “[p]lain-and-ordinary meaning wherein low complexity memories are those that do not have to be put through a complex initialization process before they can be accessed, and that have simple access protocols without dynamic restrictions.” Ex. 2001, 2. As Patent Owner points out, the Waco “District Court adopted the same construction” as the Delaware District Court. See Prelim. Resp. 6–7 (citing Ex. 1007, 3 (“**Low complexity memory**,’ as used in claims 1–13 of the ’108 patent, means ‘memory that does not have to be put through a complex initialization process before it can be accessed and that has simple access protocols without dynamic restrictions.’”)).

On this preliminary record, the ’108 patent specification provides some support for the Waco and Delaware District Courts’ constructions (which are materially the same), albeit as a lexicographic definition with negative limitations based on language in the specification.⁶ In particular, the specification states that “[l]ow complexity memories are those memories *that do not* have to be put through a complex initiali[z]ation process before

⁶ Unless otherwise noted, reference hereinafter is only to the Waco District Court’s claim construction because it is the most recent and it is materially similar to the Delaware District Court’s claim construction.

they can be accessed, and that have *simple access protocols without* dynamic restrictions.” Ex. 1001, 2:35–38 (emphasis added). See *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003) (A “negative limitation” must find support in “the words of the claim” or through an “express disclaimer or independent *lexicography in the written description* that would justify adding that negative limitation.”). In contrast to “low complexity memory,” the specification states that “[h]igh complexity memory devices are those devices which have *complex protocols* for reading from and writing into their memory array.” Ex. 1001, 3:61–63 (emphasis added).

The specification also provides examples of low complexity memories. For example, it states that “[l]ow complexity memory types like Static Random Access Memories (SRAMs) and (Programmable) ROMs can readily be tested for their connectivity using neighbo[]ring circuits equipped with boundary-scan or neighbo[]ring microprocessors and/or ASICs.” Ex. 1001, 4:61–65. As indicated above and as analyzed below, the Petition relies on disclosed SRAMs in Cuppens and Bhavsar to support one of its obviousness grounds (which addresses all of the challenged claims). See *infra* § III.E.3–4.

Patent Owner contends that “the Petition’s improper comparison of the prior art [SRAMs in Cuppens and Bhavsar] to the ’108 patent specification takes passages of the specification out of context.” Prelim. Resp. 8. According to Patent Owner,

[w]hile the patent specification passages cited indicate that some SRAMs are types of low complexity memories, it does not assert that all such memories meet the construction adopted by two District Courts (i.e., that all such memories “do not have to be put through a complex initialization process before they can be

accessed, and [] have simple access protocols without dynamic restrictions”).

Prelim. Resp. 9 (quoting Ex. 2001, 2 (Waco District Court claim construction)). Patent Owner also argues that “Petitioner’s approach is improper because a claim is applied based on the language of the claims as properly construed, not a comparison between the prior art and the embodiments of the challenged patent.” *Id.* at 8 (citing *Simmons v. Cook*, 701 F. Supp. 2d 965, 981 (S.D. Ohio 2010) (“In determining whether an accused device infringes, the accused device is to be compared with the language of the patent’s claims, not to the embodiments or specific examples provided in the patent.”); *Spectrum Intern., Inc. v. Sterilite Corp.*, 164 F.3d 1372 (Fed. Cir. 1998)).

At this preliminary stage, contrary to Patent Owner’s arguments, Petitioner’s approach is not improper. Petitioner reads the disputed limitation onto prior art SRAMs based on the specification’s example of a SRAM as low complexity memory, adopts the *Phillips* standard, and cites to the Delaware District Court claim construction order. *See* Pet. 8 (citing Ex. 1016); *infra* § III.E.3 (reading the limitation on prior art SRAMs). The cases relied upon by Patent Owner, *Simmons* and *Spectrum*, relate to infringement, which is not at issue here. *See* Prelim. Resp. 8. Contrary to Patent Owner’s other argument that the specification only describes *some* SRAMs as examples low complexity memory, on this preliminary record, the specification simply describes “[l]ow complexity memory types like Static Random Access Memories [SRAMs]” without limitation. *See* Prelim. Resp. 8; Ex. 1001, 4:61–62.

To support its argument, Patent Owner contends that “Petitioner itself acknowledges that the complexity of various SRAM devices varies

significantly, implying that SRAMs are not categorically ‘low complexity’ under the District Court construction.” Prelim. Resp. 9. According to Patent Owner, “Petitioner represented to the [Waco District Court] that ‘static random access memory (“SRAM”) products could be viewed by a POSA as possessing varying degrees of complexity.’” *Id.* (quoting Ex. 2002, 3 (alleging Petitioner cites to data sheets of different SRAM products “with varying degrees of complexity”)). This line of argument does not address the intrinsic evidence of the ’108 patent specification as discussed above. In addition, contrary to this line of argument, the record does not show that Petitioner argued in the Waco District Court or here that SRAMs are not examples of “low complexity memory” as set forth in the ’108 patent. *See* Ex. 2002, 2–9 (arguing the term “low complexity memory” is indefinite); Pet. Prelim. Reply 2 (arguing that “the indefiniteness dispute has no impact on this proceeding because the Petition relies on prior art disclosing an embodiment of ‘low complexity memory’ from the specification”).

Accordingly, for purposes of institution on this preliminary record, SRAMs are examples of “low complexity memory.” Patent Owner will have the opportunity during trial to address why “low complexity memory” does not read on the prior art SRAMs relied upon in the Petition.

This potential claim construction issue may evolve in other respects. Patent Owner acknowledges “that in the parallel [Waco] District Court proceedings, Patent Owner proposed a different construction of this term as ‘a memory that has less complex initialization processes or access protocols than the main unit.’” Prelim. Resp. 7 n.1 (citing Ex. 2001, 2). Patent Owner signifies a potential disagreement with the Waco District Court’s claim construction, because, as noted, Patent Owner indicates it may advance the claim construction it proposed in the Waco District Court here. Prelim.

Resp. 7 n.1 (stating that it “does not waive its assertion of this construction in this proceeding”). Petitioner also disagrees with the Waco District Court’s claim construction and states it plans to seek “clarification.” *See* Pet. Prelim. Reply 1–2 (stating that it will seek “clarification of the parties’ claim construction disputes” in the Austin District Court because the term raises an “indefiniteness dispute”). In any event, even if the Waco District Court’s claim construction applies here, Petitioner shows for purposes of institution that the prior art satisfies it, as determined below. *See infra* §§ III.E.3, III.F.2.

Based on the foregoing discussion, at this early stage and for purposes of institution, no need exists to adopt and incorporate the claim construction for “low complexity memory” as set forth by the Waco and Delaware District Courts. No need exists currently to explicitly construe any claim language, because doing so would have no effect in the analyses below of Petitioner’s asserted grounds. *See Nidec Motor*, 868 F.3d at 1017 (stating that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Discretion Under 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) in view of the prior Waco District Court case and current Austin District Court case. Prelim. Resp. 11–15; PO Prelim. Sur-reply 1–2. Petitioner disagrees. Pet. 77–79; Pet. Prelim. Reply 1–2. As indicated above (§ II.B.), the Waco District Court recently transferred the case to the Austin District Court after Patent Owner filed the Preliminary Response. The parties’ supplemental briefing addresses some aspects of this transfer as it relates to the Board’s discretionary authority

under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”).

Institution of an *inter partes* review is discretionary. See 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d at 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

An advanced state of a parallel district court proceeding is a “factor that weighs in favor of denying the Petition under § 314(a).” *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) (“*NHK*”). Specifically, an early trial date is part of a “balanced assessment of all relevant circumstances in the case, including the merits.” Consolidated Trial Practice Guide November 2019 (“TPG”) ⁷ at 58.

This balanced assessment involves consideration of the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;

⁷ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, Paper 11 at 5–6.

1. *Factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

As indicated above, the Waco District Court recently transferred the district court case to the Austin District Court. Pet. Prelim. Reply Br. 1; Ex. 1019. The parties do not point to any evidence of a potential stay by the Austin District Court. See Pet. Prelim. Reply Br. 1–2; PO Prelim. Sur-reply 1–2; *Google, LLC v. Parus Holdings Inc.*, IPR2020-00847, Paper 9 at 12 (PTAB Oct. 21, 2020) (declining to “engage in . . . a speculative exercise as to how the Texas District Court would apply these [stay] factors”).

Accordingly, this factor is neutral as to exercising our discretion to deny institution.

2. *Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision*

The parties do not inform the Board as to the projected trial date in the Austin District Court. The projected date of the Board's final written decision in this case is mid-January 2023.

The Board assesses this factor on a case-by-case basis. On one hand, the Board takes a district court's trial schedule at “face value” and declines to question it “absent some strong evidence to the contrary.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12–13 (PTAB May 13, 2020)

(informative). On the other hand, the Board considers the uncertainty in the schedule (including that caused by the parties agreeing to jointly request rescheduling of the trial date on several occasions) despite a scheduled trial date. *Sand Revolution II, LLC v. Cont'l Intermodal Grp. Trucking LLC*, IPR2019-01393, Paper 24 at 11–12 (PTAB June 16, 2020) (informative) (“*Sand Revolution II*”).

This factor involves comparing a district court trial date to the expected final written decision date and assessing weight. This comparison is a proxy for the likelihood that the trial court will reach a decision on validity issues before the Board reaches a final written decision. A trial set to occur soon after the institution decision is likely to happen prior to the Board’s final written decision. As noted above, the parties do not inform the Board of the trial date in the Austin District Court so there is nothing to weigh.

Accordingly, this factor weighs against exercising our discretion to deny institution or is at most neutral.

3. *Factor 3: investment in the parallel proceeding by the court and the parties*

If, at the time of the institution decision, a district court has issued substantive orders related to the challenged patent, such as a claim construction order, this circumstance weighs in favor of denial. *See Fintiv*, Paper 11 at 9–10. On the other hand, if the district court has not issued such orders, this circumstance weighs against discretionary denial. *Id.* at 10. Moreover, in evaluating this factor, “[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution under *NHK*.” *Id.* at 11.

Patent Owner argues that the claim construction process is complete. Prelim. Resp. 13. Patent Owner also argues that the Waco District Court “considered and ruled upon invalidity challenges under 35 U.S.C. § 112 to claims of the ’108 patent.” *Id.* (emphasis added). Patent Owner also argues that “[t]he parties have also exchanged *preliminary* infringement and invalidity contentions, engaged in *limited* discovery relating to *venue* issues, and *begun* full fact discovery pursuant to the schedule set by the [Waco] District Court.” *Id.* (emphasis added).

Petitioner argues that its diligence favors not exercising discretionary denial because it filed the Petition “only about two months after being served with preliminary infringement contentions on May 11, 2021,” and about five to six months before the statutory deadline. *See* Pet. 78.

Petitioner also states that based on the transfer to “the new court,” i.e., the Austin District Court, it

plans to request a case schedule that will provide sufficient time for the various case events, such as full consideration and clarification of the parties’ claim construction disputes . . . , international discovery of a prior owner of the ’108 Patent, and discovery relating to new products, infringement theories, and a claim added to the case after transfer (if the new theories are not struck).

Pet. Prelim. Reply 1 (citing Ex. 1021 (“new” infringement chart)).

The record shows that Petitioner filed the Petition diligently (i.e., within about two and a half months of the preliminary infringement contentions), and that the Austin District Court case is still in the early stages after a recent transfer to that court, with little prior investment in the Austin or Waco District Court pertaining to the invalidity issues raised in the

Petition.⁸ Ex. 3001. Although the Waco District Court has conducted a *Markman* hearing, it only addressed one claim term for the '108 patent (“low complexity memory”), Petitioner plans to seek “clarification” for that construction, and Patent Owner may propose a different construction here for the same term. See Prelim. Resp. 7 n.1; Ex. 2001, 1 (Patent Owner construing “low complexity memory”); *supra* § III.C (Claim Construction). Also, the Waco District Court analyzed that term primarily to resolve a 35 U.S.C. § 112 issue, which is not at issue here. See Ex. 2002, 2; Ex. 2005, 3–10; Prelim. Resp. 13; Pet. Prelim. Reply 2 (arguing that “the indefiniteness dispute has no impact on this proceeding because the Petition relies on prior art disclosing an embodiment of ‘low complexity memory’ from the specification”).

Aside from the Waco District Court’s claim construction of “low complexity memory,” which we do not adopt at this preliminary stage for the reasons discussed above (§ III.C), Patent Owner points to no other investment by the parties toward the patentability issues presented here. *Cf. Sand Revolution II*, Paper 24 at 11 (“[W]e recognize that much work remains in the district court case as it relates to invalidity: fact discovery is still ongoing, expert reports are not yet due, and substantive motion practice is yet to come.”). Similar to the circumstances in *Sand Revolution II*, fact and expert discovery, final invalidity contentions, and dispositive motions, were not complete in the Waco District Court, and the parties have not informed us of any developments in the Austin District Court. See Prelim. Reply 1; Prelim. Resp. 13.

⁸ The Joint Scheduling Order for the Waco District Court states that preliminary infringement contentions were due on May 11, 2021. Ex. 3001. Petitioner filed the Petition on July 22, 2021.

Accordingly, absent input by the parties, and based on the work prior to the transfer, we assume that substantial work remains in the Austin District Court, with little to no risk of the parties and Board here duplicating much if any of the work performed in the Waco District Court or the Austin District Court. *See Fintiv*, Paper 11 at 9–10 (this factor concerns, in part, “duplicative costs”); *Apple Inc. v. Parus Holdings, Inc.*, IPR2020-00686, Paper 9 at 17 (Sept. 23, 2020) (noting *Fintiv*’s concern with “duplicative costs” and finding “as far as claim construction is concerned, there is little risk of the parties or us duplicating work performed in the Texas case should we proceed to a trial” where the parties relied on the plain meaning in the IPR).

For the above reasons, this factor weighs against exercising our discretion to deny institution.

4. *Factor 4: overlap between issues raised in the petition and in the parallel proceeding*

As indicated above, Petitioner “stipulates that it will not pursue invalidity against the ’108 [p]atent asserted claims in the district court using the invalidity grounds in this [P]etition.” Pet. 79 (citing Ex. 1015 (stipulation); *Sand Revolution II*, Paper 24 at 11–12 (addressing a stipulation)). Petitioner adds that it “challenges [c]laims 2, 4, 6, 7, 8, and 10, which are not at issue in district court.” *Id.* Subsequent to that argument, Patent Owner filed new infringement contentions that include claim 6. *See* Pet. Prelim. Reply 8 (citing Ex. 1021); Ex. 1021, 1.

Patent Owner does not address Petitioner’s stipulation. *See* Prelim. Resp. 14. The stipulation “mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as

concerns of potentially conflicting decisions.” *Sand Revolution II*, Paper 24 at 12.

Accordingly, this factor weighs marginally against exercising our discretion to deny institution.

5. *Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party*

Petitioner is a defendant in the Austin District Court. *See* Ex. 1019. Because it is not clear whether the trial in the Austin District Court will precede the deadline for a final written decision in this proceeding, this factor weighs against exercising our discretion to deny institution or is at most neutral.

6. *Factor 6: other circumstances that impact the Board’s exercise of discretion, including the merits*

The factors considered in the exercise of discretion are part of a balanced assessment of all the relevant circumstances in the case, including the merits. *Fintiv*, Paper 11 at 14. For example, if the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution. *Id.* at 14–15. By contrast, if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present. *Id.* at 15. In *Sand Revolution II*, the panel determined that this factor weighed in favor of not exercising discretion when the petitioner had “set forth a reasonably strong case for the obviousness of most challenged claims.” *Sand Revolution II*, at 13.

Here, Patent Owner argues “the Petition substantively lacks merit in its failure to present evidence or argument under the claim construction [of ‘low complexity memory’] adopted by two District Courts, including the

District Court handling parallel proceedings.” Prelim. Resp. 14. As summarized below, however, Petitioner, sufficiently shows that at least challenged independent claims 1 and 11 are unpatentable for purposes of institution even if the Waco District Court’s claim construction applies.

Accordingly, this factor is neutral as to exercising our discretion to deny institution.

7. Conclusion

The Board “a holistic[ally] view[s] . . . whether efficiency and integrity of the system are best served by denying or instituting review” under § 314(a) when evaluating the *Fintiv* factors. *Fintiv*, Paper 11 at 6. Evaluating all of the factors on this record, we decline to exercise our discretion under § 314(a) to deny institution of *inter partes* review.

E. Ground 1: Asserted Obviousness Based on *Cuppens* and *Bhavsar*

Petitioner asserts that claims 1–3, 8, and 11–13 are unpatentable under 35 U.S.C. § 103(a) based on *Cuppens* and *Bhavsar*. Pet. 8–46. Patent Owner disagrees. Prelim. Resp. 6–9.

1. *Cuppens*

Cuppens discloses using a test unit such as a random access memory (RAM) to test the connections of a main unit such as a non-volatile programmable read only memory (PROM) or erasable electrically programmable read-only memory (EEPROM). See Ex. 1005, code (57), 2:26–45, 5:9–14. As testing units, *Cuppens* discloses using two RAM embodiments, “the dynamic random access type, or DRAM,” and a “[s]tatic test memory cell,” or SRAM. See Ex. 1005, 2:49–55.

Figure 1 of Cuppens, as annotated by Petitioner, follows:

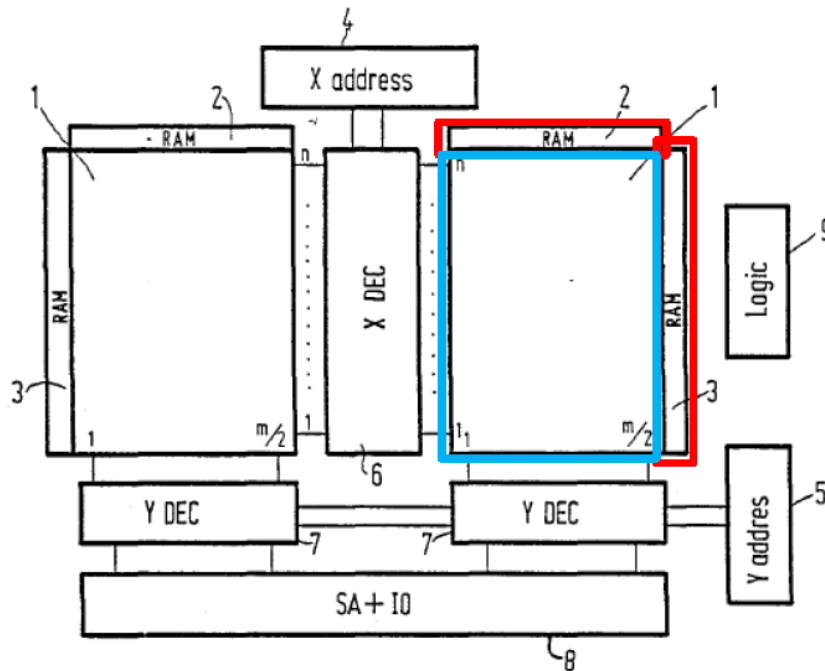


FIG. 1

Annotated Figure 1 shows RAM test memory cells (DRAM or SRAM) 2 and 3, annotated in red, and normal memory cells, such as EEPROM 1, annotated in blue. See Ex. 1005, 2:49–59, 4:8–17, 6:1–9.

Figure 1 also shows

sense or read amplifiers and input/output gates 8, as well as logic circuits 9, all of which are also part of the on-chip peripheral circuits. The logic circuits 9 provide for signals, for example, for the activation of the semiconductor memory, the activation of the output gates, and for programming or write signals.

Id. at 3:17–27.

2. Bhavsar

Bhavsar describes a “method for testing the interconnections of ordinary static RAMs [i.e., SRAMs] with a processor that has a boundary-scan register and an IEEE 1149.1 test-access port.” Ex. 1006, Abstract. Bhavsar describes RAM components as “noncompliant,” because they

cannot be tested for defects using prior art boundary-scan testing techniques. *Id.* at 63. Accordingly, Bhavsar's system improves the prior art techniques to allow for boundary-scan testing of SRAM interconnections and interconnections of other noncompliant components such as ROMs and EEPROMs. *See id.* at 70.

Figure 1 of Bhavsar follows:

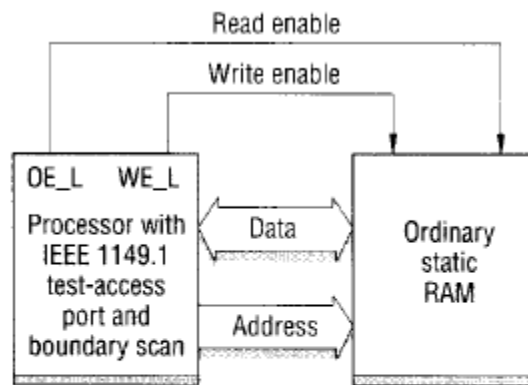


Figure 1. A typical static RAM interface.

Figure 1 shows a processor (on the left) used to test interconnections to a SRAM (on the right) using boundary-scan tests circuitry associated with the processor. *See Ex. 1006, 64.*

3. Independent Claims 1 and 11

Petitioner contends that the combination of Cuppens and Bhavsar would have rendered claims 1 and 11 obvious. Pet. 8–28, 38–41. To support its arguments, Petitioner relies on the testimony of Dr. Alpert, identifies certain passages in the cited references, and explains the significance of passages with respect to each corresponding claim limitation. *Id.* Petitioner also articulates reasons to combine the relied-upon aspects of the references with a reasonable expectation of success. *Id.* at 12–16. Patent

Owner's arguments focus on the claim construction of a "low complexity memory" as addressed below. See Prelim. Resp. 6–9.

a) Claim Limitations

The preamble of claim 1 recites "[a]n electronic circuit comprising." Petitioner contends that Cuppens' Figure 1 represents an electronic circuit including an EEPROM with supporting circuitry and input/output circuits 8. Pet. 16 (citing Ex. 1005, 2:30–23, 2:26–37, 2:42–55, 3:17–27, 5:19–7:66). Petitioner also contends that Bhavsar discloses an electronic circuit in Figure 1. Petitioner provides reasons to combine Cuppens and Bhavsar to address specific limitations of the challenged claims, including the preamble, as summarized below. See *id.* at 12–16; *infra* § III.E.3.b.

Claim 1 recites "a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects." Petitioner contends that "Cuppens discloses a plurality of input/output (I/O) nodes for connecting its electronic circuit to a further circuit via interconnects." Pet. 18–19. To support this contention, Petitioner quotes Cuppens as follows:

[T]he semiconductor memory in FIG. 1 contains sense or read amplifiers and **input/output gates 8**, as well as logic circuits 9, all of which are also part of the on-chip peripheral circuits. **The logic circuits 9 provide for signals, for example, for the activation of the semiconductor memory, the activation of the output gates and for programming or write signals.**

Finally, **provision is made for connections (not shown) for supply and bias or reference voltages (ground potential), data input and output, address signals and control signals.**

Pet. 19 (emphases by Petitioner) (quoting Ex. 1005, 3:17–27, 4:56–61 ("reading and writing take place simultaneously via the 8 input/output gates"))).

Petitioner explains that “Cuppens does not go into detail regarding the ‘further circuit’ that the electronic circuit is connected to, but a POSITA would understand that the further circuit would be a circuit that reads/writes data to Cuppens’ memory.” Pet. 20 (citing Ex. 1002 ¶ 56). Petitioner turns to the “processor” in Bhavsar’s Figure 1 (*see supra*) as a “further electronic circuit,” and contends that “address lines, data lines, write enable lines, and output enable lines input signals from and output signals to the processor, . . . constitute the claimed ‘plurality of input/output (I/O) nodes’ that connect the two circuits via interconnects.” Pet. 21–22 (citing Ex. 1006, 64, 67–70, Figs. 1, 6–9). Relying on reasons to combine Cuppens and Bhavsar as summarized below (*see* Pet. 12–16; *infra* § III.E.3.b), Petitioner explains that the combined teachings of Cuppens and Bhavsar would have rendered the limitation obvious (*id.* at 22).

Claim 1 recites “a main unit for implementing a normal mode function of the electronic circuit.” Petitioner relies on Cuppens’ EEPROM 1 as the recited “main unit” that functions in a normal mode when the RAM circuitry does not function to test EEPROM 1. *See* Pet. 22–23. To support its showing, Petitioner quotes Cuppens to show a “read mode” or “normally” conducted operational state:

The invention relates to a non-volatile, programmable semiconductor memory with . . . memory cells, with a row and/or column of test memory cells . . . and with peripheral circuits for selecting and reading the test memory cells in test mode and ***selecting and reading the normally used memory cells in read mode.***

Pet. 24 (emphasis by Petitioner) (quoting Ex. 1005, 4:8–15). In other words, Petitioner asserts that Cuppens discloses the “normal mode” limitation as “Cuppens . . . differentiates its ‘test mode’ from the normal function of the

memory.” *See id.* (citing Ex. 1001, Fig. 1, 1:10–46, 1:59–2:12, 2:26–3:28, 4:8–18, 4:40–45; Ex. 1002 ¶¶ 60–63)).

Claim 1 recites “a test unit for testing the interconnects.” Petitioner asserts that “Cuppens discloses a test unit that includes at least row 2 and column 3 of SRAM.” Pet. 25 (citing Ex. 1005, 2:42–53 (“Each half matrix 1 is filled with a row 2 and column 3 of test memory cells . . .”), 2:54–55 (“Static test memory cells can also be used . . .”). According to Petitioner, “Cuppens focuses its disclosure on the structure of a circuit incorporating a high-speed SRAM (*id.*, 1:59–2:12) [to test the EEPROM and its interconnections], but does not delve into the details of testing procedures, such using test patterns to detect shorts or stuck-at faults.” *Id.*

Petitioner turns to Bhavsar as disclosing “details of testing procedures for a test unit for testing the interconnects.” Pet. 25. Petitioner also asserts that

[l]ike Cuppens, Bhavsar discloses a test unit comprised of a “static RAM,” and Bhavsar designs specific circuits for the purpose of testing SRAM interconnects: “The author describes a method ***for testing the interconnections of ordinary static RAM ICs*** with a microprocessor . . . that has a boundary-scan register and an IEEE 1149.1 test-access port.”

Pet. 25 (emphasis by Petitioner) (quoting Ex. 1006, 63). Petitioner provides reasons to combine Cuppens and Bhavsar as summarized below. *See infra* § III.E.3.b.

Claim 1 recites “the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit.” Petitioner relies on teachings in Cuppens and Bhavsar. *See* Pet. 29 (“Cuppens and Bhavsar render this limitation obvious.”)

Petitioner contends that Cuppens describes enabling or disabling the SRAM test memory cells “to switch between the normal mode (involving, for example, EERPOM) and the test mode (involving, for example, SRAM) using a write line W and a write selection line WR.” Pet. 26. Petitioner quotes Cuppens as follows:

During the **normal** read cycles (PROM, EPROM, EEPROM) and write cycles (EPROM and EEPROM) of the memory cells **normally** used, the **write line W** is kept at 0 volt and the **write selection line WR** is kept at a supply voltage level (Vcc), so that the voltage at the gate of the memory transistor T1 is equal to 0 volt, and the memory transistor T1 blocks and **has no effect on the normal operation** of the non-volatile, programmable semiconductor memory. In **test mode** the selected memory cell, i.e. when the supply voltage Vcc is applied to the test selection line WL, can be written by applying the write selection line WR to Vcc.

Pet. 27 (emphasis by Petitioner) (quoting Ex. 1005, 6:41–52).

Petitioner contends that Bhavsar also teaches the test mode of the limitation: “Bhavsar discloses the claimed test mode because it ‘describes a method for testing the interconnections of ordinary static RAM ICs with a microprocessor . . . that has a boundary-scan register’” Pet. 28 (quoting Ex. 1006, Abstract). In addition, Petitioner explains that “Bhavsar discloses that the test unit (the ordinary static RAM) is logically connected via I/O nodes to the further circuit (the neighboring processor), because it explicitly discloses connecting those components using pins and lines.” *Id.* (citing Ex. 1006, 64–70). Petitioner provides reasons to combine Cuppens and Bhavsar as summarized below, including to efficiently test the same types of memory. *See infra* § III.E.3.b; Pet. 15.

Finally, claim 1 recites “such that in the test mode the test unit is operable as a low complexity memory via the I/O nodes.” Petitioner

contends that “Cuppens discloses use of static RAM for the test unit, which the ’108 [p]atent views as low complexity memory.” Pet. 30. Petitioner also relies on Bhavsar’s disclosure “that the test unit is an ‘ordinary static RAM.’” *Id.* (quoting (Ex. 1006, Fig. 1). As Petitioner points out, the ’108 patent lists “Static Random Access Memories (SRAMs)” as an example of “[l]ow complexity memory.” *Id.* at 29 (quoting Ex. 1001, 4:61–65). Petitioner provides reasons to combine Cuppens and Bhavsar as summarized below. *See infra* § III.E.3.b.

On this preliminary record, Cuppens and Bhavsar each disclose low complexity memories (i.e., SRAMs), because the ’108 patent describes SRAMs as examples thereof as found preliminarily in the Claim Construction section above. *See supra* § III.C; Pet. 29 (quoting Ex. 1001, 4:61–65); Ex. 1001, 4:61–65. Alternatively, even if the Waco District Court’s claim construction applies here, neither Cuppens nor Bhavsar describes the disclosed SRAMs “hav[ing] to be put through a complex initialization process” or as having “access protocols” with “dynamic restrictions” in contravention of the negative limitations in the Waco District Court construction. *See supra* § III.C (Claim Construction); *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1367 (Fed. Cir. 2019) (“Contrary to AC’s suggestion, a reference need not state a feature’s absence in order to disclose a negative limitation.”) (citing *Sud-Chemie, Inc. v. Multisorb Techs., Inc.*, 554 F.3d 1001, 1004–05 (Fed. Cir. 2009) (affirming finding that reference discloses an “uncoated” film where it does not describe the film as coated and does not suggest the necessity of coatings)).

Further supporting this preliminary finding, Bhavsar describes “a method to test interconnections to ordinary static RAMS” that include a “simple protocol” for noncompliant components like SRAMs for

communicating with compliant products. *See* Ex. 1006, 70 (emphasis added). In other words, even if the Waco District Court’s claim construction applies, the preliminary record shows that the prior art SRAMs of Cuppens and Bhavsar, like those described in the ’108 patent, “do not have to be put through a complex initialization process before they can be accessed, and . . . have simple access protocols without dynamic restrictions.” *See supra* § III.C (Claim Construction).

Independent claims 1 and 11 are similar. For claim 11, Petitioner “maps [c]laim 11’s ‘first electronic circuit’ and ‘second electronic circuit’ to Bhavsar in a slightly different way than the mapping for [c]laim 1’s ‘electronic circuit’ and ‘further circuit.’” Pet. 39. In particular, Petitioner maps claim 11’s “first electronic circuit” as including Bhavsar’s and Cuppens’ SRAM as a test unit (without including the boundary scan read/write register as it does for claim 1) and including Cuppens’ EEPROM as a main unit. *Id.* at 39–40. Petitioner maps claim 11’s “second electronic circuit” as including Bhavsar’s processor and boundary scan read/write register (unlike in claim 1, where Petitioner maps the “further circuit” only to the processor). *See id.* at 39 (citing Ex. 1006, Fig. 1, Fig. 6, 63–64 (describing use of processor with boundary scan circuits to test interconnects)).

Claim 11 further recites “wherein the putting step comprises operating the first electronic circuit as a low complexity memory by the second electronic circuit.” Petitioner states that the combined teachings of Cuppens and Bhavsar would have rendered this limitation obvious. Pet. 41. Referring to its showing with respect to claim 1, Petitioner explains as follows:

Cuppens and Bhavsar both disclose a test unit comprised of SRAM, which the '108 Patent views as a “low complexity memory.” Further, Cuppens discloses operating the first electronic circuit (including the test row and column of SRAM) as a “low complexity memory” by putting write/read data on the interconnects during testing. Similarly, Bhavsar discloses using the second electronic circuit (the processor with boundary scan circuits) to operate the first electronic circuit (the SRAM) as a “low complexity memory” by putting write/read data on the interconnects during testing.

Id. (citing Ex. 1002 ¶ 100).

Patent Owner groups the claims together and relies on its claim construction arguments addressed in connection with claim 1. *See* Prelim. Resp. 6–9. Based on the foregoing discussion and the preliminary record, and considering the reasons to combine the references as set forth below (§ III.E.3.b), Petitioner’s showing of obviousness of claims 1 and 11 based on the combined teachings of Cuppens and Bhavsar is sufficient.

b) Reasons to Combine

Petitioner asserts that combining Cuppens and Bhavsar would have amounted to using a “known technique (boundary-scan functionality on a neighboring component) to improve the testing ability of a known memory type (Cuppens’ SRAM), in the same way that Bhavsar proposes testing interconnects for SRAM.” Pet. 15 (citing Ex. 1002 ¶ 45). Petitioner explains that Bhavsar characterizes its interconnect testing system as ‘extendable to several other noncompliant components such as ROMs, EEPROMs,’ and others.” *Id.* (quoting Ex. 1006, 70). According to Petitioner, “Cuppens discloses using ‘ROMs,’ ‘PROMs,’ ‘EPROM,’ and ‘EEPROM’ as the main unit, and proposes using static random access memory to make such testing easier.” *Id.* (quoting Ex. 1005, 2:26–41). Therefore, Petitioner maintains that “a POSITA would have recognized that

both Bhavsar and Cuppens have the objective of efficiently testing the same types of memory.” *Id.* (citing Ex. 1002 ¶ 46).

Petitioner further contends that “Cuppens uses SRAM, but does not detail the test patterns for testing the SRAM’s interconnections for, for example, opens or shorts.” Pet. 13. Petitioner relies on Bhavsar’s teaching that SRAM circuits are “subject to faults, ‘such as opens and shorts,’” so that it would have been obvious to ensure SRAM interconnects do not have faults by applying “Bhavsar’s interconnect testing method to Cuppens’ SRAM memory circuits.” *Id.* at 13–14 (citing Ex. 1002 ¶ 43).

Petitioner also contends that “Bhavsar discloses a specific motivation to combine with Cuppens—it teaches a way to enable standard boundary-scan testing on a non-compliant component, such as the memory IC disclosed in Cuppens, without the need to add additional circuitry.” Pet. 16 (citing Ex. 1006, 63; Ex. 1002 ¶ 48). Petitioner also explains that “[a] POSITA would have understood that the purpose of the I/O nodes and interconnects is to connect Cuppens’ memory to a further circuit,” such as Bhavsar’s processor, which operates with memory. *Id.* at 14.

On this preliminary record, Petitioner articulates reasons supported with factual underpinnings to combine Cuppens and Bhavsar. To summarize, Petitioner shows that claims 1 and 11 recite test “structure already known in the prior art that is altered by the mere substitution of one element [memory structure] for another known in the field,” and the “combination . . . yield[s] a predictable result” of providing interconnection tests for known SRAMs and other memory types. *See KSR*, 550 U.S. at 416. In addition, Petitioner shows on this preliminary record that Bhavsar suggests an efficient manner to enable standard testing

of known memory circuitry interconnections, like those of Cuppens, which employs a similar memory testing system, with a reasonable expectation of success. Petitioner's showing is sufficient for purposes of institution. Patent Owner does not address Petitioner's showing, other than as indicated above with respect to its claim construction arguments.

Based on the foregoing discussion, we determine the Petition and Preliminary Response show a reasonable likelihood that Petitioner would prevail in its assertion that claims 1 and 11 would have been obvious over the combination of Cuppens and Bhavsar.

4. Claims 2, 3, 8, 12, and 13

Petitioner provides reasoned and detailed explanations, supported by the testimony of Dr. Alpert, indicating how the combined teachings of Cuppens and Bhavsar would have rendered claims 2, 3, 8, 12, and 13 obvious. Pet. 31–46. Patent Owner does not present arguments directed specifically to these claims. See Prelim. Resp. 6–9. On the current record, we determine that the Petition and Preliminary Response show a reasonable likelihood that Petitioner would prevail in its assertion that claims 2, 3, 8, 12, and 13 would have been unpatentable over the combined teachings of Cuppens and Bhavsar.

F. Ground 2: Asserted Anticipation by Hong

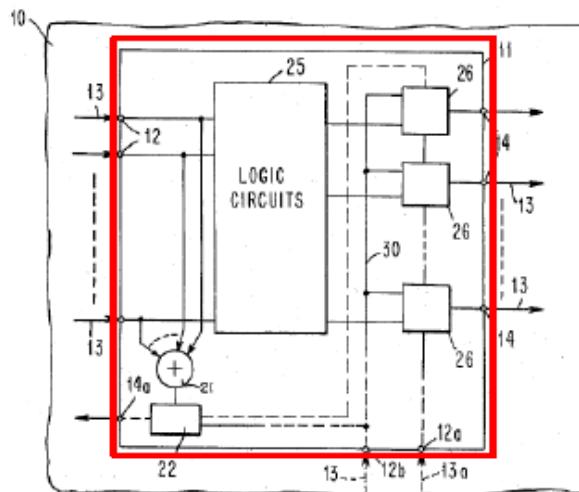
Petitioner challenges claims 1, 3, 6–8, 10, and 11 as unpatentable under 35 U.S.C. § 102(b) based on anticipation by Hong. Pet. 82–87. Patent Owner's arguments largely focus on the claim construction of a "low complexity memory," as discussed further below. See Prelim. Resp. 10–11.

1. Hong

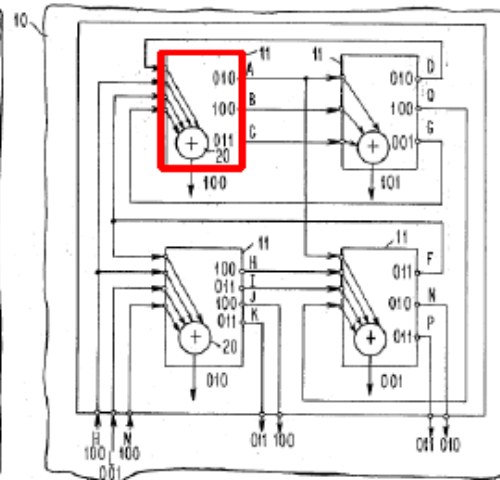
Hong "relates to the testing of connections between modules mounted on cards and more particularly to circuitry in the modules to provide simple

testing of such connections.” Ex. 1009, 1:6–10. Hong explains that after assembling modules on a card, “what really needs to be tested . . . is the connections between the modules and the card” and “generating tests for defective pin connections becomes an enormous task.” *Id.* at 1:11–24.

Petitioner provides a side-by-side annotated version of Hong’s Figure 3 (left) and Figure 4 (right), reproduced as follows (Pet. 48):



Ex-1009, Figure 3



Ex-1009, Figure 4

Figure 3 (left) is an expanded view showing module 11 (annotated in red by Petitioner), which Figure 4 (right) shows as one (red) of four modules 11. Hong explains that “FIG. 4 is a schematic view of a card containing the embodiment of FIG. 3 with test signals superimposed on the terminals and pins of the card.” Ex. 1009, 2:20–34.

Logic circuits 16/25 in modules 11 include input pins 12, output pins 14, conductors 13, Exclusive-OR circuit 22, Exclusive-OR tree 21, and stage 26 of a shift register. *See* Ex. 1009, 2:32–33, 3:23–33. Applying a binary 1 to each terminal 12b “connects the output lines 21 of the logic

circuits to the output terminals 14 so the circuits 16 on the cards can perform in their intended manner,” that is a “normal operation . . . when the modules are not being tested.” *Id.* at 2:53–57.⁹ On the other hand, applying a binary 1 to each terminal 12b instigates a test mode to test the interconnections. *Id.* at 2:57–58. This

ungates the connection between the output lines 21 of the original logic circuits and the terminals and instead connects all the terminals to line 26 so that test signals can be applied to the output terminals by their application to the card terminal connected to terminals 12a on all the modules. The test signals are a binary 0 followed by a binary 1. The first signal tests for any pin stuck at 1. If the card tests good, a binary 0 will appear at the card terminal connected to module terminals 14a, if not a binary 1 appears at this terminal.

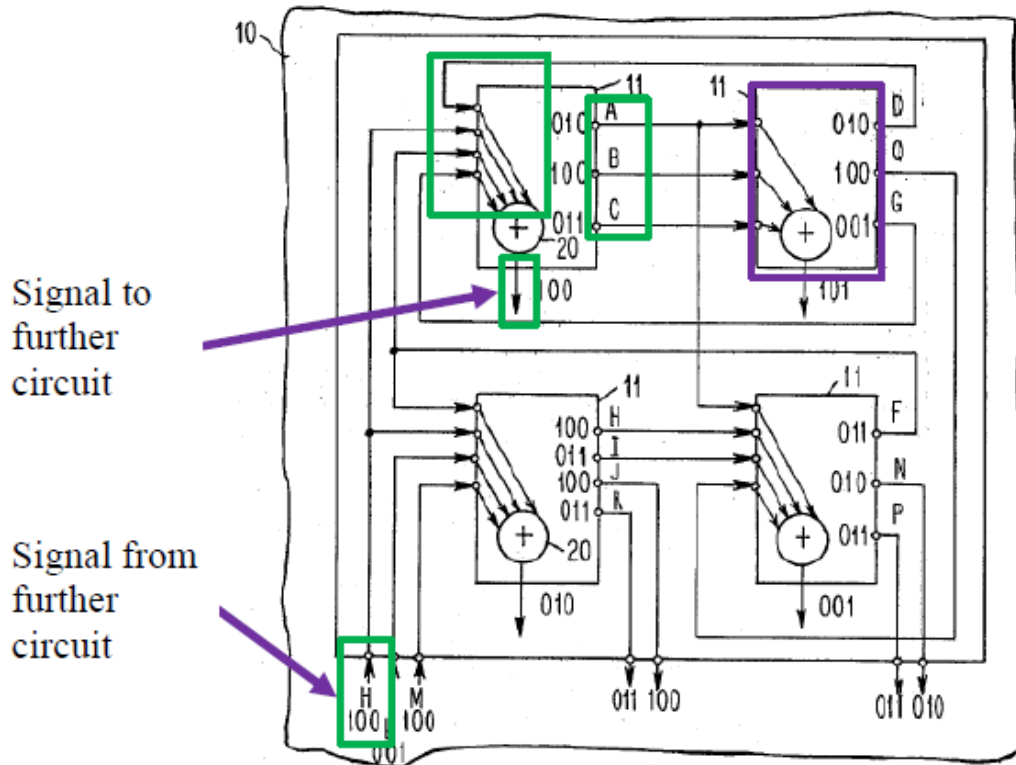
Id. at 2:58–63.

2. *Claims 1 and 11*

Claim 1 recites “[a]n electronic circuit comprising” and “a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects.” Petitioner relies on Hong’s module 11 as an electronic circuit having the claimed interconnects to a further circuit, including I/O nodes as pins 12, 13, and 14 as depicted in module 11 of Figure 3. *See* Pet. 48–52.

Petitioner’s annotated version of Hong’s Figure 4 follows:

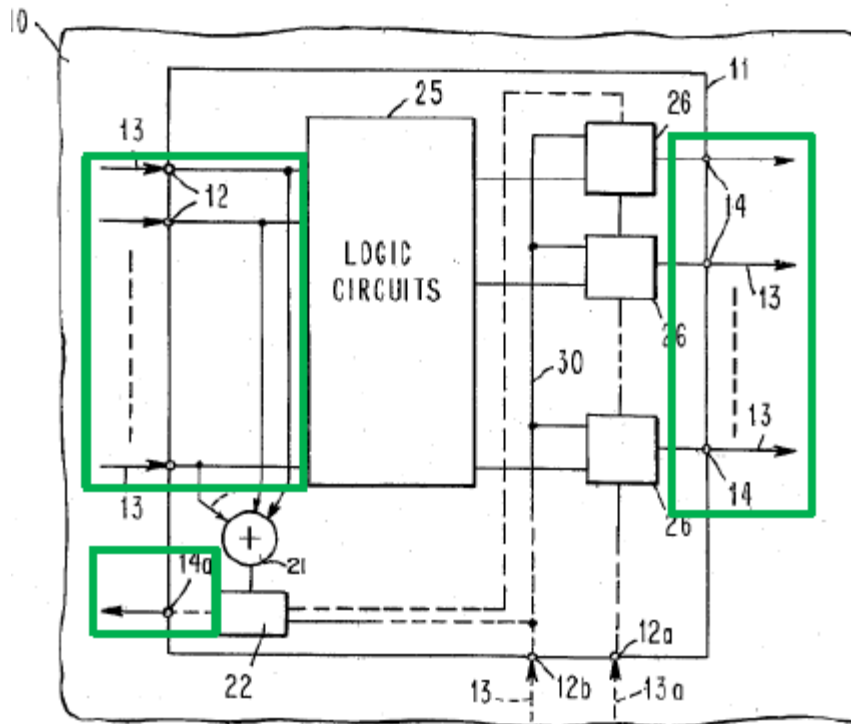
⁹ Although Hong specifically refers to Figure 1 in this passage and the following passages, Hong indicates it applies to Figures 1–4. *See id.* at 1:43–61. The embodiment of Figure 3 also “permits testing for shorts between the different interconnection networks on the card in addition to testing for simple stuck 1’s or 0’s in those networks.” *Id.* at 3:71–21



Ex-1009, Figure 4

As annotated above by Petitioner, Hong's Figure 4 shows signals to and from a further electronic circuit on I/O nodes (green) for connecting electronic circuit module 11. See Pet. 50. According to Petitioner, "Hong discloses a further electronic circuit (not shown in the figures) that supplies signal H on the lower left of Figure 4 (annotated green) and receives the signal from the arrow with test signal '100' (also annotated in green) coming off the bottom of the upper left module 11." *Id.* at 50–51. Petitioner contends that "Hong refers to this unillustrated circuit as 'circuit means . . . for . . . supplying said test signals to the test input terminals of said subassembly packages.'" *Id.* (quoting Ex. 1009, 5:42–45).

Petitioner's annotated version of Hong's Figure 3 follows:



Ex-1009, Figure 3

As annotated above by Petitioner, Hong's Figure 3 is an expanded view of an embodiment of module 11 (in Figure 4) and shows pins 12, 13, 14 (green) as I/O nodes for connecting electronic circuit module 11 to a further electronic circuit (undepicted). See Pet. 49 (citing Ex. 1009, 3:22–31). Petitioner quotes the following passage in Hong for context with respect to Figure 3:

As shown in FIG. 3, each module includes an Exclusive-OR circuit 22 [sic, 21] with an **input coupled to each of the module input pins 12 and output connected to a stage 22** is a shift register In addition the **output pins 14** are each connected to a stage 26 of the same shift register. Data can be loaded into the first stage of this shift register at input terminal 12a, stepped through all stages of the shift register with clock signals and **removed from the last stage of the shift register at output terminal 14a**.

Pet. 50 (emphasis by Petitioner) (quoting Ex. 1009, 3:22–31).¹⁰ According to Petitioner, “Hong explains that terminal 14a is used by the further circuit to take ‘the response of the Exclusive-OR tree 22 [sic, 21] . . . off the module.’” *Id.* at 51 (quoting Ex. 1009, 3:45–50).

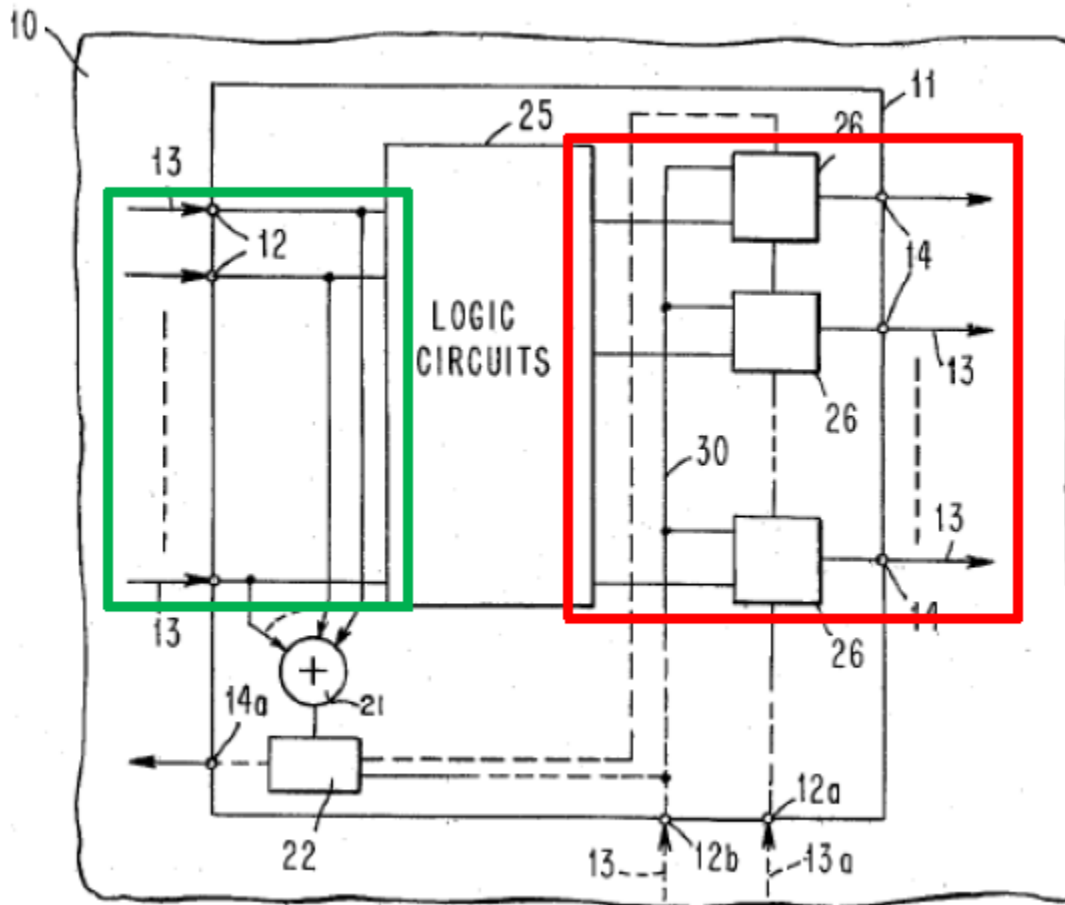
Claim 1 recites “a main unit for implementing a normal mode function of the electronic circuit.” Petitioner reads this “main unit” onto Hong’s logic circuits 25 of module 11 as depicted in Figure 3. See Pet. 52–53 (quoting Ex. 1009, 2:52–62) (“During normal operation, that is, operation when the modules are not being tested, a binary 1 is applied to each of the terminals 12b. This connects the output lines 2[0] of the logic circuits to the output terminals 14 so the circuits 16 [in Figure 1, or circuits 25 in Figure 3] on the cards can perform in their intended manner.”).¹¹

Claim 1 recites “a test unit for testing the interconnects.” Petitioner reads the test unit onto the “[e]xclusive-OR circuit” in each of the modules to test inputs and outputs of the modules. See Pet. 51 (noting Hong describes that “each of the modules has a test input circuit for accessing all of the output pins of the module in parallel” (quoting Ex. 1009, 1:51–52)).

Claim 1 recites “the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit.” Petitioner annotates Hong’s Figure 3 as follows:

¹⁰ Petitioner explains that “[a]s shown in Figure 3, the XOR tree is labeled element ‘21’ and the shift register stage is labeled element ‘22.’” Pet. 51 n.3.

¹¹ Petitioner explains that “Logic Circuits” include element 16 in Figure 1 and element 25 in Figure 3.” Pet. 52.



Ex-1009, Figure 3

As annotated by Petitioner, Hong's Figure 3 shows that in normal mode of main unit 25 (logic circuits), "the I/O nodes at pins 12 and lines 13 (annotated green) are connected to the logic circuits 25," and "the outputs of logic circuits 25 are connected to output pins 14 through shift register stages 26 (annotated red)." Pet. 56. According to Petitioner, "[i]n the test mode, data is transferred between the modules along the interconnects into the XOR circuits, and the outputs of the XOR circuits are evaluated to determine whether the interconnects are working." *Id.* at 57 (citing Ex. 1009, 1:43–67; quoting *id.* at 1:43–45 ("In accordance with the present invention circuitry is provided that permits the testing of interconnections")). Petitioner

explains that Hong’s test mode “involves inputting patterns of bits into different interconnects and evaluating the results of the XOR circuits to identify shorts or stuck-at faults.” *Id.* (citing Ex. 1009, 4:1–44). In other words, Petitioner asserts that “[i]n [Hong’s] test mode, the I/O nodes are logically connected to the test unit.” *Id.* (citing Ex. 1009, 2:25–68, 3:22–56, 5:7–11, claims 1, 3–6).

Claim 1 recites “such that in the test mode the test unit is operable as a low complexity memory via the I/O nodes.” Petitioner relies on Hong’s exclusive-OR circuit as the claimed test unit, asserting it is just like an embodiment in the ’108 patent, namely a “combinatorial circuit to write 0s and 1s to the inputs and read the results from the outputs.” *See* Pet. 60–61 (comparing Ex. 1001, 12:10–20, with Ex. 1009, 1:43–67). Petitioner contends that the ’108 patent explains that “a combinatorial XOR circuit is ‘operable as a low complexity memory.’” *Id.* at 60 (citing Ex. 1001, 12:25–36; Ex. 1002 ¶ 137).

Patent Owner argues that the ’108 patent specification does not state “that an XOR circuit is a low complexity memory.” *See* Prelim. Resp. 10 (“The patent does not make such a leap.”). This argument does not address the claim language. Claim 1 recites that “the test unit *is operable as a low complexity memory* via the I/O nodes.” It does not recite that the test unit *is* a “low complexity memory.”

Patent Owner asserts that “the Petition makes no showing that the Hong reference implements the functionality of a ROM table.” Prelim. Resp. 10. This argument also does not address why claim 1 requires implementing the functionality of a ROM table. Petitioner quotes the ’108 patent as specifically not requiring a “real ROM table” “for the test unit

being operable as a low complexity memory” and instead using “a combinatorial circuit”:

[F]or the test unit being operable as a low complexity memory, it is not required that the test unit is implemented as a real ROM table. Especially if only a small number of test patterns is used, the test unit ***could be implemented as a combinatorial circuit***, leading to more efficient area usage.

Pet. 59 (emphasis by Petitioner) (quoting Ex. 1001, 3:36–43). In the sentence preceding the above passage, the specification describes how “a *small number of test patterns pre-stored in the ROM* would normally suffice for an interconnect test capable of detecting open circuits in interconnects and short circuits between interconnects.” Ex. 1001, 3:33–37 (emphasis supplied). Therefore, as described in the ’108 patent specification on this preliminary record, the disclosed combinatorial XOR circuits do not require implementation as a ROM, but XOR circuits and ROMs provide similar test patterns at least for small numbers of such patterns. *See id.* at 3:36–43.

Tracking the specification, the Petition similarly explains that the ’108 “patent states that ‘for the test unit being operable as a low complexity memory,’ ‘the test unit could be implemented as a combinatorial circuit,’ such as an XOR or XNOR circuit.” Pet. 7 (citing Ex. 1001, 3:36–43, 4:61–67, 10:7–12:19, Figs. 4–6). As summarized above, the Petition compares the XOR combinatorial circuits in the ’108 patent and Bhavsar, and explains that the two “match[]” by testing interconnects using XOR binary (0s and 1s) combinations such that “Hong discloses that in the test mode the test unit is operable as a ‘low complexity memory’ via the I/O nodes.” *See id.* at 60–61.

The ’108 patent further supports the Petition by describing a “combinatorial circuit” as implementing rules based on “exclusive-nor

function[s]” to “implement[] the functionality of a ROM table,” and similarly specifies that “test unit 406 has [two] three-input XOR gate[s]” 602 and 604. *See id.* at 10:9–17, 12:14–16, Fig. 5, Fig. 6.

Therefore, Petitioner sufficiently shows that Hong’s XOR circuits operate in materially the same manner as the XOR circuits described the ’108 patent relative to the breadth of claim 1, which, for example, does not provide a lower limit on the number of test patterns. *See* Pet. 59–61 (citing Ex. 1009, 1:43–67).

Patent Owner also argues that “[t]he Petition does not reference or discuss initialization processes, access protocols, or dynamic restrictions at any point in its analysis of elements 1[e] and 11[e].” Prelim. Resp. 10. This argument does not address the claim language. Claims 1 and 11 do not require that the test unit is a memory; rather, claim 1 recites that “the test unit is operable as a low complexity memory” and claim 11 recites “operating the first electronic circuit as a low complexity memory.” On this limited record, Bhavsar’s XOR circuits are not memories. Patent Owner’s claim construction arguments, premised on the Waco District Court’s claim construction, apply to a memory and do not apply to XOR circuits. *See supra* § III.C (Claim Construction).

Petitioner reads the similar independent claim 11 limitations onto similar and specific disclosures in Hong, with the showing largely tracking the showing for similar independent claim 1. *See* Pet. 69–73. Patent Owner’s arguments, addressed above in connection with claim 1, group the claims together. *See* Prelim. Resp. 10–11. In summary, on this preliminary record and for purposes of institution, Petitioner persuasively provides reasoned and detailed explanations, supported by the testimony of Dr. Alpert, showing that Hong anticipates claims 1 and 11. *See* Pet. 48–61,

69–73. Accordingly, we determine that the Petition and Preliminary Response show a reasonable likelihood that Petitioner would prevail in its assertion that Hong anticipates claims 1 and 11.

3. Claims 3, 6–8, and 10

Petitioner reads dependent claims 3, 6–8, and 10 onto specific disclosures in Hong and supports the showing with the testimony of Dr. Alpert. *See* Pet. 61–79. In summary, on this preliminary record and for purposes of institution, Petitioner provides reasoned and detailed explanations, supported by the testimony of Dr. Alpert, showing how Hong anticipates claims 3, 6–8, and 10. *See* Pet. 48–61, 69–73. Patent Owner does not address these claims specifically. *See* Prelim. Resp. 10–11. Accordingly, we determine that the Petition and Preliminary Response show a reasonable likelihood that Petitioner would prevail in its assertion that Hong anticipates claims 3, 6–8, and 10.

G. Ground 3: Asserted Obviousness Based on Hong and Wakerly

Petitioner challenges claim 4 as unpatentable under 35 U.S.C. § 103(a) based on Hong and Wakerly. Pet. 74–77. Claim 4 depends from claim 1 and recites “wherein the test unit comprises a combinatorial circuit implementing an XNOR function and being connected to the I/O nodes.”

Petitioner provides sufficient reasons, supported with the testimony of Dr. Alpert, why one of ordinary skill in the art would have employed Wakerly’s XNOR teachings in Hong’s test circuitry with a reasonable expectation of success. *See* Pet. 74–77. For example, Petitioner explains that it would have been obvious to implement Wakerly’s XNOR teachings in place of Hong’s XOR teachings to test interconnections using parity checking, where both XOR and XNOR implement parity checking, and an XNOR is simply the inverse of an XOR. *See id.*

At this stage of the proceeding, Patent Owner does not dispute these contentions. *See* Prelim. Resp. 10–11. On the current record, we determine that the Petition and Preliminary Response show a reasonable likelihood that Petitioner would prevail with respect to its contention that claim 4 would have been unpatentable over the combined teachings of Hong and Wakerly.

IV. CONCLUSION

After considering the evidence and arguments of record, we determine that Petitioner has demonstrated a reasonable likelihood of success with respect to at least one of the challenged claims. Accordingly, an *inter partes* review of all of the claims and all of the grounds presented in the Petition is hereby instituted. *See* 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1354, 1359–60; TPG 64.

At this stage of the proceeding, the Board has not made a final determination as to the patentability of any challenged claims or any underlying factual or legal issues. The final determination will be based on the record as developed during the *inter partes* review.

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the challenged claims of the '108 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '108 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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FOR PETITIONER:

Ryan K. Yagura
Nicholas J. Whilt
Clarence A. Rowland
Xin-Yi Zhou
O'MELVENY & MYERS LLP
ryagura@omm.com
nwhilt@omm.com
crowland@omm.com
vzhou@omm.com

FOR PATENT OWNER:

Reza Mirzaie
James Milkey
RUSS, AUGUST & KABAT
rmirzaie@raklaw.com
jmilkey@raklaw.com