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Paper 10
Date: February 11, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA CORPORATION; KIOXIA AMERICA, INC.;
WESTERN DIGITAL TECHNOLOGIES, INC.; AND
DELL TECHNOLOGIES, INC.,
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2021-01354
Patent 7,436,232 B2

Before GREGG I. ANDERSON, GARTH D. BAER, and
JOHN D. HAMANN, *Administrative Patent Judges.*

HAMANN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Kioxia Corporation; Kioxia America, Inc.; Western Digital Technologies, Inc.; and Dell Technologies, Inc. (collectively, "Petitioner") filed a petition for *inter partes* review of claim 14 ("the challenged claim") of U.S. Patent No. 7,436,232 B2 (Ex. 1001, "the '232 patent"). Paper 5 ("Pet."). Sonrai Memory Limited ("Patent Owner") filed a Preliminary Response. Paper 9 ("Prelim. Resp.").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018); *see* 37 C.F.R. § 42.108 (2020). Upon consideration of the papers, we conclude that the information presented shows that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of the challenged claim of the '232 patent.

A. Real Parties-in-Interest

The parties identify themselves as the real parties-in-interest. Pet. 3; Paper 8, 1.

B. Related Matters

The parties identify *Sonrai Memory Limited v. Dell Technologies, Inc.*, Case No. 6:21-cv-00361-ADA as a matter that may affect, or be affected by, a decision in this proceeding. Pet. 3; Paper 8, 1. In addition, Patent Owner identifies *Sonrai Memory Limited v. Western Digital Technologies, Inc.*, Case No. 8:21-cv-01040-CJC (JDEx) (C.D. Cal.) as a matter that may affect, or be affected by, a decision in this proceeding. Paper 8, 1.

C. The Challenged Patent

The '232 patent is titled "Regenerative Clock Repeater." Ex. 1001, code (54). The '232 patent discloses "a regenerative clock repeater that uses an output driver means which receives information about the rising edge and falling edge to recover a high logical level (V_H) and a low logical level (V_L) of a clock signal." *Id.* at 2:44–48. Figure 5, shown below, illustrates an embodiment of the '232 patent. *Id.* at 3:16–18.

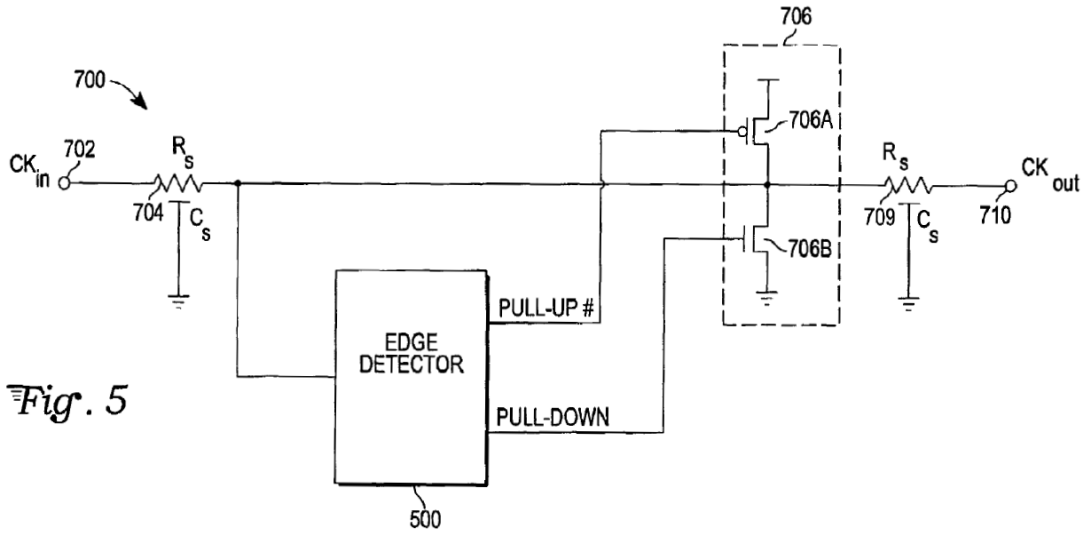

Fig. 5

Figure 5 "is a schematic block diagram illustrating the general features of a regenerative clock repeater circuit in accord with the" '232 patent. *Id.* As illustrated, "a regenerative clock repeater 700 . . . that recovers the low logical level (V_L) and a high logical level (V_H) of a degraded clock signal, comprises an edge detector circuit 500 and an output driver circuit 706." *Id.* at 3:34–38. The '232 patent discloses that "[t]he edge detector circuit 500 receives a clock signal CK_{IN} from a segment of clock distribution line 702 characterized by an intrinsic RC impedance 704 and generates either a pull-up control signal (PULLUP#) or a pull-down control signal (PULL-DOWN) based on the logic level of the clock signal 702." *Id.* at 3:38–43. "The pull-up control signal (PULL-UP#) is generated by a sensed

rising edge of the clock signal passing above a low threshold voltage level, [and] the pull-down control signal (PULL-DOWN) is generated by a sensed falling edge of the clock signal passing below a high threshold voltage level," as disclosed by the '232 patent. *Id.* at 3:42–47. As illustrated, "[t]he output driver 706 has a pull-up transistor 706A (usually p-type) connected to a power supply at a high logical level (V_H) and a pull-down transistor 706B (usually n-type) connected to a power supply at a low logical level (V_L), typically ground." *Id.* at 3:47–51. The '232 patent discloses that "[t]he pull-up and pull-down transistors 706A and 706B, respectively, receive the pull-up control signal and the pull-down control signal to recover the high logical level (V_H) and a low logical level (V_L) of the received degraded clock signal," and that they "place the recovered clock onto another segment of the clock distribution line which is likewise characterized by an intrinsic RC impedance 709 and whose output is the Ck_{out} at node 710." *Id.* at 3:52–59.

D. Challenged Claim

Petitioner challenges only independent claim 14. Claim 14 reads as follows:

> 14. A method for regenerating a clock signal in a synchronous semiconductor memory, such method comprises the following steps:
>
> detecting a rise edge from a low logical level and a fall edge from a high logical level of said clock signal;
>
> generating a pull-up control signal in response to the detecting of the rise edge of the clock signal;
>
> generating a pull-down control signal in response to the detecting of the fall edge of said clock signal;
>
> recovering said high logical level using the pull-up control signal; and
>
> recovering said low logical level using the pull-down control signal.

Ex. 1001, 10:11–23.

E. Asserted Grounds of Unpatentability

Petitioner asserts that claim 14 of the '232 patent is unpatentable based on the following grounds:

Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
14	102	Masleid[2]
14	103(a)	Masleid
14	103(a)	Masleid, Kono[3]

Pet. 15, 25–40. Petitioner submits in support of its arguments the Declaration of Vivek Subramanian, Ph.D. (Ex. 1003).

II. LEVEL OF ORDINARY SKILL IN THE ART

To determine whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In assessing the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–63 (Fed. Cir. 1986)). "[O]ne or more factors may predominate." *Id.*

Petitioner argues that one of ordinary skill in the art "would have had a Bachelor's degree in electrical engineering or an equivalent field and two

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 102, 103 that became effective on March 16, 2013. Because the '232 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of the statutory bases for unpatentability.
[2] US 7,053,680 B2, issued May 30, 2006 (Ex. 1004, "Masleid").
[3] US 6,707,758 B2, issued Mar. 16, 2004 (Ex. 1005, "Kono").

years of academic or industry experience working with the design of digital circuits." Pet. 22 (citing Ex. 1003 ¶ 35). Patent Owner does not identify a level of skill in the art that one would have had at the time of the invention of the '232 patent or identify any specific shortcoming in Petitioner's formulation. *See generally* Prelim. Resp.

For purposes of this Decision, and based on the current record, we adopt Petitioner's assessment of the level of skill for one of ordinary skill in the art. Pet. 22. This assessment is consistent with the '232 patent and the asserted prior art, and we apply it in our analysis below.

III. CLAIM CONSTRUCTION

Because the Petition was filed after November 13, 2018, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), following the standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b); 83 Fed. Reg. 51,340, 51,340–41, 51,343 (Oct. 11, 2018). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Here, neither party advances a proposed construction for any claim terms. Pet. 23; *see generally* Prelim. Resp. The parties dispute, however, whether the entirety of claim 14's preamble (i.e., "[a] method for

regenerating a clock signal in a synchronous semiconductor memory") is limiting. Pet. 26–27; Prelim. Resp. 2–5; Ex. 1001, 10:11–12 (claim 14's preamble).

Petitioner argues "that the 'clock signal' recited in the preamble provides a necessary structure for the claim and an antecedent basis for 'said clock' in the body of the claim." Pet. 26 (citing *TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323–24 (Fed. Cir. 2015)). "However, the 'in a synchronous semiconductor memory' portion of the preamble does not limit claim 14 because it merely states an intended use of the invention: a clock regeneration circuit for use in a synchronous semiconductor memory," according to Petitioner. *Id.* Petitioner argues that because "the preamble recites no other essential structure or steps beyond what is already recited in the body of the claim and the identified use of the method imposes no structural requirement on the claimed method beyond what is recited in the body of the claim, the intended use is not a claim limitation." *Id.* at 26–27 (citing *Arctic Cat, Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328–29 (Fed. Cir. 2019)). Petitioner adds that in the '232 patent's discussion of using "the claimed method in a synchronous semiconductor memory, the '232 patent states that use of the '232 patent's regenerative clock repeaters at different locations in a memory device is 'a typical use for clock repeaters in integrated circuitry.'" *Id.* at 27 (citing Ex. 1001, 5:64–6:1; Ex. 1003 ¶ 46). Petitioner argues "[t]hat the use of clock repeaters/regenerators in the such memories is 'entirely conventional apart from the improvement in the body of the claims' also indicates that the intended use is not a limitation on the claim." *Id.* (quoting *Arctic Cat,* 919 F.3d at 1329–30).

Patent Owner argues that the entirety of claim 14's preamble is limiting. Prelim. Resp. 2–5. Specifically, Patent Owner argues that the "in a

synchronous semiconductor memory" "portion of the preamble is also limiting because it is necessary to understand what is meant by 'said clock signal' in the body of the claims." *Id.* at 2–3. Patent Owner argues that "the preamble makes clear that the recited 'clock signal' must be a 'clock signal *in a synchronous semiconductor memory*.'" *Id.* at 3. According to Patent Owner, "[t]his is consistent with the [S]pecification, which explains that 'the clock signal' is regenerated 'at different locations of the [synchronous] memory device 1000.'" *Id.* (citing Ex. 1001, 5:64–67) (third alteration in original). Patent Owner argues thus "'in a synchronous semiconductor memory' is not merely an intended purpose of the claimed method as the Petition claims, but rather a structural limitation that is necessary to fully understand the scope of the claimed 'clock signal.'" *Id.* (citing *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). Patent Owner argues that "the 'intended purpose' of the method is 'for regenerating a clock signal,' and 'in a synchronous semiconductor memory' provides a structural limitation on the recited 'clock signal.'" *Id.*

In addition, Patent Owner argues that the situation here is unlike that in *TomTom* "where the Federal Circuit explained that 'language stating a purpose or intended use' has a 'standard pattern of such language: the words "a method for a purpose or intended use comprising."' *Id.* at 4 (quoting *TomTom*, 790 F.3d at 1324). According to Patent Owner, "[s]uch a pattern is not applicable to the claim language in dispute here," as "the preamble does not recite 'a method for use in a synchronous memory device,' or otherwise provide language implying that practicing the method within a synchronous memory device is merely an 'intended purpose' of the invention." *Id.*; *see also id.* at n.1 (citing Pet. 26) (arguing that words that imply an intended use (e.g., for use) never appear in the preamble). Patent

Owner adds that "the fact that the words 'in a synchronous semiconductor memory' directly follow the limiting 'clock signal' indicates that those words act as a structural limitation on the clock signal itself." *Id.* at 5.

Lastly, Patent Owner argues that *Arctic Cat* is distinguishable "because in that case the claim language clearly recited an intended purpose of the invention: a 'module ***for*** a personal recreational vehicle,'" and "in contrast, the preamble does not recite 'a synchronous memory device' as an intended purpose of the method, but rather as a further limitation on the recited 'clock signal.'" *Id.* (citing *Arctic Cat*, 919 F.3d at 1328).

For purposes of institution, and based on the current record, we do not agree with Patent Owner that the entirety of the preamble is limiting. Federal Circuit precedent provides that just because a portion of a preamble is limiting does not mean that the entire preamble is limiting. *See, e.g.*, *TomTom*, 790 F.3d at 1323. Here, the preamble of claim 14 contains two distinct portions, with the second portion reciting "in a synchronous semiconductor memory." Ex. 1001, 10:11–12. The second portion does not provide antecedent basis for any part of the claim. *Id.* at 10:11–23. Nor does the second portion provide any necessary structure to the body of the claim. *Id.* In other words, claim 14 is structurally complete without the "in a synchronous semiconductor memory" language. *Id.* Thus, we conclude that the second portion of the preamble is not limiting. *See TomTom*, 790 F.3d at 1324 ("A preamble is not regarded as limiting . . . when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention.") (citation omitted).

At this stage of the proceeding, we find Patent Owner's arguments that the "in a synchronous semiconductor memory" language is

(i) "necessary to understand what is meant by 'said clock signal'" and (ii) a structural limitation modifying the claimed "clock signal" are unsupported and conclusory. Prelim. Resp. 3. We further find that the Specification does not limit "clock signal," as Patent Owner argues. *Id.* (citing Ex. 1001, 5:64–67). The Specification instead is replete with examples of clock repeaters and clock signals being employed without regard to a synchronous semiconductor memory. *See, e.g.*, Ex. 1001, code (57) (describing the '232 patent's teachings without limiting to a particular type of integrated circuitry and making no mention of memory), 2:44–61 (describing in the Summary of the Invention section the '232 patent's teachings without limiting to a memory), Figs. 5–8 (illustrating aspects of the '232 patent without limiting to a memory), 5:64–6:1.

Moreover, at this stage of the proceeding and based on the current record, we conclude that the "in a synchronous semiconductor memory" language in the context of claim 14 provides a purpose or an intended use for the method. Ex. 1001, 10:11–23. In other words, the method of claim 14 is intended to be used in a synchronous semiconductor memory. *Id.* As such, however, this means that the second portion of the preamble is not limiting here. *TomTom*, 790 F.3d at 1323 ("[A] preamble is not limiting 'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'") (citations omitted).

At this stage of the proceeding, we also find unavailing Patent Owner's arguments concerning that the "in a synchronous semiconductor memory" language in the preamble is not an intended use because it does not adhere to a "standard pattern." Prelim. Resp. 4–5 (citing *TomTom*, 790 F.3d at 1324; *Arctic Cat*, 919 F.3d at 1328). We do not view *TomTom* or *Arctic*

Cat as requiring using talismanic language with a particular pattern to recite a non-limiting intended use. *See TomTom*, 790 F.3d at 1324; *Arctic Cat*, 919 F.3d at 1328.

At this stage of the proceeding, we also find unavailing Patent Owner's argument that "in a synchronous semiconductor memory" appearing directly following the first portion of the preamble (i.e., "[a] method for regenerating a clock signal") indicates that the second portion of the preamble "act[s] as a structural limitation on the clock signal itself." Prelim. Resp. 5. Rather, at this stage of the proceeding, we conclude that the preamble comprises two distinct portions, and as we discuss above, Patent Owner does not explain how the second portion has a structural impact on the claimed clock signal—being employed in a memory is an intended use, and not a structural limitation.

Our conclusions here are preliminary and do not preclude the parties from arguing for proposed constructions during trial. A final determination as to claim construction will be made at the close of the proceeding, after any hearing, based on all the evidence of record. The parties are welcome to assert all of their claim construction arguments and evidence during trial, as permitted by our Rules.

IV. PRINCIPLES OF LAW

A claim is unpatentable under 35 U.S.C. § 102 "if each and every [claim] limitation is found either expressly or inherently in a single prior art reference." *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1273 (Fed. Cir. 2017). "A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present." *Akamai Techs., Inc. v. Cable & Wireless Internet Servs.,*

Inc., 344 F.3d 1186, 1192 (Fed. Cir. 2003) (citing *Rosco, Inc. v. Mirror Lite, Co.*, 304 F.3d 1373, 1380 (Fed. Cir. 2002)).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness, if present.[4] *See Graham*, 383 U.S. at 17–18. When evaluating a claim for obviousness, we also must "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

V. ALLEGED ANTICIPATION BY MASLEID

Petitioner argues that Masleid anticipates claim 14 of the '232 patent. Pet. 25–36. We have reviewed the parties' arguments and the evidence of record. For the reasons that follow, we determine that Petitioner demonstrates a reasonable likelihood that it would prevail in showing that Masleid anticipates claim 14.

[4] Patent Owner does not present arguments or evidence of such objective evidence of non-obviousness. *See generally* Prelim. Resp.

A. Summary of Masleid

Masleid "relates generally to systems and methods for distributing a data signal along a 'long wire' in an integrated circuit." Ex. 1004, 1:13–15. In particular, Masleid teaches "a complement reset buffer for use on long lines or when high-amplification is needed." *Id.* at 2:36–37. Figure 1, shown below, illustrates an embodiment in accordance with Masleid's teachings. *Id.* at 3:18–19.

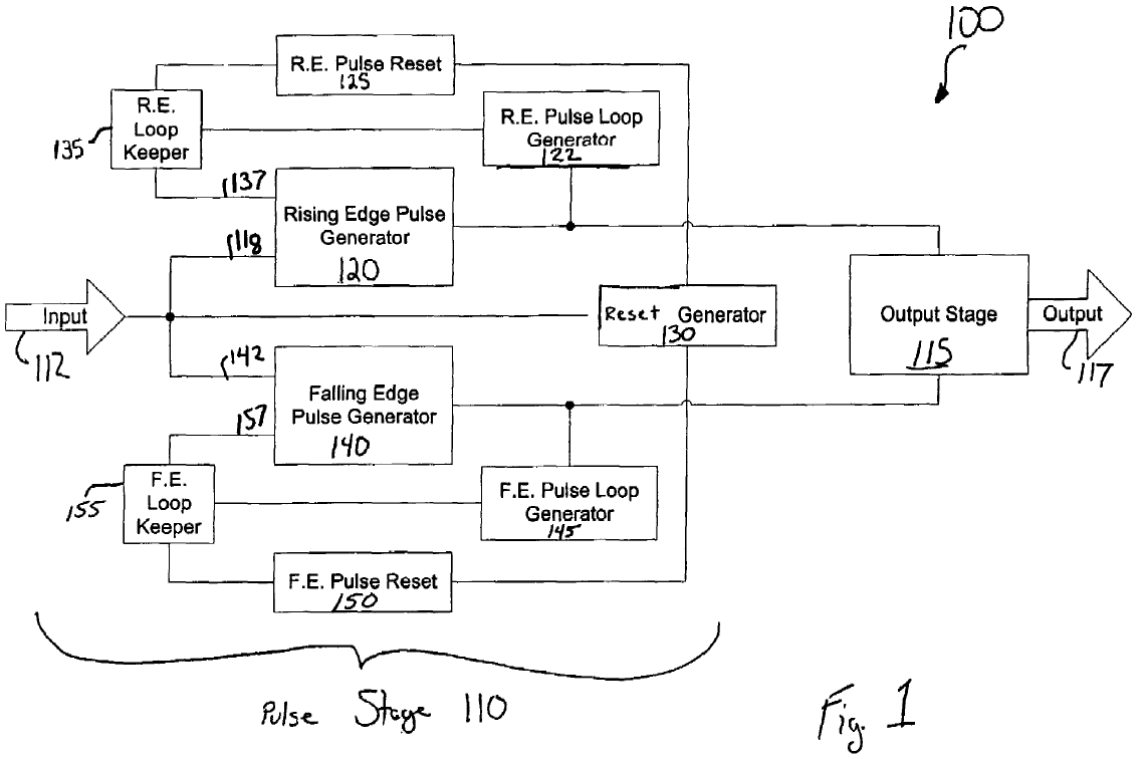

Figure 1 is a high-level block diagram of a buffer in accordance with Masleid's teachings. *Id.* at 3:63–64. As illustrated, "[t]he buffer 100 . . . includes a pulse stage 110 where pulses are generated from an input 112, and an output stage 115 where the pulses are used to create an output 117 that corresponds to the input 112." *Id.* at 3:64–4:1. Masleid discloses that "[t]he pulse stage 110 may also be divided into two separate circuits." *Id.* at 4:1–2. "The first circuit includes a rising-edge pulse generator 120, a rising-

edge pulse loop generator 122, a rising-edge loop keeper 135 and a rising-edge pulse reset 125." *Id.* at 4:18–20. "The first circuit is configured to react to the rising edge of input 112 and outputs a rising-edge pulse to the output stage 115 to trigger a transition in the output 117." *Id.* at 4:2–5. More specifically, "[i]n operation, the first circuit receives the data on input 112 at a first input 118, and outputs a rising-edge pulse to drive the output stage 115 when a rising edge is detected." *Id.* at 4:23–25.

Masleid discloses that "[t]he second circuit is configured to react to the falling edge of input 112 and outputs a falling-edge pulse to the output stage 115 to trigger a transition in the output 117." *Id.* at 4:6–9. The structure of the second circuit is similar to the structure of the first circuit, and "includes a falling-edge pulse generator 140 which receives input 112 at a first input 142, and outputs a falling-edge pulse to the output stage 115 . . . in response to a detected falling edge on the input 112." *Id.* at 5:25–31.

B. Challenged Claim 14

1. Regenerating a Clock Signal (Preamble)

Petitioner argues that Masleid discloses "[a] method for regenerating a clock signal in a synchronous semiconductor memory," as recited in the preamble of claim 14. Pet. 27–28. More specifically, Petitioner argues that Masleid discloses that its complement reset buffer is "suitable for applications requiring speed, efficiency, and the ability to handle long-wire distances," and "may be advantageously used to speed up ***clock distribution*** while reducing clock skew in an integrated circuit, or may be used to decrease access times for cache memory (i.e. wires such as L2 or L3 routes.)." *Id.* at 27 (quoting Ex. 1004, 15:62–16:3; citing Ex. 1003 ¶ 47).

In addition, Petitioner argues that Masleid discloses that "[t]he buffer 100 generally includes a pulse stage 110 where pulses are generated from an

input 112, and an **output stage 115 where pulses are used to create an output 117 that corresponds to the input 112**." *Id.* at 28 (citing Ex. 1004, 3:64–4:1, Fig. 1). According to Petitioner, "[c]reating an output that corresponds to an input clock signal constitutes regenerating the input clock signal, as recited in the preamble." *Id.* (citing Ex. 1003 ¶ 48).

Patent Owner disputes that Masleid discloses the preamble. Prelim. Resp. 5. In particular, Patent Owner argues that "[t]he Petition concedes that Masleid does not disclose a 'clock signal in a synchronous semiconductor memory,'" and thus, Petitioner fails to show that Masleid discloses the preamble. *Id.* (citing Pet. 27).

We find, at this stage of the proceeding and based on the current record, that Petitioner sufficiently demonstrates that Masleid discloses a method for regenerating a clock signal, which is the limiting portion of the preamble. More specifically, for purposes of institution, we agree with Petitioner and find that Masleid discloses regenerating a clock signal via Masleid's disclosure of the buffer 100 having "a pulse stage 110 where pulses are generated from an input 112, and an output stage 115 where pulses are used to create an output 117 that corresponds to the input 112." Ex. 1004, 3:64–4:1, Fig. 1; Ex. 1003 ¶ 48.

At this stage of the proceeding, we find unavailing Patent Owner's argument concerning Masleid failing to disclose that the regenerating of a clock signal occurs "in a synchronous semiconductor memory." Prelim. Resp. 5. As we discuss above in our claim construction analysis, this second portion of the preamble is not limiting. *See supra* Section III (construing only the first portion of the preamble to be limiting). Thus, Patent Owner's arguments are inapposite because they are directed to limitations (i.e., "in a synchronous semiconductor memory") not required by the claim. *See In re*

Hiniker Co., 150 F.3d 1362, 1369 (Fed. Cir. 1998) (finding "the name of the game is the claim"); *cf. In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating limitations not appearing in the claims cannot be relied upon for patentability).

2. Detecting a Rise Edge and a Fall Edge

Petitioner argues that Masleid discloses "detecting a rise edge from a low logical level and a fall edge from a high logical level of said clock signal," as recited in claim 14. Pet. 28–30. More specifically, Petitioner argues that Masleid's edge detector "comprises first and second circuits that sense, respectively, a rising edge from a low logical level of a clock signal to generate a pull-up control signal, and falling edge from a high logical level of a clock signal to generate a pull-down control signal." *Id.* at 28–29.

First, Petitioner argues that "Masleid discloses that 'the first circuit is configured to react to the rising edge of input 112 and outputs a rising-edge pulse to the output stage 115 to trigger a transition in the output 117.'" *Id.* at 29 (quoting Ex. 1004, 4:2–5; citing Ex. 1004, Fig. 1). "Specifically, the rising edge pulse generator 120 of Masleid detects (i.e., senses) a rising edge from (or near) a low logical level by sensing changes in the voltage level of the clock signal with P- and N-skewed gates," according to Petitioner. *Id.* (citing Ex. 1003 ¶ 50). In particular, Petitioner argues that "Masleid describes NAND gate 205 as an N-skewed gate that responds quickly to a rising edge." *Id.* (citing Ex. 1004, 5:63–66, Fig. 2). "Thus, the rising edge pulse generator 120 of Masleid detects (i.e., senses) a rising edge from (or near) a low logical level," according to Petitioner. *Id.* (citing Ex. 1003 ¶ 51).

Second, Petitioner argues that Masleid "discloses a second circuit, complementary to the first circuit, that is 'configured to react to the falling edge of input 112 and outputs a falling-edge pulse to the output stage 115 to

trigger a transition in the output 117.'" *Id.* at 30 (quoting Ex. 1004, 4:6–10). "Specifically, falling edge pulse generator 140 detects/senses a falling edge from (or near) a high logical level," according to Petitioner. *Id.* In particular, Petitioner argues that "[t]he pulse generator 140 includes a P-skewed NOR gate 245" for this. *Id.* (citing Ex. 1004,[5] 7:7–16; Ex. 1003 ¶¶ 52–54).

After reviewing Petitioner's arguments and evidence, which Patent Owner does not address at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Masleid discloses "detecting a rise edge from a low logical level and a fall edge from a high logical level of said clock signal."

3. Generating a Pull-Up Control Signal

Petitioner argues that Masleid discloses "generating a pull-up control signal in response to the detecting of the rise edge of the clock signal," as recited in claim 14. Pet. 31–32. More specifically, Petitioner argues that Masleid discloses "that the first circuit (i.e., the rising edge detection circuit . . .) 'receives the data on input 112 at a first input 118, and ***outputs a rising-edge pulse to drive the output stage 115 when a rising edge is detected***.'" *Id.* at 31 (quoting Ex. 1004, 4:23–25). Petitioner argues that Masleid discloses that "[t]he output stage 115 includes a PFET transistor 275, an NFET transistor 280, and a weak keeper buffer 285." *Id.* (quoting Ex. 1004, 8:3–4). Petitioner argues that Masleid discloses that "[t]he gate of PFET 275 is coupled to the output of NAND gate 205 of rising edge pulse generator 120, its source is coupled to a logical '1,' and the drain is coupled

[5] The Petition contains a typographical error and mistakenly cites to Exhibit 1001. Pet. 30. The context and the cited column and line numbers clearly show that Exhibit 1004 was meant.

to output 117 and NFET 280." *Id.* (citing Ex. 1004, 8:4–7). Petitioner argues that in Masleid, "PFET 275 switches on when the first circuit (i.e., the rising edge circuit) is active and generates a pulse." *Id.* (citing Ex. 1004, 8:10–11; Ex. 1003 ¶ 55).

According to Petitioner, Masleid discloses that "[w]hen the PFET 275 switches on as a result of the pulse from the rising edge pulse generator, the PFET 275 ***pulls up*** the output 117 (node F) to a logical '1.'" *Id.* (citing Ex. 1004, 9:19–24, Figs. 9a–9b). Masleid discloses that "[t]he transition 910 causes the NAND 205 to generate 952 a logical '0' at 'C' [and] 'C' then drives 954 'F' [the output] high since the PFET 275 is active and pulls 'F' up," according to Petitioner. *Id.* (citing Ex. 1003 ¶ 76) (third alteration in original). Petitioner argues "[t]hus, the output of the NAND gate 205 of rising edge pulse generator 120 is a 'pull-up control signal' that is generated in response to the detection of the rise edge of the clock signal at node A." *Id.* at 31–32 (citing Ex. 1003 ¶¶ 56–57).

After reviewing Petitioner's arguments and evidence, which Patent Owner does not address at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Masleid discloses "generating a pull-up control signal in response to the detecting of the rise edge of the clock signal."

4. Generating a Pull-Down Control Signal

Petitioner argues that Masleid discloses "generating a pull-down control signal in response to the detecting of the fall edge of said clock signal," as recited in claim 14. Pet. 32–33. More specifically, Petitioner argues that Masleid discloses that "the second circuit generates a falling-edge pulse signal to pull the output 'F' low at NFET 280." *Id.* at 32

(citing Ex. 1004, 9:49–59, Figs. 9a–9b; Ex. 1003 ¶ 59). According to Petitioner, Masleid discloses that "[t]he second circuit is configured to react to the falling edge of input 112 and ***outputs a falling-edge pulse to the output stage 115 to trigger a transition in the output 117***." *Id.* (quoting Ex. 1004, 4:6–10). In Masleid, "[t]he second circuit includes a falling-edge pulse generator 140 which receives input 112 at a first input 142, and outputs a falling-edge pulse to the output stage 115 . . . in response to a detected falling edge on the input 112," according to Petitioner. *Id.* (quoting Ex. 1004, 5:27–31; Ex. 1003 ¶ 59).

According to Petitioner, Masleid discloses "that the output of the complementary falling-edge pulse generator 140 at node C' is coupled to the gate of NFET 280." *Id.* (citing Ex. 1004, 8:7–10). Petitioner argues that Masleid discloses that "[t]he NFET 280 switches on when the second circuit (i.e., the falling edge circuit) is active and generates a pulse." *Id.* at 32–33 (citing Ex. 1004, 8:10–11). "Because the drain of NFET 280 is coupled to ground and it is switched on when it receives a pulse from the falling edge pulse generator 140, the output 177 at node F is ***pulled down***," according to Petitioner. *Id.* at 33 (citing Ex. 1004, 9:52–55, Figs. 9a–9b). Petitioner argues, "[t]hus, the output of the NOR gate 245 of falling edge pulse generator 140 (node C') is a 'pull-down control signal' that is generated in response to the detection of the fall edge of the clock signal at node A." *Id.* (citing Ex. 1003 ¶ 60).

After reviewing Petitioner's arguments and evidence, which Patent Owner does not address at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Masleid discloses "generating a pull-down control signal in response to the detecting of the fall edge of said clock signal."

5. Recovering Said High Logical Level

Petitioner argues that Masleid discloses "recovering said high logical level using the pull-up control signal," as recited in claim 14. Pet. 33–35. More specifically, Petitioner argues that Masleid discloses an output driver, which is the component that recovers the high (and low) logical levels using the pull-up and pull-down control signals. *Id.* at 33. According to Petitioner, Masleid discloses that "[i]n operation, the first circuit receives the data on input 112 at a first input 118, and outputs a rising-edge pulse to drive the output stage 115 when a rising edge is detected." *Id.* at 34 (quoting Ex. 1004, 4:23–25; citing Ex. 1003 ¶ 63). Petitioner argues that Masleid discloses that "[t]he output stage 115 includes a PFET transistor 275, an NFET transistor 280, and a weak keeper buffer 285." *Id.* at 34–35 (quoting Ex. 1004, 8:3–4). According to Petitioner, Masleid discloses that "[o]utput stage 115 is configured to transfer the input signal 112 to the output 117 as quickly as possible, with higher gain and faster transitions." *Id.* at 35 (citing Ex. 1004, 8:26–29). "In particular, Masleid teaches that the signal 'C' of the rising edge pulse generator 120 causes PFET 275 to pull the output 'F' of output stage 115 up, thereby recovering the high logical level of the clock input 112 using the pull-up control signal," according to Petitioner. *Id.* (citing Ex. 1004, 9:19–26, Figs. 9a–9b; Ex. 1003 ¶ 64).

After reviewing Petitioner's arguments and evidence, which Patent Owner does not address at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Masleid discloses "recovering said high logical level using the pull-up control signal."

6. Recovering Said Low Logical Level

Petitioner argues that Masleid discloses "recovering said low logical level using the pull-down control signal," as recited in claim 14. Pet. 35. More specifically, Petitioner argues that "Masleid's clock repeater also recovers the low logical level of the clock input 112 in the same way it recovers the complementary high logical level." *Id.* (citing Ex. 1004, 4:11–17). "In particular, when the falling-edge pulse generator 140 is active, the pull-down signal 'C' causes NFET 280 to activate, which pulls the output 'F' of output stage 115 low to recover the low logical level of the clock input 112," according to Petitioner. *Id.* (citing Ex. 1004, 9:49–59, Figs. 9a–9b). Petitioner argues thus Masleid discloses the claimed step. *Id.* (citing Ex. 1003 ¶¶ 66–67).

After reviewing Petitioner's arguments and evidence, which Patent Owner does not address at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Masleid discloses "recovering said low logical level using the pull-down control signal."

7. Summary

In summary, based on the current record, and for purposes of this institution decision, we determine that Petitioner demonstrates a reasonable likelihood that it would prevail in showing that Masleid anticipates claim 14.

VI. REMAINING OBVIOUSNESS GROUNDS

Petitioner argues that (i) Masleid alone renders claim 14 obvious; and (ii) the combination of Masleid and Kono renders claim 14 obvious. Pet. 36–40. Petitioner already has demonstrated a reasonable likelihood of success in proving that claim 14 is unpatentable. In order to provide guidance to the parties, however, we address Patent Owner's arguments

regarding these obviousness grounds. Consolidated Trial Practice Guide (November 2019)[6] 6 ("If a trial is instituted, the Board generally will provide analysis of the strengths and weaknesses of all challenges in the petition in order to provide guidance to the parties for the upcoming trial.").

A. Summary of Kono

Kono is titled "Semiconductor Memory Device Including Clock Generation Circuit." Ex. 1005, code (54). Kono "relates to a semiconductor memory device, and more particularly to a semiconductor memory device including a clock generation circuit which operates synchronously with the rise and fall of an external clock and which generates an internal clock signal synchronized with the external clock." *Id.* at 1:8–13. In particular, Kono teaches a "[s]emiconductor memory device which operates synchronously with the rise and fall of an external clock and which enables the reduction of a circuit area by generating an operation clock for driving a data output circuit in a prior stage to a data output circuit." *Id.* at 6:11–17.

B. Combining Masleid with Kono

Petitioner argues that one of ordinary skill in the art "would . . . have been motivated to modify Kono's synchronous memory . . . by replacing [Kono's] repeaters 120 with Masleid's improved clock buffer . . . to improve manufacturing yield in existing synchronous semiconductor memory devices and to allow for faster speed and greater distribution line distances." *Id.* at 37–38 (citing Ex. 1003 ¶ 75). Petitioner argues that Masleid teaches that its invention is "'suitable for applications requiring speed, efficiency, and the ability to handle long-wire distances,' and 'may be advantageously used to speed up ***clock distribution*** while reducing clock skew in an integrated

[6] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

circuit.'" *Id.* at 38 (citing Ex. 1004, 15:62–16:3). "Masleid also states that [its] improved buffer can be used in both synchronous and asynchronous applications," according to Petitioner. *Id.* (citing Ex. 1004, 16:7–67, Fig. 8; Ex. 1003 ¶ 78). Petitioner adds that Masleid "recognized the deficiencies of relatively primitive clock buffers like the clock repeater 120 described in Kono." *Id.* at 36 (*comparing* Ex. 1005, 11:25–33, Fig. 5 (Petitioner arguing that Kono "depict[s] clock repeater 120 as implemented with two sets of inverters connected in series"), *with* Ex. 1004, 1:38–2:32 (Petitioner arguing that Masleid "describ[es] the deficiencies of conventional buffers 'implemented as one or two inverters in series' and the need for an improved clock buffer")). Petitioner argues that therefore one of ordinary skill in the art "would . . . have found it obvious to use Masleid's buffer in a synchronous memory." *Id.* at 38 (citing Ex. 1003 ¶ 79).

Furthermore, Petitioner argues that "[t]he use of clock repeaters in synchronous memory circuits was well-known in the art." *Id.* (citing Ex. 1005, Fig. 2). According to Petitioner, one of ordinary skill in the art "would have recognized that Masleid's description of using the improved Masleid buffer 'to speed up clock distribution' could be applied to synchronous memories like Kono's . . ., and would have been motivated to modify Kono's [memory device] with Masleid's improved buffer." *Id.* at 38–39 (citing Ex. 1003 ¶ 79).

At this stage of the proceeding, we find that Petitioner has provided sufficiently articulated reasoning with rational underpinning to support Petitioner's modifications of Kono with Masleid. *See Kahn*, 441 F.3d at 988 (citations omitted), *cited with approval in KSR*, 550 U.S. at 418.

At this stage of the proceeding, we find unavailing Patent Owner's argument that the Petition does not allege, nor provide any analysis

regarding, a reasonable expectation of success for combining Masleid and Kono as done in the Petition. Prelim. Resp. 6. At this stage of the proceeding, we instead find that Petitioner has provided analysis and evidence to support that one of ordinary skill in the art would have had a reasonable expectation of success in using Masleid's buffer in a synchronous memory like the one taught in Kono. For example, as cited by Petitioner, Masleid teaches that its invention is "'suitable for applications requiring speed, efficiency, and the ability to handle long-wire distances,' and 'may be advantageously used to speed up ***clock distribution*** while reducing clock skew in an integrated circuit.'" Ex. 1004, 15:62–16:3 (emphasis added). This passage explicitly teaches using Masleid's clock buffer widely in integrated circuits, and evidences that one of ordinary skill in the art, being told to do so is suitable, would have a reasonable expectation of success in using Masleid's buffer in other integrated circuitry, such as a synchronous memory. *Id.*

As another example, and as explained by Petitioner, Masleid teaches that its clock buffer is an improvement over clock buffers used in conventional integrated circuits (e.g., the clock buffers taught in Kono), which at this stage of the proceeding we find teaches one of ordinary skill in the art to have a reasonable expectation of success in using Masleid's clock buffer in lieu of Kono's clock buffer. *See* Ex. 1004, 1:38 –2:32; Ex. 1005, 11:25–33, Fig. 5. And, Petitioner's expert, Dr. Subramanian, testifies that "Kono expressly discloses the context in which the clock repeater of Masleid *could be used* within a semiconductor memory." Ex. 1003 ¶ 79 (emphasis added). This testimony is at least probative of whether one of ordinary skill in the art would have had a reasonable expectation of success in combining the teachings of Masleid and Kono.

Lastly, we find nothing talismanic about the use of the phrase "reasonable expectation of success," which Petitioner does not recite verbatim, and instead find Petitioner's arguments and cited evidence show that one of ordinary skill in the art would have had a reasonable expectation of success in making the proffered combination.

C. Summary

We have reviewed the evidence and the parties' arguments regarding (i) Masleid alone rendering claim 14 obvious; and (ii) the combination of Masleid and Kono rendering claim 14 obvious. Based on the current record, and for purposes of this institution decision, we determine that Petitioner shows a reasonable likelihood that it would prevail in showing that claim 14 would have been obvious to one of ordinary skill in the art in view of these grounds.

VII. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail in proving the unpatentability of claim 14 of the '232 patent. We thus institute an *inter partes* review of claim 14 of the '232 patent on all grounds asserted in the Petition. *See* 37 C.F.R. § 42.108(a).

Any findings or conclusions in this Decision are made only for the purposes of institution and are not dispositive of any issue. We have not made a final determination with respect to the patentability of the challenged claim. Our final determination will be based on the record as fully developed during trial, including any evidence or argument timely presented by the parties under our Rules.

VIII. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '232 patent is instituted on the challenged claim and all grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this Decision.

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