

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

JUNIPER NETWORKS, INC.
Petitioner,

v.

SMART PATH CONNECTIONS, LLC,
Patent Owner.

IPR2021-01356
Patent 7,697,525 B2

Before JAMESON LEE, DAVID C. McKONE, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Juniper Networks, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–24 (the “challenged claims”) of U.S. Patent No. 7,697,525 B2 (Ex. 1001, “the ’525 patent”). Paper 1 (“Pet.”). Smart Path Connections LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). Petitioner filed an authorized Preliminary Reply. Paper 8 (“Prelim. Reply”). Patent Owner filed an authorized Preliminary Sur-Reply. Paper 9 (“Prelim. Sur-Reply”).

We have authority to determine whether to institute an *inter partes* review, under 35 U.S.C. § 314 and 37 C.F.R. § 42.4. An *inter partes* review may not be instituted unless it is determined that “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018); *see also* 37 C.F.R. § 42.4(a) (2021) (“The Board institutes the trial on behalf of the Director.”). The “reasonable likelihood” standard is “a higher standard than mere notice pleading,” but “lower than the ‘preponderance’ standard to prevail in a final written decision.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

For the reasons provided below and based on the record before us, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review on all challenged claims and on each ground set forth in the Petition.

B. Real Parties in Interest

Petitioner states that its real party-in-interest is Juniper Networks, Inc. Pet. xi. Patent Owner states that its real-party-in-interest is Smart Path Connections, LLC. Paper 4, 1.

C. Related Proceedings

Petitioner identifies the following as related litigation involving the '525 patent: *Smart Path Connections, LLC v. Juniper Networks, Inc.*, No. 6:21-cv-327 (W.D. Tex.). Pet. xi. Patent Owner identifies the following as related litigation involving the '525 patent: *Smart Path Connections, LLC v. Juniper Networks, Inc.*, No. 6:21-cv-328 (W.D. Tex.). Paper 4, 1. It appears that the two referenced district court cases are the same case and the correct case number is: 6:21-cv-00328 (W.D. Tex.). Both parties identify IPR2021-01170 as an *inter partes* review involving a related patent. Pet. xi; Paper 4, 1.

D. The '525 Patent (Ex. 1001)

The '525 patent relates to methods and systems for forwarding multicast traffic in communication networks. Ex. 1001, 1:6–8. The '525 patent discloses use of a link aggregation (“LAG”) group. *Id.* at code (57). A LAG is defined as follows:

Link aggregation (LAG) is a technique by which a group of parallel links between two endpoints in a data network can be joined together into a single logical link (referred to as a “LAG group”). Traffic transmitted between the endpoints is distributed among the physical links in a manner that is transparent to the clients that send and receive the traffic.

Id. at 1:25–30. The '525 patent describes a network node including a plurality of ports at least a subset of which is grouped in a LAG group. *Id.* at 1:40–43. The network node also includes packet processing logic,

coupled to receive data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of the ports in the LAG group and to forward only a single copy of each of the data packets via the output ports in the LAG group, while distributing the copies among the ports in the LAG group to balance the traffic load in the LAG group. *Id.* at 1:44–52. The network node includes line cards that are connected to the ports and a switching fabric that interconnects the line cards. *Id.* at 1:54–56.

The packet processing logic allocates to each of the received packets a fabric multicast identification (“FMID”) value selected from a range of possible FMID values. *Id.* at 2:7–10. Each FMID value is associated with one of the ports in the LAG, and the packet processing logic forwards a single copy of the data packet to the port associated with the allocated FMID value for that packet. *Id.* at 2:7–11. In one embodiment, a line card allocates a line card FMID (“LC-FMID”) to each received packet, and then the switching fabric maps the LC-FMID values to respective central FMID (C-FMID) values selected from a second range of possible C-FMID values that is smaller than the first range of values for the LC-FMID value. *Id.* at 2:41–47. Thereafter, the switching fabric forwards the data packets responsively to the C-FMID values. *Id.* at 2:48–49.

Figure 1 of the '525 patent shows a network node:

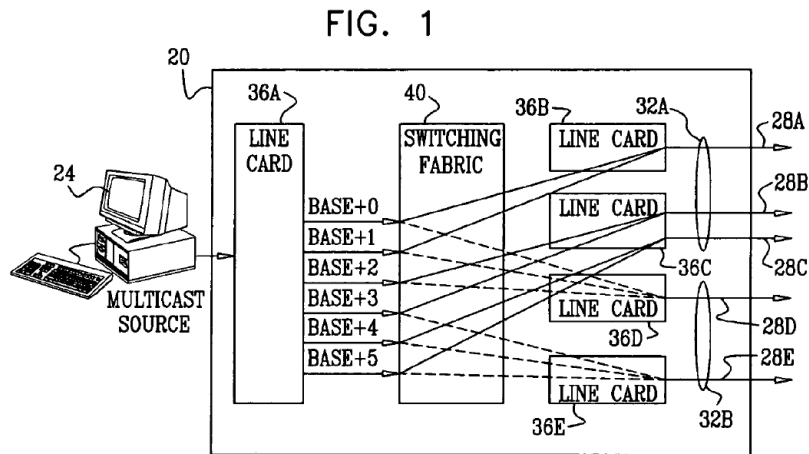


Figure 1 is a block diagram illustrating a network node. *Id.* at 3:7–9.

As shown in Figure 1, node 20 accepts multicast packets (having multiple destination addresses) from multicast source 24 and forwards the packets to two CTPs (connection termination ports) 32A and 32B. *Id.*

at 2:44–46. The '525 patent describes:

CTP 32A comprises three physical ports 28A . . . 28C, which are configured as a LAG group. CTP 32B comprises two physical ports 28D and 28E, which are configured as another LAG group. The terms CTP and LAG group are sometimes used interchangeably below. Node 20 may comprise additional CTPs (not shown in the figure), which comprise a single physical port. Such single ports are often regarded and managed by the node as LAG groups having a single member.

Id. at 2:47–54.

“Node 20 comprises line cards, which process the data packets entering and leaving the node.” *Id.* at 2:64–65. Referring to Figure 1, the '525 patent describes:

[N]ode 20 comprises five line cards denoted 36A . . . 36E. Line card 36A, which is referred to hereinbelow as the ingress card, accepts multicast packets from multicast source 24. Line cards 36B . . . 36E, which are referred to hereinbelow as the egress cards, are connected to the different output ports. Note that

output ports belonging to a particular LAG group may be served by different line cards.

Id. at 5:1–8. Switching fabric 40 accepts packets from the ingress cards and routes them to the appropriate egress cards. *Id.* at 5:9–11. Node 20 forwards only a single copy of a multicast packet to each LAG group, and distributes the forwarding approximately evenly among the different ports within a LAG group. *Id.* at 5:37–50.

Each multicast source 24 is assigned a range of N virtual addresses called fabric multicast IDs (“FMIDs”), and the ingress line card assigns one of the N FMIDs to each multicast packet arriving from the multicast source while attempting to distribute the packets approximately evenly among the different FMIDs in the range. *Id.* at 5:63–6:4. “The multicast packets are provided to fabric 40 along with their respective FMIDs. Both fabric 40 and the egress cards are pre-configured to forward each multicast packet to the appropriate output port based on its FMID.” *Id.* at 6:19–22. Fabric 40 may include a forwarding table, which maps FMIDs to line cards, and each line card includes another forwarding table, which maps FMIDs to output ports. *Id.* at 6:22–27. “Thus, each multicast packet is assigned an FMID by the ingress card, and then forwarded to a particular output port by the fabric and egress card, based on its FMID.” *Id.* at 6:27–30.

For some embodiments, the ’525 patent describes:

In some embodiments, the total number of allocable FMIDs is lower in the switching fabric than in the line cards. In other words, fabric 40 may have an FMID space having a smaller number of bits than the FMID space of the line cards. For example, the line cards may support 13-bit FMIDs, referred to hereinbelow as line card FMIDs (LC-FMIDs), while the fabric may only support 11-bit FMIDs, referred to as central FMIDs (C-FMIDs). In these cases, multiple LC-FMIDs correspond to a particular C-FMID. Depending on the fabric definition, the C-

FMID may comprise, for example, the least significant bits (LSB) or the most significant bits (MSB) of the LC-FMID.

The fabric forwards copies of the multicast packet to all egress cards having at least one output port that corresponds to the C-FMID. Because the association of multiple LC-FMIDs to a single C-FMID, superfluous multicast packets may be forwarded to egress cards unnecessarily, which causes unnecessary packet duplication and adds an unnecessary load to the interface between the fabric and the egress cards. The superfluous copies are typically discarded by the egress cards.

Id. at 8:35–55.

E. Illustrative Claims

Of challenged claims 1–24, claims 1 and 12 are independent. Claims 1 and 12 are illustrative and are reproduced below, with bracketed internal section numbering added to correspond to the labeling used by Petitioner:

1. [1.Pre] A network node in a communication network, comprising:
 - [1.1] a plurality of ports, at least a subset of which is grouped in a link aggregation (LAG) group; and packet processing logic, which is coupled to receive data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of the ports and
 - [1.2] to process the data packets so as to forward only a single copy of each of the data packets via the output ports in the subset, while distributing forwarded copies of the data packets among the output ports in the subset so as to balance a traffic load within the LAG group;
 - [1.3] wherein:

the packet processing logic is arranged to allocate to each of the received data packets a fabric multicast identification (FMID) value selected from a range of possible FMID values, each FMID being associated with

one of the ports in the subset, and to forward the single copy to the port associated with the allocated FMID value;

- [1.4] the packet processing logic comprises multiple line cards connected to the ports and a switching fabric interconnecting the line cards, wherein, for each of the received data packets, a first line card connected to a first port via which the data packet is received is arranged to allocate the FMID value to the packet and to forward the packet to the switching fabric, and
- [1.5] wherein the switching fabric and a second line card connected to a second port to which the data packet is to be sent are configured to forward the data packet responsively to the FMID value; and
- [1.6] the first line card is arranged to assign to the data packets line card FMID (LC-FMID values selected from a first range of possible LC-FMID values, and wherein the switching fabric is arranged to map the LC-FMID values to respective central FMID (C-FMID values selected from a second range of possible C-FMID values that is smaller than the first range and to forward the data packets responsively to the C-FMID values.

Ex. 1001, 10:15–55.¹

12. [12.Pre] A method of communication, comprising:

- [12.1] receiving data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of a plurality of ports, at least a subset of which is grouped in a link aggregation (LAG) group; and

¹ We read “(LC-FMID” in the claim as having the same meaning as “(LC-FMID)” and “(C-FMID” in the claim as having the same meaning as “(C-FMID),” as Petitioner suggests (Pet. vi n.2), because in both instances a close parenthesis character appears to be inadvertently left out of the claim. Patent Owner does not oppose Petitioner’s suggestion. It is reasonable to read the terms the same as though the close parenthesis is present. We recognize no other meaning.

[12.2] processing the data packets so as to forward only a single copy of each of the data packets via the output ports in the subset while distributing forwarded copies of the data packets among the output ports in the subset so as to balance a traffic load within the LAG group;

[12.3] wherein:

processing the data packets comprises allocating to each of the received data packets a fabric multicast identification (FMID) value selected from a range of possible FMID values, the FMID value being associated with one of the ports in the subset, and forwarding the single copy to the port associated with the allocated FMID value;

[12.4] for each of the received data packets, processing the data packets comprises allocating the FMID value to the data packet by a first line card connected to a first port via which the data packet is received, and

[12.5] configuring a second line card connected to a second port to which the data packet is to be sent and a switching fabric interconnecting the first and second line cards to forward the data packet responsively to the FMID value; and

[12.6] allocating the FMID value comprises assigning to the data packets line card FMID (LC-FMID) values selected from a first range of possible LC-FMID values, and wherein configuring the switching fabric comprises mapping the LC-FMID values to respective central FMID (C-FMID) values selected from a second range of possible C-FMID values that is smaller than the first range and forwarding the data packets responsively to the C-FMID values.

Id. at Ex. 1001, 11:34–12:3.²

² We read “(LC-FMID)” in the claim as having the same meaning as “(LC-FMID),” as Petitioner suggests (Pet. viii n.5), because a close parenthesis character appears to be inadvertently left out of the claim. Patent Owner does not oppose Petitioner’s suggestion. It is reasonable to read the terms

F. Evidence Relied on by Petitioner

Petitioner relies on the following evidence:³

References		Date	Exhibit
Devi	U.S. Pub. App. 2005/0238018 A1	Published Oct. 27, 2005	Ex. 1005
Mazzola	U.S. Patent 5,740,171	Issued Apr. 14, 1998	Ex. 1007
Borgione	U.S. Patent 8,155,125 B1	Issued Apr. 10, 2012	Ex. 1006

Petitioner also relies on the Declaration of Tal Lavian, Ph.D.
(Ex. 1003).

G. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–24 of the
'525 patent based on the following grounds:

Claims Challenged	35 U.S.C. § ⁴	Reference(s)/Basis
1–24	103(a)	Devi, Mazzola
1–24	103(a)	Borgione, Mazzola

the same as though the close parenthesis is present. We recognize no other meaning.

³ The '525 patent issued from Application 11/644,773, filed Dec. 21, 2006. Ex. 1001 at codes (21), (22). The '525 patent does not claim priority to earlier filed application.

⁴ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), included revisions to 35 U.S.C. § 103 that became effective after the filing of the application that led to the '525 patent. Therefore, we apply the pre-AIA version of 35 U.S.C. § 103.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art at the time of the alleged invention “would have had a bachelor’s degree in electrical engineering, computer engineering, computer science, or a closely related field, and three to four years of experience in the design and development of telecommunication networks, systems, equipment, and components.” Pet. 7. Alternatively, Petitioner contends that a POSITA “would have [had] a Master’s degree or similar post-graduate work in electrical engineering, computer engineering, computer science, or a closely related field, and fewer years of design and development experience.” *Id.*

Patent Owner at this stage takes no position with regard to what constitutes the level of ordinary skill in the art. Prelim. Resp. 27.

Petitioner’s assertion is supported by the testimony of Dr. Lavian. Ex. 1003 ¶¶ 91–100. Petitioner’s assertion also appears consistent with the content of the applied prior art references. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

Accordingly, in the absence of a contrary contention by Patent Owner, we adopt Petitioner’s proposed level of ordinary skill in the art, as stated in two alternatives noted above.

B. *Claim Construction*

We use the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and

the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). The claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) is applicable.

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and even extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

The specification may reveal a special definition given to a claim term by the patentee, or the specification or prosecution history may reveal an intentional disclaimer or disavowal of claim scope by the inventor. *Id.* at 1316. If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The disavowal, if any, can be effectuated by language in the specification or the prosecution history. *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016).

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner has not proposed a specific construction for any claim term, and states that no express construction is needed. Pet. 7. Further, Petitioner states that it understands each claim term according to its plain and ordinary meaning. *Id.* Pet. 6. Patent Owner also has not proposed a specific construction for any claim term. Prelim. Resp. 9.

We agree with Petitioner that no express claim construction of any claim term is necessary for this Decision.

C. Alleged Obviousness of Claims 1–24 over Borgione and Mazzola

1. The Law on Obviousness

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results (“the *Graham* factors”). *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

When evaluating a combination of teachings, we must also “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

2. Overview of Borgione

Borgione relates to transmitting multicast data packets across an aggregate of network connections between two network nodes. Ex. 1006, 1:7–10. It is described that pre-existing methods create a load imbalance for multicast packets among the plurality of network links. *Id.* at 3:37–49. Borgione states that its disclosed invention balances the transmission of multicast packets among an aggregate of network links that provide a logical channel or link between network nodes. *Id.* at 5:28–30.

Borgione discloses a method, system, and apparatus for transmitting multicast data packets over a plurality of physical network links that have been combined into one logical channel, in a manner that the packets are distributed over more than one network link. *Id.* at code (57), 3:60–64.

Figure 1 is reproduced below:

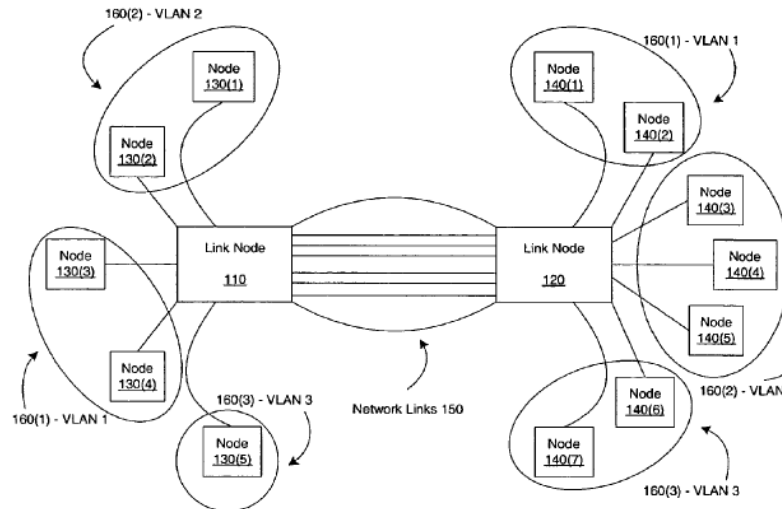


Figure 1

Figure 1 is a block diagram illustrating the network topology. Ex. 1006, 5:11–12. Link node 110 may be a switch, bridge, router, or a hub. *Id.* at 1:30–31. Link node 110 is connected to link node 120 through a plurality of network links 150, and link 120 also may be a switch, bridge, router, or a

hub. *Id.* at 1:37–40. The plurality of network links 150 between link nodes 110 and 120 are aggregated as a single logical link over which all traffic between link nodes 110 and 120 is distributed. *Id.* at 1:57–60, 1:66–67. Routing protocols see the aggregated links as a single interface with a common IP address. *Id.* at 2:5–7. Link nodes 110 and 120 are in separate locations and each has its own associated local area network (“LAN”). *Id.* at 1:55–67.

Borgione describes a first network node selecting a destination interface identifier for an outgoing multicast packet, selecting one of the plurality of network links using the destination interface identifier, and transmitting the outgoing multicast packet to the second network node over the selected network link. *Id.* at 4:16–21. Borgione explains:

An added tag header can be used [for each multicast packet] to include a destination interface identifier. For example, in a VLAN network environment, such a tag header is included in packets per IEEE Std. 802.1Q. A portion of an IEEE Std. 802.1Q tag header is a VLAN identifier (VID), which is unique to a particular VLAN. A destination interface identifier within a tag header can be used to select which network link in a logical link is to be used to transmit a replicated multicast packet. Since the destination interface identifier often varies from replicated multicast packet to replicated multicast packet, use of the destination interface identifier to select a network link will lead to a more even distribution of multicast packet transmission across the logical link. Such a distribution can reduce the likelihood of a load imbalance in the logical link.

Id. at 5:37–50. Figure 6 is reproduced below:

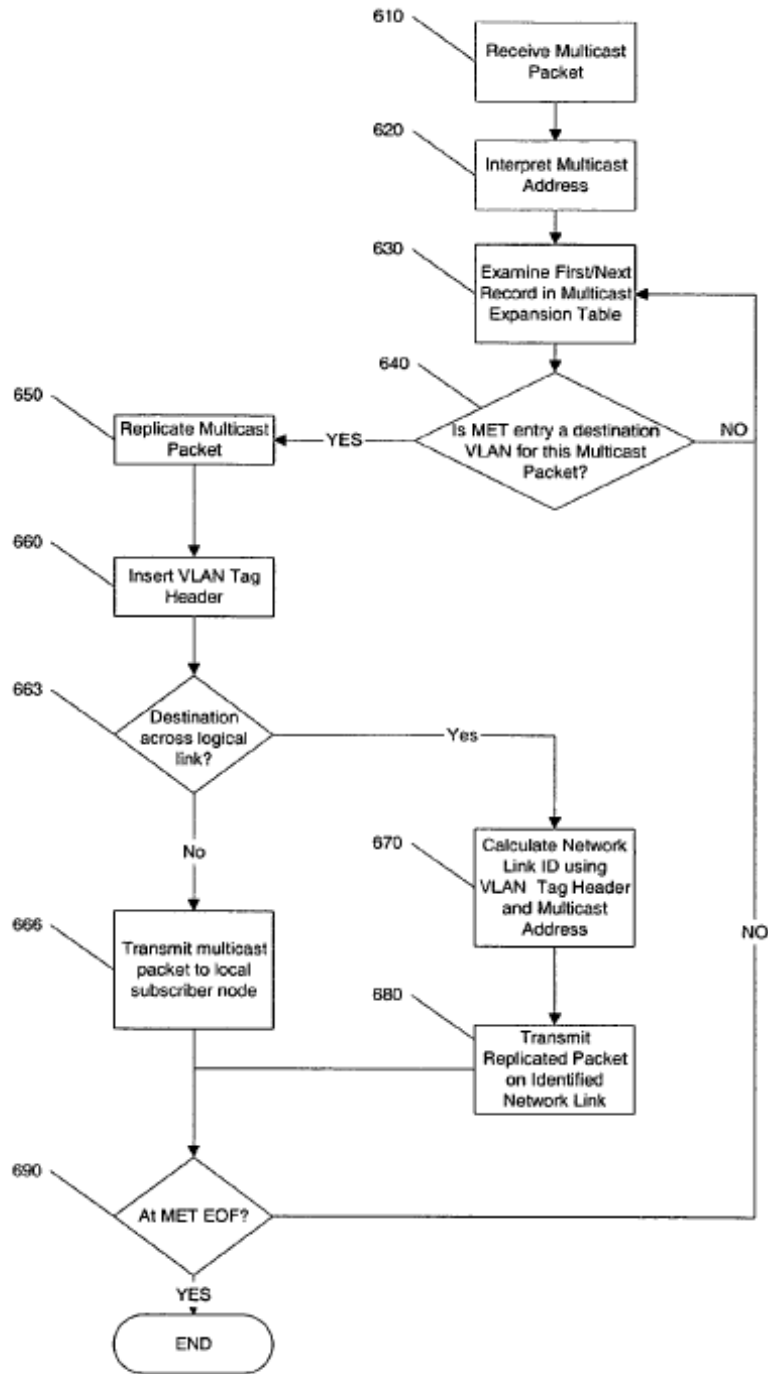


Figure 6

Figure 6 is a flow chart of actions taken in accordance with Borgione's method and system. *Id.* at 5:21–22.

After a multicast packet is received by a link node, at step 630 the link node determines the VLAN location of receivers of the multicast packet

using a table of multicast receivers, i.e., “multicast expansion table,” corresponding to the multicast group ID of the multicast packet. *Id.* at 6:40–44. For each such destination VLAN, the link node at step 660 inserts a tag header that contains the respective destination interface identifier, i.e., a VID. *Id.* at 6:47–50. Then, at step 670, the link node calculates a network link identifier corresponding to a specific network link within the logical link. *Id.* at 6:58–61. To increase distribution among the physical links within a logical link, the network link identifier is generated by analyzing the VID portion of the tag header as well as the source and destination addresses. *Id.* at 6:61–64. A hash algorithm can be used to generate the network link identifier. *Id.* at 7:1–5. At step 680, the multicast packet is transmitted on the specific network link identified by the network link identifier. *Id.* at 7:6–8.

3. *Overview of Mazzola*

Mazzola generally relates to network switches and specifically to an address translation mechanism for use in a network switch. Ex. 1007, 1:23–25. A network switch of a data communications network provides a switching function for transferring information such as data frames among network entities. *Id.* at 1:28–30. The switch includes a collection of cards interconnected by a backplane. *Id.* at 1:31–33. Each card includes a limited number of ports that couple the switch to other network entities over various types of media such as Ethernet. *Id.* at 1:33–35.

Specifically, Mazzola describes an address translation mechanism that renders forwarding decisions for data frames transported among the ports of a switch. *Id.* at 3:3–6. According to Mazzola, each port is associated with a unique index value and a VLAN (“color”) identifier to facilitate multicast

data transfer within the switch. *Id.* at 3:10–14.⁵ Additionally, the address translation mechanism comprises a plurality of forwarding tables, each of which contains entries having unique index values that translate to selection signals for ports destined to receive the data frames. *Id.* at 3:7–10.

A media access control (“MAC”) address of a data frame is combined with the “color” identifier of the data frame to produce a base line numerical quantity for searching the forwarding tables. *Id.* at 3:15–18. Each table entry, however, is directly accessed by a key comprising a hash transformation of the MAC/color quantity. *Id.* at 3:18–20. Mazzola explains:

Operationally, if the compared items [(the hashed MAC/color quantity and a lookup key for the table)] match, the index value stored in the table is provided to a target logic circuit for translation to a signal that selects a port or [a] group of ports for receiving the index frame. If the items do not match, the color identifier is passed to the target logic circuit with the result that all ports having that color identifier receive the frame in accordance with a multicast transfer.

Id. at 3:27–33.

⁵ VLAN means virtual local area network. Ex. 1007, 3:5–6.

Figure 1 is reproduced below:

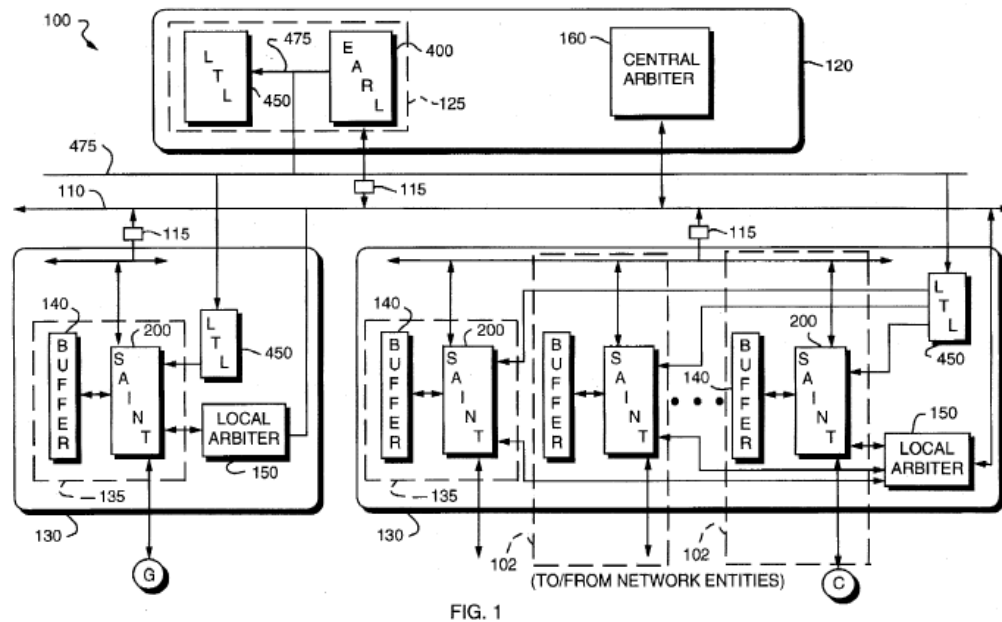


Figure 1 is a schematic block diagram of a network switch for interconnecting ports, implemented on various cards of the switch, that couple the switch to network entities of a data communications network *Id.* at 3:64–4:1. Network switch 100 includes supervisor card 120 and a plurality of line cards 130. *Id.* at 3:67–4:2. Each line card may have as many as 64 ports thereon. *Id.* at 4:2–3. Communication among the ports/cards occurs synchronously over switching bus 110. *Id.* at 4:4–6. Mazzola describes:

The architecture of the switching bus is preferably implemented as forwarding engine circuitry 125 and port interface circuitry 135 that cooperate to efficiently transmit data to, and receive data from, the switching bus 110. The forwarding engine 125 is located on the supervisor card 120 and comprises an encoded address recognition logic (EARL) circuit 400 coupled to a local target logic (LTL) circuit 450 over a result bus 475. Functionally, the EARL 400 executes all forwarding decisions for the switch 100, while the LTL 450 implements those forwarding decisions by selecting ports as destinations for receiving data frames transferred over the switching bus 110. As

can be seen in FIG. 1, the LTL may be distributed among the cards of the switch via the result bus 475.

Id. at 4:8–21. Port interface circuitry 135 includes SAINT [synchronous advanced interface network termination (*id.*, at 4:23–24)] circuit 200 which “is primarily responsible for (i) receiving data frames from the network and passing them to the switching bus, and (ii) receiving frames from the switching bus and passing them to the network.” *Id.* at 4:59–62. SAINT circuit 200 includes MAC circuit 210 coupled to DMA engine 220, and the DMA engine “modifies each frame by appending header information to it prior to arbitrating for access to the switching bus.” *Id.* at 5:8–9.

Figure 3 is reproduced below:

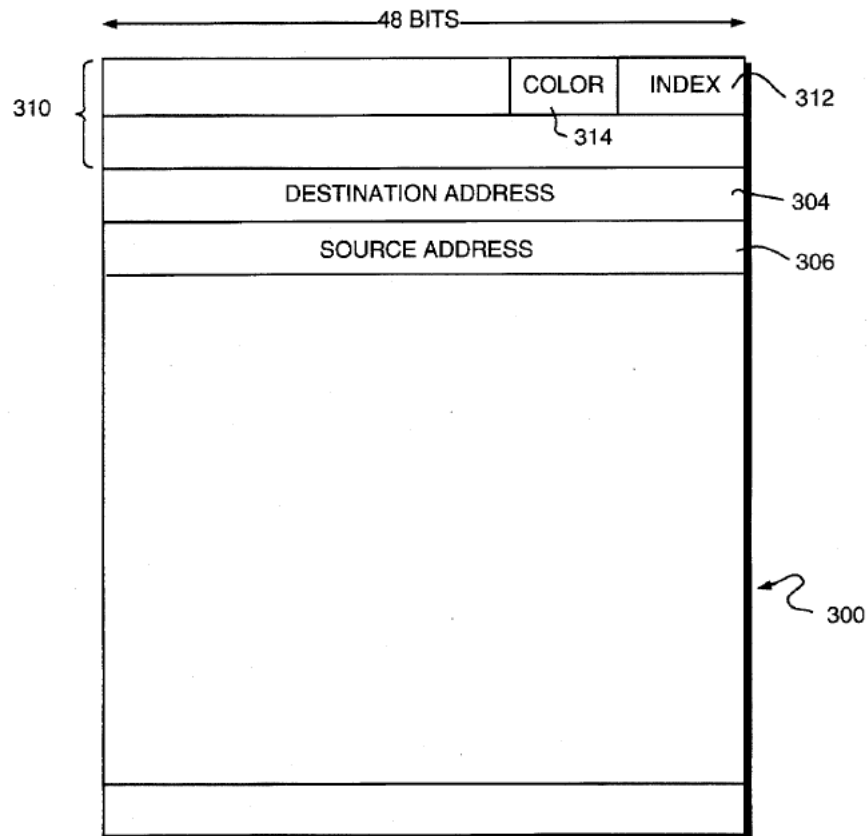


FIG. 3

Figure 3 is a block diagram illustrating the format of a data frame modified by port interface circuitry 135. *Id.* at 3:49–50. Two headers 310 are appended to data frame 300. *Id.* at 5:15–16. Mazzola describes:

When received at the port, the frame contains a 48-bit destination address in field 304 that identifies the destination network address of the frame and a 48-bit source address in field 306 identifying the source network address of the frame; the DMA engine 220 of SAINT 200 then appends two 48-bit headers 310 to the frame 300. Of interest to the present invention are a unique index value and a virtual local area network (VLAN) “color” identifier that are loaded in to a 10-bit index field 312 and a 10-bit color field 314, respectively, of the frame 300 by the engine. As described herein, these values represent the source index of the port transferring the frame over the switching bus 110 and the VLAN association of the port.

Id. at 5:11–23.

“Each port or group of ports within switch 100 is assigned a unique index value.” *Id.* at 6:20–22. Mazzola further states elsewhere that each port has a unique index number. *Id.* at 5:48–49, 5:65–66, 6:38–39, 7:5. Additionally, a virtual local area network (“VLAN”) identification, i.e., “color,” is associated with each port of the switch. *Id.* at 6:27–30. Thus, each port has associated therewith a VLAN identification “color” and a unique index value. *Id.* at 6:38–39. EARL 400 uses address translation to map a data frame’s destination address and color to a destination port using forwarding tables. *Id.* at 5:45–49.

When a data frame appears on the bus, EARL 400 extracts certain information to produce a numerical input quantity for searching the forwarding tables. *Id.* at 7:56–61. Mazzola describes that either of the 48-bit destination address DA or 48-bit source address SA is combined with the 10-bit color identifier to produce the base line numerical input quantity for

searching a table. *Id.* The combined 58-bit numerical quantity is hashed to produce a 15-bit key by a hashing function implemented by a conventional hashing algorithm. *Id.* at 8:17–20. The resulting key maps to an entry location in each of four tables. *Id.* at 8:25–27, 8:46–48. When accessing the tables, it is necessary to identify which of the four tables holds the correct index value for the MAC/color quantity of the current data frame. *Id.* at 8:49–52. “To do this, the MAC address and color are stored in the MAC/color field 514, and the index value is stored in the index field 516, when the entry is created.” *Id.* at 8:52–54. “After accessing a table with the hashed MAC/color quantity, the MAC address and color from that table is compared with the MAC/color of the current frame to verify whether the index is correct.” *Id.* at 8:54–58.

Regarding determining the appropriate destination port for a data frame, Mazzola further describes:

Operationally, the comparator 532 compares the MAC/color quantity from data frame 300 with the MAC/color value stored in field 514 of a selected mapped entry to ensure that the entry contains the correct index value. If the compared items match, the index value stored in the proper entry is selected by multiplexer 536 and provided to the input of multiplexer 538. This latter mux is enabled by the matched output signal of comparator 532 to provide the index over the result bus 475 and to the LTL 450. In response, the LTL translates the received index to a signal that selects a port or a group of ports for receiving the data frame. If the MAC/color values do not match (i.e., a “miss”), the color identifier is selected by the multiplexer 538 and passed to the LTL 450 with the result that all ports having that color identifier receive the frame in accordance with a multicast transfer.

Id. at 9:20–35.

4. *Independent Claim 1*

a) *Recitation [1.Pre]*

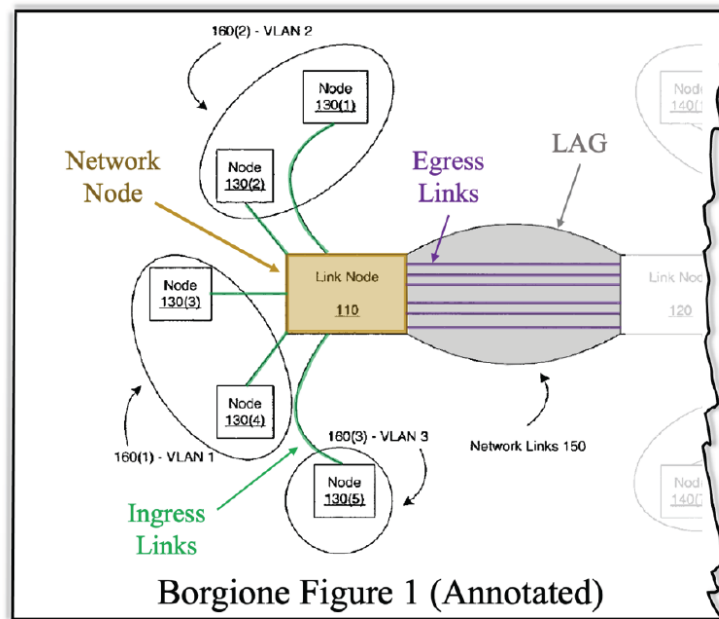
Claim 1 recites in Preamble [1.Pre]: “A network node in a communication network, comprising:” Ex. 1001, 10:15–16. Petitioner asserts that Borgione teaches a network node in a communication network and a method for communication. Pet. 55 (citing Ex. 1006, 1:6–10, 3:53–56, 7:6–8). Referring to Figure 1 of Borgione, Petitioner identifies link node 110 as the network node. *Id.* Patent Owner does not present argument to the contrary. We are sufficiently persuaded that Borgione discloses “[a] network node in a communication network.”⁶

b) *Limitation [1.1]*

Claim 1 further recites limitation [1.1]: “a plurality of ports, at least a subset of which is grouped in a link aggregation (LAG) group; and packet processing logic, which is coupled to receive data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of the ports.” Ex. 1001, 10:17–22.

Petitioner presents the following annotated partial drawing of Borgione’s Figure 1 to show satisfaction of limitation [1.1]:

⁶ We need not decide whether this preamble recitation is limiting.



The figure above is Borgione's Figure 1 with annotations in gold for Network Node, in purple for Egress Links, and in green for Ingress Links added by Petitioner (Pet. 56). Petitioner cites the follow text of Borgione:

[T]he plurality of network links between 110 and 120 *can be aggregated as a single logical link*. In this manner, each link node 110 and 120 sees the plurality of network links between them as one logical interface. . . . Routing protocols treat *the aggregated links as a single, routed interface* with a common IP address.

Id. (footnote omitted) (citing Ex. 1006, 1:17–23, 1:37–39, 1:57–65, 1:66–2:7, 3:60–64; Ex. 1003 ¶¶ 216–217).

Although Borgione's disclosure does not refer to the presence of ports, Dr. Lavian testifies:

Based on Borgione's description of the structure and function of its links, a POSITA would have understood that Borgione discloses its links include a plurality of ports for receiving and forwarding packets. For instance, Borgione explains that its links include network link identifiers which function to identify ports:

The *network link identifier* identifies which of the plurality of network links is to be used for sending the packet between link nodes 110 and 120.

Once a *network link identifier* has been calculated, the replicated multicast packet can then be transmitted on the identified network link (680).

Ex. 1003 ¶ 219 (footnotes omitted) (citing Ex. 1006, 3:34–36, 3:53–56, 4:45–54, 6:35–37, 7:6–8). We understand Dr. Lavian as testifying that each identified physical network link represents an output port on the link node sending the packet and an input port on the link node receiving the packet, and that the ports provide access of a data packet to the link. The assertion is logical and supported by the disclosure of Borgione.

Patent Owner argues that Borgione only designates a link between network nodes, but does not explain why Dr. Lavian’s testimony about each physical link identifying a specific port is incorrect. Pet. 46. We are sufficiently persuaded by Petitioner that each of Borgione’s physical links identifies a specific output port on link node 110 sending the packet and a specific input port on link node 120 receiving the packet.

Furthermore, we are sufficiently persuaded that the purple colored “Egress Links” in the above annotated Figure 1 of Borgione constitutes a LAG group in which at least a subset of a plurality of ports, specifically all of the output ports on link node 10, is grouped. Patent Owner similarly does not explain why that is not the case, given that each physical link identifies a specific port.

Regarding processing logic, Petitioner asserts:

Further, Borgione’s network node includes packet processing logic for receiving multicast traffic from VLAN nodes 130(1)–(5) wherein each packet has a respective destination address that specifies forwarding the packet to a

group of multiple recipients via egress links. And Borgione's network node includes a processor processing instructions for forwarding packets by analyzing multicast destination addresses and packet headers:

[T]he present invention provides an apparatus comprising a processor, network interfaces coupled to a plurality of network links configured to form a logical channel, and a memory for storing instructions that upon execution cause the processor to transmit a replicated multicast packet over one of the plurality of network links, and to select one of the plurality of network links by analyzing a destination ethernet address of the replicated multicast packet and a non-ethernet address component of a header of the replicated multicast packet.

Pet. 57 (emphases omitted) (alteration by Petitioner) (quoting Ex. 1006, 4:45–54) (footnotes omitted). Petitioner's assertions are reasonable and supported by the cited evidence. Patent Owner presents no contrary argument in that regard. We are sufficiently persuaded that Borgione discloses processing logic as recited in limitation [1.1].

For the foregoing reasons, we are sufficiently persuaded that Borgione discloses limitation [1.1].

c) Limitation [1.2]

Claim 1 further recites limitation [1.2]: “[and] to process the data packets so as to forward only a single copy of each of the data packets via the output ports in the subset, while distributing forwarded copies of the data packets among the output ports in the subset so as to balance a traffic load within the LAG group.” Ex. 1001, 10:22–27.

Petitioner asserts that Borgione discloses this limitation. Pet. 59. Alternatively, Petitioner contends that Borgione either alone or in

combination with Mazzola suggests this limitation. *Id.* For reasons discussed below, we are sufficiently persuaded that Borgione discloses the limitation.

Petitioner cites the following disclosure in Borgione:

[T]he present invention provides a method for transmitting a replicated multicast packet over one of a plurality of network links that form one logical channel. . . . [¶] The first network node selects a destination interface identifier for an outgoing multicast packet, selects one of the plurality of network links using the destination interface identifier, and transmits the outgoing multicast packet to the second network node over the selected network link.

Pet. 59 (footnote omitted) (emphases omitted) (citing Ex. 1006, 3:18–21, 4:3–21; Ex. 1003 ¶¶ 223–224). Because Borgione selects only one physical link to transmit the packet, it forwards only a single copy of the packet to the LAG including a plurality of ports.

With regard to distributing forwarded copies to balance the traffic load within the LAG, Petitioner cites to the following disclosure of Borgione:

The present invention balances the transmission of replicated multicast packets among an aggregate of network links that provide a logical channel or link between network nodes An added tag header can be used to include a destination interface identifier A destination interface identifier within a tag header can be used to select which network link in a logical link is to be used to transmit a replicated multicast packet. Since the destination interface identifier often varies from replicated multicast packet to replicated multicast packet, use of the destination interface identifier to select a network link will lead to a more even distribution of multicast packet transmission across the logical link. Such a distribution can reduce the likelihood of a load imbalance in the logical link.

Id. at 59–60 (footnote omitted) (citing Ex. 1006, 2:8–18, 3:37–56, 3:60–4:2, 5:37–50, 6:32–67; Ex. 1003 ¶ 225).

Petitioner’s explanation of why Borgione discloses limitation [1.2] is rational and supported by the cited evidence. Patent Owner acknowledges that Borgione’s network link identifier corresponds to a network link within the logical link but asserts that “Borgione’s network link identifier does not allow for an even distribution of multicast packets among the different output ports of the LAG Group within a particular node.” Prelim. Resp. 45. The argument is unpersuasive, because the above-quoted disclosure of Borgione expressly states that Borgione’s manner of selection of the particular link “will lead to a more even distribution of multicast packet transmission across the logical link” and “can reduce the likelihood of a load imbalance in the logical link.” Ex. 1006, 5:47–50. Borgione also explains that the distribution stems from use of its destination interface identifier which varies from one multicast packet to another. *Id.*

We are sufficiently persuaded that Borgione discloses limitation [1.2].

d) Limitation [1.3]

Claim 1 further recites limitation [1.3]:

wherein:

the packet processing logic is arranged to allocate to each of the received data packets a fabric multicast identification (FMID) value selected from a range of possible FMID values, each FMID being associated with one of the ports in the subset, and to forward the single copy to the port associated with the allocated FMID value;

Ex. 1001, 10:28–35.

Petitioner asserts that Borgione discloses this limitation. Pet. 60. Alternatively, Petitioner also contends that Borgione either alone or in combination with Mazzola suggests this limitation. *Id.* We do not address

the alternative assertion based on Borgione and Mazzola, because Petitioner relies on Mazzola only to show forwarding a single copy of the packet to the corresponding port. Pet. 64. We already determined above in the context of limitation [1.2] that Borgione itself provides that teaching. We also do not address the alternative assertion based on obviousness in light of Borgione alone, because Petitioner does not clearly articulate what is missing from Borgione to require curing by obviousness reasoning.

For reasons discussed below, Petitioner has shown that Borgione itself discloses limitation [1.3]. Petitioner identifies in Borgione the “network link identifier” (referenced in Figure 6 as calculated “Network Link ID”) as the FMID value in limitation [1.3]. Pet. 61–62. Figure 6 of Borgione is reproduced below:

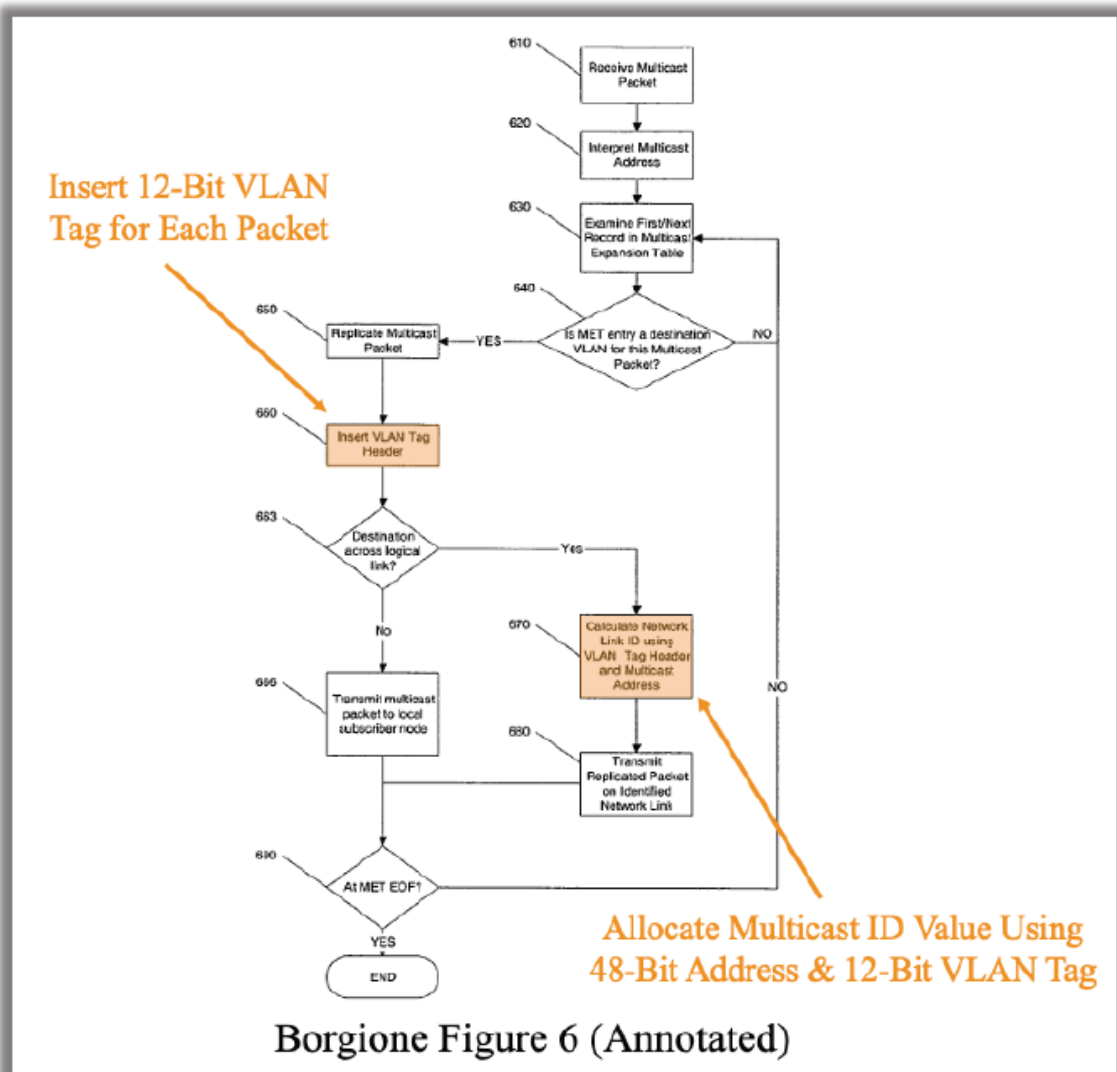


Figure 6 of Borgione, color annotated by Petitioner (Pet. 63), shows a flowchart of steps performed in Borgione's method. Ex. 1006, 5:21–22.

Petitioner asserts that Borgione's node 110 assigns a "network link identifier" to each received multicast packet by applying a hashing function to the 48-bit destination address and 12-bit VID (VLAN) tag in the packet's header fields. Pet. 61. Petitioner also asserts that the calculated "network link identifier" is based on a range of values and that each such "network

link identifier” value is associated with one of the subset links, and thus a corresponding port, for packet forwarding. Pet. 62.

The assertions are supported by Borgione’s disclosure. As discussed above, Borgione describes that a portion of an IEEE Std. 802.1Q tag header is a VLAN identifier (“VID”), and this tag header can be inserted and used to select which network link in a logical link is to be used to transmit a multicast packet. Ex. 1006, 5:40–44 (cited at Pet. 61). Annotated Figure 6 of Borgione, reproduced above, shows the tag insertion at step 660 and the calculation of the “network link identifier” at step 670. Borgione also describes that the multicast packet’s Ethernet address is 48 bits as asserted by Petitioner. *Id.* at 5:19–20. Box 670 in Figure 6 indicates that the “network link identifier” is calculated by using the 48-bit address and the VLAN tag, i.e., VID. Borgione further describes that generating the network link identifier at step 670 can take the form of a hash function algorithm. *Id.* at 7:1–5 (cited at Pet. 62). Borgione describes that the hash function generates an output “value” (cited at Pet. 62), and thus the VID is selected from a range of values. Borgione states: “Once a network link identifier has been calculated, the replicated multicast packet can then be transmitted on the identified network link (680).” *Id.* at 7:6–8 (cited at Pet. 62).

Patent Owner presents several arguments with respect to limitation [1.3], discussed below, all of which are unavailing and do not undermine Petitioner’s contentions.

Patent Owner argues that Borgione’s “network link identifier” does not associate each packet to one of the outgoing ports, because Borgione only calculates the “network link identifier” if the destination receiving node

is located across the logical link and not the local node which already received the packet. Prelim. Resp. 45. The argument is unpersuasive, because to meet limitation [1.3], the requirements need only be met for packets that are to be forwarded to another network node. The packets which have already reached its destination need not be forwarded to another network node.

First, the antecedent basis for “each of the received data packets” is in this portion of limitation [1.1]: “to receive data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of the ports.” Ex. 1001, 10:19–22. Data packets which have already arrived at their destinations and are not to be forwarded are not the claimed “each of the received data packets.” Second, we see nothing in the specification of the ’525 patent to indicate that packets which have already reached their destination in the current node would, still, have to be forwarded to another network node through any output port, and Patent Owner has identified no such disclosure. Such a reading based on endless forwarding despite having already reached the destination node is not consistent with the specification of the ’525 patent.

Patent Owner asserts that Borgione’s “network link identifier” is not selected from a range of possible FMID values but is calculated using a hash algorithm or some other method that requires an input or output. Prelim. Resp. 44. Referring to Figure 1 of the ’525 patent, Patent Owner states that as disclosed, “the range of FMID values is defined according to the LAG group configuration of the node.” *Id.* at 45 (Figure 1 shows the FMIDs as BASE+0, BASE+1, BASE+2, BASE+3, BASE+4, and BASE+5). The argument is misplaced and unavailing. Nothing in the claim precludes the

FMID from being calculated or otherwise arrived at in a certain way. It is improper to read limitations from a preferred embodiment described in the specification, even if it is the only embodiment, into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited. *EPOS Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002). A particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment. *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004). That is the case here.

e) Limitation [1.4]

Claim 1 further recites limitation [1.4]:

the packet processing logic comprises multiple line cards connected to the ports and a switching fabric interconnecting the line cards, wherein, for each of the received data packets, a first line card connected to a first port via which the data packet is received is arranged to allocate the FMID value to the packet and to forward the packet to the switching fabric, and

Ex. 1001, 10:36–42.

Petitioner asserts that Borgione and Mazzola collectively would have suggested limitation [1.4]. Pet. 64. For reasons discussed below, we are sufficiently persuaded by Petitioner’s analysis.

The ’525 patent acknowledges that network nodes typically comprise multiple line cards interconnected by a switching fabric, with each line card supporting one or more output ports. Ex. 1001, 3:18–26 (cited at Pet. 66 n.175). Dr. Lavian testifies that such a structure for network nodes was generally known in the art. Ex. 1003 ¶ 239.

Petitioner cites to Borgione’s disclosure about having network interfaces within a link node, which are coupled to a plurality of network links, and selecting one of the network links for packet transmission. Pet. 64–65. Dr. Lavian testifies that based on that disclosure, “a POSITA would have understood Borgione’s network interfaces include line cards interconnected via a switching fabric for packet transmission.” Ex. 1003 ¶ 235 (cited at Pet. 65 n.172).

Dr. Lavian explains that Mazzola discloses a configuration that was well known:

Mazzola discloses the well-known configuration of having the network node include a switching fabric interconnecting line cards for packet transmission. . . . Mazzola teaches that its packet processing logic includes line cards 130 connected to ports and a switching fabric 120 interconnecting the line cards. . . . And Mazzola teaches its ingress card (green) [shown in Mazzola Figure 1] is a first line card connected to a first port for receiving each data packet.

Id. ¶ 237 (cited at Pet. 66 n.175). Dr. Lavian further testifies that “[a] POSITA would have understood that Mazzola’s supervisor card 120 is a switching fabric because it allows for transfer of data between one or more ingress ports and one or more egress ports.” *Id.* ¶ 238 (cited at Pet. 66 n.178).

Petitioner asserts that based on Mazzola’s teachings and the general knowledge regarding network-node components, “a POSITA would have found it obvious to have Borgione’s node include a switching fabric interconnecting multiple line cards having ports wherein a first line card is arranged to allocate the FMID value to the received packet and to forward the packet to the switching fabric.” Pet. 67. The testimony of Dr. Lavian supports the assertion. Ex. 1003 ¶ 240 (cited at Pet. 68).

Petitioner explains:

A POSITA would have been motivated to do so [switching fabric interconnecting line cards having ports where a first line card arranged to allocate the FMID to the received packet and to forward the packet to the switching fabric] because this configuration allows for interconnecting ingress and egress links via line-card ports for efficient and fast packet forwarding. And a POSITA would have been motivated to do so because using line cards and a switching fabric in a network node provides components with separate processing capabilities for efficient and fast packet forwarding.

Pet. 67–68 (footnotes omitted) (citing Ex. 1003 ¶¶ 239–241). The assertion is supported by the cited testimony of Dr. Lavian. Ex. 1003 ¶¶ 239–241.

We do not see arguments of Patent Owner specifically directed to limitation [1.4]. To the extent certain arguments of Patent Owner directed to limitation [1.6] also apply to limitation [1.4], we discuss them below in the context of limitation [1.6].

f) Limitation [1.5]

Claim 1 further recites limitation [1.5]:

wherein the switching fabric and a second line card connected to a second port to which the data packet is to be sent are configured to forward the data packet responsively to the FMID value; and

Ex. 1001, 10:43–46.

Petitioner asserts that Borgione and Mazzola collectively would have suggested limitation [1.5]. Pet. 68. For reasons discussed below, notwithstanding Patent Owner’s arguments to the contrary, we are sufficiently persuaded by Petitioner’s analysis.

Petitioner cites to the following disclosure of Borgione: “[o]nce a network link identifier has been calculated, the replicated multicast packet can then be transmitted on the identified network link (680).” Ex. 1006,

7:6–8 (cited at Pet. 68). Dr. Lavian testifies that that description shows “forwarding each multicast packet out of the network node responsively to the FMID value.” Ex. 1003 ¶ 243 (cited at Pet. 68 n.181). Petitioner further explains that the interconnecting structure within the network node, i.e., ingress and egress line cards with ports, which are interconnected via a switching fabric, already has been accounted for in the context of limitation [1.4]. Pet. 68–69.

Petitioner’s reasoning is cogent and supported by the cited evidence. Notwithstanding Patent Owner’s argument to the contrary, discussed below, we are sufficiently persuaded that limitation [1.5] is met by the combined teachings of Borgione and Mazzola as presented by Petitioner.

Patent Owner argues that because Borgione requires an additional step before the packet is sent out of the node, i.e., determining if the destination is local to the node at which the packet already is received, and transmit the packet to another network node only if the destination is not local, Borgione does not transmit a data packet responsively to a FMID value. Prelim. Resp. 46–47. The argument is misplaced and not availing. As discussed above, nothing in the specification of the ’525 patent indicates that packets which have arrived at their destination node would still be forwarded to another network node responsive to its FMID. Such packets need not meet the requirements of limitation [1.5]. It is sufficient for limitation [1.5] to be met, if multicast packets meant to be forwarded to another network node are forwarded in the manner recited, as Petitioner has adequately shown here, for purposes of institution. Contrary to Patent Owner’s contention, Petitioner has not merely assumed that the limitation is met, and has not

improperly placed the burden on the Board and Patent Owner to disprove this limitation.

g) Limitation [1.6]

Claim 1 further recites limitation [1.6]:

the first line card is arranged to assign to the data packets line card FMID (LC-FMID values selected from a first range of possible LC-FMID values, and wherein the switching fabric is arranged to map the LC-FMID values to respective central FMID (C-FMID values selected from a second range of possible C-FMID values that is smaller than the first range and to forward the data packets responsively to the C-FMID values.

Ex. 1001, 10:47–55.

Petitioner asserts that Borgione and Mazzola collectively would have suggested limitation [1.6]. Pet. 69. For reasons discussed below, notwithstanding Patent Owner’s arguments to the contrary, we are sufficiently persuaded by Petitioner’s analysis.

Petitioner breaks its analysis into two parts, first asserting that it would have been obvious in light of Borgione and Mazzola to have the receiving line card assign a 58-bit LC-FMID value, and then asserting that it would have been obvious in light of Borgione and Mazzola to convert in the switching fabric that LC-FMID value to a C-FMID value of lesser range. *Id.* at 69–70.

For the first contention, Petitioner explains that Borgione already discloses a line card applying a hashing function to two multicast header fields, i.e., 48-bit destination address and 12-bit VID tag, to produce a network link identifier associated with an output port. *Id.* at 70. Petitioner further explains that Mazzola has a similar disclosure where a 48-bit address is combined with a 10-bit VLAN “color” identifier to produce a base line numerical quantity for searching Mazzola’s forwarding tables resulting in

identification of an output port. *Id.* at 71. On that basis, Petitioner asserts that it would have been obvious for one with ordinary skill in the art to combine the two header fields in Borgione, the 48-bit destination address and 12-bit VID tag, and use that as the value for subsequent processing, i.e., the disclosed hashing to generate a network link identifier. *Id.* at 71.⁷

Petitioner further asserts that the combined single value of 58 bits is an FMID value allocated to the data packet and allocating such line card FMID (“LC-FMID”) values as 58-bit values “provides a quicker, more efficient address translation mechanism particularly suited for VLAN arrangements like Borgione’s.” *Id.* (footnote omitted) (citing Ex. 1006, 2:64–67, 3:3–15, 6:28–31, 10:46–50; Ex. 1003 ¶ 252). Thus, Petitioner identifies the combined fields of destination address (48 bits) and VID tag (12 bits) as an allocated LC-FMID of 58 bits having a certain range.

Petitioner’s analysis is rational and supported by the cited evidence. Borgione discloses using the two fields in a hashing function to generate a network link identifier but does not specifically state that they are combined to form a single value. Mazzola shows combining a 48-bit address field with a 10-bit VLAN “color” identifier to form a single combined value as a base line numerical quantity for use in identifying a port.

For the second contention, Petitioner explains that Mazzola describes its switching fabric as reducing the 58 bits assigned by a line card down to just 15 bits in the switching fabric before proceeding further and that the reduction in range allows the switching fabric to forward multicast packets

⁷ Petitioner refers to the two combined fields as having 58 bits (Pet. 71), but 48 bits and 12 bits actually add to 60 bits. The exact number, whether it is 58 or 60, however, does not matter. Either one supports Petitioner’s position.

at accelerated speeds with improved addressing capabilities. Pet. 72 (footnotes omitted) (citing Ex. 1006, 3:3–26, 5:58–66, 6:41–47, 6:64–7:10, 7:47–61, 10:46–50; Ex. 1003 ¶¶ 253–254). On that basis, Petitioner asserts that “a POSITA would have found it obvious to use Mazzola’s technique in Borgione’s node to have a switching fabric map the LC-FMID values to a smaller range of respective C-FMID values for forwarding the packets” before proceeding further with the forwarding. *Id.*

Petitioner further explains that one with ordinary skill in the art would have been motivated to make the reduction in range because doing so reduces the memory size and ultimate cost for the switching fabric, and because doing so would provide a quicker and more efficient address-to-port translation mechanism particularly suited for VLAN arrangements like Borgione’s. *Id.* at 72–73 (footnote omitted) (citing Ex. 1006, 2:64–67, 3:3–15, 6:28–31, 10:46–50; Ex. 1003 ¶¶ 255–256).

Petitioner’s analysis is rational and supported by the cited evidence. Patent Owner presents several arguments with respect to limitation [1.6], discussed below, all of which are unavailing and do not undermine Petitioner’s contentions.

Patent Owner argues that Borgione does not disclose this element and that Mazzola also does not disclose this element. Prelim. Resp. 48. But Petitioner’s theory of obviousness is based on the combined teachings of Borgione and Mazzola, and Petitioner does not assert that either reference alone discloses this limitation in its entirety.

Patent Owner argues that Mazzola does not mention Link Aggregation and Mazzola does not seek to balance a traffic load within the LAG group. Prelim. Resp. 48. But Borgione does, and Petitioner’s accounting, as

discussed above, does not require Mazzola to disclose anything about Link Aggregation or balancing the traffic load within the LAG group. One cannot oppose obviousness by attacking references individually where the theory of obviousness is based on the teachings of a combination of references. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). The focus must be on the theory and reasoning presented by Petitioner. “The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art.” *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

Patent Owner argues that Mazzola’s VLAN color tag is used to search forwarding tables, not a value assigned to a packet to associate it with one of the ports. Prelim. Resp. 48. The argument is misplaced and unavailing, because, as discussed above, the tables in Mazzola are searched to yield an entry that is associated with a port. In Mazzola, EARL 400 uses address translation to map a data frame’s destination address and color to a destination port using forwarding tables. Ex. 1007, 5:45–49. The indirection provided through searching a table does not undermine or defeat the association of a port with the combined destination address and color tag.

Patent Owner argues that Mazzola’s 15-bit key is not a value allocated to each multicast data packet but is, instead, determined by hashing “the 58-bit MAC/color quantity” and is “used to search forwarding tables to determine a mapping.” Prelim. Resp. 52. The argument is misplaced, for several reasons. First, claim 1 does not require the C-FMID to be allocated to each data packet, just the LC-FMID. Second, Petitioner does not rely on Mazzola’s 15-bit key as the claimed C-FMID. Third, in any event, the 15-bit key indeed is allocated to each multicast data packet, because Mazzola

describes that the combined 48-bit address and 10-bit VLAN “color” is mapped to a 15-bit key. Ex. 1007, 8:16–20. Because the 58-bit value is allocated to a multicast packet, the 15-bit key to which the 58-bit value is mapped also is allocated to a multicast packet.

Patent Owner argues that Borgione does not allocate FMID values to packets where each of the FMID value is associated with an output port, but instead identifies which of the plurality of network links is to be used for sending the packet between link nodes 110 and 120. Prelim. Resp. 49. But, as we have explained above, Petitioner has sufficiently shown that each of Borgione’s physical link identifies a specific output port on link node 110 and an input port on link node 120, connected by the physical link. Thus, identification of a specific link identifies a specific output port.

Patent Owner asserts that Petitioner does not explain how or why Borgione’s method of identifying a plurality of network links to send between nodes can be combined with Mazzola’s address translation system. Prelim. Resp. 49. We disagree. We understand Petitioner’s explanation and have specifically identified and addressed it above in our discussion of that explanation. Specifically, Petitioner relies on Mazzola for three teachings.

First, Petitioner explains that Borgione already discloses using the 48-bit destination address and the 12-bit VID tag in a hashing function to generate the “network link identifier” but does not specifically state that the two are combined to form a single value. Pet. 70. Petitioner further explains that Mazzola has a similar disclosure where a 48-bit address is combined with a 10-bit VLAN “color” identifier to produce a base line numerical quantity for searching Mazzola’s forwarding tables resulting in identification of an output port. *Id.* at 71. Based on that teaching of Mazzola, Petitioner

proposes that one with ordinary skill in the art would have combined the two header fields of Borgione into a single value to serve as input to the hashing function. *Id.* at 71. That reasoning has been clearly articulated by Petitioner. *Id.* at 70–71.

Second, Petitioner explains that Mazzola describes its switching fabric as reducing the 58 bits assigned by a line card down to just 15 bits before proceeding further and that the reduction in range allows the switching fabric to forward multicast packets at accelerated speeds with improved addressing capabilities. Pet. 70. On that basis, Petitioner asserts that “a POSITA would have found it obvious to use Mazzola’s technique in Borgione’s node to have a switching fabric map the LC-FMID values to a smaller range of respective C-FMID values for forwarding the packets” before proceeding further with the forwarding. *Id.* at 72. That reasoning has been clearly articulated by Petitioner.

Third, Petitioner relies on Mazzola as disclosing a switching fabric, well known in the art, between ingress line cards and egress line cards in a network node. Pet. 66 (citing Ex. 1003 ¶¶ 237–238).

Contrary to Patent Owner’s contention that Petitioner does not even explain what the purported modification would be, and that Petitioner has failed to explain how or why Borgione would be redesigned with Mazzola (Prelim. Resp. 54), the what, the how, and the why all have been articulated by Petitioner reasonably clearly.

Patent Owner argues that with regard to the proposed modifications, Petitioner presumes success. Prelim. Resp. 53–54. We disagree. Mazzola demonstrates that a 48-bit address and the 10-bit VLAN “color” can be combined into a single value of 58 bits to produce a base line numerical

input quantity. Ex. 1007, 7:58–61. That is sufficient to demonstrate a reasonable expectation of success in combining Borgione’s 48-bit destination address and 12-bit VID tag into a single value of 60 bits. Mazzola demonstrates that the combined 58-bit numerical quantity can be hashed to produce a 15-bit key. *Id.* at 8:17–20. That is sufficient to demonstrate a reasonable expectation of success that Borgione’s 60-bit combined value can be reduced by hashing to a value with a smaller number of bits. Mazzola demonstrates that a network node can be configured as ingress line cards and egress line cards interconnected by a switching fabric. Ex. 1003 ¶¶ 237–238. That is sufficient to demonstrate a reasonable expectation of success that Borgione’s network node 110 can be similarly configured with success. Nothing more is required of Petitioner to show a reasonable expectation of success. Patent Owner offers no reason to doubt that these implementations and configurations would be successful.

Patent Owner argues that Petitioner does not provide “detailed explanation of how Borgione’s identification of network links would become quicker, more efficient with Mazzola’s technique of hashing different values to search forwarding tables” Prelim. Resp. 50. Petitioner, however, has not proposed to adopt the table searching disclosed in Mazzola. In any event, Petitioner has provided sufficient explanation of why the two-tier address translation of Mazzola, first having a 58-bit value, and then converting that 58-bit value to a 15-bit key, would be more efficient. Petitioner states: “a POSITA would have been motivated to do so [provide a smaller range of ID values in the switching fabric] because having the switching fabric allocate a smaller value relative to those allocated in ingress line cards reduces the memory size, and ultimate cost,

needed for the switching fabric.” Pet. 55 (footnote omitted) (citing Ex. 1007, 2:49–60; Ex. 1003 ¶ 211).

Patent Owner argues that neither Borgione nor Mazzola assigns to received packets a FMID value selected from a range of possible FMID values, and thus neither teaches or suggests a first line card which assigns to the data packets line card FMID values selected from a first range of possible LC-FMID values and neither teaches conversion by the switching fabric of LC-FMID values to C-FMID values. Prelim. Resp. 50–51, 52–53. The argument is unavailing because, as we discussed above, the single value resulting from combining the destination address and the VID tag in Borgione, based on the teachings of Borgione and Mazzola collectively, is an LC-FMID having a range of values assigned to a received data packet, and the 15-bit key generated in the switching fabric by hashing the LC-FMID value is a C-FMID value having a smaller range than the LC-FMID value. The combined teachings of Borgione and Mazzola do account for each of these requirements.

h) Conclusion for Claim 1

Petitioner has shown a reasonable likelihood that it would prevail in establishing obviousness of claim 1 over Borgione and Mazzola.

5. Independent Claim 12

Claim 12 is a method claim and its method steps performed by recited parts correspond to the functions performed by essentially the same components recited in claim 1. Ex. 1001, 10:10–55, 11:34–12:3. Limitations [1.1] through [1.3] correspond respectively to limitations [12.1] through [12.3]. Limitations [1.4] and [1.5] collectively correspond to limitations [12.4] and [12.5]. Limitation [1.6] corresponds to limitation

[12.6]. Neither Petitioner nor Patent Owner present separate arguments for claims 1 and 12.

For substantially the same reasons discussed above regarding alleged obviousness of claim 1 over Borgione and Mazzola, Petitioner has shown a reasonable likelihood that it would prevail in establishing obviousness of claim 12 over Borgione and Mazzola.

6. *Dependent Claims 2–11 and 13–24*

Claims 2–11 each depend, directly or indirectly, from claim 1. Claims 13–24 each depend, directly or indirectly, from claim 12. Petitioner addresses these claims on pages 73–79 of the Petition. Patent Owner does not present contrary arguments additional to those it presents for independent claims 1 and 12 and already discussed above. At this stage, and on the current record, Petitioner’s assertions are supported by the cited evidence and have rational underpinning. Petitioner has shown a reasonable likelihood that it would prevail in establishing obviousness of claims 2–11 and 13–24 over Borgione and Mazzola.

D. *Alleged Obviousness of Claims 1–24 over Devi and Mazzola*

1. *Overview of Devi*

Devi discloses a method performed by an ingress card including receiving a packet with a destination identifier and determining an aggregated link associated with the destination identifier that includes multiple egress ports. Ex. 1005 ¶ 5. The method further includes determining a destination port from the egress ports of the aggregated link, and communicating the packet to the destination port. *Id.*

Figure 1 of Devi shows a system coupled to a network and is reproduced below:

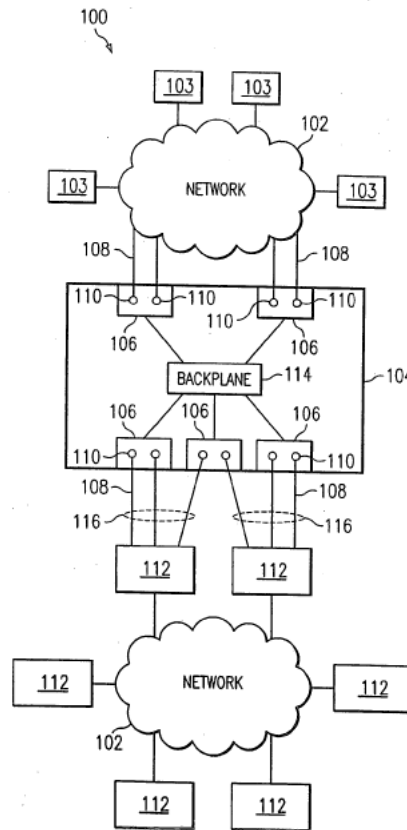


FIG. 1

Figure 1 illustrates system 100 including switch 104 coupled to network 102. *Id.* ¶ 15. “Using network 102 and switch 104, packets are communicated from sources 103 to destinations 112. Components of switch 104 are referred to as ‘ingress’ components when receiving packets from sources 103 and ‘egress’ components when sending packets to destinations 112.” *Id.* Switch 104 includes cards 106 coupled to physical links 108 and a backplane 114 that represents hardware and/or software allowing cards 106 to exchange information with one another. *Id.* ¶ 18. “Each card 106 has one or more ports 110 coupled to physical links 108.” *Id.* ¶ 19. Links 108 couple to cards 106 through ports 110. *Id.* ¶ 20.

Multiple physical links 108 to a particular destination 112 may be aggregated to form an aggregated link 116. *Id.* ¶ 23. It is treated as a single

link between switch 104 and the particular destination 112. *Id.* “Because aggregated link 116 includes multiple physical links 108 that go to the same destination 112, a packet sent to destination 112 need only be sent to one port 110 corresponding to one physical link 108 of aggregated link 116.” *Id.*

Devi refers to destination identifier 215, destination information 216, and port information. *Id.* ¶¶ 29–32. “Destination identifier 215 contemplates any information determinable from a packet that allows card 106 to identify one or more destinations 112 for the packet.” *Id.* ¶ 30. “Destination information 216 associates destination identifiers 215 in packets with egress links.” *Id.* ¶ 31. Card 106 uses destination information 216 to determine an egress link or links using destination identifier 215 from a packet. *Id.* Port information 218 refers to any form of data that identifies ports 110 associated with a particular link. *Id.* ¶ 32. “Port information 218 for an aggregated link 116 identifies the multiple ports 110 coupled to the physical links 108 of aggregated link 116, which may include ports 110 on a single card 106 or multiple cards 106.” *Id.* Destination information 216 and port information 218 are stored within card 106. *Id.* ¶ 29.

Figure 3 of Devi shows a flow chart for forwarding packets and is reproduced below:

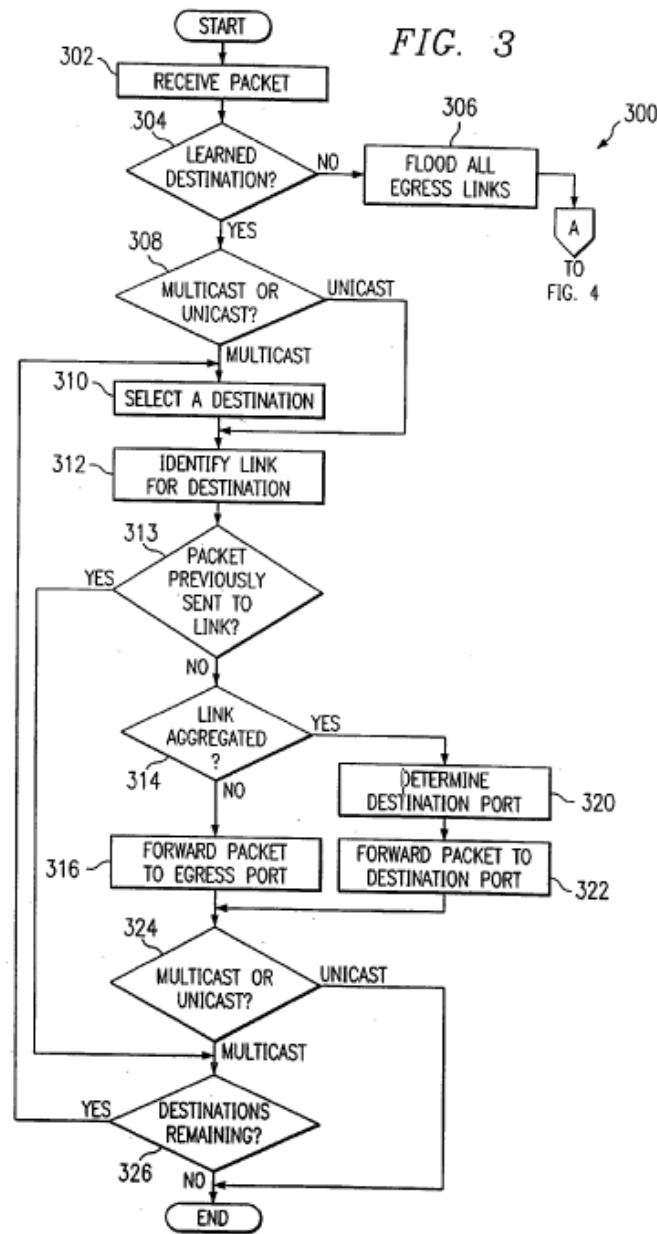


Figure 3 is a flow chart of a method in Devi for forwarding data packets. *Id.* ¶ 13.

Card 106 receives a packet at step 302. *Id.* ¶ 37. At step 304, card 106 determines destination identifier 215 for the packet and uses destination information 216 to determine if card 106 has previously learned the destination identifier 215. *Id.* If destination identifier 215 has been learned, card 106 next determines if destination identifier 215 identifies a multicast

or unicast destination at step 308. *Id.* If the packet is a multicast packet, card 106 selects one of the destinations for the packet using destination information 216 at step 310. *Id.* Card 106 identifies an egress link associated with the destination using destination information 216 at step 312. *Id.* ¶ 39. “If the link is an aggregated link 116, card 106 determines a destination port 110 of aggregated link 116 using the information in port information 218 at step 320.” *Id.* ¶ 41. The selection of a particular destination port 110 from the multiple ports 110 of the aggregated link may be by random selection, load balancing, pseudo-random selection or hashing using part of the packet information, historical tracking, round robin, or any other method of selection. *Id.* “Card 106 then communicates the packet to the destination port 110 at step 322.” *Id.*

2. *Independent Claim 1*

a) *Recitation [1.Pre]*

Claim 1 recites in Preamble [1.Pre]: “A network node in a communication network, comprising:” Ex. 1001, 10:15–16. Referring to Figure 1 of *Devi*, Petitioner asserts that *Devi* discloses a network node in a communication network and a method for communication. Pet. 17. Petitioner states: “*Devi* couples a network node (switch 104) to a communication network 102.” *Id.* (citing Ex. 1005 ¶¶ 18, 19, 23; Ex. 1003 ¶¶ 108–110). Patent Owner does not present argument to the contrary. We are sufficiently persuaded that *Devi* discloses “[a] network node in a communication network.”⁸

⁸ We need not decide whether this preamble recitation is limiting.

b) Limitation [1.1]

Claim 1 further recites limitation [1.1]: “a plurality of ports, at least a subset of which is grouped in a link aggregation (LAG) group; and packet processing logic, which is coupled to receive data packets having respective destination addresses that specify forwarding the packets to groups of multiple recipients through at least one of the ports.” Ex. 1001, 10:17–22. Referring to Figure 1 of Devi, Petitioner asserts: “Devi’s network node 104 has multiple ports 110 and packet processing logic that includes ingress and egress line cards 106 and a switching fabric 114 interconnecting the line cards. And Devi describes grouping one or more ports 110 into a link aggregation group (‘LAG’) 116.” Pet. 19 (footnotes omitted) (citing Ex. 1005 ¶¶ 18–21, 23–25, 32, 34, 41; Ex. 1003 ¶¶ 111–112).

Petitioner further asserts: “Devi’s logic receives packets having respective destination addresses that specify forwarding the packets to multicast groups through one or more ports 110 of LAG 116. For example, Devi’s ingress line card stores destination addresses of received multicast packets for forwarding to output ports of LAGs.” *Id.* at 19–20 (footnotes omitted) (citing Ex. 1005 ¶¶ 8, 26, 29–32, 34, 41; Ex. 1003 ¶¶ 113–115).

Patent Owner does not present argument to the contrary. Petitioner’s assertions are supported by the cited evidence. We are sufficiently persuaded that Devi discloses limitation [1.1].

c) Limitation [1.2]

Claim 1 further recites limitation [1.2]: “[and] to process the data packets so as to forward only a single copy of each of the data packets via

the output ports in the subset, while distributing forwarded copies of the data packets among the output ports in the subset so as to balance a traffic load within the LAG group.” Ex. 1001, 10:22–27. Petitioner explains:

Devi processes received packets to forward only one copy of each packet via output ports in a respective LAG. Devi explains that its “method allows card 106 to communicate the packet to all of its destinations 112 without sending multiple copies of the packet to the same destination.” To do so, Devi forwards one copy of each packet to a particular output port of an associated LAG.

Pet. 20–21 (footnotes omitted) (citing Ex. 1005 ¶¶ 2, 23, 34, 36, 42, 44, 46; Ex. 1003 ¶¶ 116–117). Referring to Devi’s Figure 4, Petitioner further explains: “Devi determines the destination port within the LAG 116 (step 416) and forwards a copy of the packet to the destination port in the LAG (step 418).” *Id.* at 22 (footnote omitted) (citing Ex. 1003 ¶ 118).

Additionally, Petitioner explains that Devi forwards copies among the output ports 110 to balance a traffic load within LAG 116. *Id.* at 23 (citing Ex. 1005 ¶ 23; Ex. 1003 ¶ 119). Referring to Figure 3 of Devi, Petitioner states: “Devi determines the output port for load balancing within the LAG 116 (step 320) and then forwards the packet copy to the port (step 322).” *Id.* (citing Ex. 1005 ¶ 41; Ex. 1003 ¶¶ 120–122).

Patent Owner does not present argument to the contrary. Petitioner’s assertions are supported by the cited evidence. We are sufficiently persuaded that Devi discloses limitation [1.2].

d) Limitation [1.3]

Claim 1 further recites limitation [1.3]:

wherein:

the packet processing logic is arranged to allocate to each of the received data packets a fabric multicast identification

(FMID) value selected from a range of possible FMID values, each FMID being associated with one of the ports in the subset, and to forward the single copy to the port associated with the allocated FMID value;

Ex. 1001, 10:28–35.

Petitioner makes two assertions regarding limitation [1.3]. First, Petitioner asserts that Devi alone renders obvious limitation [1.3]. Pet. 25–28. Alternatively, Petitioner asserts that Devi in combination with Mazzola teaches limitation [1.3]. *Id.* at 28–29. For reasons discussed below, we are not sufficiently persuaded by either assertion. We first discuss the contention based on Devi alone, and then the contention based on a combination of Devi and Mazzola.

As noted above, “[d]estination identifier 215 contemplates any information determinable from a packet that allows card 106 to identify one or more destinations 112 for the packet.” Ex. 1005 ¶ 30. Devi describes: “Destination identifier 215 represents information identifying an intermediate or final destination 112 for the packet. Destination identifier 215 may include a network address for destination 112, a logical address for an egress link, or any other information useful for identifying the destination of a packet.” *Id.*

Petitioner identifies Devi’s destination identifier 215 as an FMID value and asserts that for each received packet, Devi’s line card allocates destination identifier 215, a multicast value, to the packet before forwarding the packet to switching fabric 114. Pet. 25 (citing Ex. 1005 ¶¶ 30–34). We recognize, as Patent Owner points out, that the destination identifier is something already contained within each packet when it is received by the line card. But nothing requires the allocation be entirely done from scratch. Mere recognizing the destination identifier within each packet and taking

note of it in connection with that received packet, such as by storing it, reasonably constitutes allocating the destination identifier to that packet.

Petitioner further asserts that Devi's destination identifier 215, as FMID value, is associated with one egress port in a subset of ports which have been grouped in a LAG. *Id.* at 26–27. Petitioner has not made a sufficient showing for that contention, even for purposes of institution. For reasons discussed below, we agree with Patent Owner that “Devi's destination identifier 215 is associated with an aggregated link, not with ports.” Prelim. Resp. 30. We also agree with Patent Owner that Devi uses port information 218, which is not associated with any packet, to determine a port. *Id.*

Devi describes that destination information 216 associates destination identifiers 215 in packets with egress links, and that card 106 uses destination information 216 to determine an egress link or links using destination identifier 215 from a packet. Ex. 1005 ¶ 31. Regarding a port to which a packet would be forwarded, Devi describes that after the associated egress link is determined from the destination information, card 106 uses port information 218 to determine a destination egress port 110 of aggregated egress link 116 and forwards the packet to destination egress port 110. *Id.* ¶ 34. Devi describes that port information 218 for an aggregated link 116 identifies multiple ports 110 coupled to the physical links 108 of aggregated link 116. *Id.* ¶ 32. Specifically, Devi states:

If the link is an aggregated link 116, card 106 determines a destination port 110 of aggregated link 116 using the information in port information 218 at step 320. Card 106 may select a particular destination port 110 from the multiple ports 110 of the aggregated link using random selection, load balancing, pseudo-random selection or hashing using part of the

packet information, historical tracking, round robin, or any other method of selection. Card 106 then communicates the packet to the destination port 110 at step 322.

Id. ¶ 41. These manners of selecting a port once an aggregated link 116 is identified indicates that destination identifier 215 as an FMID value is not associated with any specific port.

Petitioner asserts that Devi “suggests allocating such an FMID value associated with a port to each received packet.” Pet. 27. The Petition states:

Devi discloses that each aggregated link includes a virtual address associated with the physical links of the egress ports. And Lasserre, which the ’525 Patent incorporates-by-reference, illustrates that it was generally known to allocate identifiers (e.g., VLAN ID tags) to each multicast packet. Thus, it would have been obvious to allocate Devi’s multicast ID values as FMID values and to associate each FMID with one port in the subset. A POSITA would have been motivated to do so because assigning virtual addresses based on FMID values would allow for dynamic address assignment to provide flexibility when adding or removing line cards if one card fails.

Id. at 27–28 (footnotes omitted) (citing Ex. 1005 ¶¶ 27, 32, 44, claims 3, 17; Ex. 1009, 11–13, 21–22; Ex. 1003 ¶¶ 129–130).

Petitioner’s arguments are not sufficiently persuasive. That each aggregated link has a virtual address associated with all of the physical links of the egress ports in the aggregated link means the virtual address is associated with all of the ports in the aggregated link collectively and not to any one port. Claims 3 and 17 of Devi, to which Petitioner cites, each read: “wherein the aggregated link comprises a virtual address that specifies a plurality of physical links coupled to the egress ports.” Ex. 1005, 10–11. That language does not suggest separate identification or addressing of each port, and assigning the virtual address of the aggregated link as an FMID value does not result in an FMID that is associated with a specific port. That

would not satisfy the claim requirement of “each FMID being associated with one of the ports in the subset.” Similarly, Petitioner does not point to any disclosure in Lasserre that any information in a multicast packet is associated with a specific port. Patent Owner correctly notes that “Lasserre makes no mention of associating ports with packets using VLAN ID tags.” Prelim. Resp. 30. Additionally, even if each individual port has its own virtual address, Petitioner has not adequately explained why associating a packet to a specific port would provide more flexibility than what Devi already provides by associating a packet to an egress link.

Alternatively, Petitioner argues that Devi and Mazzola together teach allocating an FMID value to each received packet, with each “FMID value associated with a port.” Pet. 28–29. Petitioner asserts:

Alternatively, a POSITA would have found it obvious to allocate an FMID value associated with a port to each received packet. Mazzola teaches its ingress line card assigns a 58-bit value to each multicast packet based on the packet’s destination address and a VLAN “color” tag. Mazzola explains that VLAN color tag “facilitate[s] multicast data transfers within the switch at accelerated speeds and addressing capabilities.”

Based on Mazzola, it would have been obvious to allocate one of Devi’s multicast ID values to each received packet as an FMID value and to associate that FMID with one port in the subset. A POSITA would have been motivated to do so because Mazzola teaches that assigning virtual addresses based on multicast ID values provides a quicker, more efficient address-to-port translation mechanism particularly suited for VLAN arrangements.

Id. (footnotes omitted) (citing Ex. 1007, 2:64–67, 3:13–15, 5:15–23, 6:28–31, 6:39–40, 7:56–61, 8:14–20, 10:46–50, code (57); Ex. 1003 ¶¶ 131–133).

Petitioner has over-simplified the issue with limitation [1.3] and has not sufficiently explained how Mazzola’s address translation mechanism

would be incorporated into Devi without affecting those portions of Devi relied on by Petitioner to account for limitation [1.2]. As Patent Owner correctly asserts, “Petitioner also does not state how its modified Devi would function.” Prelim. Resp. 42. Also as Patent Owner correctly asserts, “Petitioner does not address whether [the proposed combination] would impact Devi’s functionality.” *Id.* As Patent Owner further correctly asserts, “nowhere in the Petition is there a discussion or explanation as to why this purported combination would have been successful.” *Id.* at 41.

As discussed above, Devi does not disclose allocating to each of the received data packets a FMID value, where each FMID is associated with one of the ports among the plurality of grouped ports in a LAG group. It also does not disclose any circuitry or step to process such FMID values.

What Petitioner has proposed for limitation [1.3], as best we can understand, is to incorporate Mazzola’s address translation mechanism into Devi, and use it, rather than the circuitry and steps disclosed in Devi, to process the incoming data packets. That means in the proposed combination, there would not be, as disclosed in Devi, a mapping of each received data packet to a particular associated egress link, and then a determination of a particular port based on other criteria such as round robin distribution among the ports in a LAG group. But such disclosures are what Petitioner has relied on to account for limitation [1.2] as discussed above.

Patent Owner correctly asserts: “Mazzola does not mention Link Aggregation, nor does it seek to balance a traffic load within the LAG group.” Prelim. Resp. 39. Petitioner has not adequately explained how, in its proposed combination, limitation [1.2] would still be met when Mazzola’s address translation mechanism is incorporated into Devi.

Mazzola also does not appear to disclose sending a data packet to only a single port among the plurality of ports in a LAG. Although Mazzola describes that each port is associated with a unique index value and a VLAN “color” identifier (Ex. 1007, 3:12–14), Mazzola also describes that “[t]he destination of any frame may be one or more ports” (Ex. 1007, 6:16–17) and that a port can be a multicast port including a group of ports (Ex. 1007, 6:20–24). More importantly, Mazzola does not describe balancing the traffic load within a LAG group as is required by limitation [1.2].

For the foregoing reasons, Petitioner’s accounting for limitation [1.3] is not sufficiently specific. It is unclear how Devi would still operate successfully to meet limitation [1.2] when Devi is modified by Petitioner in light of Mazzola to meet limitation [1.3]. It also is unclear how the rest of Devi’s components would operate once a data packet is allocated an FMID associated with a port, e.g., which functionalities are kept and which are maintained.

e) Conclusion for Claim 1

Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 1 over Devi and Mazzola.

3. Independent Claim 12

Claim 12 is a method claim and its method steps performed by recited parts correspond to the functions performed by essentially the same components recited in claim 1. Ex. 1001, 10:10–55, 11:34–12:3. Limitations [1.1] through [1.3] correspond respectively to limitations [12.1] through [12.3]. Limitations [1.4] and [1.5] collectively correspond to limitations [12.4] and [12.5]. Limitation [1.6] corresponds to limitation

[12.6]. Neither Petitioner nor Patent Owner present separate arguments for claims 1 and 12.

The deficiencies of the Petition with respect to claim 1, as discussed above, equally apply to claim 12. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 12 over Devi and Mazzola.

4. *Dependent Claims 2–11 and 13–24*

Claims 2–11 each depend from claim 1, directly or indirectly. Each incorporates all of the limitations of independent claim 1. The deficiencies of Petitioner’s combination of Devi and Mazzola, as discussed above in the context of claim 1, equally apply to claims 2–11. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claims 2–11 over Devi and Mazzola.

Claims 13–24 each depend from claim 12, directly or indirectly. Each incorporates all of the limitations of independent claim 12. The deficiencies of Petitioner’s combination of Devi and Mazzola, as discussed above in the context of claim 12, equally apply to claims 13–24. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claims 13–24 over Devi and Mazzola.

E. *Discretionary Denial Under 35 U.S.C. § 325(d)*

Patent Owner contends that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) based on the framework set forth in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). Prelim. Resp. 10–19. In *Advanced Bionics*, the Board applied a two-part framework

in considering whether to exercise discretion to deny institution under § 325(d):

(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics at 8 (footnote omitted).

Within this two-part framework, the Board considers a number of non-exclusive factors in evaluating whether to exercise its discretion under § 325(d). *See Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first para.); *see also Advanced Bionics* at 9–11. The factors set forth in *Becton, Dickinson* are as follows:

(a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson at 17–18 (footnote omitted).

Becton, Dickinson factors (a), (b), and (d) relate to whether the art or arguments presented in the Petition are the same or substantially the same as those previously presented to the Office. *Advanced Bionics* at 10. Factors

(c), (e), and (f) “relate to whether the petitioner has demonstrated a material error by the Office” in its prior consideration of that art or arguments. *Id.* Only if the same or substantially the same art or arguments were previously presented to the Office do we then consider whether petitioner has demonstrated a material error by the Office. *Id.* “At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” *Id.* at 9.

Patent Owner asserts that “Petitioner relies on references that are the same or substantially the same as art that was presented to the Patent Office yet doesn’t even attempt to demonstrate that the Office erred in any way.” Prelim. Resp. 12. The issue here is whether Petitioner relies on references that are the same or substantially the same as prior art references that were presented to the Office. We agree with Petitioner’s position that it has not.

As noted above, the alleged grounds of unpatentability are:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–24	103(a)	Devi, Mazzola
1–24	103(a)	Borgione, Mazzola

Petitioner acknowledges that the Examiner during prosecution of the application resulting in the ’525 patent considered Devi. Pet. 80. Petitioner asserts, however, that the Examiner never considered Borgione or Mazzola, and therefore the Examiner never considered the combination of Devi and Mazzola and the combination of Borgione and Mazzola. *Id.* at 79–80.

Neither Borgione nor Mazzola appears in the prosecution record in any way, and Patent Owner does not contend otherwise. This supports

Petitioner's contention that the Examiner never considered Borgione or Mazzola, and therefore the Examiner never considered the combination of Devi and Mazzola or the combination of Borgione and Mazzola. Even assuming Devi and Borgione are duplicative as asserted by Patent Owner, the issue turns to whether a prior art reference that is substantially the same as Mazzola was considered by the Examiner.

Patent Owner asserts that Mazzola is substantially similar to what was overcome during prosecution. Prelim. Resp. 13. We are, however, persuaded by Petitioner that it is not.

Regarding alleged unpatentability based on Devi and Mazzola, Patent Owner's assertions are incorrect. Patent Owner asserts that for alleged obviousness of independent claims 1 and 12 over Devi and Mazzola, Petitioner relies on Devi for all claim elements and only applies Mazzola in the alternative. *Id.* at 14. That is incorrect. For limitations [1.6] and [12.6], Petitioner does not rely on Devi alone but Devi in combination with Mazzola. Pet. 33, 36. Patent Owner asserts that this alleged ground is not in fact a combination of Devi and Mazzola but an alternative proposed modification of Devi. Prelim. Resp. 14. This assertion is without merit, because the proposed modification of Devi stems from the teachings of Mazzola and thus reflects the combined teachings of Devi and Mazzola. Pet. 36–38. Patent Owner asserts that “[t]he Examiner considered similar art as Mazzola in ‘Morikawi.’”⁹ Prelim. Resp. 15. But Patent Owner does not point out where Moriwaki discloses a two-tier address translation system in which a value in a first range is allocated to a data packet, which is thereafter

⁹ The reference is U.S. Published App. 2003/0002506 A1. The inventor name, however, is Moriwaki, not Morikawi.

reduced to a value in a smaller second range, which is thereafter mapped to a corresponding output port. Patent Owner points to no such teaching in Moriwaki, and it is that teaching from Mazzola which Petitioner relies on in combination with Devi (Pet. 36–38).

Regarding alleged unpatentability based on Borgione and Mazzola, Patent Owner acknowledges that Petitioner relies on Mazzola for “the concept of assigning C-FMID values smaller than LC-FMID values required by claim elements 1.6 and 12.6.” Prelim. Resp. 17. Patent Owner asserts: “As Devi and Moriwaki in the context of the ’525 prosecution history illustrates, the Examiner already considered art duplicative of Borgione in view of Mazzola; and thus, Borgione and Mazzola do not ‘add significantly to the information considered by the Examiner during prosecution.’” *Id.* at 19 (citation omitted). But still, as noted above, Patent Owner does not identify any teaching from Moriwaki on the concept of assigning C-FMID values smaller than LC-FMID values as required by claim elements 1.6 and 12.6.

As Petitioner correctly notes (Prelim. Reply 1–2), the Petition relies on Mazzola’s teachings to meet the limitation that the switching fabric maps a range of LC-FMID values to a smaller range of C-FMID values. Pet. 36–38, 72–74. Also as Petitioner correctly notes, the Examiner deemed application claim 13 which included this limitation to be allowable over Devi and Moriwaki. Prelim. Reply 2 (citing Ex. 1002, 589–595). While the Examiner rejected application claims which did not have this limitation, the Examiner stated that application claim 13 which included this limitation, “would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include

all of the limitations of the base claim and any intervening claims.”

Ex. 1002, 595.

Petitioner sufficiently has shown that Mazzola is not substantially the same in content to Moriwaki. Patent Owner has not, either in the Preliminary Response or in its Sur-Reply, identified any other prior art reference in the prosecution record which even in Patent Owner’s view provides the same or substantially the same disclosure as Mazzola with respect to limitations [1.6] and [12.6]. On this record, no prior art reference in the prosecution history is the same or substantially the same as Mazzola, a key reference in both alleged grounds of unpatentability. For that reason, we decline to exercise discretion under 35 U.S.C. § 325(d) to deny the Petition.

III. CONCLUSION

After considering the evidence and arguments presented in the current record, we determine that Petitioner has demonstrated a reasonable likelihood of success in proving that at least one of the challenged claims of the ’525 patent is unpatentable. We also find that discretionarily denying the Petition based on 35 U.S.C. § 325(d) would be inappropriate. We therefore institute trial on all challenged claims and grounds raised in the Petition. *See PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (indicating that a decision whether to institute an *inter partes* review “require[s] a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

At this stage of the proceeding, we have not made a final determination as to the patentability of any challenged claim or as to the construction of any claim term.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–24 of the '525 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '525 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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Patent 7,697,525 B2

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