

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

FUTURE LINK SYSTEMS, LLC,
Patent Owner.

IPR2021-01487
Patent 6,622,108 B1

Before KARL D. EASTHOM, KEVIN C. TROCK, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Apple Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1, 3, 6, and 11–13 of 6,622,108 B1 (Ex. 1001, the “’108 patent”). Future Link Systems, LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2020). Institution of an *inter partes* review requires that the information presented in the Petition shows “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons set forth below, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim. Accordingly, we institute an *inter partes* review of the ’108 patent.

II. BACKGROUND

A. *Real Parties in Interest*

The parties identify themselves as real parties in interest. Pet. 86; Paper 4, 1.

B. *Related Matters*

The parties identify the following proceedings as related matters involving the ’108 patent: *Future Link Systems, LLC v. Advanced Micro Devices, Inc.*, No. 6:20-01176-ADA (W.D. Tex.) (the “AMD District Court”); *Future Link Systems, LLC v. Apple Inc.*, No. 6:21-cv-00263-ADA (W.D. Tex.) (the “WDTX,” “WDTX Court,” or “WDTX litigation”); *Intel*

Corp. v. Future Link Systems, LLC, No. 14-377-LPS (D. Del.) (the “Delaware District Court”).¹ See Paper 4, 1; Pet. 13 (citing Ex. 1007), 86.

A co-pending *inter partes* review trial also involves challenges to the ’108 patent claims. *Advanced Micro Devices, Inc. v. Future Link Systems, LLC*, IPR2021-01301 (PTAB Jan. 19, 2022) (institution decision).

C. The ’108 Patent

The ’108 patent discloses systems and methods for testing interconnects of electronic circuits. Ex. 1001, code (57). The ’108 patent describes using a test unit operated as a low complexity memory as part of a first electronic circuit for testing the interconnects between that first circuit and a second electronic circuit. *Id.* at 5:4–8, 6:15–19. “Low complexity memories are those memories that do not have to be put through a complex initiali[z]ation process before they can be accessed, and that have simple access protocols without dynamic restrictions.” *Id.* at 2:35–38.

Some examples of “[l]ow complexity memory types” include “Static Random Access Memories (SRAMs)” and “Programmable” Read Only Memories (“ROMs”). Ex. 1001, 4:61–62. These memory types “can readily be tested for their connectivity using neighbo[r]ing circuits equipped with boundary-scan or neighbor[r]ing microprocessors and/or ASICs.” *Id.* at 4:63–65. An example of high complexity memory is an SDRAM (synchronous dynamic random access memory). *Id.* at 3:61–4:2.

The ’108 patent describes another embodiment for “the test unit being operable as a low complexity memory” as a “combinatorial circuit.” Ex. 1001, 3:37–43. Generally, “it is not required that the test unit is

¹ Each short-hand designation does not refer to the case citation. Rather, each one refers to the particular District Court for the identified related matter. See *infra* § III.D.

implemented as a real ROM table. Especially if only a small number of test patterns is used, the test unit could be implemented as a combinatorial circuit, leading to more efficient area usage.” *Id.* Examples of combinatorial circuits include circuits with XOR (exclusive or) or XNOR (exclusive nor) gates. *Id.* at 10:42–49, 13:12–19, Fig. 5 (2 XNOR gates), Fig. 6 (2 XOR gates).

Figure 4 of the '108 patent follows:

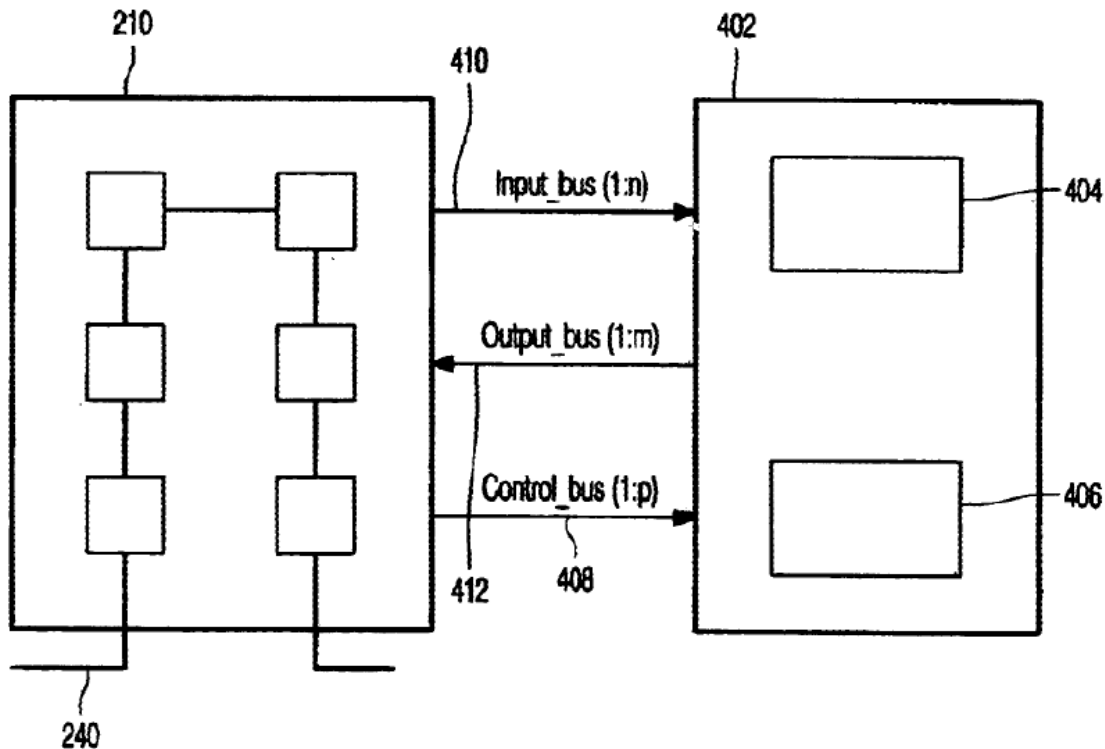


FIG. 4

Figure 4 above illustrates an embodiment for testing circuit 402’s interconnects using boundary scan chain 240 of neighboring processor 210. Ex. 1001, 9:30–36. Circuit 402 includes main unit 404 and test unit 406. *Id.* at 9:30–31. Test unit 406 is a “combinatorial circuit” between input bus 410 and output bus 412 and “implements the functionality of a ROM table.” *Id.* at 10:8–9. “The main unit 404 is active in the normal operational mode of

the circuit and the test unit is active in the test mode of the circuit.” *Id.* at 9:33–35.

According to the specification, “an embodiment of the electronic circuit is defined in claim 3.” Ex. 1004, 3:43–44. In this embodiment, “no address bus is needed since only a single register is used.” *Id.* at 3:49–51. Claim 3 recites “[a]n electronic circuit as recited in claim 1, wherein the test unit comprises a read/write register.” *Id.* at 12:61–62.

D. Illustrative Claims

Independent claims 1 and 11 follow:

1. An electronic circuit comprising:

[1a] a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,

[1b] a main unit for implementing a normal mode function of the electronic circuit, and

[1c] a test unit for testing the interconnects,

[1d] the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit,

[1e] such that in the test mode the test unit is operable as a low complexity memory via the I/O nodes.

11. A method of testing interconnects between a first electronic circuit and a second electronic circuit, the first electronic circuit comprising a main unit implementing a normal mode function of the first electronic circuit, and a test

unit for testing the interconnects, the method comprising the steps of

[11a] logically connecting the test unit to the interconnects, and

[11b] putting test data on the interconnects by the second electronic circuit,

[11c] wherein the putting step comprises operating the first electronic circuit as a low complexity memory by the second electronic circuit.

Ex. 1001, 12:45–57, 14:5–17 (bracketed nomenclature added to conform to the Petition).

E. Asserted Grounds of Unpatentability

Petitioner contends that claims 1, 3, 6, and 11–13 are unpatentable as follows:²

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3, 6, 11–13	103(a)	Langford ³
6	103(a)	Langford, Hong ⁴

Pet. 2–3. Petitioner supports its Petition with the Declaration of Dr. David Kuan-Yu Liu (Ex. 1006).

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. Because the ’108 patent’s effective filing date precedes the March 16, 2013, effective date of the applicable AIA amendments, the pre-AIA version of § 103 applies.

³ U.S. Pat. No. 5,115,435, issued May 19, 1992 (Ex. 1004).

⁴ U.S. Pat. No. 4,241,307, issued Dec. 23, 1980 (Ex. 1005).

III. ANALYSIS

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). “[W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.” *KSR*, 550 U.S. at 416 (citing *United States v. Adams*, 383 U.S. 39, 50–51 (1966)). The question of obviousness involves resolving underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Determining whether an invention would have been obvious under 35 U.S.C. § 103 requires resolving the level of ordinary skill in the pertinent art at the time of the effective filing date of the claimed invention. *Graham*, 383 U.S. at 17. The person of ordinary skill in the art is a hypothetical person who knows the relevant art. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors in determining the level of ordinary skill in the art include the types of problems encountered in the art, the sophistication of the

technology, and educational level of active workers in the field. *Id.* One or more factors may predominate. *Id.*

Petitioner contends that a person having ordinary skill in the art (“POSITA”) “would have had at least a bachelor’s degree in electrical engineering or equivalent with at least one year of experience in the field of circuit design or circuit testing,” with “[a]dditional education or experience . . . substitut[ing] for the[se] requirements.” Pet. 11 (citing Ex. 1006 ¶¶ 30–32). Patent Owner does not dispute Petitioner’s proposed level of ordinary skill in the art in its Preliminary Response, nor does it propose a different level of skill.

In the related co-pending *inter partes* review, IPR2021-01301, the Board’s institution decision relies on and adopts a slightly different proposed level based on the petitioner’s input in that case: “[A] person having ordinary skill in the art . . . ‘would have had a bachelor’s degree in electrical or computer engineering or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa.’” IPR2021-01301, Paper 9, 8 (quoting the petition there). Petitioner’s proposal here largely overlaps with the Board’s adopted level of skill in the IPR2021-01301 institution decision. The IPR2021-01301 trial involves challenges to some of the same ’108 patent claims, and it involves similar prior art. *See* IPR2021-01301, Paper 9, 6 (listing, *inter alia*, Hong as a prior art reference).

Based on our review of the record, for purposes of this Institution Decision, we adopt the level of ordinary skill in the art as stated in the IPR2021-01301 institution decision (as repeated above) as reasonable,

because it is consistent with the evidence of record, including the asserted prior art.

C. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the district-court-type standard, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 37 C.F.R. § 42.100(b) (2020). Under this standard, claim terms have their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. See *Phillips*, 415 F.3d at 1313–14. Any extrinsic evidence should be considered in the context of the intrinsic evidence. See *id.* at 1317–19.

Claims 1 and 11 recite that “in the test mode the test unit is operable as a low complexity memory.” Petitioner points out that in the prior Delaware District Court litigation (not involving Petitioner), Patent Owner agreed to construe “low complexity memory” as “memory that does not have to be put through a complex initialization process before it can be accessed and that has simple access protocols without dynamic restrictions.” Pet. 14 (citing Ex. 1001, 2:35–38; Ex. 1007, 20; Ex. 1012, 11). Petitioner contends that even though “no construction of this claim language is necessary to resolve the proposed grounds herein, Petitioner has applied the previously agreed construction below.” *Id.*

Patent Owner does not provide a claim construction for any claim term here. At this stage, it is not necessary to explicitly construe any claim terms, because doing so would have no effect in the analyses below of Petitioner’s asserted grounds. See *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that “we

need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Discretion Under 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) in view of the District Court litigation. Prelim. Resp. 4–8 (citing, *inter alia*, *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”)).

Institution of an *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

An advanced state of a parallel district court proceeding is a “factor that weighs in favor of denying the Petition under § 314(a).” *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) (“*NHK*”). Specifically, an early trial date is part of a “balanced assessment of all relevant circumstances in the case, including the merits.” Consolidated Trial Practice Guide November 2019 (“TPG”) 58.⁵

⁵ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

This balanced assessment involves consideration of the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, Paper 11 at 5–6.

1. *Factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

Petitioner filed a recent WDTX Court order that stays the WDTX litigation and indicates the WDTX Court's intention to transfer the case to the District Court for the Northern District of California ("NDCA" or "NDCA Court"). Ex. 3001; Ex. 3002.

Accordingly, this factor weighs against exercising our discretion to deny institution.

2. *Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision*

The projected date of the Board's final written decision in this case is early April 2023. As indicated above, Petitioner filed a recent WDTX Court order that indicates that the WDTX litigation will be transferred to the

NDCA Court. Ex. 3001. The transfer has not yet occurred, so the NDCA Court has not yet scheduled a trial.

Accordingly, this factor weighs against exercising our discretion to deny institution or is at most neutral.

3. *Factor 3: investment in the parallel proceeding by the court and the parties*

If, at the time of the institution decision, a district court has issued substantive orders related to the challenged patent, such as a claim construction order, this circumstance weighs in favor of denial. *See Fintiv*, Paper 11 at 9–10. On the other hand, if the district court has not issued such orders, this circumstance weighs against discretionary denial. *Id.* at 10. Moreover, in evaluating this factor, “[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution under *NHK*.” *Id.* at 11.

The following refers to what transpired prior to the stay order by the WDTX Court:

The Preliminary Response, filed prior to the stay order by the WDTX Court, states that “[t]he District Court has already conducted claim construction proceedings on this patent in the parallel proceeding.” Prelim. Resp. 7. Patent Owner appears to be referring to a “separate action against Advanced Micro Devices [AMD] asserting the ’108 patent,” wherein “the [AMD] District Court considered various claim construction arguments and rendered claim construction rulings.” *Id.* (citing Ex. 2003). Patent Owner states that “the [AMD] District Court offered Petitioner here (Apple, Inc.) the opportunity to participate in those proceedings.” *Id.* at 7 (citing Ex. 2003). Yet the record does not show, and Patent Owner does not assert, that

Petitioner participated in the AMD District Court action. *See id.* Patent Owner also does not identify any particular claim term of the '108 patent construed in the AMD District Court (or in any District Court) that is relevant to Petitioner's unpatentability contentions in this case.⁶

In addition, the WDTX Court's scheduling order states that with respect to Petitioner, the *Markman* hearing for the '108 patent is "TBD" and that the listed date "is a placeholder." Ex. 2001. In light of this, and based on the present record, it is not clear if a *Markman* hearing involving the '108 patent and Petitioner occurred during the WDTX litigation.

According to the Petition (prior to the stay order), "the parties have invested little in the parallel proceeding. Invalidity contentions were just served on Sept. 17, 2021, no claim construction positions have been taken by either party, and little discovery has been conducted." Pet. 78–79.

According to the Preliminary Response (prior to the stay order), "[t]he parties have . . . engaged in early discovery relating to licensing and venue issues, and are about to begin full fact discovery pursuant to the schedule set by the [WDTX] Court." Prelim. Resp. 7. Patent Owner's argument, and the WDTX Court's scheduling order, shows that fact discovery was open and

⁶ In the related IPR2021-01301, in which AMD is the petitioner (*supra* § II.B), the Board's institution decision notes that the AMD District Court (referred to as the "Waco District Court" there) adopted the same claim construction for "low complexity memory" as the Delaware District Court. *See* IPR2021-01301, Paper 8–13, 16–19. As here, the Board did not adopt a specific claim construction for any claim term or give any district court claim construction much weight in the Board's *Fintiv* analysis even though AMD participated in the AMD/Waco District Court action. *See id.* at 18 ("Aside from the [AMD/]Waco District Court's claim construction of 'low complexity memory,' which we do not adopt at this preliminary stage for the reasons discussed above . . ., Patent Owner points to no other investment by the parties toward the patentability issues presented here.").

incomplete prior to the stay order. *See* Ex. 1008, 6 (noting the parties’ proposed deadline of “8/10/2022” for close of fact discovery). On this record, there is little indication that significant discovery on relevant patentability issues had occurred prior to the stay order. The parties’ proposed deadlines in the WDTX Court for the close of expert discovery (“10/5/2022”) and for dispositive and *Daubert* motions (“10/19/2022”) further show that significant patentability work remained at the time of the stay order. *See id.* at 6–7.

Therefore, even if we were to consider the filings, discovery, findings, or other work performed during the WDTX litigation as being applicable to the forthcoming proceeding before the NDCA Court, the record does not show a significant investment in the WDTX litigation related to the substantive patentability issues presented here. *Cf. Sand Revolution II*, Paper 24 at 11 (“[W]e recognize that much work remains in the district court case as it relates to invalidity: fact discovery is still ongoing, expert reports are not yet due, and substantive motion practice is yet to come.”). Similar to the circumstances in *Sand Revolution II*, fact and expert discovery, final invalidity contentions, and dispositive motions, were not complete in the WDTX litigation. *See Fintiv*, Paper 11 at 9–10 (this factor concerns, in part, “duplicative costs”); *Apple Inc. v. Parus Holdings, Inc.*, IPR2020-00686, Paper 9 at 17 (PTAB Sept. 23, 2020) (noting *Fintiv*’s concern with “duplicative costs” and finding “as far as claim construction is concerned, there is little risk of the parties or us duplicating work performed in the Texas case should we proceed to a trial” where the parties relied on the plain meaning in the IPR).

Petitioner also asserts that it filed the Petition with due diligence and “approximately six months before the filing deadline.” *Id.* at 79. Patent

Owner does not address the timeliness of the Petition. The record shows that Petitioner filed the Petition diligently (i.e., on September 28, 2021). The filing date was about six months after the filing date of the complaint (March 16, 2021), about two months after the due date for service of preliminary infringement contentions (July 8, 2021), and about two weeks after the due date for service of preliminary invalidity contentions (September 16, 2021). *See* Pet. 78–79; Prelim. Resp. 7 (“The parties have . . . exchanged preliminary infringement and invalidity contentions”); Ex. 2001. Petitioner’s due diligence factors holistically with the noted minimal investment in the District Court parallel proceeding as summarized above.

Accordingly, this factor weighs against exercising our discretion to deny institution.

4. Factor 4: overlap between issues raised in the petition and in the parallel proceeding

Petitioner “stipulate[s] that, if this IPR is instituted, Petitioner will not pursue invalidity grounds in the district court litigation that rely on the base reference advanced herein (Langford (Ex. 1004)).” Pet. 79 (citing *Sand Revolution II*, Paper 24 at 11–12 (addressing a stipulation)). Patent Owner argues that the stipulation is “hollow” and “virtually meaningless because if the Petition is instituted but unsuccessful (such that one or more claims are held not-unpatentable[]), Petitioner would be estopped from reliance on Langford, Hong, or indeed any patent or printed publication that could have been identified in the Petition.” *See* Prelim. Resp. 7–8.

Notwithstanding Patent Owner’s arguments, Petitioner’s stipulation “mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.” *Sand Revolution II*, Paper 24 at 12.

Accordingly, this factor weighs slightly against exercising our discretion to deny institution.

5. Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

The same parties here will be the parties in the NDCA Court after the transfer. Prelim. Resp. 8. Because it is not clear whether the trial in the NDCA will precede the deadline for a final written decision in this proceeding, this factor weighs against exercising discretion to deny institution or is at most neutral.

6. Factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

Patent Owner argues that “[t]he ’108 patent is at issue in two District Court actions (and in a previous petition filed by Advanced Micro Devices).” Prelim. Resp. 8. Nevertheless, Patent Owner’s argument does not explain persuasively how the Board should weigh the AMC District Court action or the previous petition. *See id.* Neither involves Petitioner here.

Petitioner argues that “the strength of the proposed grounds weighs strongly in favor of institution.” Pet. 80. The factors typically considered in the exercise of discretion are part of a balanced assessment of all the relevant circumstances in the case, including the merits. *Fintiv*, Paper 11 at 14. For example, if the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution. *Id.* at 14–15. By contrast, if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present. *Id.* at 15. In *Sand Revolution II*, the panel determined that this factor weighed in favor of not exercising discretion

when the petitioner had “set forth a reasonably strong case for the obviousness of most challenged claims.” *Sand Revolution II*, Paper 24 at 13.

As summarized below, Petitioner sufficiently shows for purposes of institution that at least challenged independent claims 1 and 11 would have been obvious over the asserted art.

Accordingly, this factor is neutral as to exercising discretion to deny institution.

7. Conclusion

The Board “holistic[ally] view[s] . . . whether efficiency and integrity of the system are best served by denying or instituting review” under § 314(a) when evaluating the *Fintiv* factors. *Fintiv*, Paper 11 at 6. Evaluating all of the factors on this record, we decline to exercise our discretion under § 314(a) to deny institution of *inter partes* review.⁷

E. Ground 1: Asserted Obviousness Based on Langford

Petitioner asserts that claims 1, 3, 6, and 11–13 are unpatentable under 35 U.S.C. § 103(a) based on Langford. Pet. 15–60.

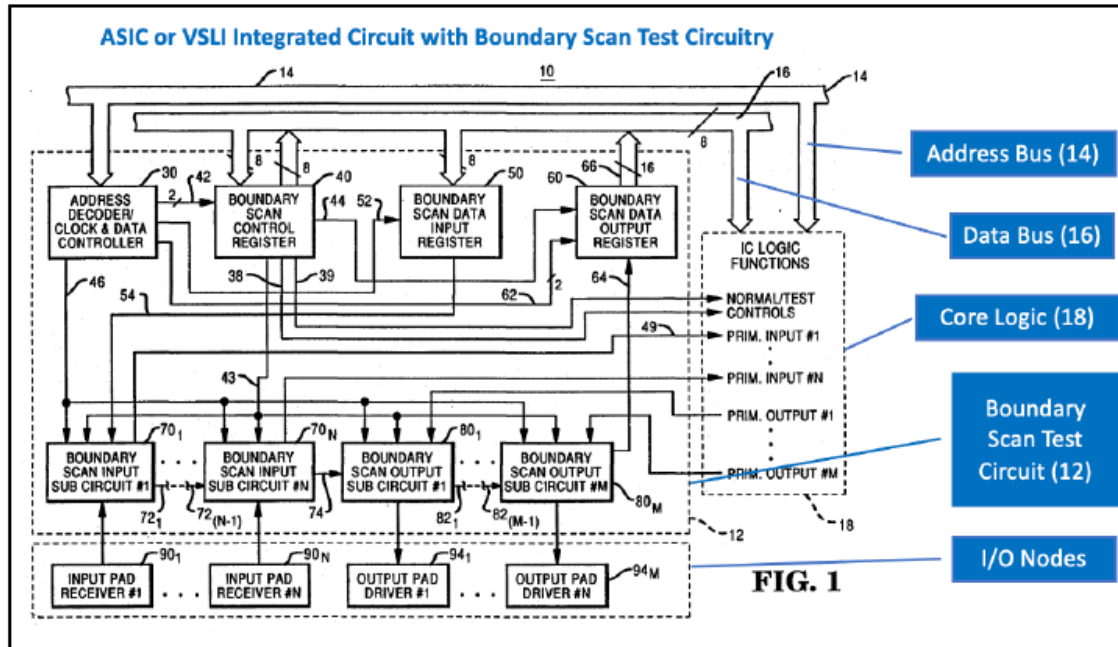
1. Langford

Langford discloses a “boundary scan test circuit . . . which does not require any additional pads/pins to support full boundary scan functionality” by using “the power and capability of existing address and data buses to transfer test data into the integrated circuit under boundary scan test, and

⁷ Given the decision here, we do not address Petitioner’s direct challenges to *Fintiv*. See Pet. 81–84.

uses the same buses to transfer test results out of the integrated circuit under test.” Ex. 1004, code (57).

Figure 1 of Langford, as annotated by Petitioner, follows:



Annotated Figure 1 above illustrates integrated circuit 10 with boundary scan test circuit 12, input/output nodes 90, 94, core logic 18, data bus 16, and address bus 14. See Ex. 1004, 4:30–51. Langford’s circuit operates as follows:

During normal operation, . . . buses 14, 16 communicate address and data information between IC logic functions 18 and a larger external system (not shown). However, during a test operation, the buses 14, and 16 communicate with the boundary scan test circuit 12 primarily, and with the IC logic functions 18 as required by the test operation.

Ex. 1004, 4:37–42.

2. Independent Claims 1 and 11

Petitioner contends that Langford would have rendered independent claims 1 and 11 obvious. Pet. 21–46, 52–54. To support the Petition, Petitioner relies on the testimony of Dr. Liu. *Id.* Patent Owner does not

address Petitioner's showing with respect to claims 1 and 11. *See generally* Prelim. Resp.

a) Claim 1

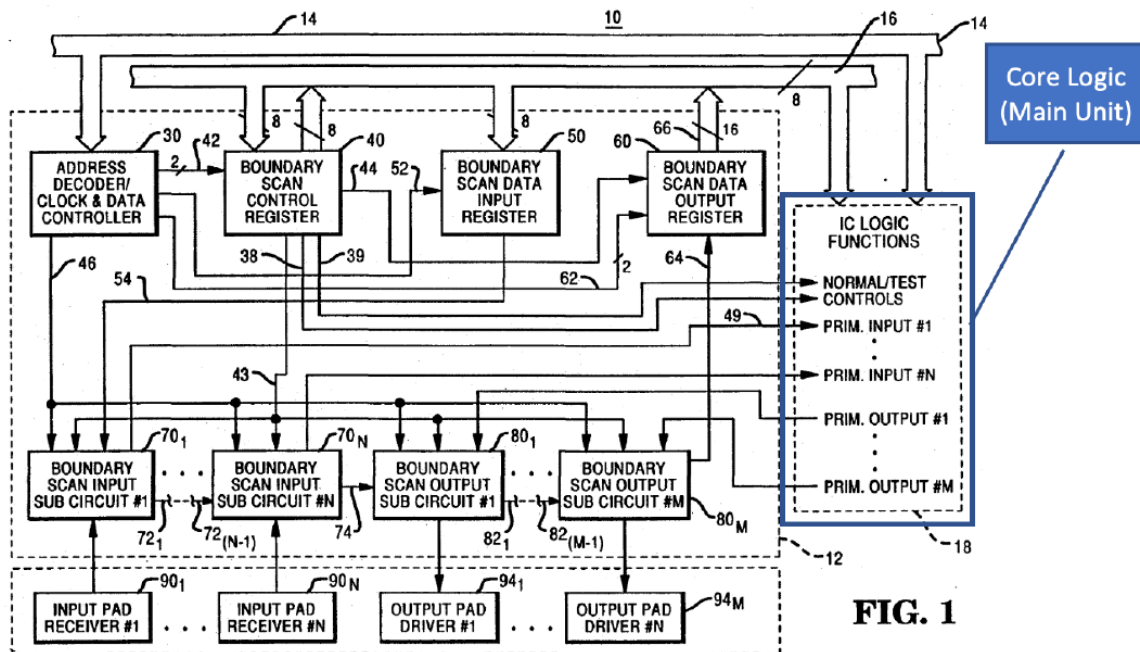
The preamble of claim 1 recites “[a]n electronic circuit comprising.” Petitioner contends that “to the extent the preamble is limiting,” Langford discloses an electronic circuit. *See* Pet. 21. Specifically, Petitioner relies on Langford's electronic circuit as illustrated in Figure 1. *See id.* Petitioner explains that Langford discloses a “boundary scan test circuit ‘for inclusion into ASIC and or VLSI circuits.’” *Id.* (quoting Ex. 1004, code (57))

Limitation 1a recites “a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects.” In one alternative showing, Petitioner reads this limitation on Langford's “data inputs and data outputs” associated with address bus 14 and data bus 16. *See* Ex. 1004, Fig. 1 (reproduced as annotated by Petitioner above); Pet. 24–26 n.4 (citing Ex. 1004, Fig. 1, 5:52–54, 5:56–6:9, 6:29–7:43, 6:43–46, 7:44–8:99:65–10:7, 12:48–52; Ex. 1006 ¶¶ 48–49). According to Petitioner, “*Langford* acknowledges tested circuits typically have address and data buses ‘electrically connected’ to ‘input/output pin[s],’” so that an artisan of ordinary skill would have recognized that the address and data buses would have been connected to external circuitry (using the external pins). *Id.* at 24 (quoting Ex. 1004, 1:51–55; citing Ex. 1006 ¶¶ 48–49).

In a second alternative showing, Petitioner reads limitation 1a onto Langford's input pads 90 and output pads 94 as depicted in Figure 1. Pet. 23–24 (citing Ex. 1004, 3:3–20, 11:36–41, 13:2–11, Fig. 1). According to Petitioner, “[d]uring boundary scan testing, test data may be input through the input pads and output through the output pads.” *Id.* at 24 (citing

Ex. 1004, 10:64–11:1 (describing external source data buffered into the integrated circuit over the input pad receivers), 6:21–25 (describing shifting test data out the output drivers to external circuits)).

Limitation 1b recites “a main unit for implementing a normal mode function of the electronic circuit.” Petitioner reads this limitation onto Langford’s IC logic functions circuit 18. Pet. 26–27. To illustrate its showing, Petitioner annotates Langford’s Figure 1 as follows (*id.* at 27):



Langford’s Figure 1 above shows IC logic functions unit/circuit 18 identified by Petitioner as “Core Logic (Main Unit)” (blue) on the right-hand side. According to Petitioner,

[i]n “normal operation,” *Langford’s* circuit uses additional “switching circuits” to “logically connect” input and output signals communicated between the circuit’s input/output pads and the IC logic functions. [Ex. 1004,] 4:43–48. A “tri-state gate” is used to logically connect input pad receivers to the “normal input” of IC logic functions. *Id.* at 11:1–6. Another tri-state gate is used to logically connect the IC logic function to “an input of the output pad driver” during “normal operation.” *Id.* at 12:13–16. Additionally, *Langford’s* address and data buses

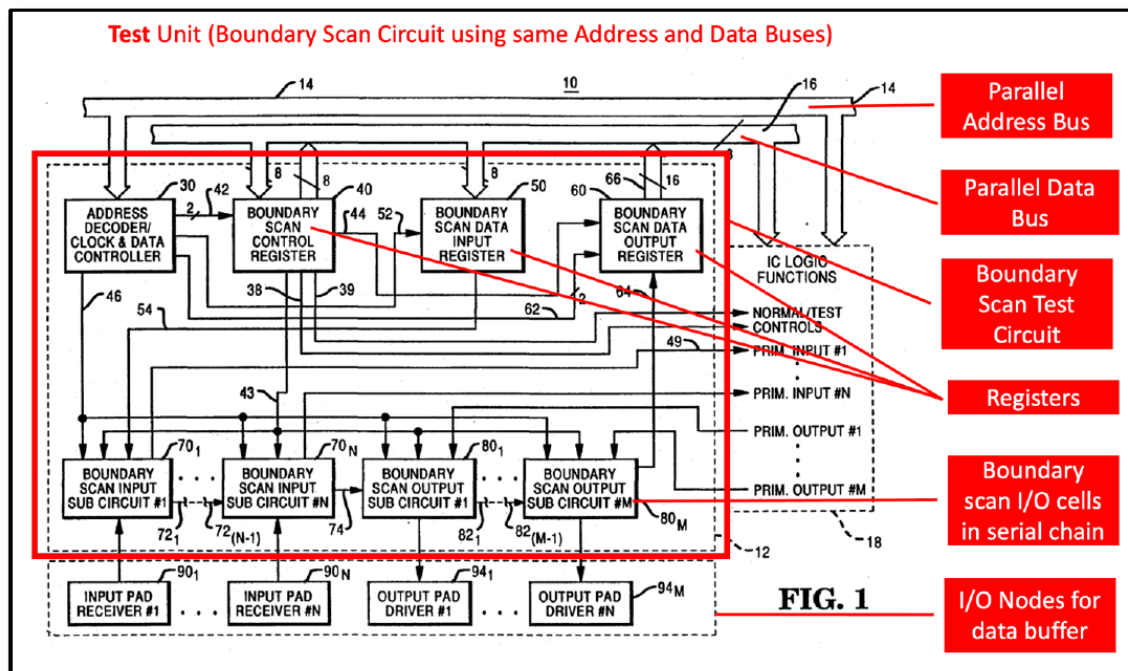
“communicate address and data information between IC logic functions 18 and a larger external system” during normal operation. *Id.* at 4:33–42.

Pet. 27.

Limitation 1c recites “a test unit for testing the interconnects.”

Petitioner reads this limitation onto Langford’s “boundary scan test circuit” 12 as depicted in Figure 1. Pet. 28 (emphasis omitted) (quoting Ex. 1004, code (57)). Petitioner explains that in Langford, “[t]est data may also be input directly to the input sub-circuits and output from the output sub-circuits.” *Id.* at 29. Petitioner further explains that Langford’s boundary scan test circuit 12 “includes ‘switching circuits’ used to ‘logically connect . . . input signals and . . . output signals communicated between the IC logic functions . . . and the input/output pads of the integrated circuit.’” *Id.* (quoting Ex. 1004, 4:43–48).

Petitioner annotates Langford’s Figure 1, shown below, to illustrate the claimed test unit as including boundary scan test circuit 12 (Pet. 28):



Langford's Figure 1 above shows Langford's "boundary scan test circuit 12" (outlined in red) connected via address buses 14 and data buses 16 for testing interconnects of main unit (IC logic functions unit) 18. *See* Ex. 1004, 4:12–66.

According to Petitioner,

[a]n eight-bit "boundary scan control register" controls the operation of boundary scan circuit. [Ex. 1004,] 7:1–15. A collection of input sub-circuits and output sub-circuits form a boundary scan path, or chain, for serially shifting test data from the boundary scan data input register 50 to boundary scan data output register 60. *Id.* at 5:52–6:33. From boundary scan data output register 60, the test data "may be read to the data bus 16 for transmission to a processor or other system bus device." *Id.* at 6:36–38.

Pet. 29. Petitioner also relies on and annotates Figures 6 and 7 to show how Langford's switch gates (sub-circuit tri-state gates in circuits 70) "logically connect the input pad receivers to the boundary scan circuitry rather than normal IC logic functions." *See* Pet. 30–31. "Similarly, control lines operate output sub-circuit tri-state gates to logically connect the output sub-circuit to the output pad drivers rather than normal IC logic functions" *See id.* at 31–32 (annotating Ex. 1004, Figs. 6, 7).

Limitation 1d recites "the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit." Petitioner quotes Langford as disclosing a "**normal mode** of operation and a **boundary scan test mode** of operation." Pet. 32 (emphasis by Petitioner) (quoting Ex. 1004, 3:1–3).

Petitioner explains further as follows:

[A]ddress bus and data bus communicate with the main unit (IC logic functions 18) during a normal mode and with the test unit

during test mode: “[d]uring normal operation, these buses 14, 16 communicate address and data information between IC logic functions 18 and a larger external system (not shown). However, during a test operation, the buses 14, and 16 communicate with the boundary scan test circuit 12 primarily[.]” [Ex. 1004,] 4:36–41; *see also id.* at 5:4–6:38 (describing the process by which addresses may be input from the address bus into address decoder/clock and data controller 30 to initiate a test and by which test data is written from the data bus into scan data input register 50, shifted through the boundary scan sub-circuits to scan data output register 60, and read back to the data bus).

Pet. 32–33.

Finally, limitation 1e recites “that in the test mode the test unit is operable as a low complexity memory via the I/O nodes.” Petitioner contends that “*Langford’s* boundary scan test circuitry operates as low complexity memory in both structure and function.” Pet. 39.

Petitioner explains that “[s]tructurally,” *Langford’s* “boundary scan test circuitry employs registers comprising basic latch storage circuits for conducting boundary scan testing.” Pet. 40 (citing Ex. 1004, 2:41–44 (describing a method of boundary scan testing using registers), 2:49–52 (describing boundary scan testing apparatus using registers), 6:26–33 (describing latch based storage sub-circuits)).

Petitioner explains further as follows:

Langford expressly describes registers as an aggregation of latches when he refers to the boundary scan input register’s eight, 1-bit “flip-flops” synonymously as “latches.” *Id.* at 7:47–50, 7:56–59, and Fig. 3. *Langford* makes the same association with respect to the boundary scan output register when describing the output register as sixteen, 1-bit flip-flops as latches at 9:67–10:1, 10:36–45, and Fig. 5. A [person of ordinary skill in the art] would have recognized *Langford’s* latch-based registers as low complexity memory. Liu Dec. (Ex. 1006), ¶¶ 51–54 (noting the ’108 Patent further defines the instant “test unit . . . operable as

low complexity memory” of Claim 1 as a “read/write register” in Claim 3 at 12:61–62 (emphasis added), and concluding *Langford*’s latches aggregate into the same type of register-based low complexity memory as claimed in the ’108 Patent).

Pet. 40. In other words, citing and relying on the testimony of Dr. Liu at paragraphs 51–54, Petitioner contends that *Langford*’s registers are flip-flops or latches and are operable as low complexity memory. *See id.*

Relying on the knowledge of an ordinarily skilled artisan, the ’108 patent specification, and Patent Owner’s agreed upon construction (in prior litigation) of “low complexity memory” (*see supra* § III.C), Dr. Liu testifies as follows in support of Petitioner:

Latches and registers are simple circuits that do not require complex initialization processes and that can be simply accessed without dynamic restrictions. Indeed, the fundamental operation is a simple process of inputting, *storing*, and outputting bit values and does not involve the complexity of the SDRAM or flash memories described by the ’108 Patent at 3:61–4:22.

Ex. 1006 ¶ 52 (emphasis added). Dr. Liu also testifies that “[a] POSITA would have recognized *Langford*’s registers 30, 40, 50, and 60 depicted in Fig. 1, as well as the series of input and output sub-circuits, are low complexity memory analogous to the ’108 Patent’s read/write register.” *Id.* ¶ 53 (citing Ex. 1001, 1:46–65 (describing a “boundary-scan register,” 12:61–62 (claim 3 reciting a “read/write register”))).

As summarized above, Petitioner’s showing is sufficient for purposes of institution. As noted above, Patent Owner does not address Petitioner’s showing with respect to claim 1. *See generally* Prelim. Resp.

b) Claim 11

Independent product claim 1 and method claim 11 are materially similar for purposes of institution. Petitioner essentially relies on its showing with respect to claim 1, pointing out applicable claim language

differences where they exist. *See* Pet. 52–54. Patent Owner does not address Petitioner’s showing with respect to claim 11. *See generally* Prelim. Resp.

With respect to the preamble of claim 11, Petitioner asserts that Lanford discloses the recited “method of testing interconnects,” as follows:

The method includes “testing a portion of an integrated circuit” including steps of “receiving a scan data word from [a] data bus . . . shifting said scan data word . . . as a sequence of serial bits . . . over [a] scan path” and “receiving a test response” for “transmitting . . . to the data bus.” [Ex. 1004,] 3:39–59. This method uses a first electronic circuit as described in limitation 1[P], *supra*, with a main integrated circuit and boundary scan test unit as described in limitations 1[b–c], *supra*. *Langford* also describes connecting this electronic circuit to another circuit via external data circuit as described in limitation 1[a], *supra*, where the “further electronic circuit” there constitutes the “second electronic circuit” here. *Langford*’s boundary scan circuitry configuration “allows the logic of each input pad receiver and the interconnect of the input pad receiver to the outside . . . to be tested.” *Id.* at 11:36–41. Further, the configuration “allows the scan data to be transmitted by the output pad drivers . . . to test the output pad driver circuit[s and] . . . connections.” *Id.* at 13:5–11.

Pet. 52–53.

With respect to limitations 11a (“logically connecting the test unit to the interconnects, and”), 11b (“putting test data on the interconnects by the second electronic circuit”), and 11c (“wherein the putting step comprises operating the first electronic circuit as a low complexity memory by the second electronic circuit”), Petitioner largely points to its showing with respect to the similar limitations in claim 1 and also to its showing with respect to claim 3 (reciting “wherein the test unit comprises a read/write register”). *See* Pet. 53–54.

On this record and as summarized above, Petitioner’s showing is sufficient for purposes of institution. As noted above, Patent Owner does not address Petitioner’s showing with respect to claim 11. *See generally* Prelim. Resp.

c) Summary of Claims 1 and 11

Based on the record, we determine that Petitioner shows a reasonable likelihood of prevailing in its assertion that claims 1 and 11 would have been obvious over Langford.

3. Claims 3, 6, 12, and 13

Petitioner provides reasoned and detailed explanations, supported by the testimony of Dr. Liu, indicating how Langford would have rendered claims 3, 6, 12, and 13 obvious. Pet. 46–52, 54–56. Patent Owner does not present arguments directed specifically to these claims. *See generally* Prelim. Resp. On this record, we determine that Petitioner shows a reasonable likelihood of prevailing in its assertion that claims 3, 6, 12, and 13 would have been obvious over Langford.

F. Ground 2: Asserted Obviousness Based on Langford and Hong

Petitioner contends that Langford and Hong would have rendered dependent claim 6 obvious. Pet. 61–71. To support the Petition, Petitioner relies on the testimony of Dr. Liu. *Id.* Patent Owner does not address Petitioner’s showing with respect to claim 6. *See generally* Prelim. Resp.

1. Hong

Hong “relates to the testing of connections between modules mounted on cards and more particularly to circuitry in the modules to provide simple testing of such connections.” Ex. 1005, 1:6–10. Hong explains that after assembling modules on a card, “what really needs to be tested . . . is the connections between the modules and the card.” *Id.* at 1:11–19. Because

the “circuitry is rich in interconnections, generating tests for defective pin connections becomes an enormous task.” *Id.* at 1:22–24.

Petitioner provides a side-by-side annotated version of Hong’s Figure 3 (left) and Figure 4 (right), reproduced as follows (Pet. 70):

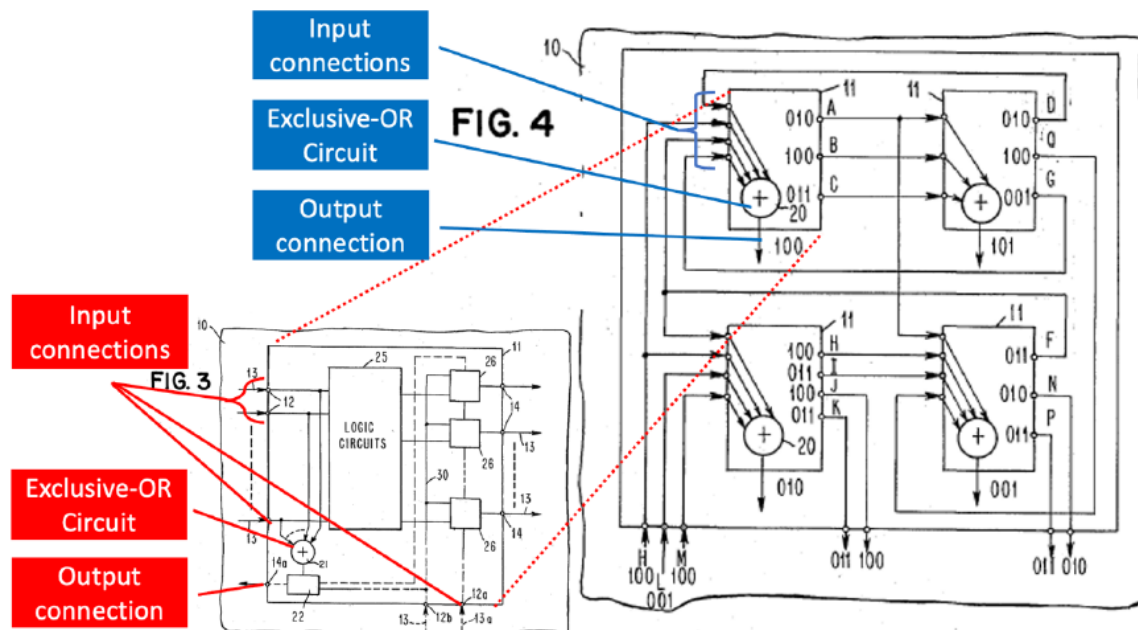


Figure 3 (left) is an expanded view showing module 11, which Figure 4 (right) shows as one of four modules 11. Hong explains that “FIG. 4 is a schematic view of a card containing the embodiment of FIG. 3 with test signals superimposed on the terminals and pins of the card.” Ex. 1005, 2:20–34.

Logic circuits 16/25 in modules 11 include input pins 12, output pins 14, conductors 13, Exclusive-OR circuit 22, Exclusive-OR tree 21, and stage 26 of a shift register. *See* Ex. 1005, 2:32–33, 3:23–33. Applying a binary 1 to each terminal 12b “connects the output lines 21 of the logic circuits to the output terminals 14 so the circuits 16 on the cards can perform

in their intended manner,” that is a “normal operation . . . when the modules are not being tested.” *Id.* at 2:53–57.⁸

On the other hand, applying a binary 0 to each terminal 12b instigates a test mode to test the interconnections. *Id.* at 2:57–58. This

ungates the connection between the output lines 21 of the original logic circuits and the terminals and instead connects all the terminals to line 26 so that test signals can be applied to the output terminals by their application to the card terminal connected to terminals 12a on all the modules. The test signals are a binary 0 followed by a binary 1. The first signal tests for any pin stuck at 1. If the card tests good, a binary 0 will appear at the card terminal connected to module terminals 14a, if not a binary 1 appears at this terminal.

Id. at 2:58–63.

2. Claim 6

Claim 6 recites “[a]n electronic circuit as recited in claim 1, wherein the test unit comprises a combinatorial circuit implementing an XOR function and connected to the I/O nodes.” Petitioner contends that Langford discloses an electronic circuit with boundary scan test circuitry as described in its showing with respect to the preamble of claim 1 and limitation 1c, and further relies on Hong to address the claimed combinatorial circuit as recited in claim 6. Pet. 69–71.

Petitioner relies on Hong’s disclosure of “circuitry . . . that permits the testing of interconnections with a very simple electrical test.” Pet. 69 (quoting Ex. 1005, 1:43–46). Petitioner explains that “[t]he interconnections

⁸ Although Hong specifically refers to Figure 1 in this passage and the following passages, Hong indicates it applies to Figures 1–4. *See id.* at 1:43–61. The embodiment of Figure 3 also “permits testing for shorts between the different interconnection networks on the card in addition to testing for simple stuck 1’s or 0’s in those networks.” *Id.* at 3:17–21.

are disposed between modules mounted on a card and tested for shorts and ‘stuck ones and zeroes.’” *Id.* (citing Ex. 1005, 1:55–65).

Petitioner further contends that Hong’s XOR inputs and outputs directly connect to input and output nodes of each module. Pet. 69. To support its showing, Petitioner quotes Hong as follows:

Each of the modules has an Exclusive-OR circuit which receives an input from each of the input pins of the module and has a single output which is taken off an output pin of the module. Also, each of the modules has a test input circuit for accessing all of the output pins of the module in parallel. The test input circuits are used to apply a binary 0 followed by a binary 1 to all the outputs of all the modules while the Exclusive-OR outputs are monitored for response to those signals.

Id. (emphasis by Petitioner) (quoting Ex. 1005, 1:46–56).

Based on these teachings and teachings in Langford, Petitioner contends that “a POSITA would have been motivated to implement *Hong’s* Exclusive-OR circuit in *Langford’s* boundary scan test circuitry to achieve an increasingly robust and decreasingly expensive form of test circuitry in terms of actual, logical, and spatial cost.” Pet. 70.

On the current record, we determine that Petitioner shows a reasonable likelihood that it would prevail with respect to its contention that claim 6 would have been obvious over the combined teachings of Langford and Hong. As noted above, at this stage of the proceeding, Patent Owner does not dispute these contentions.

IV. CONCLUSION

After considering the evidence and arguments of record, we determine that Petitioner has demonstrated a reasonable likelihood of success with respect to at least one of the challenged claims. Accordingly, an *inter partes* review of all of the claims and all of the grounds presented in the Petition is

hereby instituted. *See* 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1354, 1359–60; TPG 64.

At this stage of the proceeding, the Board has not made a final determination as to the patentability of any challenged claims or any underlying factual or legal issues. The final determination will be based on the record as developed during the *inter partes* review.

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the challenged claims of the '108 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '108 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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