

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

FUTURE LINK SYSTEMS, LLC,
Patent Owner.

IPR2021-01488
Patent 6,807,505 B2

Before KARL D. EASTHOM, KEVIN C. TROCK, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Apple Inc. (“Petitioner”) filed a Petition, Paper 1 (“Pet.” or “Petition”), to institute an *inter partes* review of claims 1, 6, and 8 (the “challenged claims”) of U.S. Patent No. 6,807,505 B2 (Ex. 1001, “the ’505 patent”). Future Link Systems, LLC (“Patent Owner”) timely filed a Preliminary Response, Paper 7 (“Prelim. Resp.”).

The Director has discretion to institute an *inter partes* review under 35 U.S.C. § 314(a) and has delegated that authority to the Board under 37 C.F.R. § 42.4(a). *See* 35 U.S.C. § 314(a) (stating “[t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition).”

Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. Real Party in Interest

Petitioner identifies itself as the only real party in interest. Pet. 55. Patent Owner also identifies itself as the only real party in interest. Paper 4, 1.

C. Related Proceedings

According to the parties, the ’505 patent is the subject of the following action: *Future Link Systems, LLC v. Apple Inc.*, No. 6:21-cv-00263 (W.D. Tex.) (the “parallel proceeding”). Pet. 55; Paper 4, 1.

D. The '505 Patent (Ex. 1001)

The '505 patent relates to an electronic circuit comprising a plurality of input/output (“I/O”) nodes for connecting the electronic circuit to a further electronic circuit via interconnects, a main unit for implementing a normal mode function of the electronic circuit, and a test unit for testing the interconnects. Ex. 1001, 1:7–12. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. *Id.* at 12–15.

Figure 1 of the '505 patent is shown below.

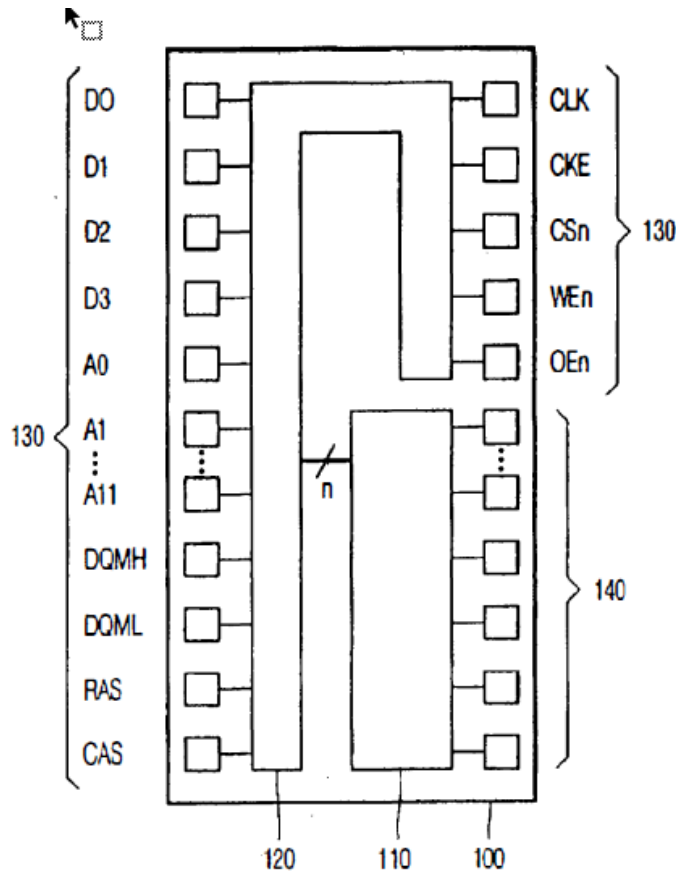


FIG. 1

Figure 1, above, illustrates electronic circuit 100. *Id.* at 5:31–32.

Circuit 100 has I/O nodes 130, 140, through which circuit 100 is connectable to external circuits. *Id.* at 5:32–34. Circuit 100 is part of an assembly, whereas interconnects between circuit 100 and further parts of the assembly are testable. *Id.* at 5:41–43. Circuit 100 further has test unit 120, which is connected to main unit 110 via n parallel connections and to I/O nodes 130. *Id.* at 5:43–46. In a normal mode of circuit 100, test unit 120 is transparent, and signals can pass freely between I/O nodes 130 and main unit 110. *Id.* at 5:46–48. In a test mode of circuit 100, main unit 110 is logically disconnected from I/O nodes 130 and test unit 120 is in control. *Id.* at 5:48–50.

Figure 2 of the '505 patent is shown below.

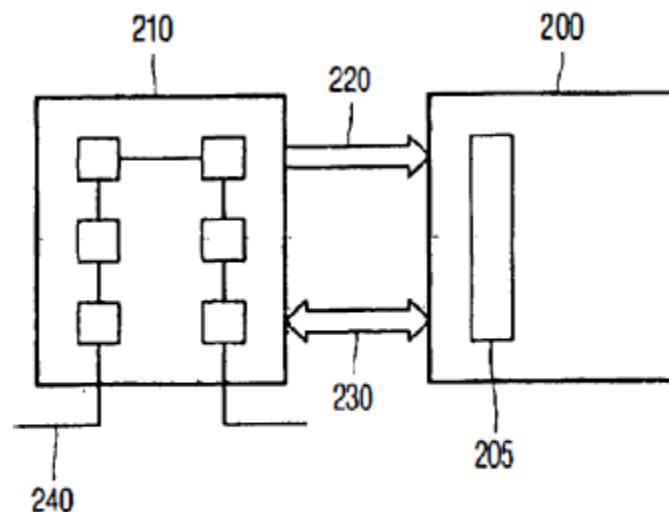


FIG. 2

Figure 2, above, illustrates a way to provide access during interconnect test to circuit 200 that is testable. *Id.* at 8:21–23. Circuit 200 includes test unit 205 that is operable as a low complexity memory. *Id.* at 8:23–24. Neighboring circuit 210, which has boundary-scan circuitry, provides data

to, and receives data from, circuit 200 via control and address bus 220 and bi-directional data bus 230. *Id.* at 8:24–27. Via boundary-scan chain 240, data is shifted to circuit 210, where the data makes up read and/or write commands to be supplied to circuit 200. *Id.* at 8:39–41. After a read command, boundary-scan chain 240 captures data supplied to data bus 230 by circuit 200. *Id.* at 8:41–43. Subsequently, the data is shifted out to be analyzed externally. *Id.* at 8:43–44.

Figure 6 of the '505 patent is shown below.

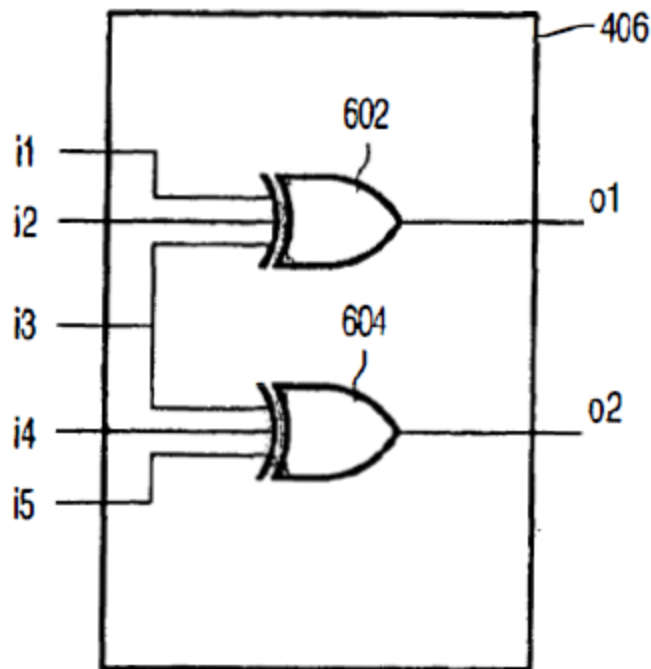


FIG. 6

Figure 6, above, schematically shows a test unit for five inputs and two outputs. *Id.* at 11:62–63. Test unit 406 has three-input XOR gate 602, which implements an exclusive-or function between output pin o1 and input pins i1, i2, and i3. *Id.* at 11:64–66. Test unit 406 further has three-input

XOR gate 604, which implements an exclusive-or function between input pins i3, i4, and i5 and output pin o2. *Id.* at 11:66–12:2.

E. Challenged Claims

Petitioner challenges claims 1, 6, and 8 of the '505 patent. Pet. 1. Claim 1 is independent.

1[P] An electronic circuit comprising:

1[a] a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,

1[b] a main unit for implementing a normal mode function of the electronic circuit,

1[c] and a test unit for testing the interconnects,

1[d] the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit,

1[e] wherein the test unit comprises at least one combinatorial circuit implementing at least one of an XNOR function and an XOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

Ex. 1001, 12:29–49 (numbering and formatting designated by Petitioner; *see* Pet. 22–41).

F. Evidence

Reference or Declaration	Date	Exhibit No.
U.S. Patent No. 4,241,307 (“Hong”)	December 23, 1980	Ex. 1006

Petitioner also relies on the declaration of David Kuan-Yu Liu, Ph.D. (Ex. 1004).

G. Asserted Ground of Unpatentability

Claims Challenged	35 U.S.C. §	Reference
1, 6, 8	103(a)	Hong

II. ANALYSIS

A. Discretionary Denial Under 35 U.S.C. § 314(a)

Patent Owner asserts that we should exercise our discretion to deny institution under 35 U.S.C. § 314(a). Prelim. Resp. 7–13 (citing *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”)); *NHK Spring Co., Ltd. v. Intri-Plex Technologies, Inc.*, IPR2018-00752, Paper No. 8 (PTAB Sept. 12, 2018) (precedential) (“*NHK*”).

35 U.S.C. § 314(a) states:

[t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

The Director has delegated the discretion to deny institution of an *inter partes* review under § 314(a) to the Board.¹ See also *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”). Under our precedent, the Board may exercise this discretion if instituting

¹ “The Board institutes the trial on behalf of the Director.” 37 C.F.R. § 42.4(a) (2021).

inter partes review would lead to “inefficient use of Board resources.” *See NHK*, Paper 8 at 20.

In *Fintiv*, the Board discussed various factors that “relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution.” *Fintiv*, Paper 11 at 6. Pursuant to *Fintiv*, the Board assesses the following factors to determine whether to exercise its discretion to deny institution:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Id.

For the reasons discussed below, we do not agree with Patent Owner that the circumstances of this case warrant the exercise of discretion to deny institution under § 314(a). In evaluating the *Fintiv* factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Fintiv*, Paper 11 at 6.

1. Stay in the Parallel Proceeding

Petitioner filed a recent order that stays the parallel proceeding and indicates the district court’s intention to transfer the case to the Northern

District of California (“NDCA” or “NDCA Court”). *See* Ex. 3001; Ex. 3002.

Accordingly, this factor weighs against exercising our discretion to deny institution.

2. The Trial Date in the Parallel Proceeding

The projected date of the Board’s final written decision in this case is early April 2023. As indicated above, Petitioner filed a recent order indicating that the parallel proceeding will be transferred to the NDCA. Ex. 3001. The transfer has not yet occurred, so the NDCA Court has not yet scheduled a trial.

Accordingly, this factor weighs against exercising our discretion to deny institution or is at most neutral.

3. Investment by the Court and the Parties in the Parallel Proceeding

Patent Owner asserts this factor favors denial of institution because the parties and the district court have invested substantial resources. Prelim. Resp. 10–11. According to Patent Owner, the district court has already begun claim construction proceedings in the parallel proceeding; the parties have completed all claim construction briefing; and the district court has scheduled a claim construction hearing for February 23, 2022. *Id.*

Petitioner asserts this factor weighs against discretionary denial because the parties have invested little in the parallel proceeding. Pet. 48. According to Petitioner, invalidity contentions were only served on September 17, 2021; no claim construction positions have been taken by either party; and little discovery has been conducted. *Id.*

Based on the current record before us, and even if the work in the parallel proceeding prior to the transfer is deemed applicable in the NDCA

after the transfer, it appears that only a minimal amount of work has been done in the parallel proceeding that might be relevant to the issues raised in the Petition with respect to the '505 Patent. For example, Patent Owner indicates that a claim construction hearing was scheduled for February 23, 2022, and Petitioner indicates that little discovery has been conducted. Moreover, the parties have not indicated specifically whether any of the issues to be addressed by the district court in a claim construction hearing would bear on the challenged claims of the '505 Patent or the asserted ground in this Petition.

Petitioner also asserts that it timely filed the Petition in this case, “approximately six months before the filing deadline.” *Id.* Patent Owner does not address the timeliness of the Petition. The record indicates that the complaint in the parallel proceeding was filed on March 16, 2021, preliminary infringement contentions were due to be served on July 8, 2021, preliminary invalidity contentions were due to be served on September 16, 2021, and the Petition was filed on September 28, 2021. *See* Ex. 2001, 2. Based on this record, the Petition was filed approximately six months after the filing of the complaint in the parallel proceeding and approximately two months after preliminary infringement contentions were served. Petitioner’s diligence in filing the Petition factors holistically with the minimal investment in the parallel proceeding discussed above.

Accordingly, this factor weighs against exercising our discretion to deny institution.

4. Overlap of the Issues

Patent Owner asserts this factor favors denial of institution because the overlap between the issues raised in the Petition and the parallel proceeding is essentially complete, as evidenced by the fact that the Petition

presents grounds based on the Hong prior art reference, and Petitioner indicates its intention to rely on this reference as invalidating art in the district court. Prelim. Resp. 11–12 (citing Ex. 2002).

Petitioner asserts this factor weighs against discretionary denial because Petitioner stipulates that, if this proceeding is instituted, Petitioner will not pursue invalidity grounds in the parallel district court proceeding that rely on Hong. Pet. 48–49.

Affirmative stipulations, such as Petitioner’s here, mitigate to some degree concerns of duplicative efforts between the Board and the parallel proceeding with respect to the challenges raised in the Petition. *See Sand Revolution II, LLC v. Cont’l Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24 at 11–12 (June 16, 2020) (informative). Therefore, given the potential overlap here, but taking into account Petitioner’s stipulation, we find this factor weighs slightly against exercising discretionary denial.

5. *Whether Petitioner is Unrelated to the Defendant in the Parallel Proceeding*

Patent Owner asserts there is no dispute that the parties to the Petition are the same as the parties to the parallel district court proceeding. Prelim. Resp. 12.

Petitioner agrees that the parties are the same in the parallel district court proceeding, but indicated that “members of the Board have noted that *Fintiv* addresses only the scenario in which the petitioner is unrelated to a defendant in a parallel proceeding.” Pet. 49.

Because of the recent stay issued in the parallel proceeding and the pending transfer of the parallel proceeding to the NDCA, it is not clear whether the trial in the parallel proceeding will precede the deadline for a

final written decision in this case. Accordingly, this factor weighs against exercising our discretion to deny institution or is at most neutral.

6. *Other Considerations*

Patent Owner asserts this factor favors denial of institution as the Petition substantively lacks merit in its failure to present evidence or argument sufficient to warrant institution. Prelim. Resp. 12.

Petitioner asserts this factor weighs strongly in favor of institution based on the strength of the proposed grounds. Pet. 49–50.

Based on the current record, we consider the merits to be particularly strong. For example, as discussed below with respect to independent claim 1, Petitioner provides persuasive evidence that the recited limitations of independent claim 1 are taught by Hong and would have been obvious to one of ordinary skill in the art. Instituting *inter partes* review under these circumstances would “serve the interest of overall system efficiency and integrity because it allows the proceeding to continue in the event that the parallel proceeding settles or fails to resolve the patentability question presented.” *Fintiv*, Paper 11 at 15.

Given the particularly strong merits based on the current record, we determine this factor weighs against exercising discretionary denial.

7. *Fintiv Framework*

Apart from contending that the *Fintiv* factors favor institution, Petitioner additionally asserts that the *Fintiv* framework should be overturned because the framework (1) exceeds the Director’s authority; (2) is arbitrary and capricious; and (3) was adopted without notice-and-comment rulemaking. Pet. 50–53.

Given our determination below that the *Fintiv* factors weigh against exercising discretion to deny institution, we decline to consider Petitioner’s direct challenges to the *Fintiv* framework.

8. *Conclusion*

We consider “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. In our view, the facts weighing against exercising discretion to deny institution collectively outweigh those favoring exercising discretion to deny institution. For these reasons, we decline to exercise our discretion under 35 U.S.C. § 314(a) to deny *inter partes* review.

B. *Level of Ordinary Skill in the Art*

Petitioner describes a person of ordinary skill in the art as a person having “at least a bachelor’s degree in electrical engineering or equivalent with at least one year of experience in the field of circuit design or circuit testing.” Pet. 10 (citing Ex. 1004 ¶¶ 30–32).

Patent Owner does not contest Petitioner’s description of a person of ordinary skill in the art. *See generally* Prelim. Resp.

Petitioner’s description of a person of ordinary skill appears to be consistent with the subject matter of the ’505 patent. This is supported by the testimony of Petitioner’s declarant, Dr. Liu. *See* Ex. 1004 ¶¶ 30–32. We adopt Petitioner’s assessment of a person of ordinary skill for purposes of this Decision, with the exception of the qualifier “at least,” to keep the description from being vague and extending to a level reflecting that of an expert. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

C. Claim Construction

For petitions filed on or after November 13, 2018, a claim shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100 (2019). The Petition was accorded a filing date of September 28, 2021. Paper 4. Thus, we apply the claim construction standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

Under *Phillips*, claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and even extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (in the context of an *inter partes* review, applying *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner proposes that the Board adopt the construction that Patent Owner previously advanced in the parallel district court proceeding and construe “testing the interconnects” as “applying test data to one end of an interconnect and observing response data at the other end.” Pet. 13.

Patent Owner responds by asserting that Petitioner fails to apply its own claim construction and arguing that “Petitioner’s failure to apply its own proffered claim construction is an additional, independent reason to deny institution of the Petition.” Prelim. Resp. 6–7. Patent Owner, however, does not cite to any authority to support its position.

For purposes of this Decision, we determine that no claim terms require express construction. *See Vivid Techs.*, 200 F.3d at 803.

D. Patentability Challenge

Petitioner presents a single ground challenging the patentability of claims 1, 6, and 8 of the ’505 patent under 35 U.S.C. § 103 as being obvious over Hong in view of the knowledge of a person of ordinary skill in the art. Pet. 11.

1. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

The Supreme Court has made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have

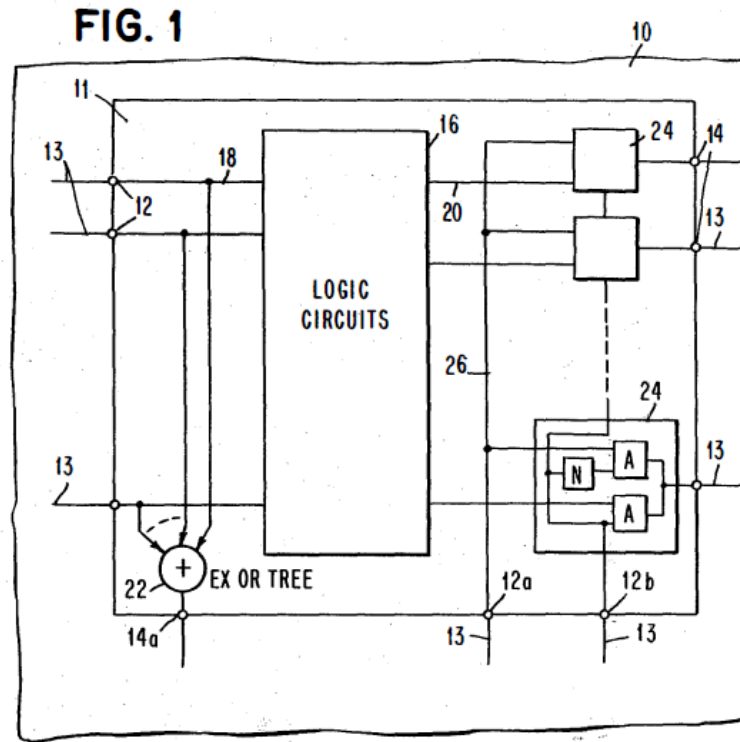
been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. Reaching this conclusion, however, requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention. *Id.*

2. *Hong (Ex. 1006)*

Hong is a U.S. Patent that issued on December 23, 1980, more than one year before the earliest priority date of the '505 patent. Ex. 1006, code (45). Petitioner asserts that Hong is prior art under pre-AIA 35 U.S.C. § 102(a), (b), and (e). Pet. 14.

Hong relates to the testing of connections between modules mounted on cards and to circuitry in the modules to provide simple testing of such connections. Ex. 1006, 1:6–9. In Hong, each of the modules has an exclusive-OR circuit that receives an input from each of the input pins of the module and has a single output that is taken off an output pin of the module. *Id.* at 1:46–49. Each of the modules also has a test input circuit for accessing all of the output pins of the module in parallel. *Id.* at 1:49–51. The test input circuits are used to apply a binary 0 followed by a binary 1 to all the outputs of all the modules while the exclusive-OR outputs are monitored for response to those signals. *Id.* at 1:51–55. Doing this checks the connections between the modules and between the modules and the card terminals for stuck ones and zeros. *Id.* at 1:55–57.

Hong Figure 1 is reproduced below.



Hong's Figure 1, shown above, is a schematic view of a portion of a card that permits testing of the module pin to card wiring connections without probing the cards or modules. *Id.* at 2:7–10. Each of modules 11 are mounted on card 10 and contain a plurality of input pins 12 and output pins 14. *Id.* at 2:25–27. Pins 12 and 14 are connected by conductors 13 on card 10 to output and input pins of other modules on the card and to input and output terminals of the card. *Id.* at 2:27–30.

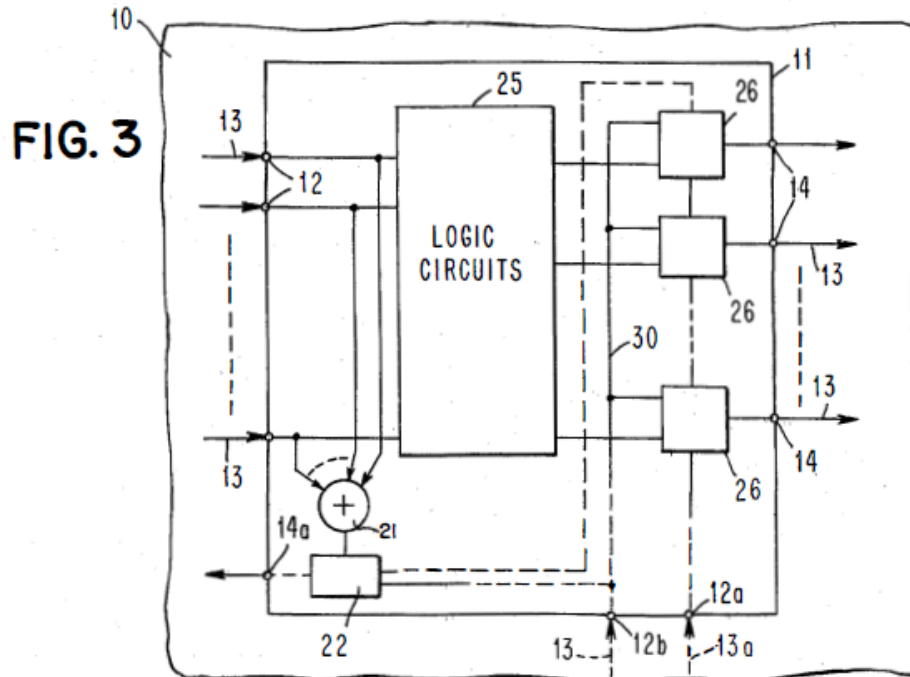
Circuits 16 on each of the modules are connected to input pins 12 by input lines 18 and output pins 14 by output lines 21. *Id.* at 2:31–33. Additional circuits are provided on each of the modules. *Id.* at 2:33–34. These include exclusive-OR tree 22 that receives input from each of input pins 12 and has a single output which is taken off the module on pin 14a. *Id.* at 2:34–37. Each output line 21 is connected through half-select circuit 24

to output pins 14 of the module. *Id.* at 2:37–39. Half-select circuits have two inputs: one from one of output lines 21; the other from line 26 connected to input pin 12a. *Id.* at 2:40–42. Outputs of select circuits each go to one of output pins 14 while the control terminals for each of the circuits is connected to input pin 12b. *Id.* at 2:42–45.

When the circuits are to be tested, a binary 0 is applied to terminals 12b on all the modules. *Id.* at 2:56–57. This “ungates” the connection between output lines 21 of the original logic circuits and the terminals, and, in its place, connects all terminals to line 26 so that test signals can be applied to the terminals by their application to the card terminal connected to terminals 12a on all the modules. *Id.* at 2:57–63. The test signals are a binary 0 followed by a binary 1. *Id.* at 2:63–64.

The first signal tests for any pin stuck at 1. *Id.* at 2:64–65. If the card tests good, a binary 0 will appear at the card terminal connected to module terminals 14a, if not a binary 1 appears at this terminal. *Id.* at 2:65–67. The second signal tests for any pin stuck at binary 0. *Id.* at 3:1. For a good card, a binary 1 will appear in response to the test, while a bad card will produce a binary 0 in response thereto. *Id.* at 3:2–4. This gives an indication as to where a bad connection occurred. *Id.* at 3:4–5.

Hong Figure 3 is reproduced below.

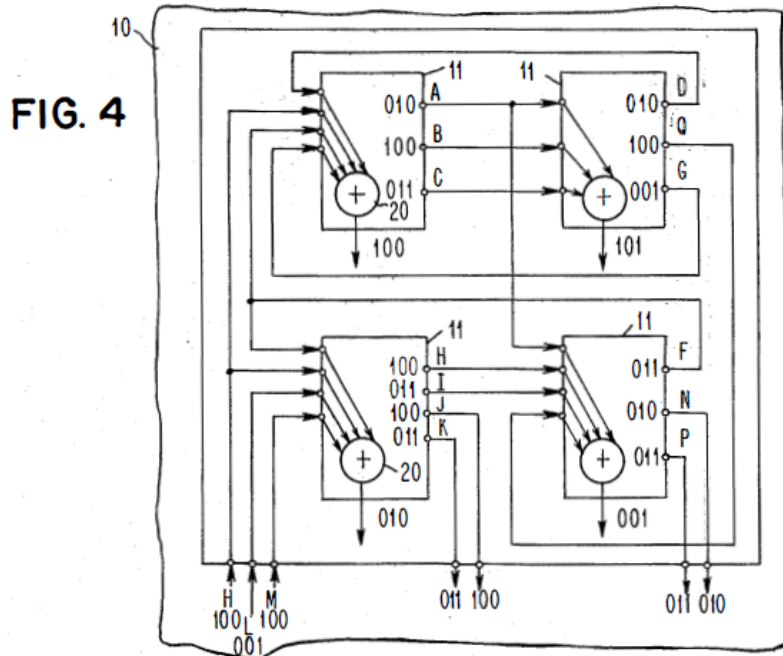


Hong's Figure 3, shown above, is a schematic view of a portion of a card that permits the testing of interconnection nets on the cards along with the connections between the module pins and the card wiring. *Id.* at 2:15–19. As shown in Figure 3, each module includes exclusive-OR circuit 22 with an input coupled to each of the module input pins 12 and an output connected to a stage 22 in a shift register. *Id.* at 3:22–25. In addition, output pins 14 are each connected to stage 26 of the same shift register. *Id.* at 3:26–27. Data is loaded into the first stage of this shift register at input terminal 12a, stepped through all stages of the shift register with clock signals, and removed from the last stage of the shift register at output terminal 14a. *Id.* at 3:27–31. Data also enters all shift register stages in parallel from logic circuit 25 and from the output of exclusive-OR tree 31. *Id.* at 3:31–34.

The circuitry illustrated in Figure 3 is used to check the interconnections on the card for shorts between the nets based on the number of separate interconnecting nets on the card. *Id.* at 3:57–60. The number of

nets on the card is equal to the number of source pins for the nets that include all the module output pins and the card primary input pins. *Id.* at 3:61–63.

Hong Figure 4 is reproduced below.



Hong's Figure 4, shown above, is a schematic view of a card containing the embodiment illustrated in Figure 3 with test signals superimposed on the terminals and pins of the card. *Id.* at 2:20–22. The card shown in Figure 4 has three input terminals and a total of 13 output pins on the modules of the card for a total of 16 nets on the card. *Id.* at 5:7–9.

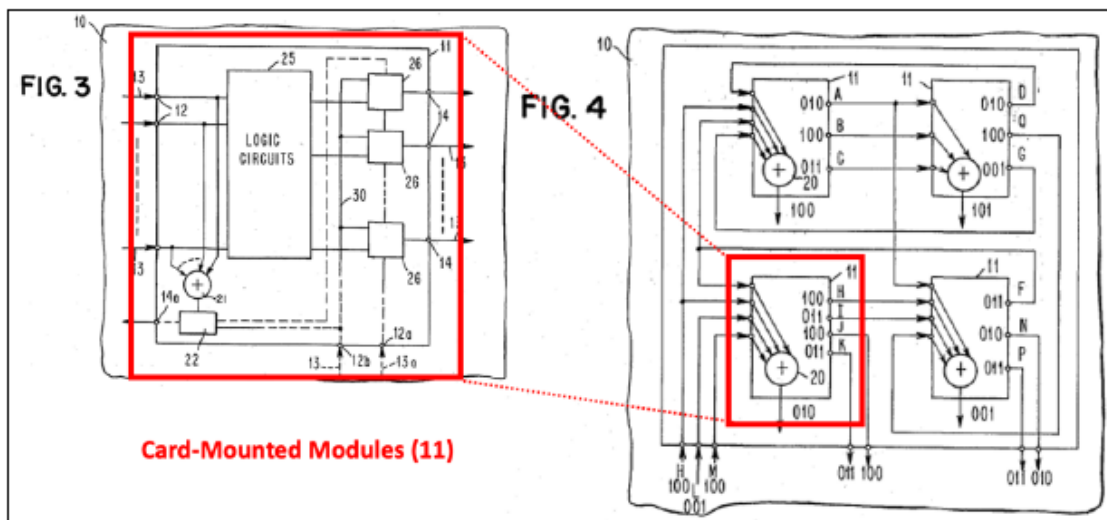
E. Obviousness Based on Hong

As noted above, Petitioner asserts claims 1, 6, and 8 are unpatentable as obvious under 35 U.S.C. § 103 over Hong, in view of the knowledge of a person of ordinary skill in the art. Pet. 14–44.

1. Independent Claim 1

a) 1[P] An electronic circuit comprising:

For the preamble, Petitioner relies on Hong's description of "testing . . . interconnections between **modules** mounted on a card." Pet. 22 (quoting Ex. 1006, Abstr. (emphasis added by Petitioner). Petitioner points out that Hong's "Figure 3 shows 'connections between . . . module pins and the card wiring' while Figure 4 shows 'a card containing the embodiment of Fig. 3 with test signals superimposed on the terminals and pins of the card.'" Pet. 22–23 (citing Ex. 1006, 2:15–34, Figs. 3, 4). Petitioner argues that a person of ordinary skill in the art "would have recognized each of *Hong's* modules as an electronic circuit." Pet. 23 (citing Ex. 1004 ¶ 48). Hong's Figures 3 and 4 are shown below, annotated by Petitioner in red. *Id.*



Hong's Figures 3 and 4, annotated in red shown above, are schematic diagrams showing the relationship between module 11 with input pins 12 and output pins 14 shown on a portion of card 10 in Figure 3 and modules 11 shown on card 10 in Figure 4. Ex. 1006, 2:15–30, 3:22–34.

Dr. Liu testifies that "*Hong* refers to these modules as circuits when disclosing 'what really needs to be tested after the assembly of the **circuits**

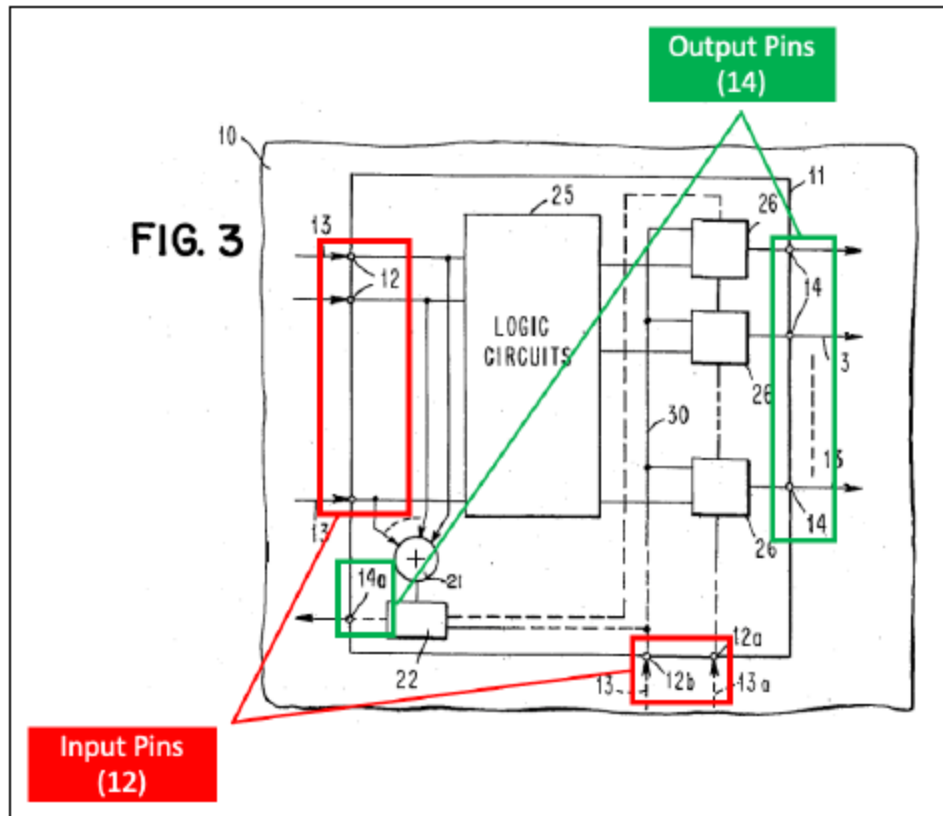
on the cards is [sic] the connections between the **modules and the cards.**” Ex. 1004 ¶ 48 (citing Ex. 1006, 1:16-19 (emphases and alteration added by declarant)). “Accordingly,” Dr. Liu testifies, a person of ordinary skill in the art “would have recognized *Hong* refers to modules and circuits interchangeably and would have therefore considered *Hong*’s modules to be electronic circuits.” Ex. 1004 ¶ 48.

Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to this limitation. *See* Prelim. Resp. 3–7.

Based on the record before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong meets the preamble of independent claim 1.

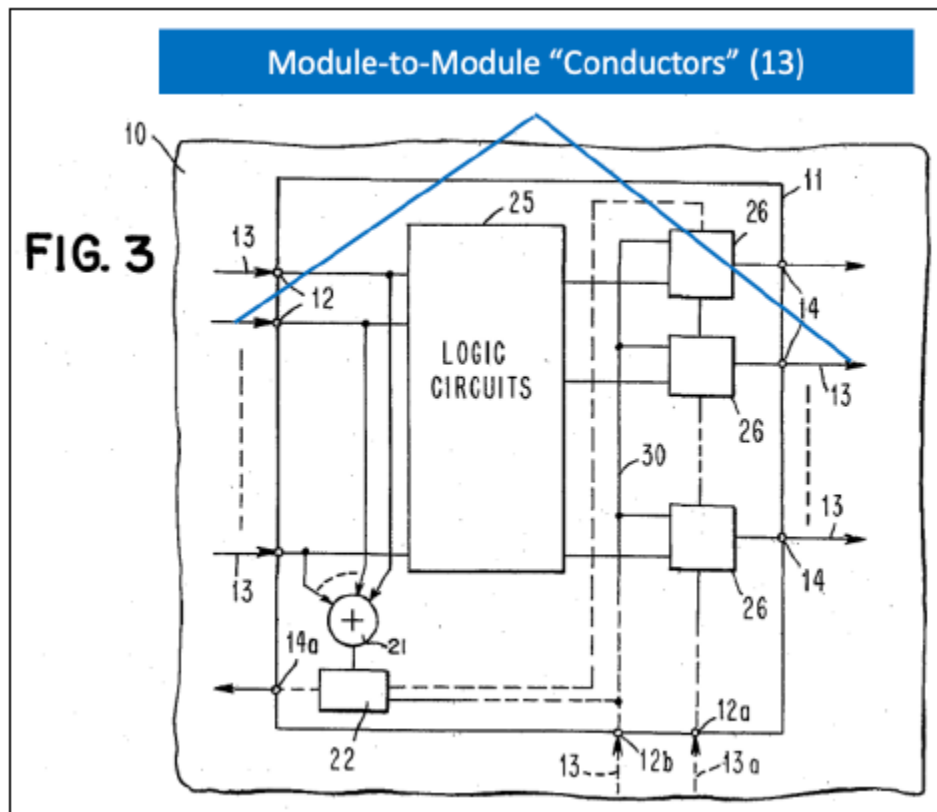
- b) *1[a] a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects,*

For this limitation, Petitioner relies on Hong’s description of “testing . . . interconnections between modules mounted on a card . . . for stuck ones and zeros.” Pet. 23 (quoting Ex. 1006, Abstr.). Petitioner points to Hong’s description that each module has a “plurality of both input pins 12 and output pins 14.” Pet. 23–24 (quoting Ex. 1006, 2:25–27). Petitioner asserts that Hong’s Figure 3 “illustrates this arrangement with respect to *Hong*’s more complex embodiment,” and provides an annotated version of Hong’s Figure 3, shown below. Pet. 24.



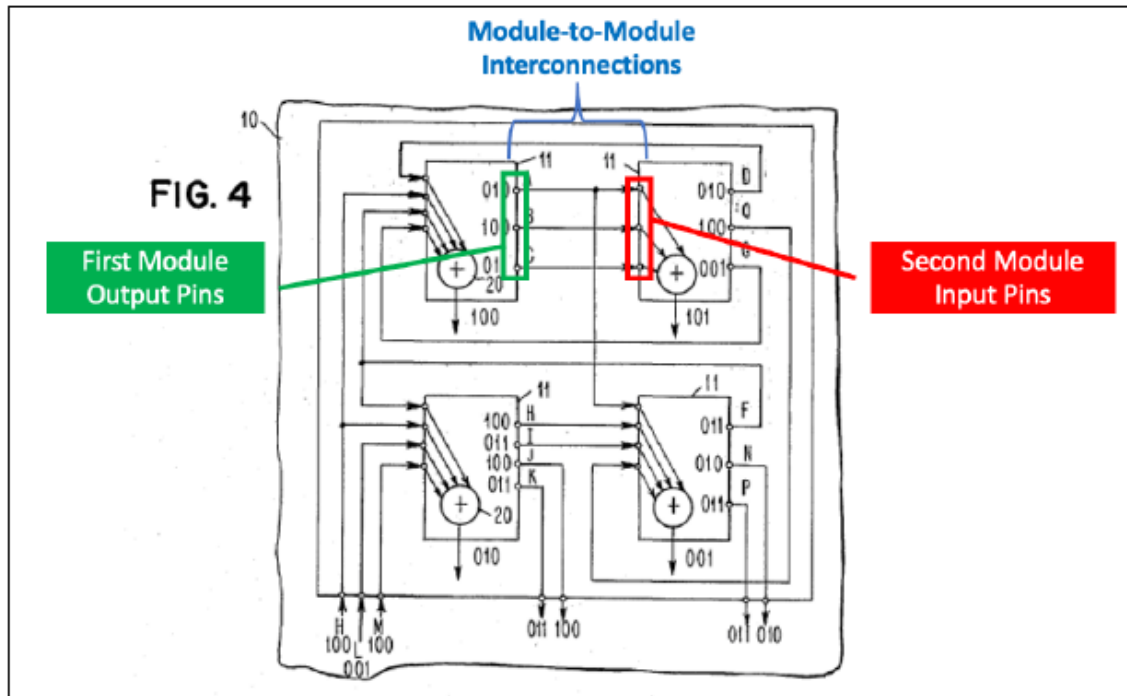
Hong's Figure 3, annotated by Petitioner, shown above, identifies input pins 12 (in red) and output pins 14 (in green). Pet. 24. Petitioner asserts that Hong's "input and output pins 'are **connected by conductors** . . . on the card . . . to output and input pins of other modules on the card.'" *Id.* at 25 (quoting Ex. 1006, 2:27–30 (emphasis added by Petitioner)).

To further explain its position, Petitioner provides an annotated version of Hong's Figure 3, shown below.



Hong's Figure 3, above, is annotated in blue by Petitioner to show Hong's module-to-module conductors 13. Pet. 25. Petitioner argues that "[t]he conductors 13 are used to 'permit[] the testing of interconnection nets on the cards.'" *Id.* (quoting Ex. 1006, 2:15–19). Petitioner asserts that "Figure 4 'contain[s] the embodiment of Fig. 3' and depicts this module-to-module interconnection testing." *Id.* at 25–26 (quoting Ex. 1006, 2:20–22).

Petitioner additionally provides an annotated version of Hong's Figure 4, shown below.



Petitioner’s annotated version of Hong’s Figure 4, shown above, depicts Hong’s first module output pins (in green), second module input pins (in red), and module-to-module interconnections (in blue). Pet. 26.

Dr. Liu testifies that a person of ordinary skill in the art “would have recognized the conductors as interconnections because *Hong* refers to the conductors as connections, and because Figure 4 is a ‘schematic view of a card containing the embodiment of Fig. 3 with test signals superimposed on the . . . pins of the card’ showing the conductors depicted in Figure 3 interconnecting the modules of Figure 4.” Ex. 1004 ¶ 51 (quoting Ex. 1006, 2:20–22).

Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to this limitation. See Prelim. Resp. 3–7.

Based on the record before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong teaches the recited

“plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects” of limitation 1[a].

c) *1[b] a main unit for implementing a normal mode function of the electronic circuit,*

For this limitation, Petitioner directs us to Hong’s description of “a main unit in terms of ‘logic circuits on each of the modules mounted on the card.’” Pet. 27 (citing 1006, 1:24–29 (emphasis omitted)). Petitioner first points to Hong’s Figure 1, identifying Hong’s “logic circuits 16” as the recited “main unit.” *Id.* (citing Ex. 1006, 2:32–35). Petitioner also identifies Hong’s logic circuits 25 in Figure 3 as the same type of logic circuitry in Hong’s second embodiment. *Id.* at 27–28 (citing Ex. 1006, 3:31–34). Petitioner argues that a person of ordinary skill in the art “would have recognized *Hong’s* second embodiment uses the same logic circuitry functionality described in the first embodiment. *Id.* at 29 (citing Ex. 1004 ¶¶ 52–53).

Dr. Liu’s testimony supports Petitioner’s identification of Hong’s logic circuits as the recited “main unit,” explaining that Hong “describes a ‘normal operation’ of the module that ‘connects . . . the logic circuits to the output terminals . . . so the [logic] circuits 16 on the cards **can perform in their intended manner.**’” Ex. 1004 ¶ 53 (quoting Ex. 1006, 2:52–57 (emphasis and alteration added by declarant)).

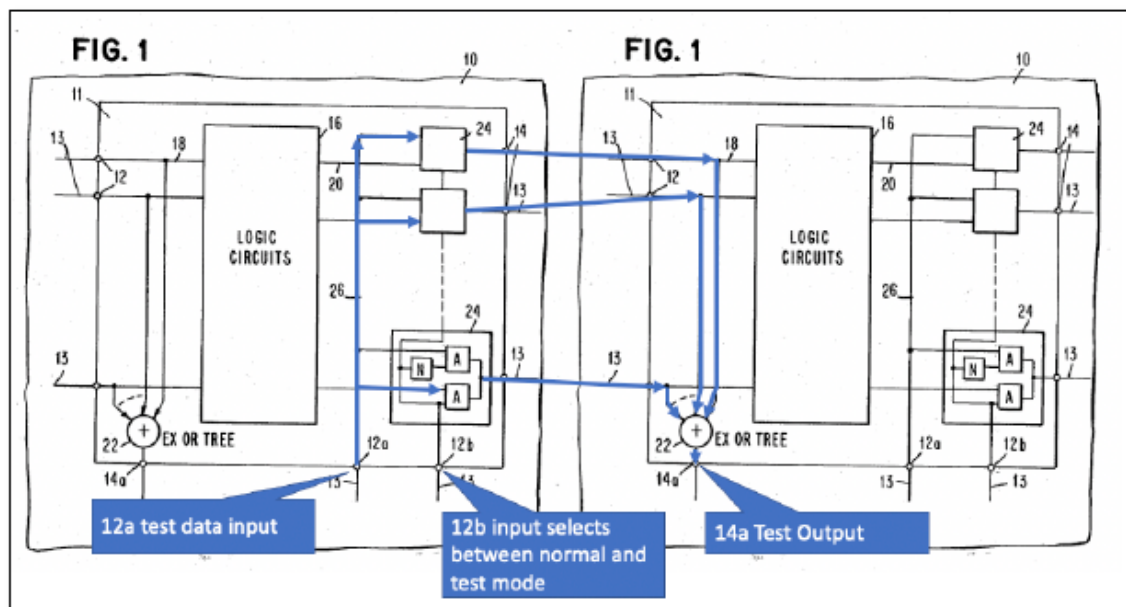
Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to this limitation. *See* Prelim. Resp. 3–7.

Based on the record before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong teaches the recited “*main unit for implementing a normal mode function of the electronic circuit*” of limitation 1[b].

d) *I[c] a test unit for testing the interconnects,*

For this limitation, Petitioner argues that the simple embodiment in Hong's Figure 1 "teaches a test unit comprising XOR gates and half-select circuits 24 that allow logically disconnecting the main unit from the I/O nodes and shifting test data in such that input pins 12 and output pins 14 (interconnects) can be tested to ensure no pin is stuck at a binary 1 or binary 0." Pet. 30 (citing Ex. 1006, 2:52–63; Ex. 1004 ¶¶ 54–56).

Petitioner points out that in Hong, multiple modules are placed on a single card such that the outputs of a first module are connected as the input to an adjacent module. Pet. 30–31 (citing Ex. 1006, Fig. 4, 2:47–50). Hong's Figure 1, annotated by Petitioner, is shown below.



Petitioner explains that "[t]o best illustrate the signal flow in test mode, two modules (from [Hong's Figure] 1) are placed side-by-side [above] and the signal flow during test mode is depicted" in blue. Pet. 31. Petitioner explains that in Hong's annotated Figure 1, above, "a test mode signal flow [is shown in blue] in which test data input through node 12a becomes the input to half-select circuits 24, the half-select circuits 24 output through

output pins 14, which become inputs to input pins 12 in the adjacent module, and where each such input flows through XOR gate 22, producing the test output on output node 14a.” *Id.*

Petitioner also argues that “*Hong*’s more complex second embodiment describes a two-component test unit comprising an (i) Exclusive-OR circuit and (ii) shift register for testing interconnects.” Pet. 32 (citing Ex. 1006, 3:22–26). Petitioner explains that “[w]orking together, the test input circuit, *i.e.*, shift register, and Exclusive-OR circuit configuration enable a ‘whole series of bits’ to be ‘loaded into each of the stages . . . [and] the response of the Exclusive-OR tree 22 can be taken off the module.’” *Id.* at 33 (quoting Ex. 1006, 3:35–49).

Dr. Liu supports Petitioner’s positions by testifying that a person of ordinary skill in the art “would have recognized *Hong*’s ‘simple’ and ‘complex’ embodiments create several testing configurations that detect enumerated faults by uniformly placing a module into test mode, communicating binary (0, 1) test signals across input pins and interconnections, and evaluating the binary (0, 1) response to that test at a module output pin.” Ex. 1004 ¶ 54.

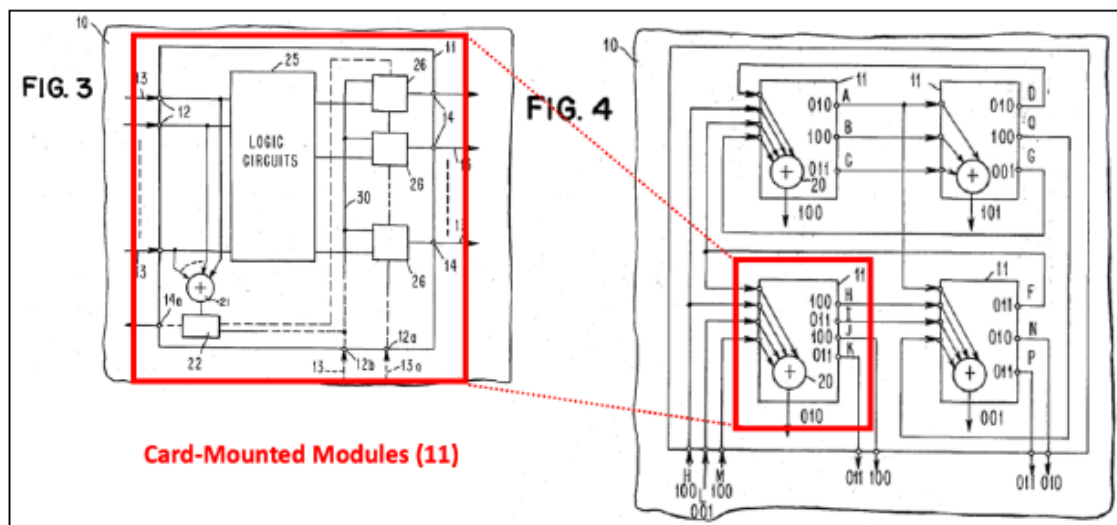
Patent Owner argues that:

[i]n discussing the preamble, Petitioner highlights what it contends to be the “electronic circuit” in the *Hong* reference corresponding to the electronic circuit of the challenged claims. Petitioner draws a red box around this alleged electronic circuit at page 23 of the Petition. In connection with claim element 1c (the test unit), however, Petitioner draws from not only the previously-identified electronic circuit, but from a separate, adjacent electronic circuit. Petitioner creates a new figure (never shown in the *Hong* reference) at page 31 of the Petition in which the alleged “electronic circuit” of *Hong* is replicated, adjacent to the previously identified electronic circuit. Petitioner appears to

suggest that the “test unit” spans not just the electronic circuit identified in connection with the preamble, but also another, separate electronic circuit. However, the test unit of the challenged claims is part of the same electronic circuit as the other components, not part of a further electronic circuit as Petitioner seems to argue.

Prelim. Resp. 4. In other words, Patent Owner argues that Petitioner is not mapping the identified “electronic circuit” in Hong to the claim limitations consistently.

The figure referred to by Patent Owner found on page 23 of the Petition is shown below.



The figure, shown above, depicts Hong’s Figures 3 and 4, annotated by Petitioner in red. Hong’s Figure 3, shown on the left, is a schematic diagram of a portion of card 10 with a single module 11 outlined by a red box along with the words “Card-Mounted Modules (11)” added in red by Petitioner. *See* Pet. 23. Hong’s Figure 4, shown on the right, is a schematic diagram of card 10 with four modules 11, one of which is also outlined by a red box added by Petitioner. *Id.* Connecting the two red boxes are two red

dotted lines indicating a relationship between module 11 shown on the left in Figure 3 and one of the modules 11 shown on the right in Figure 4. *Id.*

With respect to these annotated figures, Petitioner states the following: “[d]epicted [above], Figure 3 shows ‘connections between . . . module pins and the card wiring’ while Figure 4 shows ‘a card containing the embodiment of Fig. 3 with test signals superimposed on the terminals and pins of the card.’” Pet. 22–23 (quoting Ex. 1006, 2:15–34). Petitioner then argues that a person of ordinary skill in the art “would have recognized each of *Hong*’s modules as an electronic circuit.” Pet. 23 (citing Ex. 1004 ¶ 48).

Petitioner does not state, as Patent Owner alludes (Prelim. Resp. X), that it is mapping the recited “electronic circuit” of the preamble to a single module 11 of *Hong*. Indeed, with respect to the preamble, Petitioner states with emphasis, that “*Hong* discloses ‘testing . . . interconnections between **modules** mounted on a card.’” Pet. 22 (quoting Ex. 1006, Abstr. (emphasis added by Petitioner)).

With respect to the figure referred to by Patent Owner from page 31 of the Petition (shown above), Petitioner explains that “[t]o best illustrate the signal flow in [*Hong*’s] test mode, two modules (from [*Hong*’s] Fig. 1) are placed side-by-side [above] and the signal flow during test mode is depicted” in blue. Pet. 31. Petitioner also explains that “[a]s illustrated in [*Hong*’s] Fig. 4, multiple modules are placed on a single card such that the outputs of a first module are connected as the input to an adjacent module.” *Id.* at 30–31 (citing Ex. 1006, Fig. 4, 2:47–50 (noting the invention requires multiple modules on a single card)). Dr. Liu further testifies that a person of ordinary skill in the art “would have recognized *Hong* refers to modules and

circuits interchangeably and would have therefore considered *Hong's* modules to be electronic circuits.” Ex. 1004 ¶ 48.

Based on this preliminary record, we do not agree with Patent Owner that Petitioner is mapping the identified “electronic circuit” in Hong to the claim limitations inconsistently as Patent Owner argues.

On the record currently before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong teaches the recited “*test unit for testing the interconnects*” of limitation 1[c].

- e) *1[d] the electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit,*

For this limitation, Petitioner points out that Hong’s “modules operate in either (1) a normal mode with the input and output pins connected to the logic circuits or (2) a test mode with the input and output pins connected to the Exclusive-OR circuits.” Pet. 34–35 (citing Ex. 1006, 2:52–64).

Petitioner argues that a person of ordinary skill in the art “would have recognized *Hong's* more complex second embodiment uses the same normal and test mode connections as the first embodiment.” *Id.* at 35 (citing Ex. 1004 ¶¶ 59–60). Dr. Liu’s testimony supports this position. *See* Ex. 1004 ¶¶ 59–60.

Patent Owner does not respond substantively to Petitioner’s evidence and arguments with respect to this limitation. *See* Prelim. Resp. 3–7.

Based on the record before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong teaches the recited “*electronic circuit having a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit*” of limitation 1[d].

- f) I[e] wherein the test unit comprises at least one combinatorial circuit implementing at least one of an XNOR function and an XOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.*

For this limitation, Petitioner explains that “each of *Hong*’s modules in the first [simple] embodiment include input pins 12 that feed test data into an XOR gate 22, which outputs the result through output pin 14a.” Pet. 38. Petitioner explains that “test data input through node 12a becomes the input to half-select circuits 24, the half-select circuits 24 output through output pins 14, which become inputs to input pins 12 in the adjacent module, and where each such input flows through XOR gate 22, producing the test output on output node 14a.” *Id.* at 39 (citing Ex. 1006, 2:32–45 (describing circuit elements), 2:57–68 (describing test signal flow)).

In the second (complex) embodiment, Petitioner explains that “*Hong*’s Exclusive-OR circuit has “an input **coupled to each of the module input pins 12** and [an] **output** connected to a stage 22 in a shift register.” Pet. 39 (citing Ex. 1006, 3:22–35 (emphases added by Petitioner). Petitioner explains that “[t]he ‘response of [the] Exclusive-OR tree captured in stage 22’ is ‘read . . . out of terminal 14a.’” Pet. 39–40 (quoting Ex. 1006, 3:38–45).

Dr. Liu testifies that

[w]hile *Hong* describes the Exclusive-OR component in both of these embodiments as “Exclusive-OR circuits,” an “Exclusive-OR tree,” and an “Exclusive-OR gate” at Abstract, 2:33-37, and 4:18-20, *Hong* does not expressly describe it using an “XOR” designation. However, a POSITA would have easily recognized the “Exclusive-OR” components *Hong* describes above as an

“XOR” circuit because the ’505 Patent explicitly describes a **“three-input XOR gate . . . which implements the required Exclusive-OR function.**

Ex. 1004 ¶ 61 (citing Ex. 1001, 11:64–66 (emphases added by declarant).

Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to this limitation. *See* Prelim. Resp. 3–7.

Based on the record before us, we are persuaded that Petitioner has shown sufficiently for purposes of institution that Hong teaches limitation 1[e].

g) Conclusion on Independent Claim 1

Based on the current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to independent claim 1 under 35 U.S.C. § 103(a) as obvious over Hong.

2. Dependent Claims 6 and 8

Petitioner argues that Hong teaches the recited limitations of dependent claims 6 and 8. *See* Pet. 41–44. Dr. Liu provides testimony supporting Petitioner’s position with respect to independent claim 1 and dependent claim 8. *See* Ex. 1004 ¶¶ 48–63.

Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to dependent claims 6 and 8. *See* Prelim. Resp. 3–7.

We have considered the evidence and arguments presented in the Petition and the Preliminary Response, as well as the testimony of Petitioner’s declarant, Dr. Liu. Based on the current record before us, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that Hong meets the recited limitations of dependent claims 6 and 8.

III. CONCLUSION

For the foregoing reasons, we are persuaded that the Petition demonstrates a reasonable likelihood of prevailing in showing the unpatentability of at least one of the challenged claims of the '505 patent.

IV. ORDER

Accordingly, it is

ORDERED that an *inter partes* review is instituted as to all challenged claims on the ground raised in the Petition; and

FURTHER ORDERED that *inter partes* review is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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