

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

LED WAFER SOLUTIONS, LLC,
Patent Owner.

IPR2021-01491
Patent 8,952,405 B2

Before LYNNE E. PETTIGREW, JEFFREY W. ABRAHAM, and
TERRENCE W. McMILLIN, *Administrative Patent Judges*.

McMILLIN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Samsung Electronics Co., Ltd. (“Petitioner”)¹ filed a Petition to institute an *inter partes* review of claims 1–17 of U.S. Patent No. 8,952,405 B2 (Ex. 1001, “the ’405 patent”) pursuant to 35 U.S.C. § 311 *et seq.* Paper 1 (“Petition” or “Pet.”). LED Wafer Solutions, LLC (“Patent Owner”)² filed a Preliminary Response. Paper 6 (“Preliminary Response” or “Prelim. Resp.”). With our authorization, Petitioner filed a Reply to the Preliminary Response (Paper 7 (“Reply”)) and Patent Owner filed a Sur-reply (Paper 8 (“Sur-reply”)).

We have authority under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). After considering the Petition, the Preliminary Response, the Reply, the Sur-Reply and the evidence of record, we do not institute an *inter partes* review as to the challenged claims of the ’405 patent on the grounds of unpatentability presented.

B. *Related Proceedings*

The parties identify *LED Wafer Solutions LLC v. Samsung Electronics Co.*, No. 6:21-cv-292 (W.D. Tex.) as a related matter. Pet. 1; Paper 4, 1.

¹ Petitioner identifies Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. as real-parties-in interest in this proceeding. Pet. 1.

² Patent Owner identifies LED Wafer Solutions, LLC as the real party-in-interest to this proceeding. Paper 4, 1.

Patent Owner also identifies IPR2021-01479 as a related matter. Paper 4, 12. In IPR2021-01479, claims 1–4, 6, 8–14, and 16 of the '405 patent are challenged as unpatentable. IPR2021-01479, Paper 1, 2. Patent Owner further identifies the following related matters in which additional patents owned by Patent Owner are challenged: IPR2021-01504, IPR2021-01506, IPR2021-01516, IPR2021-01526, and IPR2021-01554. Paper 4, 1–2.

C. The '405 Patent

The '405 patent is titled “Light Emitting Diode Package and Method of Manufacture.” Ex. 1001, code (54). The '405 patent explains that “output energy or light is determined by the materials and operating conditions of the LED, including the energy band gap of the LED material and the electrical biasing of the LED” but that “conventional LED devices can be relatively costly to manufacture by some metrics when compared to other light sources” due to their exacting package requirements. *Id.* at 1:28–31, 45–54. The '405 patent provides a light emitting diode (LED) device and packaging for the same in which “the LED is manufactured by epitaxial growth or other chemical or physical deposition techniques of a plurality of layers” and has certain layers which “act to promote mechanical, electrical, thermal, or optical characteristics of the device.” *Id.* at 1:66–2:8. According to the '405 patent, its device “avoids design problems, including manufacturing complexities, costs and heat dissipation problems found in conventional LED devices.” *Id.* at 2:8–10.

Figure 3 of the '405 patent, reproduced below, shows an exemplary LED device with metallization. *Id.* at 2:55–56.

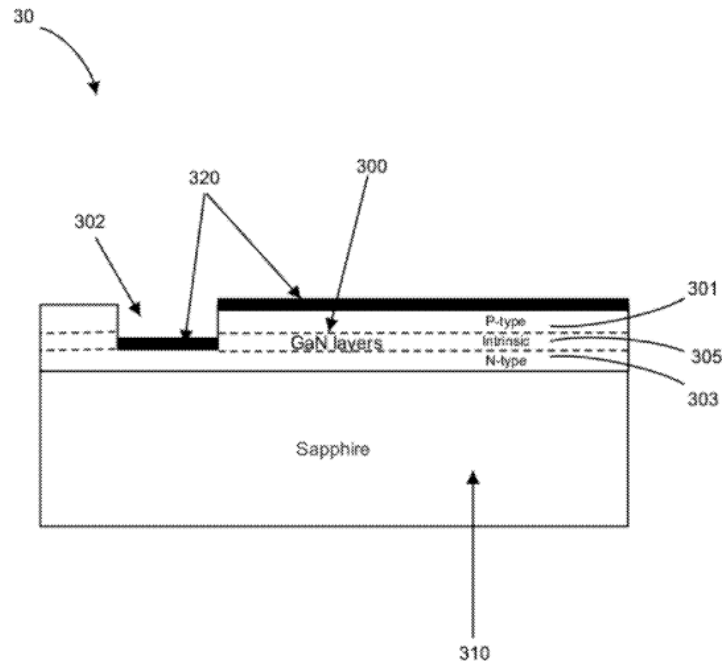


Fig. 3

Figure 3 depicts a LED device with metallization on its surface. *Id.* at 3:64–65. LED device 30 has GaN layer 300 that is disposed on sapphire layer 310. *Id.* at 3:67–4:1. GaN layer 300 comprises intrinsic semiconductor layer 305 positioned between P-type doped layer 301 and N-type doped layer 303 so that electrical biasing of P-type doped layer 301 against N-type doped layer 303 causes photon emission from intrinsic semiconductor layer 305. *Id.* at 4:1–10. Recess 302 is etched into “a portion of the surface of GaN layer 300.” *Id.* at 4:11–12. Suitable metallic layer 320 is applied “to portions of LED device 30.” *Id.* at 3:66–67, 4:15–16.

Figure 5 of the '405 patent, reproduced below, shows a cross sectional view of another exemplary LED device. *Id.* at 2:58–59.

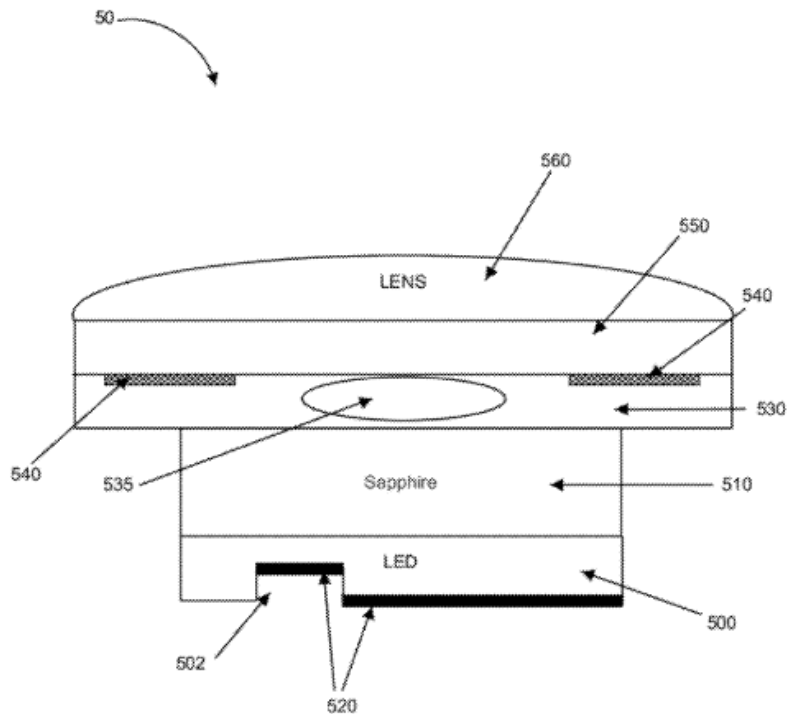


Fig. 5

Figure 5 depicts LED device 50 that “includes the stated LED semiconducting layer or layers 500 as discussed above, along with etched recess 502 and metallization areas 520”³ in which LED layer 500 “is disposed on” sapphire layer 510 “as before.” *Id.* at 4:65–5:2. Optically transparent or transmissive adhesive layer 530 “is placed against the opposing side” of sapphire layer 510 “than the LED material 500 (meaning, one face of the sapphire layer 510 is proximal to the LED material layer 500 and the other opposing face of sapphire layer 510 is proximal to the

³ LED semiconducting layer or layers 500 were not “discussed above” in the ’405 patent and it appears that this is in reference to the layers discussed for Figure 3.

transparent adhesive layer 530[]].” *Id.* at 5:3–8. Within transparent adhesive layer 530 “is a region containing phosphor and/or quantum dot material (QD) 535” such that “photons emitted from LED layer 500 travel through sapphire layer 510 and pass through optically transparent layer 530 and the region containing the phosphor and/or quantum dots 535” so that “color (wavelength) and emission of selective desired light out of the LED device can be controlled.” *Id.* at 5:16–23. Cover substrate 550 is aligned over transparent adhesive layer 530 to provide “structural presence and mechanical coupling for elements of the LED device 50.” *Id.* at 5:24–29.

Figure 10 of the ’405 patent, reproduced below, shows another exemplary LED device. *Id.* at 3:1.

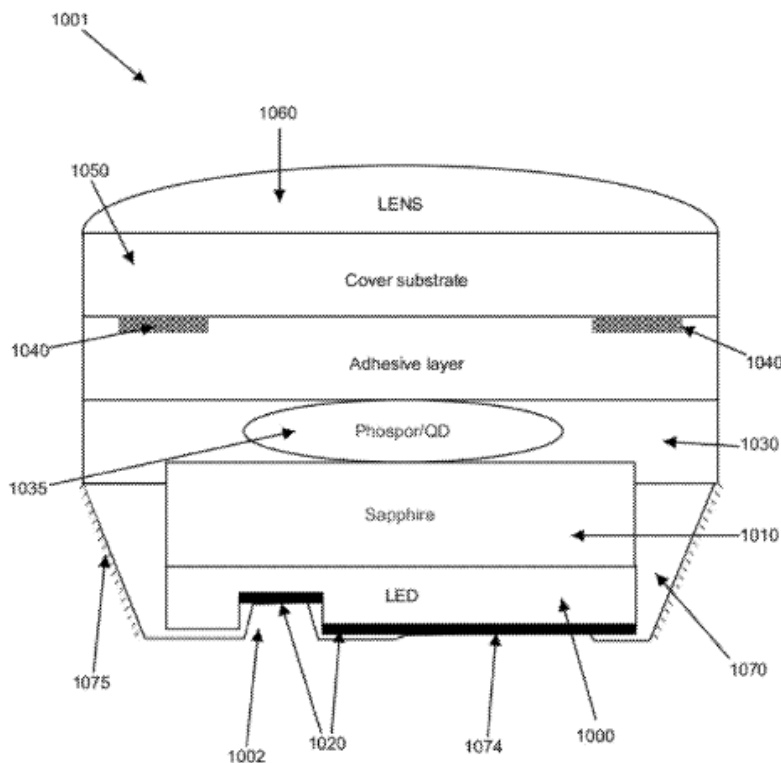


Fig. 10

Figure 10 depicts LED device 1001 in which “[s]imilarly numbered elements discussed earlier are common to or similar to those in this exemplary embodiment.”⁴ *Id.* at 6:45–47. According to the ’405 patent, this embodiment shows “contact holes are drilled” using a laser, “through the passivation layer until reaching the metal pad and silicon substrate.” *Id.* at 6:47–50. Passivation layer 1075 “is cut or etched away as stated above so as to provide conducting access at least to the N-type semiconductor proximal to laser drilled recess 1002 and the P-type semiconductor proximal to portion 1074 of metallization layer 1020.” *Id.* at 6:60–64.⁵ According to the ’405 patent, the passivation layer is “removed to enhance the heat conduction of the LED.” *Id.* at 6:64–65.

D. Challenged Claims

Petitioner challenges claims 1–17 (all) of the ’405 patent. Pet. 2–3. Of the challenged claims, claim 1 is an independent apparatus claim and claim 12 is an independent method claim. Ex. 1001, 8:6–56, 9:24–10:25. Claim 1 recites:

1. A light emitting device, comprising:
a semiconductor LED including a positively-doped region,
an intrinsic region, and a negatively-doped region,
wherein *said intrinsic region is between said positively-doped region and said negatively-doped region*, said semiconductor LED defining a first recess to expose a negatively-doped surface of said negatively-doped region;

⁴ Certain reference numbers, such as reference numbers 1040 and 1050, in Figure 10 are not discussed in the description of the ’405 patent.

⁵ Reference number 1070 is not discussed in the description although reference number 1170 is identified as a passivation layer for Figure 11. *See* Ex. 1001, 7:26.

- an electrically conducting metallization layer in direct contact with at least a portion of each of a positively-doped surface and said negatively-doped surface of said semiconductor LED, wherein said positively-doped surface is on an exposed portion of said positively-doped region of said semiconductor LED and said negatively-doped surface and said positively-doped surface are parallel with each other;
 - a sapphire layer in direct contact with a first surface of said semiconductor LED, said positively-doped surface and said first surface of said semiconductor LED being parallel with one another and on opposing faces of said semiconductor LED;
 - an optically permissive layer in direct contact with said sapphire layer, said optically permissive layer comprising an optically definable material containing quantum dots and/or phosphor, said optically definable material adapted to change the frequency of at least some of emitted light passing therethrough;
 - an optically permissive cover substrate covering at least a portion of the above components; and
 - a passivation layer in direct contact with said metallization layer, said sapphire layer, a surface of said optically permissive layer, and said semiconductor LED,
- wherein said passivation layer defines a first contact hole to expose a first portion of an upper metal surface of said metallization layer disposed on said negatively-doped surface and said passivation layer is in direct contact with a second portion of said upper metal surface of said metallization layer disposed on said negatively-doped surface,
- wherein said passivation layer defines a second contact hole to expose a first portion of a lower metal surface of said metallization layer disposed on said positively-doped surface and said passivation layer is in direct contact with a second portion of said lower metal surface of said metallization layer disposed on said positively-doped surface, and

wherein said upper metal surface, said lower metal surface, said negatively-doped surface, said positively-doped surface, and said surface of said optically permissive layer are parallel with one another.

Id. at 8:6–56 (emphasis added).

E. The Asserted Grounds

Petitioner challenges claims 1–17 of the '405 patent based on the grounds set forth in the table below.

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 5, 6, 8–16	103(a) ⁶	Sugizaki, ⁷ Camras ⁸
4	103(a)	Sugizaki, Camras, Tanimoto ⁹
7, 17	103(a)	Sugizaki, Camras, Tanaka ¹⁰
1, 3, 8–16	103(a)	Sugizaki, Applicant Admitted Prior Art

Pet. 2–3. Petitioner supports its showing of unpatentability of the challenged claims of the '405 patent with the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002).

II. ANALYSIS

A. Claim Construction

Petitioner asserts that it “believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged

⁶ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. §§ 102, 103 effective March 16, 2013. Because the challenged patent claims priority to applications filed before March 16, 2013, we refer to the pre-AIA version of §§ 102, 103. Our opinions on the present record would not change if the AIA versions of §§ 102, 103 were to apply.

⁷ US 2010/0148198 A1, published June 17, 2010 (Ex. 1005).

⁸ US 7,419,839 B2, issued Sept. 2, 2008 (Ex. 1006).

⁹ US 2009/0001869 A1, published Jan. 1, 2009 (Ex. 1007).

¹⁰ US 2008/0031295 A1, published Feb. 7, 2008 (Ex. 1008).

claims.” Pet. 11 (citing Ex. 1002 ¶ 39). Patent Owner “requests that the Board adopt the ordinary and customary meaning of the claim terms as understood by one of ordinary skill in the art.” Prelim. Resp. 11.

We determine that no terms require express construction for purposes of determining whether to institute a trial. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In this Decision, we give the claim terms their ordinary and customary meanings.

B. Legal Standards

A patent claim is unpatentable as obvious if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented, objective evidence of non-obviousness.¹¹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

With regard to combining the teachings of multiple references, an articulated reason with some rational underpinning to combine the known elements in the fashion claimed must be provided to support a conclusion of

¹¹ The parties have not asserted or otherwise directed our attention to any objective evidence of nonobviousness.

obviousness. *See KSR*, 550 U.S. 418; *see also In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (It is the petitioner’s “burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.”) (citation and internal quotation omitted).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioners cannot satisfy their burden of proving obviousness by employing “mere conclusory statements.” *Magnum Oil*, 829 F.3d at 1380.

C. *Level of Ordinary Skill in the Art*

With regard to the level of ordinary skill in the art, Petitioner contends that “[a] person of ordinary skill . . . would have had a bachelor’s degree in electrical engineering, material science, or the equivalent, and two or more years of experience with light emitting diodes (LEDs)” and that “[m]ore education can supplement practical experience and vice versa.” Pet. 4 (citing Ex. 1002 ¶¶ 20–21). Patent Owner states that it “takes no position with respect to Petitioner’s proposed level of ordinary skill in the art.” Prelim. Resp. 32.

Petitioner’s undisputed proposal is consistent with the technology described in the Specification of the ’405 patent and the cited prior art. In

order to determine whether Petitioner has demonstrated a reasonable likelihood of showing the unpatentability of at least one of the challenged claims, we adopt Petitioner’s proposed level of skill in the art.

D. Consideration of Alleged Obviousness in View of Sugizaki and Camras

Our decision is based on consideration of Petitioner’s arguments and evidence regarding the combination of Sugizaki and Camras. *See* Pet. 2 (Grounds 1–3 challenge all the claims in the ’405 patent and rely on a combination of Sugizaki and Camras). We start with a description of the disclosures of Sugizaki and Camras and then consider the arguments and evidence.

1. Sugizaki (Ex. 1005)

Sugizaki is titled “Light Emitting Device and Method for Manufacturing Same.” Ex. 1005, code (54). Specifically, Sugizaki relates to “a method for manufacturing a light emitting device” including “forming a multilayer body” having “a light emitting layer so that a first surface thereof is adjacent to a first surface side of a translucent substrate.” *Id.* ¶ 7. Sugizaki discloses that prior light emitting devices need an interconnect layer and a columnar electrode for bonding a light emitting element chip onto a transparent substrate with high positional accuracy, and are insufficient to meet the requirements for downsizing and mass productivity. *Id.* ¶ 6.

Figure 1A of Sugizaki, reproduced below, shows an exemplary light emitting device. *Id.* ¶ 10.

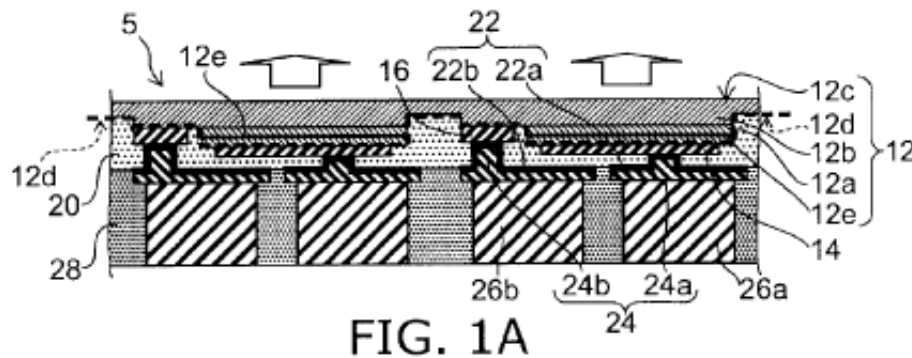


Figure 1A depicts a schematic cross-sectional view of a light emitting device. *Id.* ¶ 31. The light emitting device includes multilayer body 12 that has upper layer 12a, light emitting layer 12e, lower layer 12b, first surface 12c which is exposed, and second surface 12d on the opposite side. *Id.* ¶ 32. Upper layer 12a may include a p-type cladding layer, light emitting layer 12e, and an n-type cladding layer. *Id.* Lower layer 12b “may be of n-type and serve[s] as a lateral path of current.” *Id.* P-side electrode 14 is provided on the surface of upper layer 12a and n-side electrode 16 is connected to n-side metal interconnect layer 24b through n-side seed metal 22b. *Id.* ¶ 33. Sugizaki discloses that “n-side electrode 16 can be a multilayer of Ti/Al/Pt/Au” and “p-side electrode 14 can be a multilayer of Ni/Al (or Ag)/Au.” *Id.* ¶ 49. The light emitting device also has dielectric film 20 that is made of an organic or inorganic material and is filled between seed metal 22a, 22b and second surface 12d. *Id.* ¶ 33.

Figure 18B of Sugizaki, reproduced below, shows a “process cross-sectional view[] of a manufacturing method of a variation of the fourth embodiment.” *Id.* ¶ 27.

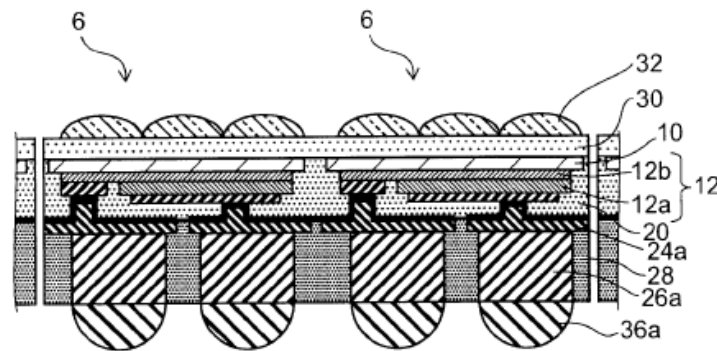


FIG. 18B

Figure 18B depicts a schematic cross-sectional view of a light emitting device with an arrangement of convex lens 32, phosphor layer 30, sapphire substrate 10, dielectric film 20, and multilayer body 12 having upper layer 12 and lower layer 12b, as described previously. Sugizaki discloses that “in separation into packages, because the portion free from the rigid translucent substrate is cut (FIG. 18B), high productivity and yield can be achieved.” *Id.* ¶ 93.

2. *Camras (Ex. 1006)*

Camras is titled “Bonding an Optical Element to a Light Emitting Device.” Ex. 1006, code (54). *Camras* “relates generally to light emitting devices and, more particularly, to bonding an optical element to one or more light emitting device [dies].” *Id.* at 1:6–8.

Figure 1B of *Camras*, reproduced below, shows an optical element bonded to an LED die. *Id.* at 1:59–60.

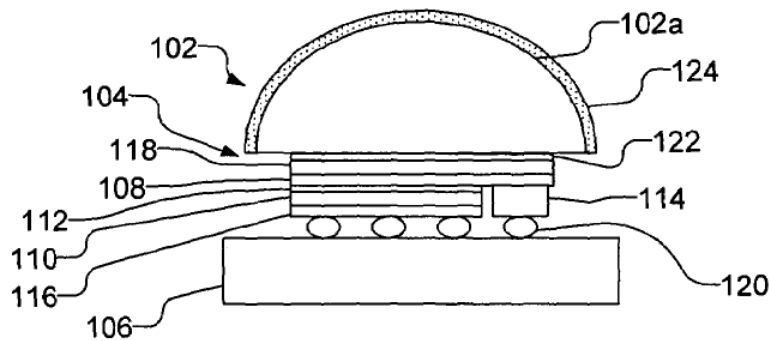


Fig. 1B

Figure 1B depicts transparent optical element 102 bonded to light emitting diode (LED) die 104 on submount 106. *Id.* at 2:31–32. First semiconductor layer 108 “of n-type conductivity (n-layer)” and second semiconductor layer 110 “of p-type conductivity (p-layer)” are “electrically coupled to an active region 112.” *Id.* at 2:44–48. Camras provides that “[a]ctive region 112 is, for example, a p-n diode junction associated with the interface of layers 108 and 110. Alternatively, active region 112 includes one or more semiconductor layers that are doped n-type or p-type or are undoped.” *Id.* at 2:48–52. Transparent superstrate 118 is coupled to first semiconductor layer 108 and is formed from a material such as sapphire. *Id.* at 2:56–58. Camras discloses that “[a]ctive region 112 emits light upon application of a suitable voltage across contacts 114 and 116.” *Id.* at 2:62–63.

3. *Motivation to Combine Sugizaki and Camras*

Independent claims 1 and 12 of the ’405 patent are directed to a LED including a positively-doped region or layer, a negatively-doped region or layer, and an intrinsic region or layer between the positively-doped region or layer and the negatively-doped region or layer. Ex. 1001, 8:7–8 (claim 1), 9:26–28 (claim 12). For the independent claims of the ’405 patent, Petitioner relies on a combination of the teachings of Sugizaki and Camras.

See Pet. 2, 12–45 (discussion of claim 1), 61–72 (discussion of claim 12 (relying on discussion of claim 1)). Patent Owner argues that “Petitioner fails to meet its burden to provide adequate explanation on the motivation to combine [for] any of the grounds.” Prelim. Resp. 3; *see also id.* at 40–48.

Petitioner acknowledges that Sugizaki does not disclose an intrinsic region or layer as recited in the claims of the ’405 patent. The Petition states, “Sugizaki does not explicitly disclose ‘an intrinsic region’ where the ‘intrinsic region is between said positively-doped region and said negatively-doped region’ as recited in claim 1.” Pet. 14; *see also id.* at 16 (“Sugizaki does not disclose the details of the composition of the light emitting layer included in its LED device.”), 87 (“Sugizaki discloses or suggests all of the features of claims 1, 3, and 8-16 with the exception of ‘an intrinsic region’ ‘between said positively-doped region and said negatively-doped region’ as recited in claim 1 and an ‘intrinsic layer’ ‘between said positively-doped layer and a first surface of said LED’ as recited in claim 12.”).

Petitioner relies on Sugizaki in view of Camras to teach or suggest the use of an intrinsic region or layer in an LED as claimed in the ’405 patent. *See* Pet. 13. In this combination, Petitioner relies on Sugizaki’s disclosure of a light emitting layer in the multilayer body of an LED. The Petition states:

Sugizaki discloses that the light emitting device in figure 18B includes a multilayer body 12 (“semiconductor LED”), where details of the multilayer body 12 that are also applicable to figure 18B are described in the context of figures 1A and 1B of Sugizaki. Sugizaki discloses that the multilayer body “has an upper layer 12a, including a light emitting layer 12e, and a lower layer 12b.” (Ex. 1005, ¶[0032].) Sugizaki further discloses that “[t]he upper layer 12a may include a p-type cladding layer” and “[t]he lower layer 12b may be of n-type and serve as a lateral path of current.” (*Id.*) As described by Sugizaki, “light from the light emitting layer 12e can be emitted primarily from the first

surface 12c of the multilayer body 12 in the upward direction of figure 1A.” (*Id.*, ¶[0039]; Ex. 1002, ¶52.)

Id. Thus, with regard to the “intrinsic region” element of claim 1 (and the “intrinsic layer” element of claim 12), Petitioner relies on the disclosure of “light emitting layer [12e]” in Sugizaki. Petitioner identifies no further description of the composition of this “light emitting layer [12e]” in Sugizaki. *See generally id.* Specifically, Petitioner identifies, and we discern, no teaching or suggestion in Sugizaki that this “light emitting layer [12e]” is an intrinsic region or layer or is undoped or not doped. We determine that in Sugizaki an intrinsic region or layer is neither shown nor described.

With regard to the “intrinsic region” and “intrinsic layer” elements of claims 1 and 12, Petitioner directs our attention to a single, one-word reference to using an undoped active layer in LEDs in Camras. Pet. 15 (citing Ex. 1006, 2:44–54). In the cited passage, Camras states, “[a]ctive region 112 is, for example, a p-n diode junction associated with the interface of layers 108 and 110. Alternatively, active region 112 includes one or more semiconductor layers that are doped n-type or p-type or are **undoped**.” Ex. 1006, 2: 48–52 (emphasis added). And, in this passage, using an undoped layer is presented as an alternative to “a p-n diode junction associated with the interface” of two doped layers, or “doped n-type or p-type” layers. *Id.* Although Camras presents an undoped active layer as one of several alternatives, Camras does not describe using an undoped active layer as a preferred option or provide any indication as to why the use of an undoped active layer would be advantageous. And, this single word reference in Camras to using an undoped active layer is the only reference in the asserted

combination of prior art relied upon in the Petition to teach the intrinsic region or layer elements of claims 1 and 12. *See* Pet. 13–15, 61–62.

With regard to motivation to combine the relevant teachings of Sugizaki and Camras, the Petition states:

A POSITA would have looked to Camras for guidance regarding implementing LED devices as disclosed by Sugizaki, particularly **because Camras and Sugizaki are references in the same field that disclose LED devices with many common features.** (Ex. 1002, ¶59.) Having looked to Camras, such a POSITA would have found it obvious to implement the light-emitting layer in Sugizaki such that it includes an intrinsic layer between the p-type and n-type doped regions. (*Id.*)

* * *

Such a POSITA would also have been motivated to use an intrinsic layer for the light emitting layer in an LED as disclosed by Sugizaki **because using an intrinsic layer is one of a limited number of alternatives disclosed by Camras, where those alternatives include p-type, n-type and intrinsic semiconductor material.** (Ex. 1006, 2:50-52; Ex. 1002, ¶61.) Indeed, the '405 patent discloses that LEDs with an intrinsic layer between p-type and n-type material were known and in use. (*See supra* Section VII; Ex. 1001, 3:9-16, 3:33-35, 3:44-47, 3:64-4:8, FIGs. 1-3; Ex. 1002, ¶61.) Similarly, Sugawara also demonstrates that a POSITA would have been aware of the use of intrinsic layers between p- and n-type layers in LEDs. (Ex. 1009, 3:45-51.)

A POSITA reading Sugizaki would have understood that various known light-emitting multilayer bodies could be used in conjunction with Sugizaki's LED devices. (Ex. 1002, ¶62.) Indeed, Sugizaki explicitly contemplates that the use of different multilayer structures. (Ex. 1005, ¶[0104]; Ex. 1002, ¶62.)

A POSITA would have found it straightforward to use an intrinsic layer as disclosed by Camras in an LED device as disclosed by Sugizaki **because Camras discloses such an intrinsic layer in a device very similar to that of Sugizaki.** (Ex. 1002, ¶63.) Such an implementation would have been a straightforward combination of well-known technologies using

known methods and would have had predictable results. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Camras, as well as Sugawara and the ’405 patent (*see supra* Section VII.A; Ex. 1001, 3:9-16, 3:33-35, 3:44-47, 3:64-4:8, FIGs. 1-3), LEDs with intrinsic light-emitting layers were well known in the art, and Sugizaki specifically contemplates using different multilayer bodies with the light emitting device embodiments disclosed. *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) (“only a reasonable expectation of success, not a guarantee, is needed” in an obviousness analysis). Therefore, the Sugizaki-Camras combination discloses or suggests a multilayer structure 12 like that shown in the figures of Sugizaki, where the multilayer structure includes an intrinsic layer sandwiched between p-type and n-type regions (“an intrinsic region . . . between said positively-doped region and said negatively-doped region”). (Ex. 1002, ¶63.)

Pet. 15–18 (emphasis added; footnote omitted). Liberally interpreting these passages, Petitioner contends that a motivation to combine the relevant teachings of the cited references is established because: (1) Sugizaki and Camras “are references in the same field that disclose LED devices with many common features;” (2) “an intrinsic layer for the light emitting LED as disclosed in Sugizaki . . . is one of a limited number of alternatives disclosed by Camras;” and (3) “Camras discloses such an intrinsic layer in a device very similar to that of Sugizaki.” *Id.* Even accepting these statements as accurate and proven, Petitioner still fails to provide any rationale or reasoning as to why a skilled artisan would have chosen to use the undoped layer of Camras in the light emitting device of Sugizaki. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns not only whether a skilled artisan *could have made* but *would have been motivated to make* the combinations or modifications of prior art to

arrive at the claimed invention.”). To the extent that Petitioner relies on the allegation that the use of an intrinsic (undoped or not-doped) light emitting layer in an LED was well-known technology or “well known in the art,” Petitioner fails to support such an allegation. We determine that the Petition fails to establish that a skilled artisan would have been motivated to combine the cited references to arrive at the invention recited in the challenged claims of the ’405 patent, which includes an intrinsic region or layer.

Patent Owner argues that “Petitioner has failed to meet its burden to show that a POSITA would have been motivated to combine Sugizaki with Camras.” Prelim. Resp. 40. Patent Owner contends that the showing in the Petition as to motivation to combine is conclusory and fails to provide any specific reasoning for combining Sugazaki and Camras. *Id.* at 40–46. For example, Patent Owner argues that Sugizaki discloses LEDs with “P/N junctions, which fail to have an intrinsic region and instead have a depletion region” (*id.* at 43–44 (citing Ex. 1003, Fig. 18B (as relied on in the Petition); Ex. 2006, 293; Ex. 2007, 1)), whereas “[t]he ’405 Patent discloses the P-I-N junction and how it possesses an intrinsic layer (*id.* (citing Ex. 1001, 1:19–32)). Patent Owner argues that, in the Petition’s discussion of motivation to combine Sugazaki with Camras, Petitioner does not take into account the different types of LED junctions and appears to conclude that an intrinsic LED layer would have been obvious merely because it was known in the art. Prelim Resp. 43–45 (citing Pet. 19). We determine on this preliminary record that Patent Owner’s criticism of the showing in the Petition as to motivation to combine the cited references has some merit.

Based on this record, we determine that Camras shows that it was known in the prior art to use an intrinsic (undoped) region or layer in an

LED. However, we further determine that Petitioner has not adequately shown in the Petition a motivation to combine with a reasonable expectation of success the teachings of Sugizaki as to a light emitting layer with the teaching of Camras as to the use of an intrinsic (undoped) region or layer in an LED, especially in the context of the relied-upon embodiment of Figure 18B of Sugizaki depicting a 2-layer structure and in light of the limited (one word) teaching in Camras relating to the use of an undoped, light emitting layer. The obviousness case based on the combination of Sugizaki and Camras in the Petition is not well-supported.

4. *Summary*

We determine that Petitioner has failed to show a reasonable likelihood of establishing, based upon the relied-upon teachings in Sugizaki and Camras, that a skilled artisan would have been motivated to combine the cited prior art references with a reasonable expectation of success such that the LED device disclosed in Sugizaki would include an intrinsic region or layer as recited in independent claims 1 and 12 of the '405 patent.

E. Consideration of Alleged Obviousness in View of Sugizaki and Applicant Admitted Prior Art

Petitioner challenges claims 1, 3, 8–16 of the '405 patent based on Sugizaki and Applicant Admitted Prior Art (“AAPA”). Pet. 2, 87–91. With regard to this challenge, the Petition begins:

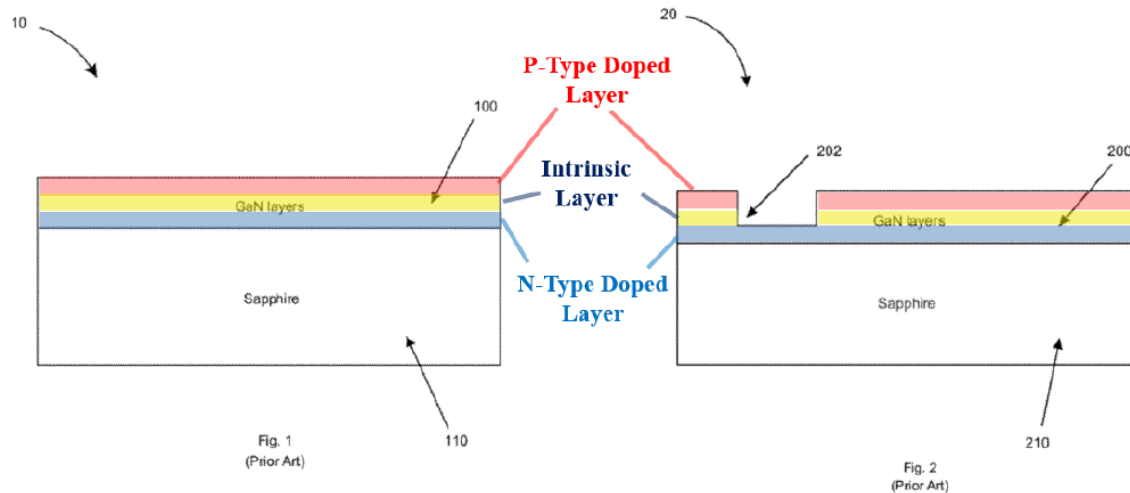
Sugizaki in view of the AAPA discloses or suggests all of the features of claims 1, 3, and 8-16. As discussed above with respect to the Sugizaki-Camras combination, Sugizaki discloses or suggests all of the features of claims 1, 3, and 8-16 with the exception of “an intrinsic region” “between said positively-doped region and said negatively-doped region” as recited in claim 1 and an “intrinsic layer” “between said positively-doped layer and a first surface of said LED” as recited in claim 12. As

also discussed above, it would have been obvious to include such an intrinsic layer in an LED device like that disclosed by Sugizaki in view of Camras. A POSITA would also have found it obvious to include such an intrinsic layer in an LED device like that disclosed by Sugizaki in view of the Applicant Admitted Prior Art (AAPA) of the '405 patent, and therefore the Sugizaki-AAPA combination discloses or suggests all of the features of claims 1, 3, and 8-16.

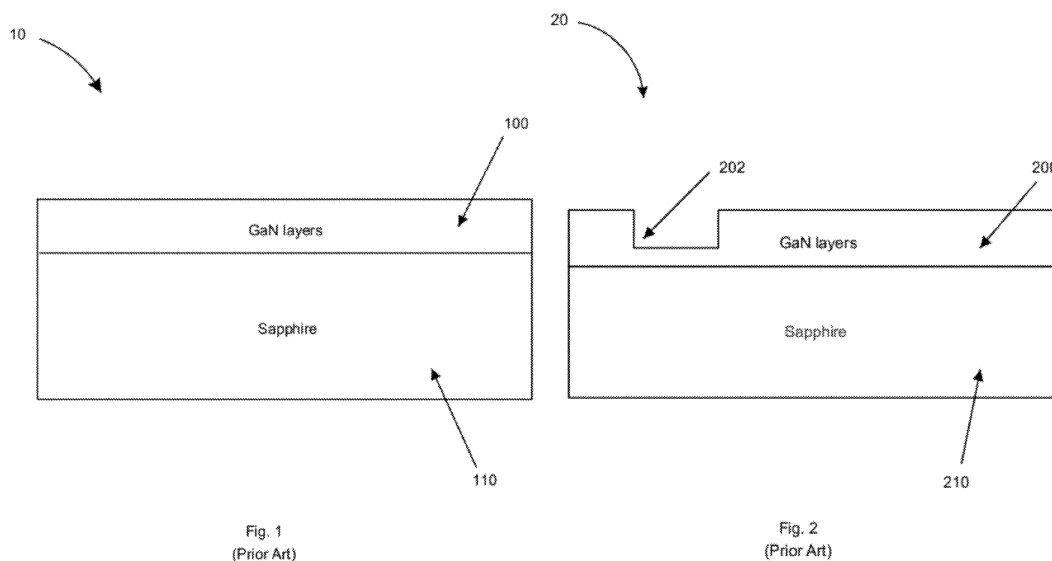
Id. at 87 (citations omitted). Thus, Petitioner relies on AAPA to supply an element of the claimed invention (the intrinsic region or layer) in the same way as a prior art reference (Camras) is used for the other grounds in the Petition.¹²

Petitioner does not clearly establish that an intrinsic layer in an LED device like that disclosed by Sugizaki is AAPA in the '405 patent. In this section of the Petition, annotated versions of Figures 1 and 2 of the '405 patent, reproduced below, are provided. Pet. 89.

¹² In its recent opinion in *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367 (Fed. Cir. 2022), the U.S. Court of Appeals for the Federal Circuit held that 35 U.S.C. § 311(b) does not permit AAPA to form the “basis” of a ground in an *inter partes* review but that other uses of AAPA in an *inter partes* review may be permissible. *Qualcomm*, 24 F.4th at 1373–1377. Here, Petitioner does not establish that the cited disclosure in the challenged patent is in fact AAPA, so we need not reach the issue of whether *Qualcomm* precludes its use in this proceeding.



In these depicted annotated versions of Figures 1 and 2 in the Petition, “Figures 1 and 2 of the ’405 patent, both of which are labeled ‘Prior Art,’ are annotated . . . to show the doped and intrinsic layers that the ’405 patent describes as being present in prior art LED devices.” *Id.* at 88. These annotated versions of Figures 1 and 2 are not fair or accurate reproductions of Figures 1 and 2 of the ’405 patent which are reproduced below.



Ex. 1001, Figs. 1, 2. As depicted in the ’405 patent, Figures 1 and 2 are labelled “Prior Art,” but do not depict the 3-layer structure including the

intrinsic layer shown in Petitioner's annotated versions of Figures 1 and 2. This 3-layer structure is shown in Figure 3 of the '405 patent, reproduced below.

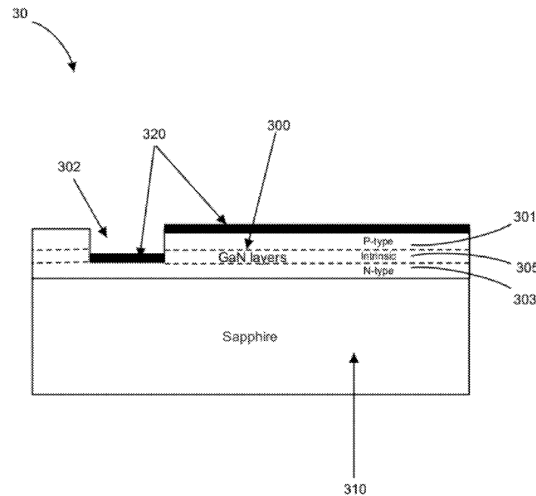


Fig. 3

Ex. 1001, Fig. 3. Figure 3 depicts the 3-layer structure including the intrinsic layer but is not labelled as prior art. *Id.* Figures 1 and 2 are also described as “prior art” in the “Brief Description of the Drawings” section in the '405 patent, while Figure 3 is not. *Id.* at 2:50–56. Here, the '405 patent states:

FIG. 1 illustrates a semiconducting LED layer above a sapphire layer ***according to the prior art***;

FIG. 2 illustrates a semiconducting LED layer with a cavity etched in a portion thereof on a sapphire layer ***according to the prior art***;

FIG. 3 illustrates metallization of a LED device according to some aspects.

Id. (emphasis added). The detailed description of Figure 3 does not contain any admission by the Applicant that this 3-layer structure including the intrinsic layer is prior art. *See* Ex. 1001, 3:64–4:8.

Petitioner also quotes a sentence from the '405 patent that states, "GaN LEDs are *typically* epitaxially grown on a sapphire substrate." Pet. 87 (quoting Ex. 1001, 3:12–13)(emphasis added). This sentence describing what is typical is followed by a sentence that describes a LED with a 3-layer structure including an intrinsic layer. *See* Ex. 1001, 3:13–16 ("These LEDs comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer."). Notably, the sentence describing the 3-layer structure including an intrinsic layer does not indicate that such a structure is typical.

Based on this record, we determine that the Petition does not provide an adequate explanation or showing that an LED with a 3-layer structure including an intrinsic layer should be considered as AAPA based on the disclosure of the '405 patent. For these reasons, we decline to institute on Petitioner's challenge to the claims based on a combination of Sugizaki and AAPA.

III. CONCLUSION

Petitioner has not demonstrated a reasonable likelihood of showing at least one of the claims challenged in the Petition would have been unpatentable. Accordingly, for the reasons stated herein, we deny the Petition.

IV. ORDER

In consideration of the foregoing, it is:

ORDERED that the Petition is *denied* and no *inter partes* review as to any claim of the '405 patent is instituted.

IPR2021-01491
Patent 8,952,405 B2

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