

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA CORPORATION; KIOXIA AMERICA, INC.; WESTERN
DIGITAL TECHNOLOGIES, INC.; DELL TECHNOLOGIES INC.;
GOOGLE LLC; KINGSTON TECHNOLOGY COMPANY, INC.;
KINGSTON TECHNOLOGY CORPORATION; AND SAMSUNG
ELECTRONICS CO., LTD.,
Petitioners,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2021-01561
Patent 6,724,241 B1

Before GREGG I. ANDERSON, GARTH D. BAER, and
JOHN D. HAMANN, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Kioxia Corporation; Kioxia America, Inc.; Western Digital Technologies, Inc.; Dell Technologies Inc.; Google LLC; Kingston Technology Company, Inc.; Kingston Technology Corporation; and Samsung Electronics Co., Ltd; (together, “Petitioner”) filed a Petition (Paper 1, “Pet.”), requesting an *inter partes* review of claims 1–3, 6–13, 15–17, 19, 21, and 23–25 of U.S. Patent No. 6,724,241 B1 (Ex. 1001, “the ’241 patent”). Sonrai Memory Limited (“Patent Owner”) did not file a Preliminary Response to the Petition.

We have authority under 35 U.S.C. § 314 to determine whether to institute *inter partes* review. For the reasons discussed below, we institute *inter partes* review of the challenged claims.

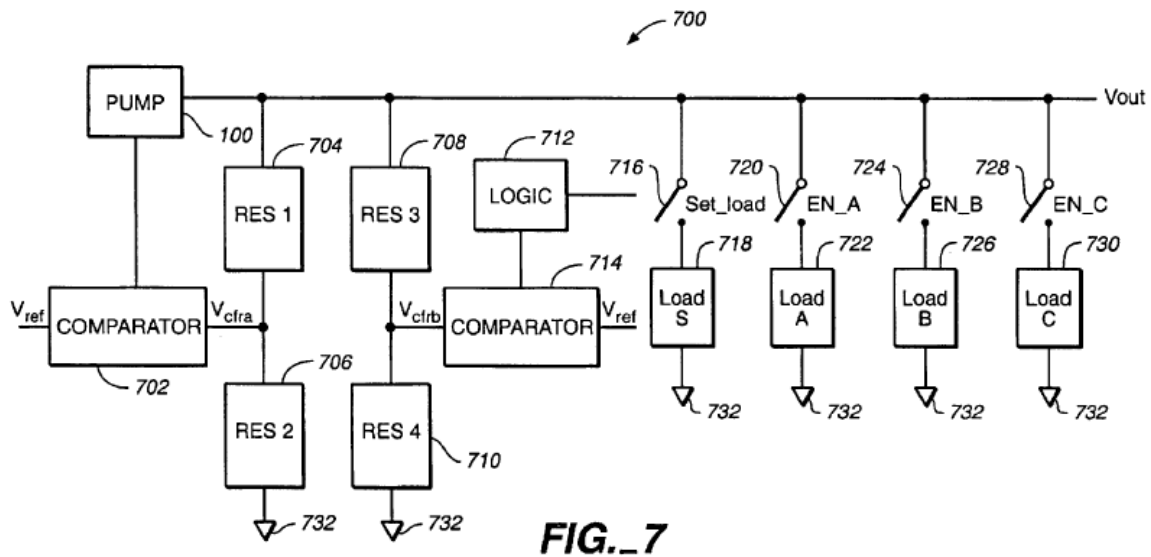
II. BACKGROUND

A. RELATED MATTERS

The ’241 patent is at issue in *Sonrai Memory Ltd. v. Kioxia Corp. and Kioxia Am., Inc.*, 6:21-cv-00400-ADA (WDTX), *Sonrai Memory Ltd. v. Kioxia Corp. and Kioxia Am., Inc.*, 6:21-cv-00400-ADA (WDTX), *Sonrai Memory Ltd. v. Western Digital Corp.*, 8:21cv1040 (C.D. Cal.), *Sonrai Memory Ltd. v. Dell Tech., Inc.*, 6:21-cv00361-ADA (WDTX), *Sonrai Memory Ltd. v. Google LLC*, 6:21-cv-00167-ADA (WDTX), *Sonrai Memory Ltd. v. Kingston Technology Company, Inc. and Kingston Tech. Corp.*, 8:21cv1039 (C.D. Cal.), and *Sonrai Memory Ltd. v. Samsung Electronics Co., and Samsung Elect. Am., Inc.*, Case No. 6:21-cv-00169-ADA (WDTX). Pet. 2, Paper 11, 1–2.

B. THE '241 PATENT

The '241 patent is directed to charge pumps, which are devices that generate voltages higher than the voltage of the available power source. Ex. 1001, 1:5–18. In particular, the '241 patent teaches a technique for minimizing the voltage ripple. *Id.* at code (57). The '241 patent's Figure 7 is reproduced below.



[t]he first comparator 702 disables the pump 100 whenever the pump output voltage (V_{cfra}) sampled by means of the first resistive network is greater than the reference voltage (V_{ref}). Otherwise, the first comparator 702 leaves the pump circuit 100 to continue to operate. When the voltage V_{cfra} is greater than the reference voltage (V_{ref}) the charge pump circuit 700 performs the second test to further minimize the voltage ripple at the pump output (V_{out}). The second comparator 714 instructs the logic circuit 712 to add the load S 718 whenever the maximum acceptable ripple on target output sampled at node V_{cfrb} is greater than the reference voltage (V_{ref}); otherwise, the second

comparator 714 leaves the pump circuit 700 to operate without adding any load.

Id. at 6:4–17.

C. THE CHALLENGED CLAIMS

Of the challenged claims, claims 1, 13, and 24 are independent.

Claim 1 is representative and reproduced below:

1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:

a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;

b) a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and

c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.

Ex. 1001, 8:16–27.

D. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner asserts the following grounds of unpatentability. Pet. 12.

Reference(s)	Basis	Challenged Claims
Ujii ¹	§ 102	1, 7, 8
Ujii	§ 103	6, 9, 10
Ujii, Doluca ²	§ 103	1–3, 11–13, 15–17, 19, 21, 23–25
Ujii, Cleveland, ³ Doluca	§ 103	1–3, 6–12

¹ JP S61-24094, Pub. Feb. 1, 1986 (Ex. 1004, “Ujie”).

² US 4,769,784, Sept. 6, 1988 (Ex. 1005, “Dolucas”).

³ US 6,486,728, B2, Nov. 26, 2002 (Ex. 1007, “Kleveland”).

Hosono ⁴	§ 102	1, 2, 6, 11, 24
Hosono	§ 103	7–10
Hosono, Doluca	§ 103	1–3, 12, 13, 15–17, 19, 21, 23, 25

Petitioner also relies on a declaration from Dr. Vivek Subramanian (Ex. 1003).

III. ANALYSIS

A. LEVEL OF SKILL IN THE ART

Petitioner contends a person of ordinary skill in the art “would have had a Bachelor’s degree in electrical engineering or an equivalent field and two years of academic or industry experience working with analog and digital circuits.” Pet. 12 (citing Ex. 1003 ¶ 36). At this stage, Patent Owner does not provide a description of the person of ordinary skill.

Petitioner’s description is supported by credible expert testimony. *Id.* For the purpose of our decision, we adopt Petitioner’s description.

B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2020).

1. “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” (claim 1)

Petitioner asserts this a means-plus-function limitation, subject to construction under § 112 ¶ 6. Pet. 14. Petitioner asserts the claimed

⁴ US 6,404,274 B1, June 11, 2002 (Ex. 1006, “Hosono”).

function matches the claim language, and that we should construe that function as “choosing a load based on the target pump voltage, such that the load is coupled to the output of the pumping circuit when the target pump voltage is selected.” *Id.* Petitioner identifies switches 320, 324, and 328, which may be transistors, and their control signals EN_A, EN_B, and EN_C as the ’241 patent’s disclosed structure corresponding to the claimed load-selector means. *Id.* at 14–15. According to Petitioner, the corresponding structure may further include a controller for generating the control signals. *Id.* at 15–16. For purposes of this decision, we agree with and adopt Petitioner’s construction.

2. “target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 2) and “a target output pump selector sampling the output of the pump circuit for shutting down the variable charge pump circuit whenever the sampled output voltage (v_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 13)

Petitioner asserts these limitations are means-plus-function limitations, “as evidenced by claims 12 and 13 referring to these limitations as the ‘target output pump selector means.’” *Id.* at 16 (quoting Ex. 1001). According to Petitioner, the claimed function matches the claim language, and the disclosed structure for both functions is comparator 702. *Id.* at 17. For purposes of this decision, we agree with and adopt Petitioner’s construction.

3. “a load selector means coupled to the output pump for selecting a load that satisfies a specific pump voltage” (claim 13)

Petitioner asserts this is a means-plus-function limitation, the claimed function matches the claim language, and the disclosed structure is the same

as identified above for the load-selector means in claim 1. *Id.* For purposes of this decision, we agree with and adopt Petitioner's construction.

C. DESCRIPTION OF PRIOR ART REFERENCES

1. Ujiie (Ex. 1004)

Ujiie relates to semiconductor memory technology. Ex. 1004 ¶ 1.

Ujiie's Figure 3 is reproduced below.

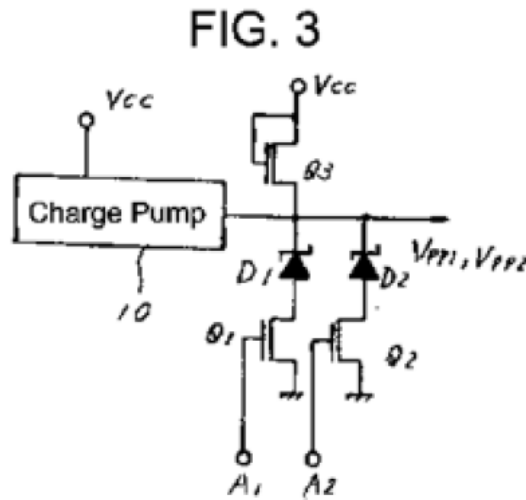


Figure 3 is a voltage boosting circuit. *Id.* ¶ 19. In Figure 3, clamping diodes D1 and D2 are coupled to a charge pump by transistors Q1 and Q2, which are turned on and off by control signals A1 and A2. *Id.* ¶¶ 22–23.

2. Doluca (Ex. 1005)

Doluca discloses a circuit for enabling either a charge pump or charge bleeder to regulate voltage at a level above the circuit's supply voltage.

Ex. 1005, code (57). Doluca's Figure 2 is reproduced below.



Figure 2 is a block schematic of Doluca's capacitor-plate bias circuit.

Ex. 1005, 2:51–52.

3. Kleveland (Ex. 1007)

Kleveland discloses a multi-stage charge pump. Ex. 1007, code (54). According to Kleveland, various stages can be selected to generate different output voltages. *Id.* at 1:34–36.

4. Hosono (Ex. 1006)

Hosono teaches a voltage generating circuit capable of generating variable multi-level voltages. Ex. 1006, code (54). Hosono's Figure 2 is reproduced below.

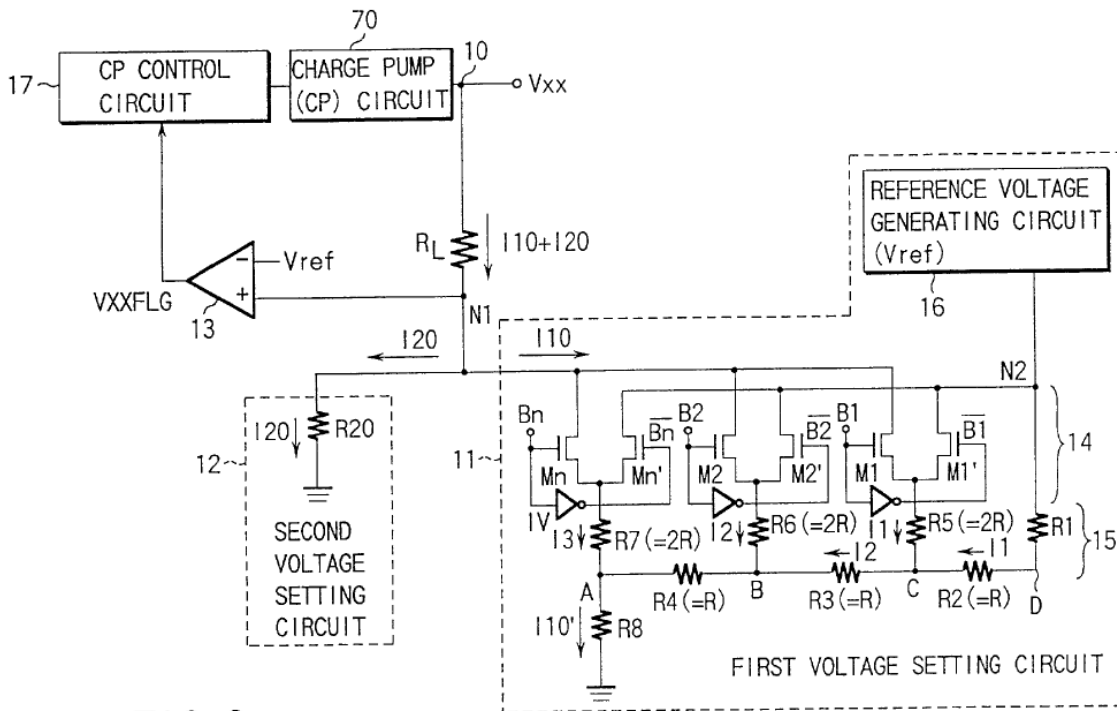


FIG. 2

Figure 2 is an embodiment of Hosono's internal voltage generating circuit. *Id.* at 6:17–19. Figure 2 depicts charge pump circuit 70, load resistor element R_L , as well as first and second voltage setting circuits, 11 and 12. *Id.* at 8:22–28. First voltage setting circuit 11 includes resistor elements R_5 , R_6 , and R_7 , as well as switch elements M_1 , M_2 , and M_n . *Id.* at 8:36–37, 8:60–65.

D. UNPATENTABILITY ANALYSIS

1. Anticipation of Claims 1, 7, and 8 based on Ujiie

Petitioner contends Ujiie anticipates claims 1, 7, and 8. Pet. 21–27. Specifically, Petitioner corresponds the charge pump in Ujiie's Figure 3 to claim 1's "charge pump circuit." *Id.* at 21–22 (citing Ex. 1004, Fig. 3, ¶¶ 20–21; Ex. 1003 ¶ 56). Ujiie teaches the claimed "pumping circuit," recited in claim 1 because, Petitioner contends, Ujiie's "Figure 4 illustrates the well-known 'Dickson' charge pump with multiple stages and operable to receive

a supply voltage (VCC), which is the same type of charge pump disclosed in the '241 patent.” *Id.* at 22–23 (citing Ex. 1004, Fig. 4, ¶¶ 28–33; Ex. 1003 ¶ 58). Petitioner explains that Ujiie also teaches claim 1’s “plurality of loads” because “[t]he charge pump circuit of [Ujiie’s] Figure 3 contains a plurality of loads, specifically, Zener diode D1 and Zener diode D2.” *Id.* at 23 (citing Ex. 1004 ¶¶ 20–23; Ex. 1003 ¶ 60). Last, Petitioner explains, Ujiie discloses claim 1’s “load selector means” because “Ujiie discloses select transistors Q1 and Q2, which are turned on by control signals A1 and A2 to connect loads D1 and D2, respectively, to the output of the charge pump when the target voltage is selected.” *Id.* at 24 (citing Ex. 1004 ¶ 23). We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 1 based on Ujiie.

Claim 7 depends from claim 1 and additionally requires that “each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.” Petitioner explains that Ujiie teaches claim 7’s additional feature because in Ujiie’s Figure 3, “Switches Q1 and Q2 are NMOS transistors.” *Id.* at 26 (citing Ex. 1003 ¶ 65). Further, Petitioner explains, “[t]he gate of Q1 receives enable signal A1, the source of Q1 is coupled to ground, and the drain of Q1 is coupled to load D1,” while similarly “the gate of Q2 receives enable signal A2, the source of Q2 is coupled to ground, and the drain of Q2 is coupled to load D2.” *Id.* at 26 (citing Ex. 1004, Figure 3; Ex. 1003 ¶ 65).

We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 7 based on Ujiie.

Claim 8 depends from claim 7 and further requires “each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.” Petitioner explains that Ujiie teaches the additional feature recited in claim 8 because Ujiie’s “[l]oads D1 and D2 . . . sink current.” *Id.* (citing Ex.1003 ¶ 66). Further, Petitioner explains, “[l]oad D1 has a first terminal coupled to the pump voltage that is output from the charge pump and a second terminal coupled to the drain of the NMOS transistor Q1,” while “load D2 has a first terminal coupled to the pump voltage that is output from the charge pump and a second terminal coupled to the drain of the NMOS transistor Q2.” *Id.* at 26–27 (citing Ex. 1004, Figure 3; Ex.1003 ¶ 66). We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 8 based on Ujiie.

2. Additional Grounds

Petitioner additionally asserts claims 6, 9, and 10 would have been obvious over Ujiie (*id.* at 27–30); claims 1–3, 11–13, 15–17, 19, 21, and 23–25 would have been obvious over Ujiie and Doluca (*id.* at 30–57); and claims 1–3 and 6–12 would have been obvious over Ujiie, Cleveland, and Doluca (*id.* at 57–59). Further, Petitioner contends, Hosono anticipates

claims 1, 2, 6, 11, and 24 (*id.* at 59–66); claims 7–10 would have been obvious over Hosono (*id.* at 66–68); and claims 1–3, 12, 13, 15–17, 19, 21, 23, and 25 would have been obvious over Hosono and Doluca (*id.* at 68–81). As noted above, Patent Owner does not challenge Petitioner’s analysis at this stage. We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its additional challenges to claims 1–3, 6–13, 15–17, 19, 21, and 23–25.

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. ORDER

Accordingly, it is:

ORDERED that *inter partes* review of claims 1–3, 6–13, 15–17, 19, 21, and 23–25 of the ’241 patent is instituted on all grounds in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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PETITIONER:

James M. Heintz
DLA PIPER LLP (US)
jim.heintz@us.dlapiper.com

Brian M. Buroker
Nathan Curtis
GIBSON, DUNN & CRUTCHER LLP
bburoker@gibsondunn.com
ncurtis@gibsondunn.com

Christopher TL Douglas
Ben Pleune
ALSTON & BIRD LLP
christopher.douglas@alston.com
ben.pleune@alston.com

Naveen Modi
Daniel Zeilberger
PAUL HASTINGS LLP
naveenmodi@paulhastings.com
danielzeilberger@paulhastings.com

David Hoffman
FISH & RICHARDSON P.C.
hoffman@fr.com

Martha Hopkins
LAW OFFICE OF S.J. CHRISTINE YANG
mhopkins@sjclawpc.com

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PATENT OWNER:

Reza Mirzaie
James Milkey
RUSS AUGUST & KABAT
rmirzaie@raklaw.com
jmilkey@raklaw.com