

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,
Petitioner,

v.

OPTICAL LICENSING, LLC,
Patent Owner.

IPR2021-01593
Patent 6,791,898 B1

Before KRISTEN L. DROESCH, NEIL T. POWELL, and
DAVID C. McKONE, *Administrative Patent Judges*.

POWELL, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. BACKGROUND

STMicroelectronics, Inc. (“Petitioner”) filed a Petition for *inter partes* review of claims 1–18 of U.S. Patent No. 6,791,898 B1 (Ex. 1001, “the ’898 patent”). Paper 2 (“Pet.”). Optical Licensing LLC (“Patent Owner”) filed a Preliminary Response. Paper 8 (“Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and the associated evidence, for the reasons described below, we institute *inter partes* review of all the challenged claims on all the grounds set forth in the Petition.

B. RELATED MATTERS

Petitioner argues that Patent Owner has asserted infringement of the ’898 patent in a number of district court proceedings. Pet. 1–2. Patent Owner contends that these include “two highly relevant parallel proceedings,” which are *Optical Licensing, LLC v. Future Electronics Corp.*, No. 6:21-cv-00188 (W.D. Tex.) (“the ’188 proceeding”) and *Optical Licensing, LLC v. Arrow Electronics, Inc.*, No. 6:21-cv-00186 (W.D. Tex.) (“the ’186 proceeding”). Prelim. Resp. 2; Pet. 1; Paper 6, 2.

Other district court proceedings identified by the parties include *Optical Licensing LLC v. Home Depot U.S.A., Inc.*, No. 6:21-cv-904 (W.D. Tex.); *Optical Licensing LLC v. Lowe’s Companies, Inc. et al.*, No. 6:21-cv-905 (W.D. Tex.); *Optical Licensing LLC v. HEICO Corp. et al.*, No. 0:21-cv-61832 (S.D. Fla.); *Optical Licensing LLC v. Analog Devices, Inc.*, No.

8:21-cv-02308 (M.D. Fla.); and *Optical Licensing LLC v. TTM Technologies North America, LLC*, No. 4:21-cv-01858 (N.D. Ohio). Pet. 1–2; Paper 6, 2.

C. REAL PARTIES-IN-INTEREST

In its section addressing real party-in-interest, the Petition states that Petitioner, STMicroelectronics, Inc. (“ST”) is the real party-in-interest. 37 C.F.R. § 42.8(b)(1). Although STMicroelectronics N.V., ST’s parent company, is not a real party-in-interest under the governing legal standard for making that determination, ST identifies it as a real party-in-interest for purposes of this Petition to avoid any disputes over that issue. Further, Future Electronics Corp. and Arrow Electronics, Inc. are suppliers of certain ST products and have a legal relationship with ST. Accordingly, Future and Arrow may be real-parties-in-interest.

Pet. 1.

Patent Owner states that “[t]he real party-in-interest for the Patent Owner is Optical Licensing LLC.” Paper 6, 2.

D. THE ’898 PATENT

The ’898 patent relates to memory device data transfer modes. Ex. 1001, 1:7–9. According to the ’898 patent, “[i]n the conventional art, memory devices either transfer data synchronously or asynchronously. In asynchronous transfer, one device may initiate the transfer and wait until the another device responds. In synchronous transfer, the transfer occurs according to a clock signal that can be shared between two devices.” *Id.* at 1:12–17. The ’898 patent considers it disadvantageous for a memory device to provide only synchronous or only asynchronous operation. *Id.* at 2:24–29. Accordingly, the ’898 patent discloses that “[e]mbodiments of the present invention provide a memory device having multiple modes of data transfer. Embodiments of the present invention provide for asynchronous data transfer. Embodiments of the present invention provide for

synchronous data transfer.” *Id.* at 2:33–37. The ’898 patent discusses details in connection with Figure 3, which is reproduced below.

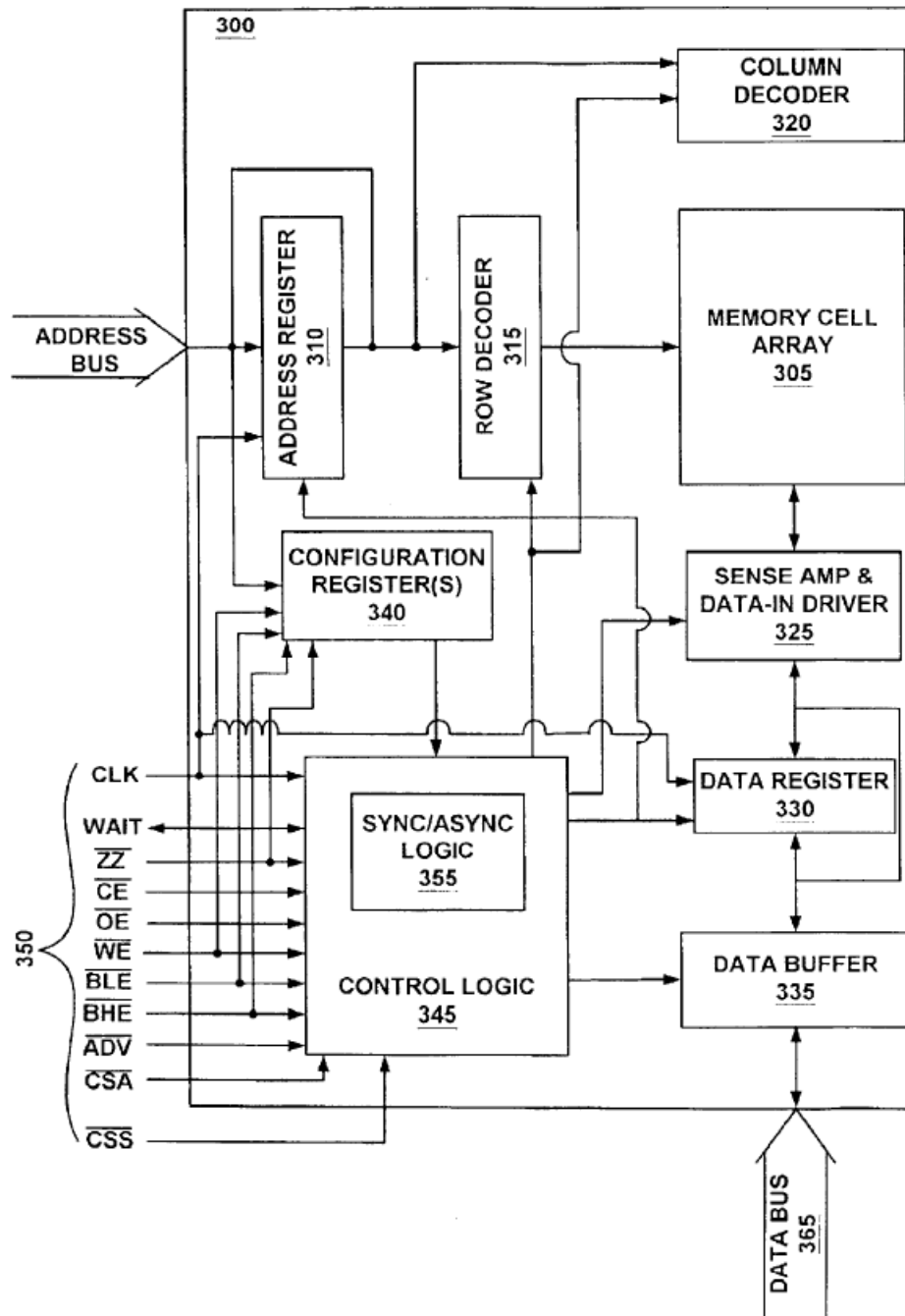


FIGURE 3

Figure 3 shows a block diagram of memory device 300. *Id.* at 4:12–14.

Memory device 300 includes “an array of memory cells 305, address register 310, a row address decoder 315, a column address decoder 320, sense amplifier and data-in driver 325, data register 330, data buffer 335, configuration register 340 and control logic 345.” *Id.* at 4:14–19. Control logic 345 has “asynchronous/synchronous (async/sync) logic 355.” *Id.* at 21–23. Control logic 345 receives control signals 350. *Id.* at 4:19–20.

Memory device 300 may operate asynchronously or synchronously: “The async/sync logic 355 provides for multiple modes of data transfer by the memory device 300. The memory device 300 in asynchronous mode provides for asynchronous read and write transfers. The memory device 300 in synchronous mode provides for synchronous read and asynchronous write transfers.” *Id.* at 4:28–33. The ’898 patent discloses multiple implementations of such operation. For example, “[i]n one implementation, the async/sync logic 355 portion of the control logic 345 controls operation in asynchronous and synchronous modes, based upon the state of various control signals 350. Operation may either be asynchronous read, asynchronous write, or synchronous read.” *Id.* at 4:34–38. “In another implementation, the async/sync logic 355 portion of the control logic 345 controls operation in asynchronous and synchronous modes based upon the contents of a plurality of configuration registers 340.” *Id.* at 4:57–60.

The '898 patent further discusses asynchronous and synchronous operation in connection with Figures 4A and 4B, which are reproduced below.

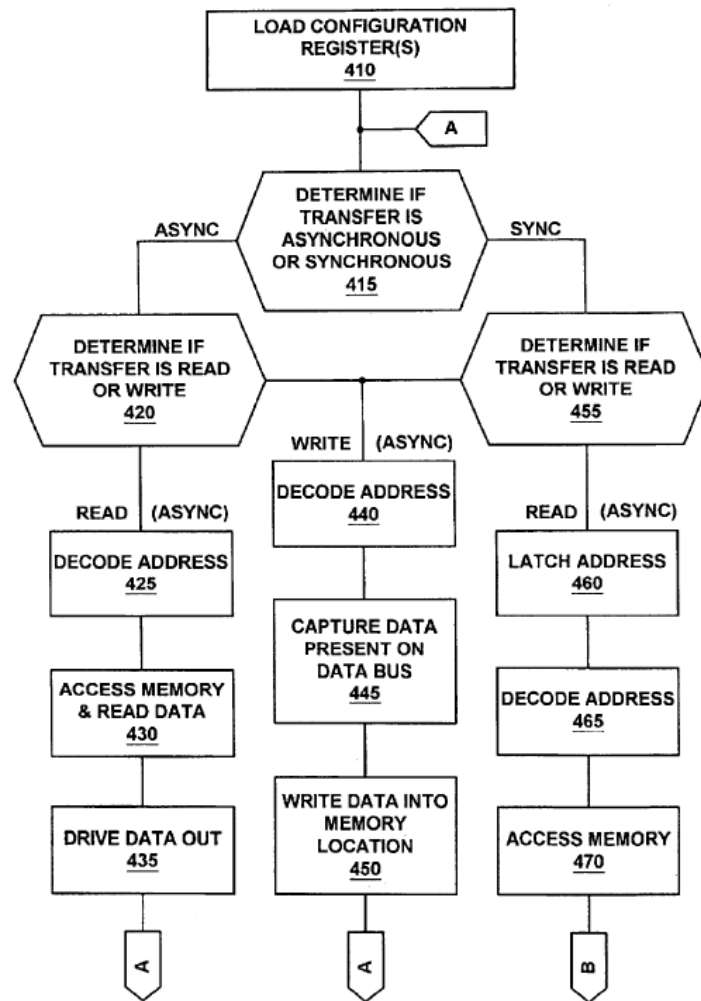


FIGURE 4A

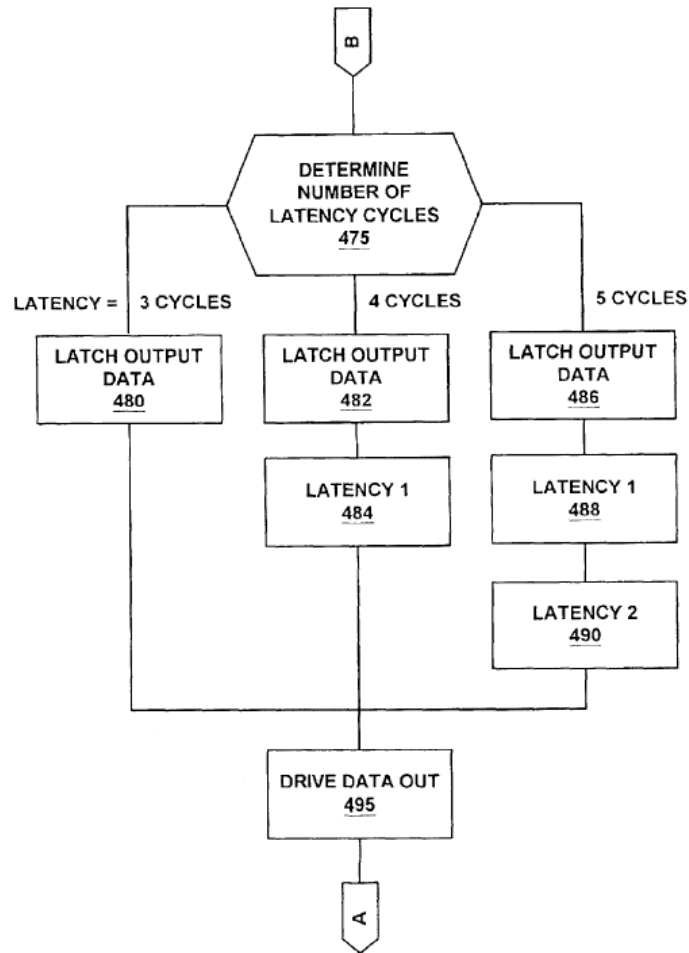


FIGURE 4B

The '898 patent explains that Figures 4A and 4B “show a flow diagram of a data transfer method utilized in a memory system.” *Id.* at 3:3–5.

First, configuration information is loaded into one or more configuration registers at step 410. *Id.* at 5:52–54. Subsequently, “[a]t step 415, an async/sync logic portion of control logic accesses the configuration register to determine whether asynchronous or synchronous transfer is chosen, in one implementation.” *Id.* at 5:60–63. “If the transfer is asynchronous, then the system determines whether it is a read or write operation, at step 420.” *Id.* at 6:1–2. Similarly, “[i]f the transfer is

synchronous, the system determines whether it is a read or write operation, at step 455.” *Id.* at 6:15–16.

Depending on the result of these determinations, the system executes various other actions (steps 425, 430, 435, 440, 445, 450, 460, 465, 470, 475, 480, 482, 484, 486, 488, 490), culminating in driving data out at step 495. *Id.* at 6:5–41. For example, in the event that the transfer is an asynchronous read transfer, “the system decodes an address present on the address bus, at step 425. At step 430, the system then accesses a memory location to read data therefrom. At step 435, the system then drives the data out on a data bus.” *Id.* at 6:5–9. In the event the transfer is a synchronous read transfer, “then the address present on the address bus is latched at step 460,” certain other steps are taken, and “[a]t step 495, the system then drives the data out.” *Id.* at 6:22–32.

E. ILLUSTRATIVE CLAIM

Of the challenged claims, claims 1, 7, and 9 are independent. Each of claims 2–6, 8, and 10–18 depends, directly or indirectly, from one of claims 1, 7, and 9. Claim 1 is illustrative and is reproduced below with certain reformatting:

1. A memory device data transfer method comprising:
determining a transfer mode between synchronous and asynchronous, wherein a configuration register specifies said transfer mode between synchronous and asynchronous;
determining whether said transfer mode is write or read; and
transferring data according to said determined mode.

Ex. 1001, 10:9–16.

F. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner challenges the patentability of claims 1–18 of the '898 patent on the following grounds (Pet. 14):

Claims Challenged	35 U.S.C. §	References
1–7, 9, 10, 13, 15, 18	102(b) ¹	Childs ²
1–10, 13, 15–18	102(b)	Shiomi ³
1–10, 13, 15–18	103	Shiomi
11, 12, 14	103	Shiomi, Stephens ⁴

In support of its challenges, Petitioner also relies on the Declaration of Farrokh Ayazi, Ph.D. Ex. 1011.

II. ANALYSIS

A. PATENT OWNER’S ARGUMENT UNDER 35 U.S.C. § 314(A) BASED ON PARALLEL PROCEEDINGS

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”); 35 U.S.C. § 314(a). In the Preliminary Response, Patent Owner contends that we should exercise our discretion to deny the Petition based on the involvement

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. Because the '898 patent has an effective filing date prior to the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102, 103.

² Lawrence F. Childs et al., U.S. Patent No. 5,384,737, issued Jan. 24, 1995 (Ex. 1008, “Childs”).

³ Toru Shiomi et al., U.S. Patent No. 5,124,589, issued June 23, 1992 (Ex. 1009, “Shiomi”).

⁴ Stephens et al., U.S. Patent No. 5,548,560, issued Aug. 20 1996 (Ex. 1010, “Stephens”).

of the '898 patent in the '188 proceeding and the '186 proceeding. Prelim. Resp. 2–5.

The Board has held that the advanced state of a parallel district court action is a factor that may weigh in favor of denying a petition under § 314(a). *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential); Patent Trial and Appeal Board, Consolidated Trial Practice Guide, 58 & n.2 (Nov. 2019) (“Trial Practice Guide”), available at <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>. We consider the following factors to assess “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding”:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). In evaluating these factors, we “take[] a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* at 6. In its arguments that we should exercise our discretion to deny institution based on parallel

proceedings, Patent Owner does not discuss any parallel proceeding other than the '186 and '188 proceedings. Prelim. Resp. 1–5. Accordingly, we focus on those proceedings when analyzing the *Fintiv* factors. Upon consideration of these factors, we decline to exercise our discretion to deny the Petition.

1. *Whether the court granted a stay or evidence exist that one may be granted if a proceeding is instituted;*

The *Fintiv* panel indicated that, in previous Board decisions, the existence of a district court stay pending Board resolution of an *inter partes* review has weighed strongly against discretionary denial, while a denial of such a stay request sometimes weighs in favor of discretionary denial. *Fintiv*, Paper 11 at 6–8.

Petitioner explains that a stay has not been instituted in the '186 and '188 proceedings. Pet. 9. Patent Owner argues that “[t]here is no stay in these Western District of Texas cases and there is no evidence that the Western District of Texas Court would grant a stay if this proceeding was instituted.” Prelim. Resp. 3.

Determining how the Texas court might handle a motion for stay that has not yet been filed invites conjecture. It would be improper to speculate, at this stage, what the Texas court might do regarding a motion to stay, given the particular circumstances of this case. Accordingly, this factor is neutral to the exercise of our discretion. *Cf. Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“In the absence of specific evidence, we will not attempt to predict how the district court in the related district court litigation will proceed because the court may determine whether or not to stay any individual case, including the related one, based

on a variety of circumstances and facts beyond our control and to which the Board is not privy.”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) (“*Fintiv II*”) (“We decline to infer, based on actions taken in different cases with different facts, how the District Court would rule should a stay be requested by the parties in the parallel case here. This factor does not weigh for or against discretionary denial in this case”).

2. *Proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision*

Petitioner states “[t]he trial date . . . is currently January 13, 2023.” Pet. 9. Petitioner posits that this makes the trial date for the ’186 and ’188 proceedings “likely to be very close in time” with the “projected statutory deadline for a final written decision, should this proceeding be instituted.” *Id.* Petitioner also asserts that “the underlying litigation is still in its early stages.” *Id.*

Patent Owner argues that “[t]he [’186 proceeding and ’188 proceeding] are set for trial on January 13, 2023.” Prelim. Resp. 3. Based on this, Patent Owner argues that “the projected statutory deadline for a final written decision would be April 1, 2023—three months *after* the trial in both [the ’186 and ’188 proceedings].” *Id.*

The parties appear to agree that a trial in the ’186 and ’188 proceedings is likely to happen before a final written decision would be due in this proceeding, although still in close proximity (approximately two months prior, assuming no delay in the Texas court’s schedule). Accordingly, this factor is neutral as to whether to exercise our discretion to deny the Petition.

3. *Investment in the parallel proceeding by the court and the parties*

The more pretrial activities that have been completed in any parallel district court proceedings, the more this factor weighs in favor of denial, and vice-a-versa. *See Fintiv*, Paper 11 at 9–10. In evaluating this factor, “[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution under *NHK*.” *Id.* at 11 (footnote omitted).

Petitioner argues that it filed the Petition promptly and the ’186 and ’188 proceedings are in early stages. Pet. 10. Petitioner explains that, at the time of the Petition, no claim construction order had issued. *Id.* Additionally, Petitioner notes that “[n]one of the parties have begun discovery in earnest, exchanged substantial volumes of documents or taken any depositions.” *Id.*

Patent Owner argues that “[t]he parties in the trial court cases are well into claim construction briefing and are set for trial in January 2023.” *Id.* The Texas court issued a claim construction order in the ’186 and ’188 proceedings. Ex. 3001. However, neither party argues that the two terms construed in that order have any bearing on the patentability issues presented in this proceeding.

Although the parties and the district court have invested some effort in the ’186 and ’188 proceedings, we find the investment at this stage relatively minor, especially considering the tasks not yet completed in the district court proceeding. Patent Owner does not dispute Petitioner’s assertion that no depositions yet have occurred. Pet. 10; Prelim. Resp. 1–5. Although some pretrial activity has been completed, much more remains, including the

deadline for amended pleadings, fact discovery, submission of expert reports, expert discovery, and a number of other pretrial activities. Ex. 3001, 4–5. Additionally, Patent Owner does not dispute Petitioner’s position that it promptly filed the Petition. Prelim. Resp. 4. On the whole, this factor weighs against exercising discretion to deny institution.

4. *Overlap between issues raised in the petition and in the parallel proceeding*

“[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *Fintiv*, Paper 11 at 12. “Conversely, if the petition includes materially different grounds, arguments, and/or evidence than those presented in the district court, this fact has tended to weigh against exercising discretion to deny institution under *NHK*.” *Id.* at 12–13.

Petitioner argues that the Petition challenges all 18 claims of the ’898 patent, whereas none of the parallel district court proceedings involve all 18 claims. Pet. 11. Petitioner notes that the ’186 and ’188 proceedings involve only claim 7. *Id.*

Patent Owner argues that the invalidity contentions in the ’186 and ’188 proceedings involve the same prior art asserted in the Petition. Prelim. Resp. 4. Patent Owner adds that “[t]he invalidity contentions [in the ’186 and ’188 proceedings] assert the specific combination of [Shiomi] with [Stephens].” *Id.*

At this stage, the ’186 and ’188 proceedings are not sufficiently advanced to determine that there will be significant overlap between the grounds of the Petition and the invalidity disputes in the Texas court. According to the Agreed Scheduling Order in the ’186 and ’188 proceedings, June 15, 2022, is the “[d]eadline for the first of two meet and

confers to discuss significantly narrowing the . . . prior art references at issue.” Additionally, as Petitioner notes, the ’186 and ’188 proceedings involve only one of the 18 claims challenged in the Petition. Accordingly, we find this factor neutral with respect to whether to exercise discretion to deny institution.

5. *Whether the petitioner and the defendant in the parallel proceeding are the same party*

“If a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution under *NHK*.” *Fintiv*, Paper 11 at 13–14. Petitioner argues that it is not a defendant in any of the district court proceedings. Pet. 12. In view of Petitioner’s statement that the defendants in the ’186 and ’188 proceedings “may be real-parties-in-interest” (Pet. 1), Patent Owner contends that “has essentially admitted that Petitioner filed this Petition on behalf of these parties due to their relationship” (Prelim. Resp. 4–5).

Because Petitioner has identified the defendants as potential real-parties-in-interest, this factor is neutral.

6. *Other circumstances that impact the Board’s exercise of discretion, including the merits*

Regarding this factor, Petitioner argues that “the merits of this Petition are particularly strong.” Pet. 13. Patent Owner does not address this factor specifically, nor does Patent Owner address the merits of the Petition at this stage of the proceeding. *See, generally*, Prelim. Resp. As explained in detail below in Sections II.C–F, Petitioner’s presently undisputed assertions that claims 1–18 of the ’898 patent are unpatentable are reasonably strong, at least at this stage of the proceeding. Thus, this factor favors institution. *See Sand Revolution*, Paper 24 at 13 (PTAB June 16, 2020) (informative) (“We

determine, on this preliminary record, that Petitioner has set forth a reasonably strong case for the obviousness of most challenged claims. Thus, this factor weighs in favor of not exercising discretion to deny under 35 U.S.C. § 314(a).”); *compare with Fintiv II*, Paper 15 at 17 (PTAB May 13, 2020) (informative) (“It is sufficient that Patent Owner has pointed out that Petitioner’s case, at least as to two of three independent claims, is a close call. . . . The merits, taken as a whole, do not tip the balance in favor of Petitioner and instead also weigh in favor [of] discretionary denial in a balanced assessment of all the circumstances.”).

7. *Holistic Assessment of Fintiv Factors*

We consider the above factors and take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. For the foregoing reasons, we decline to deny institution under § 314(a).

B. CLAIM CONSTRUCTION

We construe a claim

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

Petitioner contends that no need presently exists to construe any claim language expressly. Pet. 14. Patent Owner does not state a position on claim construction, and does not propose any constructions. *See, generally*, Prelim. Resp.

We note that, after the parties filed the Petition and the Preliminary Response, the Texas court conducting the '186 and '188 proceedings construed certain terms of independent claim 7. Ex. 3004. The Texas court construed claim 7's recitation of "asynchronous/synchronous logic" as meaning "logic controlling asynchronous or synchronous data transfer operations." *Id.* at 2. The Texas court construed claim 7's recitation of a "configuration register" as meaning "register storing configuration information." *Id.* Neither party asks us to adopt those constructions here.

At this stage, Patent Owner does not dispute Petitioner's assertions that the challenged claims are unpatentable over the asserted prior art. As explained below in Sections II.C, II.D, and II.F, we find that Petitioner's arguments and evidence demonstrate a reasonable likelihood of establishing that the challenged claims are unpatentable. Cognizant of the Texas court's claim constructions and the present record as a whole, we currently do not discern any claim-construction issue affecting Petitioner's demonstration of a reasonable likelihood of prevailing. Thus, at this stage, we do not find it necessary to evaluate expressly the Texas court's claim constructions or to construe expressly any language of the challenged claims. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that "we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

C. ALLEGED ANTICIPATION BY CHILDS

1. Overview of Childs

Childs' invention generally relates to integrated circuit memories and more specifically to a pipelined memory with asynchronous and synchronous operating modes. Ex. 1008, 1:31–33. Childs discusses an embodiment in connection with Figure 1, which is reproduced below.

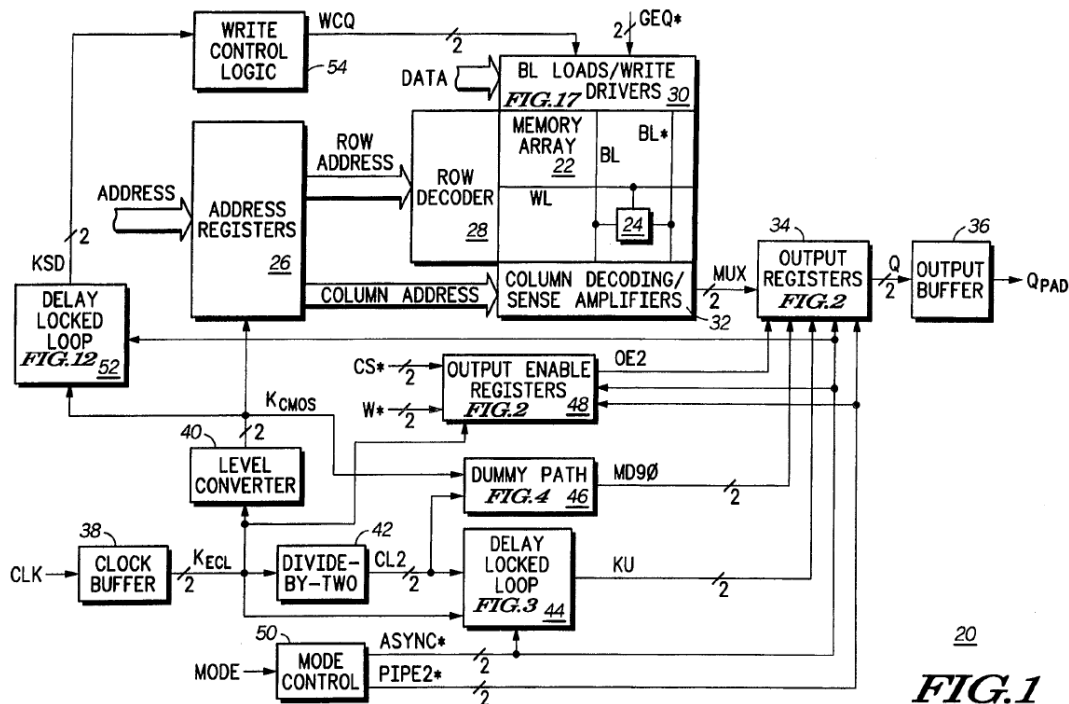


Figure 1 shows memory 20 in a block diagram. *Id.* at 2:30–31. Childs explains that

[m]emory 20 includes memory array 22, bit line loads/write drivers 30, address registers 26, row decoders 28, column decoding sense amplifiers 32, output registers 34, output buffer 36, clock buffer 38, level converter 40, divide-by-two circuit 42, read control delay locked loop circuit 44, dummy path 46, output enable registers 48, write control delay locked loop circuit 52, and write control logic 54.

Id. at 3:15–23. Memory array 22 has multiple memory cells, each connected to “a word line pair and a bit line pair.” *Id.* at 3:24–26.

Childs discloses that various components of memory 20 receive certain inputs and respond with actions or outputs. For example, “[a]ddress registers 26 receive ECL level address signals labeled ‘ADDRESS’, and provide row address signals labeled ‘ROW ADDRESS’ to row decoders 28, and column address signals labeled ‘COLUMN ADDRESS’ to column decoding/sense amplifiers 32.” *Id.* at 3:43–47. Additionally, “[c]lock buffer 38 receives an external ECL clock signal labeled ‘CLK’, and provides a buffered clock signal labeled ‘K_{ECL}’.” *Id.* at 3:59–61. Other components of memory 20 provide and receive certain other signals, including other clock signals. *Id.* at 3:61–4:26. For example, “[o]utput enable registers 48 receives clock signal K_{ECL}, a chip select signal labeled ‘CS*’, a write enable signal labeled ‘W*’, mode control signal ASYNC*, a pipelining control signal labeled ‘PIPE2*’, and in response, provides an output enable signal labeled ‘OE2.’” *Id.* at 4:9–14. Additionally, “[m]ode control circuit 50 receives an external mode control signal labeled ‘MODE’, and in response, provides mode control signal ASYNC* and pipeline control signal PIPE2*.” *Id.* at 4:20–23.

Childs explains that “an asterisk ‘*’ after a signal name indicates that the signal is a logical complement of a signal having the same name but lacking an asterisk ‘*’.” *Id.* at 3:31–34. Childs elaborates that “[i]f the logically true state of a signal is a digital logic level one, the logically complement state is a digital logic level zero. And if the logically true state of a signal is a digital logic level zero, the logically complement state is a digital logic level one.” *Id.* at 3:34–38.

Childs discloses a read cycle of memory 20. *E.g., id.* at 4:27–5:5. In a read cycle, to choose a column and word line, column decoding/sense

amplifiers 32 receive “address signals COLUMN ADDRESS,” and row decoders 28 receive “address signals ROW ADDRESS.” *Id.* at 4:27–31. “Memory cells located on the enabled word line provide data to their respective bit line pairs. A data signal labeled ‘MUX’, corresponding to data provided by a bit line pair, is provided by column decoding/sense amplifiers 32.” *Id.* at 4:31–35. Output registers 34 receive data signal MUX and “provide a data signal labeled ‘Q’ to output buffer 36.” *Id.* at 4:35–40. Subsequently, output buffer 36 “provides an output data signal labeled ‘Q_{PAD}’ to an output pad (not shown).” *Id.* at 4:40–42.

Childs also discloses that “[d]uring a write cycle, the flow of data is essentially reversed.” *Id.* at 4:49–50. Childs elaborates that

[a]s in the read cycle, memory cells located on an enabled word line provide data to bit line pairs. However, a voltage differential driven onto the bit line pairs by bit line loads/write drivers 30 is greater than the drive voltage of the memory cell and overwrites a stored bit in the memory cell.

Id. at 4:58–63. Childs’ Figure 2 is reproduced below.

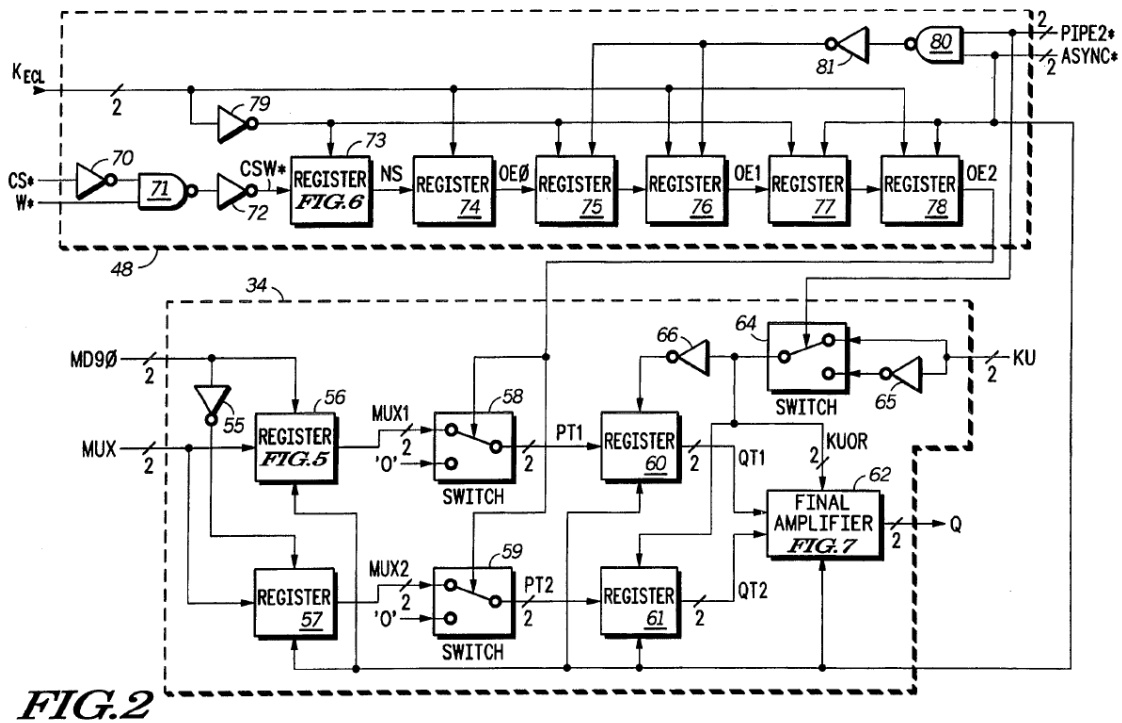


Figure 2 “illustrates in partial block diagram form and partial logic diagram form, output registers 34 and output enable registers 48.” *Id.* at 5:6–8.

Childs explains that “[o]utput registers 34 includes registers 56, 57, 60, and 61, switches 58, 59, and 64, and inverters 55, 65, and 66.” *Id.* at 5:8–10. Childs elaborates that “[o]utput registers 34 have two parallel, interleaved, output data paths. One output data path is through register 56, switch 58, and register 60 to final amplifier 62. The other data path is through register 57, switch 59 and register 61 to final amplifier 62.” *Id.* at 6:36–40. Operation of the parallel data paths includes sending data signal MUX “through register 56 as data signal MUX1” and “through register 57 as data signal MUX2.” *Id.* at 8:44–51. “During a read cycle, output enable signal OE2 is a logic high, so that data signals MUX1 and MUX2 will be provided to registers 60 and 61, respectively.” *Id.* at 7:3–6.

Childs discloses multiple ways of passing data through output registers 34. In one of the disclosed ways,

[d]elayed clock signal KU controls the operation of registers 60 and 61. When pipelining control signal PIPE2* is a logic high, clock signal KUOR is the same logic state as delayed clock signal KU. When clock signal KUOR is a logic low, data signal PT1 is sent through register 60 to become corresponding data signal QT1, while data signal QT2 is latched by register 61. Also, while clock signal KUOR is a logic low, data signal QT2 is provided as output data signal Q by final amplifier 62. While clock signal KUOR is a logic high, data signal PT2 is sent through register 61 to become corresponding data signal QT2, while data signal QT1 is latched by register 60. Also, data signal QT1 is provided as output data signal Q through final amplifier 62.

Id. at 7:17–31. Setting forth another way of passing data through output registers 34, Childs discloses that

In the asynchronous mode, output data is generated directly from clock signal CLK. Clock signals MD90 and KU, are ignored. The asynchronous mode is accomplished by adding a flow through mode to output register 34. Registers 56, 57, 60, and 61 and final amplifier 62 receive mode control signal ASYNC* to provide the flow through mode. When mode control signal ASYNC* is a logic low, data passes through output registers 34 regardless of the state of the clock signals. Mode control signal ASYNC* is also used to provided a flow through mode for output enable registers 48. When mode control signal ASYNC* is a logic low, registers 75, 76, 77, and 78 are in flow through mode. An advantage of this method of mode control is that it is accomplished electrically, allowing memory 20 to operate in either mode by changing the logic state of an external input signal, instead of by changing a metal layer, or some other manufacturing change.

Id. at 8:28–45. As Childs' Abstract explains, “pipelined memory (20) has a synchronous operating mode and an asynchronous operating mode. The memory (20) includes output registers (34) and output enable registers (48)

which are used to electrically switch between the asynchronous operating mode and the synchronous operating mode.” *Id.* at code [57].

2. *Discussion*

Asserting anticipation of claims 1–7, 9, 10, 13, 15, and 18 by Childs, Petitioner cites disclosures of Childs as allegedly disclosing each of these claims’ limitations. Pet. 15–31. At this stage, Patent Owner does not dispute Petitioner’s position that Childs anticipates claims 1–7, 9, 10, 13, 15, and 18. *See, generally*, Prelim. Resp.

We turn now to a detailed discussion of Petitioner’s arguments that Childs anticipates claim 1. We consider the Petition’s arguments about each recitation of claim 1 in sequence.

a) *Claim 1*

(1) *Preamble—“A memory device data transfer method”*

Addressing the preamble, Petitioner cites Childs’ title: “Pipelined Memory Having Synchronous and Asynchronous Operating Modes.” Ex. 1008, code [54]. To the extent claim 1’s preamble is limiting, we find Petitioner has shown sufficiently that Childs discloses the preamble.

(2) *“determining a transfer mode between synchronous and asynchronous, wherein a configuration register specifies said transfer mode between synchronous and asynchronous”*

Petitioner argues that “Childs discloses a memory device that determines whether to transfer data synchronously or asynchronously through signals stored in a configuration register.” Pet. 16 (citing Ex. 1008, code [57]). Petitioner cites Childs’ disclosure of output registers 34, output enable registers 48, and those registers’ subcomponents and operation. *Id.* at 16–19. Petitioner contends that Childs discloses both asynchronous and

synchronous data transfer via output registers 34. *Id.* at 19. Petitioner argues that “Childs discloses that differential mode control signals ASYNC/ASYNC* determine the operation of output register 56—which is a register within output registers 34—and controls whether data is transmitted synchronously or asynchronously.” *Id.* at 17.

At this stage, we find Petitioner has shown sufficiently that Childs discloses claim 1’s recitation of “determining a transfer mode between synchronous and asynchronous, wherein a configuration register specifies said transfer mode between synchronous and asynchronous.”

(3) *“determining whether said transfer mode is write or read”*

Petitioner argues that “Childs discloses determining whether the transfer mode is a read or write mode.” Pet. 19. Petitioner cites Childs disclosure of various signals with output registers 34 and output enable registers 48. *Id.* at 19–20. For example, Petitioner contends that “[t]hrough the state of the write enable signal (W*) and output enable signal (OE2), Childs determines whether the transfer is a read or write operation.” *Id.* at 20.

At this stage, we find Petitioner has shown sufficiently that Childs discloses claim 1’s recitation of “determining whether said transfer mode is write or read.”

(4) *“transferring data according to said determined mode”*

Addressing this claim language, the Petition contends that

Childs discloses transferring data according to said determined mode. For example, Childs describes a synchronous read cycle at Col. 4:27–48 (“during a read cycle of memory 20. . .”), and a synchronous write cycle at Col. 4:49–Col. 5:5 (“during a write

cycle...”). Further, an example of transferring data according to the asynchronous mode is described at Col. 8:28–45 (“In the asynchronous mode. . .”). In both synchronous and asynchronous modes, data is transferred as data signal Q from output register 34. See Ex. 1008 (Childs) at Col. 4:15–19; Ex. 1011 (Ayazi Decl.) at ¶¶ 107.

Id. at 20.

At this stage, we find Petitioner has shown sufficiently that Childs discloses claim 1’s recitation of “transferring data according to said determined mode.”

(5) *Summary for Claim 1*

At this stage, we find Petitioner’s arguments and evidence regarding each of the limitations of independent claim 1 sufficient to demonstrate a reasonable likelihood of establishing that Childs anticipates claim 1.

b) *Claims 2–7, 9, 10, 13, 15, and 18*

As with independent claim 1, Petitioner addresses each limitation of claims 2–7, 9, 10, 13, 15, and 18, arguing that Childs discloses all of these claims’ limitations. Pet. 20–31. Based on the present record, we find Petitioner’s arguments and evidence regarding the limitations of claims 2–7, 9, 10, 13, 15, and 18 sufficient to demonstrate a reasonable likelihood of establishing that Childs anticipates these claims.

D. ALLEGED ANTICIPATION BY SHIOMI

1. *Overview of Shiomi*

Shiomi notes that “[v]arious types of memories have been developed and put into practice using semiconductor circuit integration techniques.” Ex. 1009 1:21–23. Shiomi’s Figure 1 is reproduced below.

FIG.1 PRIOR ART

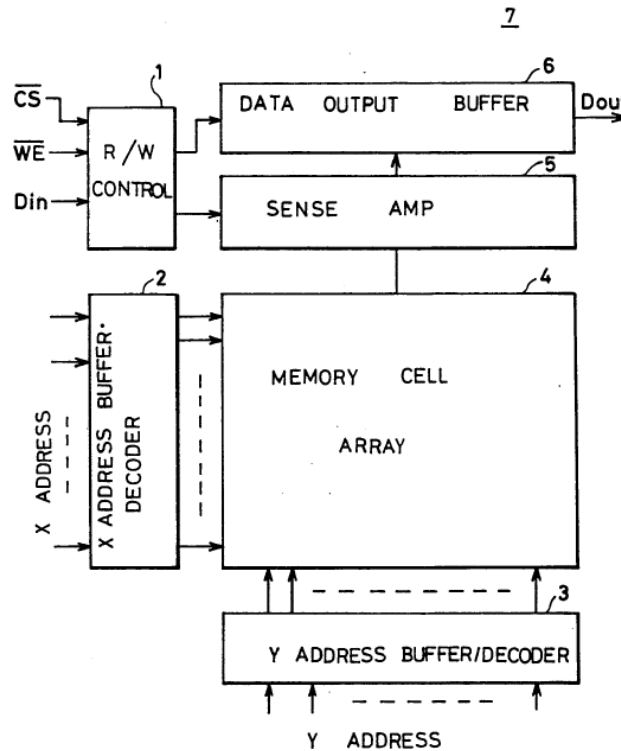


Figure 1 “is a diagram schematically showing an overall arrangement of a conventional semiconductor memory.” *Id.* at 1:33–35.

Specifically, Figure 1 shows semiconductor memory 7, which includes R/W control circuit 1, X address buffer decoder 2, Y address buffer decoder 3, memory cell array 4, sense amplifier 5, and data output buffer 6. *Id.* at 1:35–38, 1:44–46, 1:56–58. X address buffer decoder 2 and Y address buffer decoder 3 allow choosing a memory cell from memory cell array 4. *Id.* at 1:44–46.

R/W control circuit 1, sense amplifier 5, and data output buffer 6 interact with one another in connection with reading data from and writing data to memory cell array 4. *Id.* at 1:56–2:53. R/W control circuit 1 receives chip-select signal $\overline{CS}$, write enable signal $\overline{WE}$ and input data D_{in} .

Id. at 1:58–60. These signals affect operations of semiconductor memory 7.

Id. at 1:58–2:36. The state of chip-select signal $\overline{CS}$ affects whether “writing and reading of data are inhibited.” *Id.* at 2:7–10. The state of write-enable signal $\overline{WE}$ affects whether “a data-read mode is designated” or “a data-write mode is designated.” *Id.* at 2:22–23, 2:32–33.

Shiomi discloses that a memory like semiconductor memory 7

is frequently used in combination with a logic circuit. In such case, to achieve high-speed and accurate data inputting and outputting, it is preferred to synchronize the logical operation of the logic circuit with write/read operation in the semiconductor memory. In consideration of such situation, a synchronous RAM, i.e., a self-timed RAM (hereinafter briefly called “STRAM”), in which input and output of signals are controlled according to a clock signal used as a synchronizing signal is developed.

Id. at 2:54–64. Shiomi shows an example of a STRAM in Figure 2.

Id. at 2:65–66. Figure 2 is reproduced below.

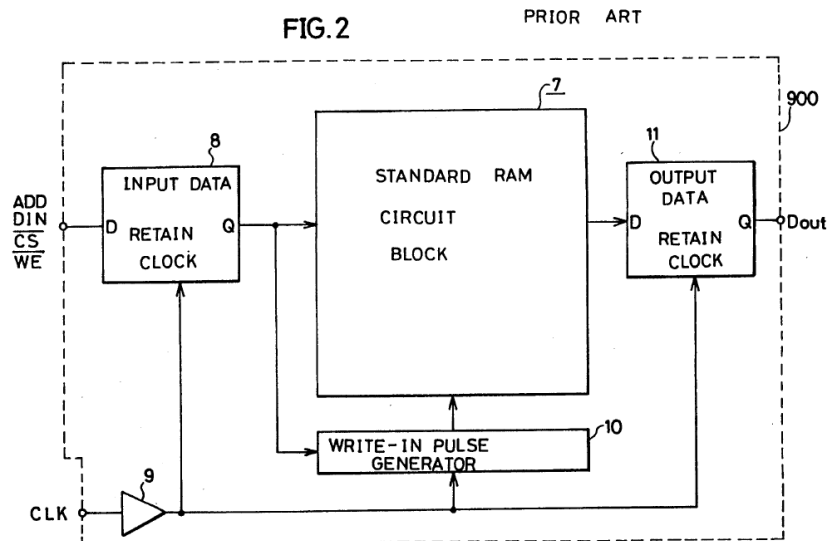


Figure 2 is a block diagram “showing a conceptual structure of a STRAM.”

Id. at 2:65–66, 13:5–6.

The STRAM shown in Figure 2 is integrated on chip 900. *Id.* at 2:66–67. Chip 900 “includes a standard RAM circuit block 7 having the same structure as that of the RAM shown in [Figure] 1.” *Id.* at 2:66–3:1. Additionally, chip 900 includes “an input data retaining circuit 8, a clock signal generator 9, a write pulse generating circuit 10 and an output data retaining circuit 11, for performing data inputting to and data outputting from the standard RAM circuit block 7.” *Id.* at 2:66–3:6. Shiomi explains that

[t]he clock generator 9 buffers an externally supplied clock signal . . . CLK and generates an internal clock signal.

The input data retaining circuit 8 receives the clock signal from the clock generator 9 at its clock input CLOCK, latches input signals (address ADD, input data Din, chip-select signal $\overline{CS}$, and write-enable signal $\overline{WE}$) supplied to its input terminal D, and outputs these signals from its output terminal Q in response to the clock signal.

The write pulse generating circuit 10 generates a write pulse for controlling data writing in response to the internal clock signal from the clock generator 9 and the internal control signals (generated in response to the signals $\overline{CS}$ and $\overline{WE}$) from the input data retaining circuit 8. The write pulse is a pulse signal having the pulse width corresponding to the period that the write-enable signal overline is held in an activation state in the RAM shown in Figure 1.

The output data retaining circuit 11 receives the internal clock signal from the clock generator 9 at its clock input CLOCK, latches the data from the standard RAM circuit block 7 received at its input terminal D and outputs the output data Dout from its output terminal Q in response to the internal clock signal.

The STRAM shown in [Figure] 2 differs from the standard RAM shown in [Figure] 1 in that its write operation is not started by the signals $\overline{CS}$ and $\overline{WE}$, but started by the clock signal

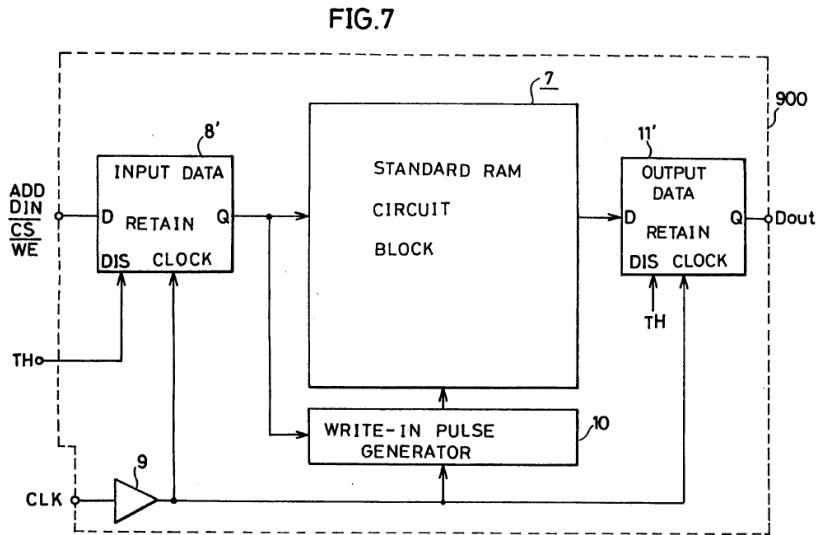
CLK and that the write pulse is generated by the write pulse generating circuit 10 within the chip 900.

Id. at 3:7–37.

Shiomi expresses concern about “problems aris[ing] not only in STRAMs but also in general synchronous semiconductor circuits having input/output circuits and internal functional circuits with each of such circuits operating in synchronization with a clock signal.” *Id.* at 11:57–61. In view of this, Shiomi sets forth certain objects of its invention, disclosing that

[t]he semiconductor integrated circuit according to the present invention comprises an input data retaining circuit responsive to a clock signal for latching and outputting externally applied input signals, internal functional circuitry responsive to the signals transmitted from the input data retaining circuit for performing a predetermined functional operation, an output data retaining circuit responsive to the clock signal for latching and outputting the data output from the internal functional circuitry, and functional setting circuit means response to a functional mode specifying signal for disabling the latch function of the input data retaining circuit and the output data retaining circuit, thereby setting both the retaining circuits in the through state where each retaining circuit allows supplied signals to pass therethrough regardless of the state of the clock signal.

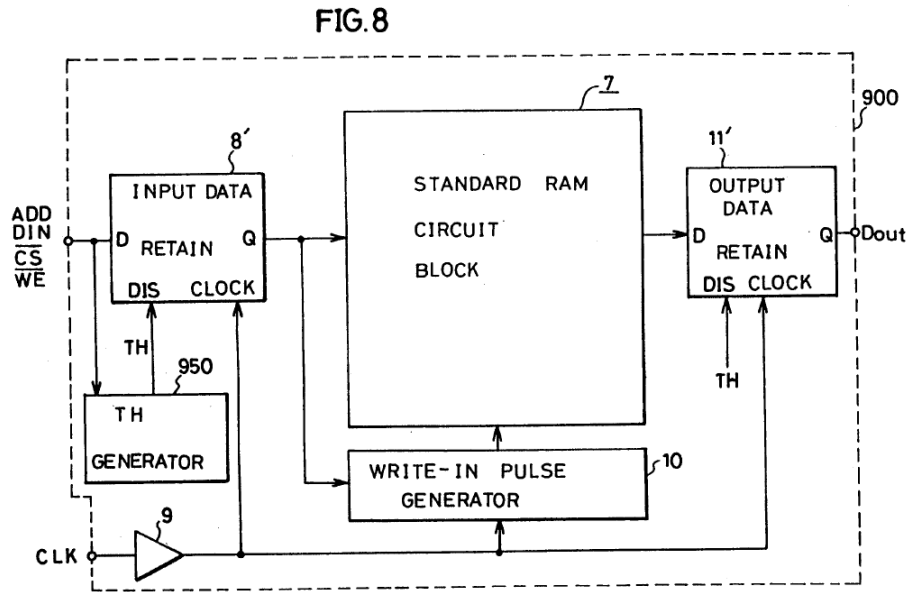
Id. at 12:30–46. Shiomi discusses an example in connection with Figure 7. Figure 7 is reproduced below.



Shiomi explains that Figure 7 “is a block diagram representing schematically a structure of a semiconductor integrated circuit according to an embodiment of the present invention.” *Id.* at 13:59–60. In the embodiment of Figure 7,

input data retain circuit 8' and output data retain circuit 11' each receive at its disable input DIS an externally applied control signal (through signal) TH. When the through signal TH is made active or at a higher level than the clock signal (CLKB, NCLKB) at the input CLOCK the latching function of the data retain circuits 8 and 11" is disabled regardless of the application of the clock signal CLK. That is, the data retain circuits 8' and 11' are set in the through state.

Id. at 13:62–14:2. Shiomi discusses another example in connection with Figure 8, which is reproduced below.



Shiomi states that Figure 8 shows “another schematic representation of the semiconductor integrated circuit according to the present invention.”

Id. at 14:3–5. According to Shiomi, in the example shown in Figure 8, the through signal TH is generated by a built-in TH generator 950. The TH generator 950 is activated when an external pin terminal such as $\overline{CS}$ pin, $\overline{WE}$ pin is set at a potential level different from a normal “H” or “Low” level, to generate a through signal TH for disabling the latching function of the data retaining circuits 8' and 11".

In the structures shown in FIGS. 7 and 8, when the through signal TH is generated to be active, the semiconductor integrated circuit 900 operates as a standard RAM, or as asynchronous type circuit when the through signal TH is not generated and is set inactive, the data retain circuits 8' and 11" have their latching functions enabled, so that the integrated circuit 900 operates as an STRAM, or operates as a clock-synchronized type device.

Id. at 14:5–21.

2. Discussion

Asserting anticipation of claims 1–10, 13, and 18 by Shiomi, Petitioner cites disclosures of Shiomi as allegedly disclosing each of these

claims' limitations. Pet. 31–57. At this stage, Patent Owner does not dispute Petitioner's position that Shiomi anticipates claims 1–10, 13, and 18. *See, generally*, Prelim. Resp.

We turn now to a detailed discussion of Petitioner's argument that Shiomi anticipates claim 1. We consider the Petition's arguments about each recitation of claim 1 in sequence.

a) *Claim 1*

(1) *Preamble—“A memory device data transfer method”*

Addressing the preamble, Petitioner cites Shiomi's disclosure in the Abstract of “[a] self-timed random-access memory device.” Ex. 1009, code [57]; Pet. 38. To the extent claim 1's preamble is limiting, we find Petitioner has shown sufficiently that Shiomi discloses the preamble.

(2) *“determining a transfer mode between synchronous and asynchronous, wherein a configuration register specifies said transfer mode between synchronous and asynchronous”*

In support of its assertion that Shiomi discloses this limitation, Petitioner cites Shiomi's disclosures regarding using various components with the “through state specifying signal” to switch the memory device “between a mode operating synchronously with the externally supplied clock signal and another mode operating asynchronously with the externally supplied clock signal.” Ex. 1009, code [57]; Pet. 38–39 (citing Ex. 1009 code [57], 13:62–14:2, 14:13–21, 14:42–48, 14:58–64; Ex. 1011 ¶¶ 156–158). Specifically, Petitioner argues that input data retaining circuit 8' (shown in Figure 7) is a configuration register that receives through state specifying signal TH, which specifies whether transfer of data into RAM circuit block 7 is synchronous or asynchronous. *Id.*

At this stage, we find Petitioner has shown sufficiently that Shiomi discloses claims 1's recitation of "determining a transfer mode between synchronous and asynchronous, wherein a configuration register specifies said transfer mode between synchronous and asynchronous."

(3) *"determining whether said transfer mode is write or read"*

In support of its position that Shiomi teaches this limitation, Petitioner cites certain disclosures of Shiomi related to "write-enable signal WE." Pet. 39–40. For example, Petitioner cites Shiomi's disclosure that "[w]hen write-enable signal $\overline{WE}$ is at 'H' level, a data-read mode is designated." Ex. 1009, 2:22–23; Pet. 39. Additionally, Petitioner cites Shiomi's disclosure that "[w]hen the write-enable signal $\overline{WE}$ is at 'H' level, a data-read mode is designated." Ex. 1009, 2:32–33; Pet. 39. Petitioner also argues that "[t]he write-enable signal is similarly received and latched by the input data retaining circuit 8' and the state of the signal determines whether the data transfer mode is read or write." Pet. 39–40 (citing Ex. 1009, 3:10–16, 12:30–46, 14:3–21; Ex. 1011 ¶ 159).

At this stage, we find Petitioner has shown sufficiently that Shiomi discloses claim 1's recitation of "determining whether said transfer mode is read or write."

(4) *"transferring data according to said determined mode"*

Addressing this claim limitation, Petitioner argues that

Shiomi discloses transferring data according to said determined mode. For example, Shiomi describes a synchronous data-read operation at Col. 5:5 – Col. 6:4, and a synchronous data-write operation at Col. 3:66 – Col. 4:55. Further, an example of transferring data according to the asynchronous mode is

described at Col. 13:62 to Col. 14:21. Accordingly, this limitation is disclosed by Shiomi.

Pet. 40 (citing Ex. 1011 ¶¶ 160).

(5) *Summary for Claim 1*

At this stage, we find Petitioner's arguments and evidence regarding each of the limitations of independent claim 1 sufficient to demonstrate a reasonable likelihood of establishing that Shiomi anticipates claim 1.

b) *Claims 2–10, 13, and 15–18*

As with independent claim 1, Petitioner addresses each limitation of claims 2–10, 13, and 15–18, arguing that Shiomi discloses all of these claims' limitations. Pet. 40–57. Based on the present record, we find Petitioner's arguments and evidence regarding each of the limitations of claims 2–10, 13, and 15–18 sufficient to demonstrate a reasonable likelihood of establishing that Shiomi anticipates these claims.

E. ALLEGED OBVIOUSNESS OVER SHIOMI

In support of its assertion that claims 1–10, 13, and 15–18 would have been obvious over Shiomi, Petitioner asserts that

[t]o the extent it is determined that any limitation is not expressly disclosed, such limitation would have been obvious to a person of ordinary skill in the art in view of Shiomi. See Ex. 1011 (Ayazi Decl.) at ¶¶ 209-215.

For example, Shiomi disclose a plurality of registers that receive control signals that dictate the particular data transfer mode that the memory circuit will employ, namely, synchronous or asynchronous and read or write. Further, when operating in synchronous mode, control signals such as the chip select and write enable signals, among other control signals, are latched. And when operating in asynchronous mode, the TH signal is maintained, and the latching operations of the registers is disabled. A person of ordinary skill in the art would have found the relevant claims of the '898 Patent identified above to have

been obvious given the detailed disclosure of Shiomi. See Ex. 1011 (Ayazi Decl.) at ¶¶ 209-215.

Pet. 58.

As discussed above in Section II.D, we find Petitioner has demonstrated a reasonable likelihood of establishing that Shiomi anticipates claims 1–10, 13, and 15–18. To the extent Petitioner may not show that Shiomi anticipates claims 1–10, 13, and 15–18, Petitioner’s vague, conclusory arguments in support of obviousness of claims 1–10, 13, and 15–18 over Shiomi are unavailing.

To allow us to assess properly the merits of Petitioner’s challenges, the Petition must explain clearly its bases for asserting unpatentability of the challenged claims. A proper petition “identifies, in writing and with particularity, each claim challenged, the grounds on which the challenge to each claims is based, and the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a). We require that a petition include “[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.” 37 C.F.R. § 42.22(a)(2). We also require that a petition “specify where each of the elements of the claim is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4).

Petitioner’s challenge of claims 1–10, 13, and 15–18 as allegedly obvious over Shiomi fails to meet these requirements. The Petition neither identifies any difference between the teachings of Shiomi and the challenged claims, nor identifies any specific allegedly obvious modification of Shiomi’s teachings. Thus, Petitioner’s presentation of its challenge of claims 1–10, 13, and 15–18 as allegedly obvious over Shiomi stymies a

proper obviousness analysis, which requires ascertaining the “differences between the prior art and the claims at issue.” *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

Nevertheless, because we institute a trial on other grounds, we institute a trial on this ground as well. See 37 C.F.R. § 42.108(a) (“When instituting inter partes review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). See also *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

F. ALLEGED OBVIOUSNESS OVER SHIOMI AND STEPHENS

Petitioner argues that claims 11, 12, and 14 would have been obvious over Shiomi and Stephens. Pet. 58–63. Each of claims 11, 12, and 14 depends from either claim 10 or claim 13, both of which depend from independent claim 9. Ex. 1001, 11:20–21, 11:24–25, 12:1–2, 12:4–5, 12:7–8. Claim 11 recites “wherein said reading data asynchronously comprises reading a plurality of words.” *Id.* at 11:25–26. Claim 12 recites “wherein said writing data asynchronously comprises writing a plurality of words.” *Id.* at 12:2–3. Claim 14 recites “wherein said reading data synchronously comprises reading a burst of words.” *Id.* at 12:8–9.

Noting its position that Shiomi anticipates or renders obvious claims 9, 10, and 13, Petitioner concedes that “Shiomi, however, does not expressly disclose reading or writing in a burst mode, or where the reading or writing operation is able to read or write multiple memory addresses when receiving address information.” Pet. 59. Addressing this difference between claims 11, 12, and 14, Petitioner cites Stephens, alleging that it discloses “a burst mode random access memory (SRAM) that provides for

synchronous and asynchronous data transfer.” *Id.* Petitioner argues that it would have been obvious to modify Shiomi’s memory device with Stephens’ teachings. *Id.* at 59–61. Petitioner asserts that a person of ordinary skill in the art would have been motivated to do so for certain reasons. *Id.* For example, Petitioner argues that “[a]dding the burst mode operation would have furthered Shiomi’s objective of improving the operating method of synchronous semiconductor integrated circuits and providing high-speed data read and write operations.” *Id.* at 60–61.

Based on the present record, we find Petitioner has demonstrated a reasonable likelihood of establishing that claims 11, 12, and 14 would have been obvious over Shiomi and Stephens.

III. CONCLUSION

For the foregoing reasons, we institute an *inter partes* review of all challenged claims under all grounds set forth in the Petition.

Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

IV. ORDER

For the reasons given, it is:

ORDERED that *inter partes* review is instituted on all challenged claims under all challenged grounds; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the ’898 patent is hereby instituted commencing on the

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entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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