

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CHONGQING HKC OPTOELECTRONICS
TECHNOLOGY CO., LTD.,

Petitioner,

v.

VIDA SENSE INNOVATION LTD.,

Patent Owner.

IPR2022-00109

Patent 7,433,202 B2

Before JO-ANNE M. KOKOSKI, NATHAN A. ENGELS, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

KOKOSKI, *Administrative Patent Judge*.

DECISION

Granting Institution of *Inter Partes* Review

35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Chongqing HKC Optoelectronics Technology Co., Ltd. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–14 (“the challenged claims”) of U.S. Patent No. 7,433,202 B2 (“the ’202 patent,” Ex. 1001). Paper 1. Vida Sense Innovation Ltd. (“Patent Owner”) did not file a Preliminary Response.

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2021). Upon consideration of the Petition and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’202 patent. Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 1–14 of the ’202 patent.

A. *Real Parties-in-Interest*

Petitioner identifies HKC Corporation Limited, HKC Overseas Limited, and Chongqing HKC Optoelectronics Technology Co. as the real parties-in-interest. Pet. 83; Paper 6, 1. Patent Owner identifies itself as the real party-in-interest. Paper 3, 1.

B. *Related Matters*

The parties indicate that the ’202 patent is asserted in *Vida Sense Innovation Ltd. v. HKC Corporation Ltd.*, Case No. 1:20-cv-10825 (S.D.N.Y.). Pet. 83; Paper 3, 1.

C. *The ’202 Patent*

The ’202 patent, titled “Electronic Device and Method of Manufacture Thereof,” relates to an electronic device comprising a body of electrically

insulating material and an electrical component. Ex. 1001, code (54), 1:4–6. The '202 patent explains that in such electronic devices, the choice of materials for the body is limited when an electrical component is included therein. *Id.* at 1:29–30. In particular, “[t]hermoplastic materials do not always adhere sufficiently to embedded components and/or the conductors,” which “may result in delamination of the conductors from the body.” *Id.* at 1:31–34. To prevent this problem, the '202 patent describes placing the electric component in a through-hole or cavity in the body. *Id.* at 1:40–42. The electric component is fixed in the through-hole using an attachment layer that is mechanically and/or chemically fixed to the body. *Id.* at 1:42–46, 1:53–56. A pattern of electrical conductors is provided on the attachment layer “for electrically coupling the component to other components and/or contact means for external coupling.” *Id.* at 1:43–46. At least one of the electrical conductors “extends into the body and is connected to a further conductor embedded in the body and is at least partially exposed to a surface of the body.” *Id.* at 1:46–49. In this way, the electrical component “is kept outside the body of electrically insulating material, but is not outside the shape of the body.” *Id.* at 1:50–52.

Figures 5 and 6 of the '202 patent are reproduced below.

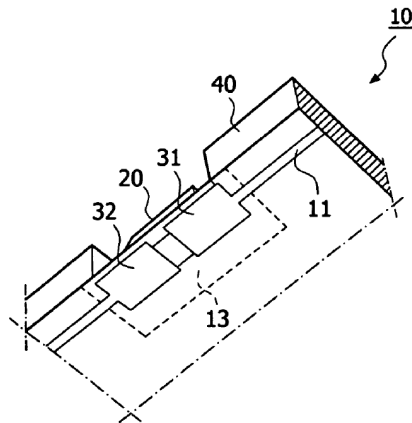


Fig.5

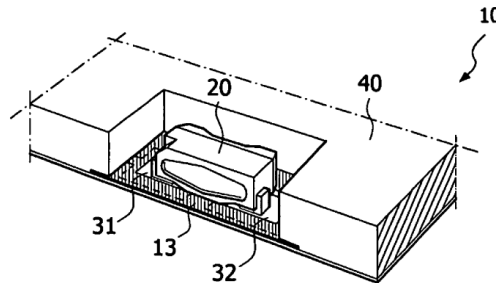


Fig.6

Figures 5 and 6 show “a bird’s eye view” of the device described in the '202 patent from different directions. Ex. 1001, 1:3–4. Device 10 includes attachment layer 13, component 20, electrical conductors 11, bond pads 31 and 32, and body 40. *Id.* at 6:27–35, 6:46–50. In the device depicted in Figures 5 and 6, component 20 is a light-emitting diode. *Id.* at 6:35–36. Body 40 comprises electrically insulating material, such as epoxy. *Id.* at 6:43–45. Component 20 is “kept in a mechanically stable manner through the presence of attachment layer 13 that is partially over molded and thus well maintained in the body 40.” *Id.* at 6:47–50. Conductors 11 are “present at the surface of the body, and may be include further contact pads for coupling to external components or an external board.” *Id.* at 6:50–53.

D. Illustrative Claim

Petitioner challenges claims 1–14 of the '202 patent. Pet. 1. Claim 1, the only independent claim, is illustrative of the claimed subject matter and is reproduced below.

1. An electronic device comprising a body of electrically insulating material that is provided with a through-hole or cavity, in which an electric component is present having a top

portion, a bottom portion and side portions, the component being attached to the body through an attachment layer, provided with a pattern of electrical conductors for electrically coupling the component to other components and/or contact means for external coupling, at least one of which electrical conductors extends into the body and is electrically coupled to a further conductor that is embedded in the body and is at least partially exposed to a surface of the body, wherein the body only partially surrounds the side portions of the electric component.

Ex. 1001, 6:58–7:3.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–14 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–14	103	Peterson, ² Hiromoto ³
1, 3–5, 7–13	103	Fujii ⁴
2, 6	103	Fujii, Ikuta ⁵
2, 5	103	Fujii, Durocher ⁶
4	103	Fujii, Mandler ⁷
1, 3–11, 13	103	Mandler, Hiromoto
2	103	Mandler, Hiromoto, Ikuta
2	103	Mandler, Hiromoto, Durocher
1–8, 10, 11, 13	103	Ido ⁸

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. §§ 102 and 103 that became effective on March 16, 2013. Because the ’202 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of §§ 102 and 103.

² Peterson, US 6,674,159 B1, issued Jan. 6, 2004 (Ex. 1005).

³ Hiromoto, Japanese Patent App. No. 2000031544A, with English translation (Ex. 1009).

⁴ Fuji, US 2002/0123163 A1, published Sept. 5, 2002 (Ex. 1008).

⁵ Ikuta, US 2003/0169575 A1, published Sept. 11, 2003 (Ex. 1010).

⁶ Durocher, US 6,733,711 B2, issued May 11, 2004 (Ex. 1011).

⁷ Mandler, US 7,084,935 B2, issued Aug. 1, 2006 (Ex. 1007).

⁸ Ido, US 2003/0156608 A1, published Aug. 21, 2003 (Ex. 1006).

Petitioner relies on the Declaration of Carl Sechen, Ph.D. (“Sechen Declaration,” Ex. 1002) in support of its contentions.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person having ordinary skill in the art (“POSITA”) would have had “either a bachelor’s degree in electrical engineering with two years of experience in the field of electronic device design, manufacturing and packaging, as well as printed circuit board design and manufacturing,” or “a master’s degree with an emphasis on electronic device design, manufacturing and packaging, as well as printed circuit board design and manufacturing.” Pet. 5 (citing Ex. 1002 ¶¶ 32–35). Petitioner’s unopposed proposed definition appears to be consistent with the cited prior art and the disclosure of the ’202 patent, and we adopt it for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

B. *Claim Construction*

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed.

Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner does not propose a specific construction for any claim term. Pet. 6. For purposes of this Decision, based on the record before us, we determine that no claim term requires an explicit construction.

C. Alleged Obviousness over Peterson and Hiromoto

Petitioner contends that claims 1–14 would have been obvious over the combined teachings of Peterson and Hiromoto. Pet. 9–28.

1. Overview of Peterson

Peterson relates “to a package for housing at least one microelectronic device, comprising a hollow assembly of stacked, electrically insulating plates and an integral window.” Ex. 1005, 7:62–65. “The integral window is bonded directly to the package without having a separate layer of adhesive material disposed in-between the window and the package.” *Id.* at 5:1–4. The microelectronic device can be, for example, a semiconductor chip or a laser diode. *Id.* at 5:4–6. Peterson teaches that “[t]he microelectronic device can be flip-chip bonded so that the light-sensitive side is optically accessible through the window.” *Id.* at 5:9–11. “The package has at least two levels of circuits for making electrical interconnections to a pair of microelectronic devices.” *Id.* at 5:11–13. According to Peterson, “[t]he result is a compact, low-profile package having an integral window that is hermetically sealed to the package prior to mounting and interconnecting the microelectronic device(s).” *Id.* at 5:13–16.

2. *Overview of Hiromoto*

Hiromoto relates to a semiconductor light-emitting diode configured to emit light from the side surface. Ex. 1009 ¶ 1. Hiromoto's device includes a semiconductor light-emitting element, a pair of electrodes, a semiconductor light-emitting chip connected to the electrodes, and a synthetic resin for sealing the semiconductor light-emitting chip. *Id.* ¶ 8.

Hiromoto explains that at least one side of the device comprises a sealing body that is formed of translucent synthetic resin. Ex. 1009 ¶ 8. A curved surface is formed on an end surface of the translucent synthetic resin, “and the output light of the semiconductor light emitting chip is collected and emitted in a direction inclined with respect to the horizontal direction.” *Id.* ¶ 9. Hiromoto further explains that the mounting position of the semiconductor light emitting element on the mounting substrate can be changed in order to reliably emit light to “the irradiation target whose setting positions from the surface of the mounting substrate are different.” *Id.* As a result, Hiromoto states that “the application of the semiconductor light emitting device is expanded.” *Id.*

3. *Analysis*

Petitioner contends that Peterson teaches all of the elements of independent claim 1 except “wherein the body only partially surrounds the side portions of the electric component.” Pet. 9–15. For example, Petitioner contends that Peterson discloses “a body of electrically insulating material that is provided with a through-hole or cavity” because Peterson describes an assembly that includes plates made from an electrically insulating material, wherein at least one of the plates has an aperture through it for providing physical access to insert a microelectronic device into the package. *Id.* at 9–10 (citing Ex. 1002 ¶¶ 47–48; Ex. 1005, 9:16–25, 11:25–30). Petitioner

further contends that Peterson teaches that the microelectronic device, which is located within the aperture, has a top, bottom, and side portions. *Id.*

at 10–11 (citing Ex. 1002 ¶ 50; Ex. 1005, 8:52–56, Fig. 3A). Petitioner also contends that Peterson teaches an attachment layer because the assembly has a first plate attaching the microelectronic device to the second plate. *Id.*

at 11. An electrically conductive metallized trace (i.e., electrical conductor) that conducts an electrical signal between interior and exterior interconnect locations is disposed on the surface of the first plate, and Peterson’s microelectronic device can be attached to this surface. *Id.* (citing Ex. 1002 ¶ 50; Ex. 1005, 9:6–12, Fig. 3A).

Petitioner also contends that Peterson “describes how single or multilayer printed wiring board materials can be used for constructing” the assembly, and that multilayer printed wiring boards “can have more than two layers of circuitry (*i.e.*, metallized traces).” Pet. 12 (citing Ex. 1002 ¶ 53; Ex. 1005, 13:5–9). Petitioner contends that Peterson “describes how ‘conductive vias 700, 702 can interconnect metallic traces on multiple levels, as is well known to those skilled in the art.’” *Id.* at 13 (citing Ex. 1002 ¶ 53; Ex. 1005, 27:24–27, Fig. 15C).

Petitioner further contends that Hiromoto teaches the “wherein the body only partially surrounds the side portions of the electric component” limitation of claim 1. Pet. 14–15. In particular, Petitioner contends that Hiromoto “teaches a side surface light emitting type semiconductor LED where the semiconductor light emitting chip 5 is mounted on the upper surface of one of the lead electrode patterns 4.” *Id.* at 15 (referring to Ex. 1009, Figs. 4, 6). Petitioner contends that Hiromoto’s lead electrode patterns and the semiconductor light-emitting chip are covered with a body made of an opaque synthetic resin, which “has an opening on one side

surface, hosting the semiconductor light emitting chip 5, and only partially surrounds the side portions of the semiconductor light emitting chip 5.” *Id.* Petitioner further contends that Hiromoto teaches filling the opening with transparent synthetic resin to seal the semiconductor light-emitting chip, and, as a result, the output light is emitted from the side of the electronic device in a direction parallel to the mounting substrate. *Id.* (citing Ex. 1002 ¶ 57; Ex. 1009 ¶¶ 3–5).

Petitioner asserts that “a POSITA would have found it obvious to implement Hiromoto’s arrangement of assembly elements into the assembly of Peterson” in order to “include an edge-emitting LED device into the assembly of Peterson.” Pet. 27 (citing Ex. 1002 ¶ 75). Petitioner also asserts that a POSITA would have been motivated to modify Peterson with Hiromoto “in order to have finer control over the direction of light emission by an LED contained within the assembly.” *Id.* at 27–28 (citing Ex. 1002 ¶ 76). According to Petitioner, because Peterson and Hiromoto relate to assemblies for electronic devices such as LEDs and describe similar functions, “a POSITA would have found it straightforward to combine Hiromoto’s arrangement of elements with Peterson’s assembly” with predictable results. *Id.* at 28 (citing Ex. 1002 ¶ 76).

We are persuaded, on this record, that Petitioner’s discussion of the particular structures in Peterson and Hiromoto, and the explanations in the Petition and the Sechen Declaration, are sufficient to establish a reasonable likelihood that claim 1 would have been obvious over the combined teachings of Peterson and Hiromoto. Pet. 9–15, 27–28; Ex. 1002 ¶¶ 45–57, 75, 76. We have also considered the arguments and evidence with respect to dependent claims 2–14. Pet. 15–27; Ex. 1002 ¶¶ 58–76. At this stage of the

proceeding, based on the record before us, we are persuaded that Petitioner establishes a reasonable likelihood of prevailing as to claims 2–14 as well.

D. Remaining Grounds

Petitioner contends that: (1) claims 1, 3–5, and 7–13 would have been obvious over Fujii; (2) claims 2 and 6 would have been obvious over the combined teachings of Fujii and Ikuta; (3) claims 2 and 5 would have been obvious over the combined teachings of Fujii and Durocher; (4) claim 4 would have been obvious over the combined teachings of Fujii and Mandler; (5) claims 1, 3–11, and 13 would have been obvious over the combined teachings of Mandler and Hiromoto; (6) claim 2 would have been obvious over the combined teachings of (a) Mandler, Hiromoto, and Ikuta or (b) Mandler, Hiromoto, and Durocher; and (7) claims 1–8, 10, 11, and 13 would have been obvious over Ido. Pet. 28–82. Having determined that Petitioner establishes a reasonable likelihood of showing that at least one of the challenged claims is unpatentable, we institute an *inter partes* review with respect to these grounds as well. *See Guidance of the Impact of SAS on AIA Trial Proceedings* (April 26, 2018) (explaining that “the PTAB will institute as to all claims or none” and “if the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition”).

III. CONCLUSION

Based on the arguments in the Petition and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail on its challenge to at least one challenged claim of the ’202 patent. Thus, we institute an *inter partes* review of all challenged claims on all the grounds presented.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of claims 1–14 of the '202 patent is instituted with respect to the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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